energies

MDPI

Article

Quasi-Resonant Single-Switch High-Voltage-Gain DC-DC Converter with Coupled Inductor and Voltage Multiplier Cell

Giordano Luigi Schiavon, Eloi Agostini, Jr. * and Claudinor Bitencourt Nascimento

Department of Electrical Engineering, Federal University of Technology–Parana–UTFPR, Ponta Grossa 84017-220, PR, Brazil
* Correspondence: eloiagostini@utfpr.edu.br

Abstract: This paper introduces a quasi-resonant high-efficiency high-step-up DC–DC converter requiring a reduced number of components. The proposed circuit uses a coupled inductor associated with voltage multiplier cells to ensure high-voltage-gain operation without the necessity of an extremely high number of turns ratio. Quasi-resonant operation guarantees zero current switching (ZCS) for some diodes of the converter. A detailed steady-state analysis is carried out aiming at the adequate design of the circuit. Experimental results taken from the testing of a 400 W prototype operating in closed loop with an input voltage range of 25–48 V, output voltage of 400 V and switching frequency of 100 kHz validate the analysis carried out and demonstrate the feasibility of the proposed converter.

Keywords: DC–DC converter; high voltage gain; coupled inductor; voltage multiplier cell

check for updates

Citation: Schiavon, G.L.; Agostini, E., Jr.; Nascimento, C.B. Quasi-Resonant Single-Switch High-Voltage-Gain DC-DC Converter with Coupled Inductor and Voltage Multiplier Cell. *Energies* **2023**, *16*, 3874. https://doi.org/10.3390/en16093874

Academic Editor: Salvatore Musumeci

Received: 6 March 2023
Revised: 26 April 2023
Accepted: 27 April 2023
Published: 3 May 2023

Copyright: © 2023 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (https://creativecommons.org/licenses/by/4.0/).

1. Introduction

Techniques associated with the generation of electrical energy have been improved to address the challenges associated with climate change and contribute to sustainable development. In this sense, production of electrical energy from renewable resources, such as wind, solar and biomass, is not an alternative anymore but a necessity [1,2]. Considering photovoltaic (PV) and fuel cell (FC) systems, the voltage levels are usually low and in the form of direct current (DC), diverging from the usual alternate current (AC) system that prevails in the distribution of electricity in most segments [3]. Thus, in order to adapt the voltage levels while taking into account technical and economic aspects, electronic energy processing is mandatory, from which low cost and high efficiency are expected. In this sense, high-step-up DC–DC converters are widely employed in applications where the primary energy source is characterized by a voltage level much lower than that required for the end use [4–8].

Providing energy to a DC distribution system or conditioning the voltage as an intermediate stage of a DC–AC conversion system are some applications of DC–DC converters. One of the main challenges in the use of such converters is to avoid expressive switching and conduction losses. Therefore, using circuits with a reduced number of components, featuring low-voltage stress on the semiconductors and with the ability of recycling the leakage energy are key to improving the overall system efficiency. However, achieving all these characteristics is not an easy task. One classic example is the boost converter, which is indeed a simple circuit but exhibits poor performance under high-voltage-gain conditions [9]. Addressing the limitations of the boost converter by the use of techniques to improve the voltage gain has been extensively investigated in the literature [10–12]. Among the several techniques discussed in [12], one can be highlighted: boost-based solutions using a single active switch, a single coupled inductor and voltage multiplier cells (VMCs), such as the boost-flyback and the boost associated with VMCs introduced in [13] and [14], respectively, in addition to other solutions recently reported in the literature [15–19]. In

all these examples, voltage gain is dependent on the duty cycle (D) and on the number of turns ratio (n) of the coupled inductor. As a result, higher voltage conversion ratios can be achieved without extreme duty cycle values, and therefore a higher efficiency is expected, since conduction and switching losses are lower compared to the conventional step-up converters.

Converters employing a single active switch and reduced number of diodes and capacitors are usually not suited for applications where the power processed is higher than a few hundred watts. However, these circuits are interesting for processing energy from PV modules rated in the range of 200–600 W. In this sense, this work introduces a high-voltage-gain DC–DC converter based on the boost configuration using coupled inductor and voltage multiplier cells, as depicted in Figure 1. The key features of the proposed circuit that make it suitable for PV applications are: high efficiency; reduced number of components; low voltage stress on the semiconductors; and voltage distribution among the output capacitors. In addition, quasi-resonant characteristics guarantee ZCS operation for diodes D_2 and D_3, thus contributing to improving the system efficiency [20–22]. In addition, a high voltage conversion ratio can be achieved if compared with similar topologies, even though a relatively low number of turns ratio of the coupled inductor is adopted. Therefore, weight, volume and magnetic losses can be minimized.

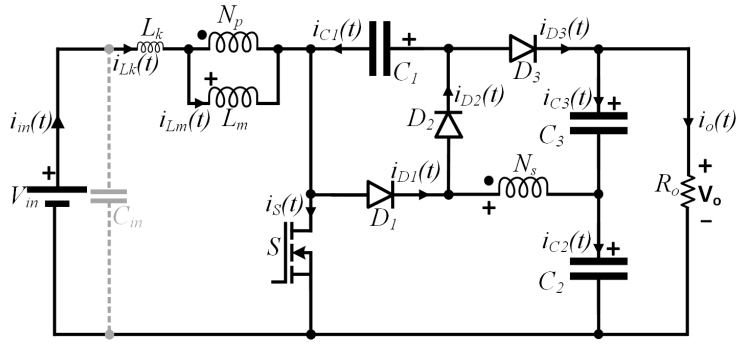


Figure 1. Proposed high-voltage-gain DC–DC converter employing coupled inductor and voltage multiplier cells.

2. Principle of Operation in Steady State

The proposed high-step-up DC–DC converter depicted in Figure 1 contains a VMC composed of the winding N_s of the coupled inductor associated with the pairs D_2/C_2 and D_3/C_3. Since this topology is able to impose high voltage levels on the capacitors, adopting a number of turns ratio close to one is possible without the need for overly high values of duty cycle. The steady-state analysis of the proposed converter is carried out for deriving a mathematical model that allows the proper choice of every component contained in the circuit. In this sense, the following assumptions are made:

- All elements are considered ideal, except for the leakage inductance of the coupled inductor;
- The voltage on the capacitors and the magnetizing current are assumed to be ripple free;
- The analysis is carried out within one period of the switching frequency f_s.

Six operating stages are verified from the analysis of the converter during one switching period, as depicted in Figure 2. From these six stages, only four are relevant in terms of the energy processed by the system. Hence, transition stages regarding the intervals Δt_1 and Δt_4 will be neglected from the mathematical analysis.

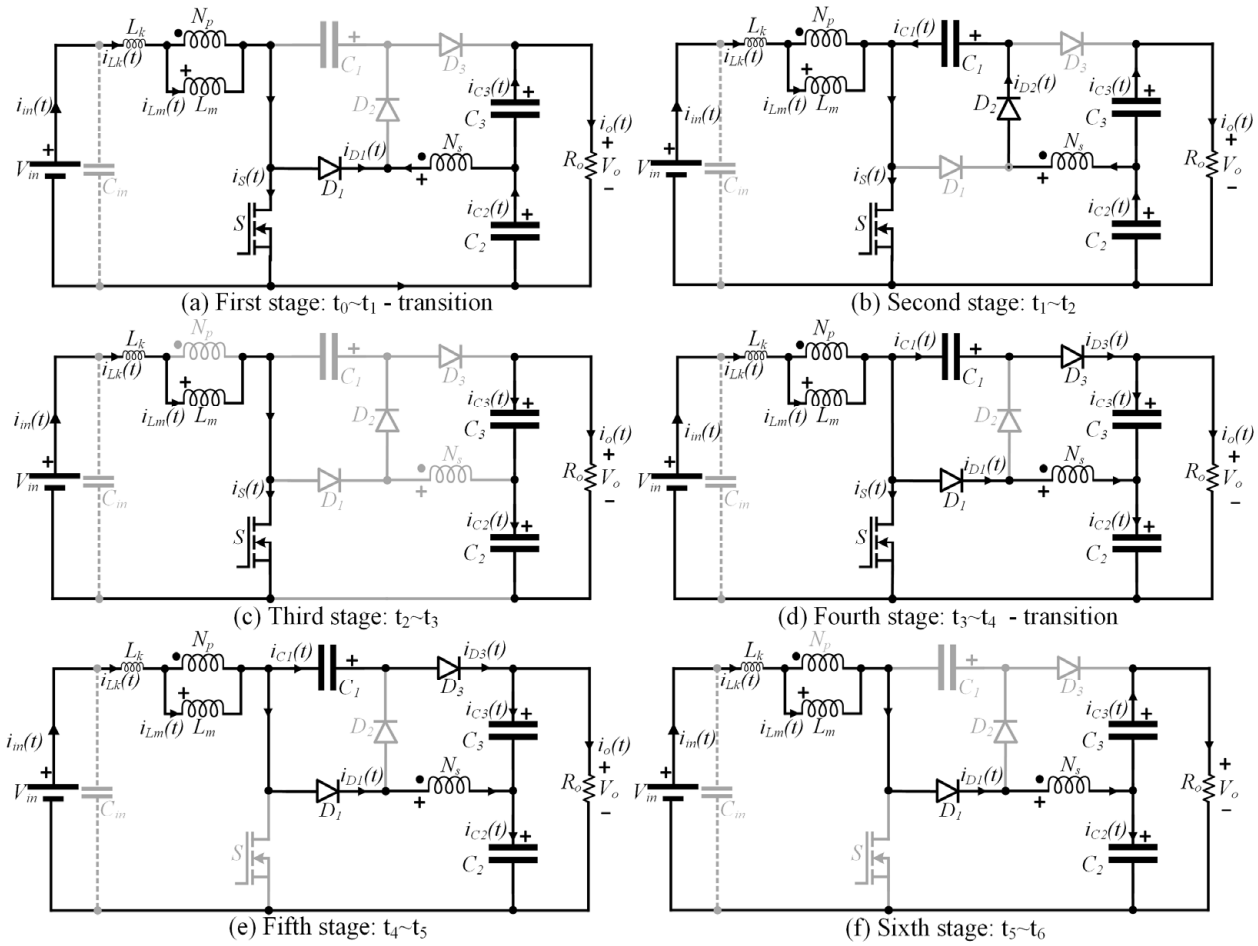


Figure 2. Operating stages in steady state. First and fourth stages correspond to brief transition intervals that play minor roles in the energy processed by the system.

During the second and third stages, which correspond to the intervals Δt_2 and Δt_3, respectively, switch S is turned on, the magnetizing inductance L_m stores energy, and capacitors C_2 and C_3 provide energy that has been stored during the previous stages to the system. These intervals are characterized as linear stages, since resonance between the leakage inductance L_k and the capacitors contained in the circuit is not expressive. This operational condition is finished when S is turned off.

The fifth and sixth stages, defined by the intervals Δt_5 and Δt_6, occur when S remains in the off state. During these stages, energy stored in L_m is provided to the circuit. Resonance between L_k, C_1 and C_3 becomes expressive during the fifth stage. In this sense, if it is guaranteed that the resonant frequency is higher than the switching frequency, D_2 operates with ZCS, thus contributing to increasing the system efficiency. It is noteworthy that the fifth stage plays a crucial role in defining the voltage gain of the converter. Regarding the sixth stage, the converter returns to a linear operating characteristic.

Figure 3 presents the main theoretical waveforms regarding the converter operation in steady state. As can be seen, an abrupt change in i_{Lk} occurs at the end of interval Δt_3, which is a simplifying assumption justified by the fact that the fourth stage corresponds to a very brief transition state, during which the energy processed can be neglected.

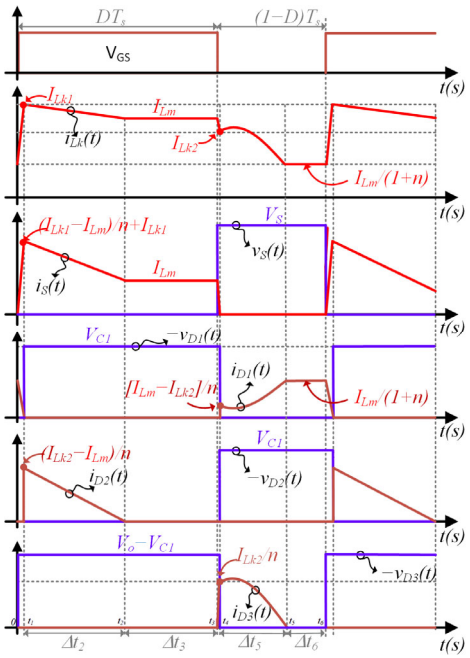


Figure 3. Main theoretical waveforms within one switching period for steady-state operation.

3. Mathematical Model

Fundamental information regarding the operation of the proposed converter can be extracted from the mathematical model of the circuit, such as the voltage conversion ratio and voltage stress on the semiconductor devices. Such knowledge is key to designing the circuit properly, aiming at reduced conduction and switching losses to ensure high-efficiency operation.

3.1. Steady-State Analysis

The proposed mathematical model takes into consideration the following definitions:

$$\begin{aligned} &\Delta t_i = t_i - t_{i-1};\ T_s = \tfrac{1}{f_s};\ n = \tfrac{N_s}{N_p};\ \lambda = \tfrac{L_k}{L_m};\ k = \tfrac{L_m}{L_k+L_m};\\ &M = \tfrac{V_o}{V_{in}};\ M_{C1} = \tfrac{V_{C1}}{V_{in}};\ M_{C2} = \tfrac{V_{C2}}{V_{in}};\ M_{C3} = \tfrac{V_{C3}}{V_{in}}, \end{aligned} \tag{1}$$

where i defines the interval of each stage beginning at t_{i-1} and ending at t_i; T_s corresponds to the switching period; f_s is the switching frequency; n defines the number of turns ratio of the coupled inductor; the factors λ and k relate the magnetizing and leakage inductances; and M, M_{C1}, M_{C2} e M_{C3} correspond to the total and partial static gains of the circuit.

The fundamental equation for $i_{Lk}(t)$ valid for the interval Δt_2 is given by (2).

$$I_{Lm} = I_{Lk1} + \left(1 - \frac{M_{C1} - M_{C2}}{n}\right)\frac{\Delta t_2}{\lambda L_m} V_{in} \tag{2}$$

The energy balance of the algebraic sum of the leakage and magnetizing inductances yields (3).

$$M_{C2} + M_{C3} - M_{C1} = \frac{1}{1-D} \tag{3}$$

Equation (4) can be determined from the analysis of the equivalent circuit of the second stage depicted in Figure 2b.

$$M_{C1} - M_{C2} = nk \tag{4}$$

As previously mentioned, resonance between L_k and the pair C_1/C_3 is expressive during the fifth stage of the proposed high-step-up DC–DC converter. Thus, the analysis of this stage can be carried out using the current and voltage on these elements.

Currents on C_1 and C_3 can be written in terms of $i_{Lk}(t)$ as given by (5) and (6), respectively.

$$i_{C1}(t) = \frac{I_{Lm}}{n} - \frac{(1+n)}{n} i_{Lk}(t) \tag{5}$$

$$i_{C3}(t) = -\left(\frac{I_{Lm}}{n} + I_o\right) + \frac{(1+n)}{n} i_{Lk}(t) \tag{6}$$

Equation (7) provides the voltage on the leakage inductance during the resonant stage.

$$v_{Lk}(t) = V_{in} - V_o + \frac{(1+n)}{n} v_{C1}(t) - \frac{1}{n} v_{C3}(t) \tag{7}$$

Differentiating (7) results in

$$\frac{dv_{Lk}(t)}{dt} = \frac{(1+n)}{n} \frac{dv_{C1}(t)}{dt} - \frac{1}{n} \frac{dv_{C3}(t)}{dt}. \tag{8}$$

Equation (8) can be rewritten in terms of the currents on C_1 and C_3, as given by

$$L_k \frac{d^2 i_{Lk}(t)}{dt^2} = \frac{(1+n)}{nC_1} i_{C1}(t) - \frac{1}{nC_3} i_{C3}(t). \tag{9}$$

Substituting (5) and (6) into (9) results in the differential equation

$$L_k C_{eq} \frac{d^2 i_{Lk}(t)}{dt^2} + i_{Lk}(t) = A, \tag{10}$$

where

$$C_{eq} = \frac{n^2}{(1+n)} \left[\frac{C_1 C_3}{C_1 + (1+n)C_3}\right], \tag{11}$$

$$A = \frac{1}{(1+n)} \left[I_{Lm} + \frac{nC_1}{C_1 + (1+n)C_3} I_o\right]. \tag{12}$$

Applying the Laplace transform in (10) results in (13), which represents the current $i_{Lk}(t)$ in the s domain.

$$I_{Lk}(s) = \frac{\frac{A\omega_o^2}{s} + sI_{Lk2}}{s^2 + \omega_o^2} \tag{13}$$

where

$$\omega_o = \frac{1}{\sqrt{L_k C_{eq}}}. \tag{14}$$

At this time, current $i_{Lk}(t)$ during the fifth stage can be determined by applying the inverse Laplace transform in (13), as given by (15). It is noteworthy that the resonant frequency f_o must be higher than the switching frequency f_s to guarantee ZCS for D_3.

$$i_{Lk}(t) = \left(V_o - \frac{1+nD}{1-D} V_{in} - V_{C3}\right) \frac{\sin(\omega_o t)}{nL_k \omega_o} + A + (I_{Lk2} - A)\cos(\omega_o t) \tag{15}$$

Differentiating (15) and multiplying the result by L_k provides the value of v_{Lk}, as given by

$$v_{Lk}(t) = \frac{1}{n}\left[V_o - V_{C3} - \frac{(1+nD)V_{in}}{(1-D)}\right] \cos(\omega_o t) + \omega_o L_k (I_{Lk3} - A)\sin(\omega_o t). \tag{16}$$

Assuming that at $t = 0$ v_{Lk} is approximately equal to 0, one can derive the partial static gain M_{C3} as

$$M_{C3} = M - \frac{1+nD}{1-D}. \tag{17}$$

The circuit analysis reveals that the static gain M corresponds to the sum of M_{C2} and M_{C3}, as given by (18), which allows computing M_{C2} as (19).

$$M = M_{C2} + M_{C3} \tag{18}$$

$$M_{C2} = \frac{1 + nD}{1 - D} \tag{19}$$

Substituting (19) into (4) yields the value of M_{C1} given by

$$M_{C1} = \frac{1 + n}{1 - D} + n\,k\,. \tag{20}$$

Lastly, the total voltage gain M can be determined by substituting (4) and (17) into (3).

$$M = \frac{2 + n\,D}{1 - D} + n\,k \tag{21}$$

It can be concluded from (21) that lower values of k yield lower voltage conversion ratios. On the other hand, if the leakage inductance is low, the factor k tends toward one, and consequently the voltage gain converges to an ideal operating condition. In addition, the impact of k is minimized when the number of turns ratio is lower.

Figure 4 presents several curves of the voltage gain M as a function of the duty cycle D for different values of n and k. For the condition n = 1, it is evident that the influence of k is neglectable. On the other hand, as n increases and k decreases, the voltage gain deviates from the ideal case.

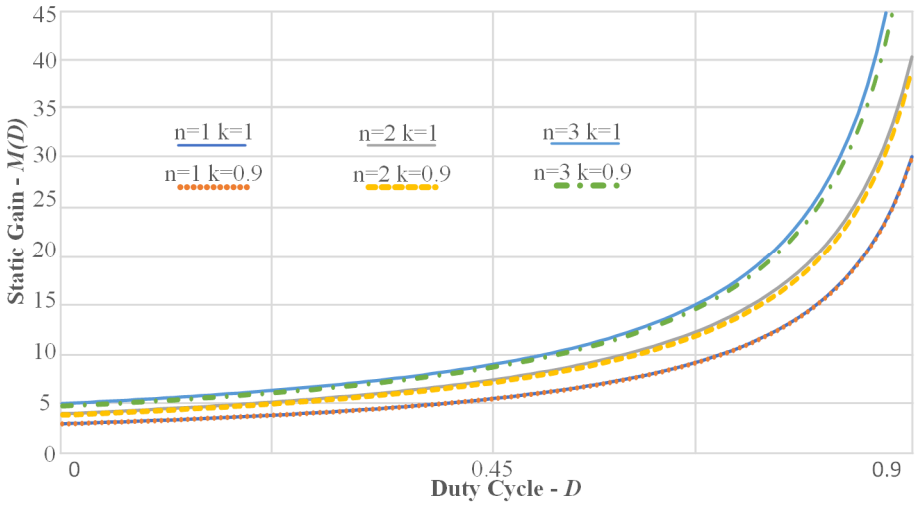


Figure 4. Voltage gain M as a function of the duty cycle D for different values of n and k.

The unknowns I_{Lk1} and I_{Lk2}, as well as the intervals Δt_2 and Δt_5, can be determined using (2) and (15) along with the average current on D_2 e D_3, which in turn are equivalent to the average output current I_o and are given by (22) and (23), respectively.

$$\frac{1}{T_s}\int_0^{\Delta t_5} i_{C1}(t)\,dt = I_o \tag{22}$$

$$\left(\frac{I_{Lk1} - I_{Lm}}{2n}\right)\frac{\Delta t_2}{T_s} = I_o \tag{23}$$

To complete the mathematical model of the proposed converter, it is fundamental that the equations defining the values of C_1, C_2 and C_3, the magnetizing inductance L_m and the voltage stress on the semiconductor devices are derived.

Based on the operating stages depicted in Figure 2, it is possible to conclude that the values of C_1, C_2 and C_3 can be determined by (24), (25) and (26), respectively. However, C_1 and C_3 can also be determined using the resonance criterion given by (14) and (11), which is used in this work to calculate these capacitances.

$$C_1 = \frac{1}{\Delta V_{C1}} \int_0^{\Delta t_5} i_{C1}(t)\, dt \tag{24}$$

$$C_2 = \frac{1}{\Delta V_{C2}} \left[\int_0^{\Delta t_5} \left(\frac{i_{Lk}(t)}{n} - I_o \right) dt + \frac{I_{Lm}}{1+n} \Delta t_6 \right] \tag{25}$$

$$C_3 = \frac{D T_s I_o}{\Delta V_{C3}} \tag{26}$$

where ΔV_{C1}, ΔV_{C2}, ΔV_{C3} are the voltage ripples on C_1, C_2 and C_3, respectively.

The magnetizing inductance L_m can be computed using

$$L_m = \frac{(1-D)(V_{C1} - V_{C3}) T_s}{n \Delta I_{Lm}}, \tag{27}$$

where ΔI_{Lm} is the current ripple on L_m.

It can be concluded from Figure 2b,e that the voltage stress on D_1 and D_2 is equal to the voltage on C_1 given by (20).

$$V_{D1} = V_{D2} = \left(\frac{1+n}{1-D} + n\, k \right) V_{in} \tag{28}$$

The voltage stress on S and D_3 can be determined from the analysis of the second and fifth operating stages, resulting in

$$V_S = V_{D3} = \frac{V_{in}}{1-D}. \tag{29}$$

The proposed converter can be designed and validated in the laboratory based on the mathematical analysis detailed so far. Moreover, a detailed efficiency analysis can be performed to determine the advantages of the proposed circuit for the intended applications, especially PV and FC systems.

3.2. Control Strategy

As known, PV and FC systems require a proper control system to ensure maximum power point tracking (MPPT) operation. In such a system, the DC–DC converter stage is directly responsible for MPPT realization by means of controlling the input voltage or current. In this paper, a control strategy aiming at controlling the input current is adopted, in accordance with the schematic depicted in Figure 5.

In the proposed scheme, input voltage and current are measured using the digital signal processor TMS320F28377S, in which an input current compensator is implemented. First-order filters with a cutoff frequency of 1 kHz are used for signal conditioning and analog-to-digital conversion is performed with a sampling frequency equal to 100 kHz. In this work, a proportional–integral (PI) controller with proportional and integral gains of 0.005 and 15, respectively, is used to adjust the input current, which in turn allows MPPT to be realized. It is noteworthy that the small-signal analysis of the proposed circuit is very extensive due to the high number of operating stages and quasi-resonant operation, and therefore it will not be detailed in this paper. Nevertheless, closed-loop operation will be investigated to demonstrate the suitability of the proposed converter for PV and FC applications.

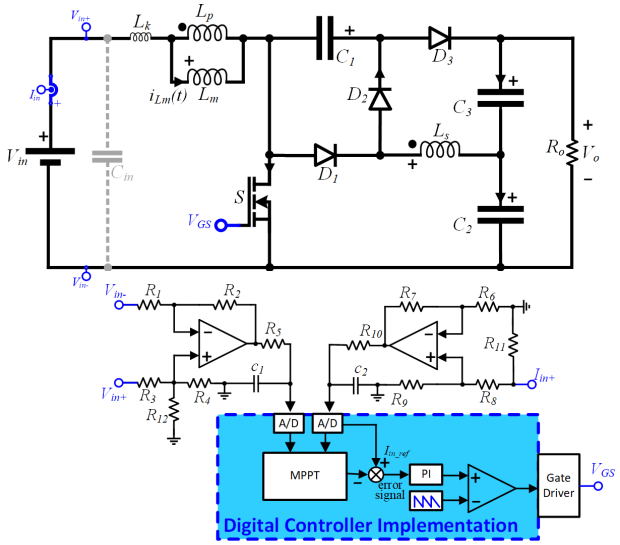


Figure 5. Control strategy for the proposed converter.

4. Experimental Results

The experimental verification of the proposed converter is carried out using a 400 W prototype designed in consideration of the specifications shown in Table 1.

Table 1. Design specifications for a 400 W prototype.

Symbol	Description	Value
V_{in}	Input voltage	48 V
f_s	Switching frequency	100 kHz
P_o	Output power	400 W
V_o	Output voltage	400 V
n	Number of turns ratio	1
k	Inductance factor	95%
L_k	Leakage inductance	2 µH
f_o	Resonant frequency	$1.6 \cdot f_s$
ΔI_{Lm}	Current ripple on L_m	45% of I_{in}
ΔV_{C3}	Voltage ripple on C_3	1% of V_{C3}

As previously mentioned, the resonance criterion was adopted to determine the capacitances C_1, C_2 and C_3. In this sense, the leakage inductance was initially estimated as L_k = 2 µH. Next, Equation (14) was used to determine C_{eq}, which in turn can be used to calculate C_1 and C_3 using (11). It is noteworthy that f_o was chosen to be higher than f_s, and thus ZCS is guaranteed for D_3. Based on the knowledge that the most expressive resonance occurs in the fifth stage, which corresponds to the interval Δt_5 that can last as long as $(1 - D) \cdot T_s$, it was decided that $f_o = 1.6 \cdot f_s$. The main results obtained from the design of the proposed converter are listed in Table 2 and a picture of the prototype is shown in Figure 6.

Table 2. Main design results.

Parameter	Value
D	0.644
L_m	80 µH, E42/15, $N_p = N_s = 16$
C_1	3 µF/400 V
C_2	3 µF/400 V
C_3	3 µF/400 V
D_1, D_2 and D_3	MUR 840
S	IRFP4668PBF

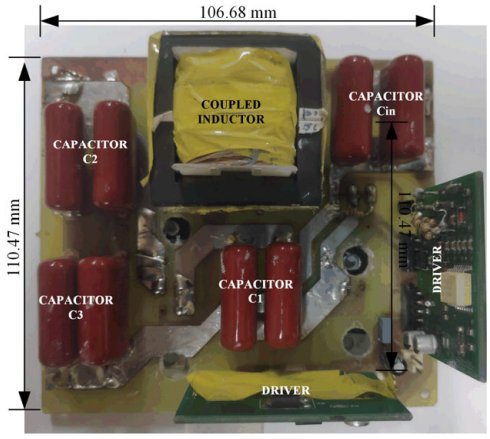
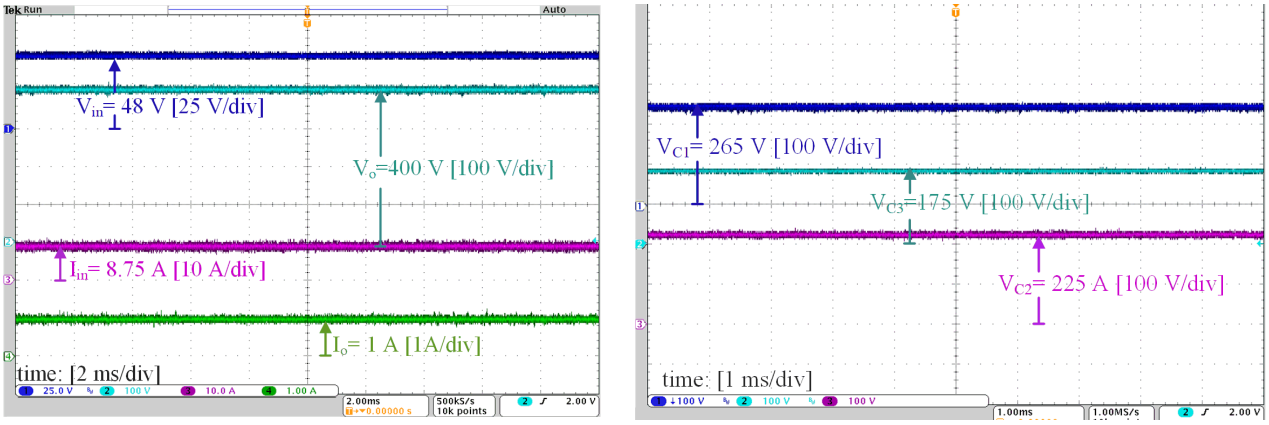


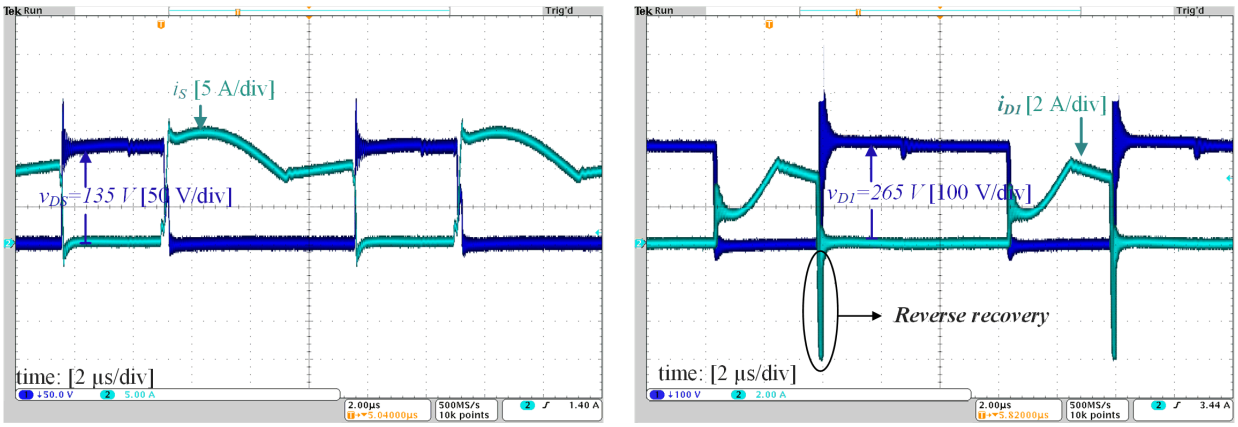
Figure 6. Picture of the 400 W prototype of the proposed converter.

Voltage and current at the input and output are depicted in Figure 7a. Input current was measured before the decoupling capacitor C_{in}, resulting in a filtered low-current ripple waveform. Figure 7b shows the voltage on capacitors C_1, C_2 and C_3. The results are in accordance with the theoretical predictions given by (20), (19) and (17), respectively. The voltage and current on the switch S are depicted in Figure 8a. The waveforms indicate dissipative commutation, but it is evident that the drain-to-source voltage is much lower than the output voltage. Consequently, a low-R_{DSon} MOSFET can be used, thus minimizing the conduction and switching losses on this device. Voltage and current on D_1, D_2 and D_3 are shown in Figures 8b and 9a,b, respectively. These results confirm that the commutation of D_1 is dissipative, as a considerable reverse recovery current is observed. However, this reverse current does not appear on the switch current (c.f., Figure 8a), and therefore its impact on the switching losses becomes limited. It can be also verified that D_2 and D_3 operate with ZCS as a result of the resonant characteristic of the current on these devices. The most expressive resonance occurring during the fifth stage and predicted in the theoretical analysis is evident on the waveform of the current on D_3. The measured resonant frequency was approximately 190 kHz, deviating from the 160 kHz ($1.6 \cdot f_s$) defined in Table 1. This difference was expected, because the actual leakage inductance of the coupled inductor measured in laboratory was L_k = 1.45 µH, a value lower than the 2 µH estimated during design.



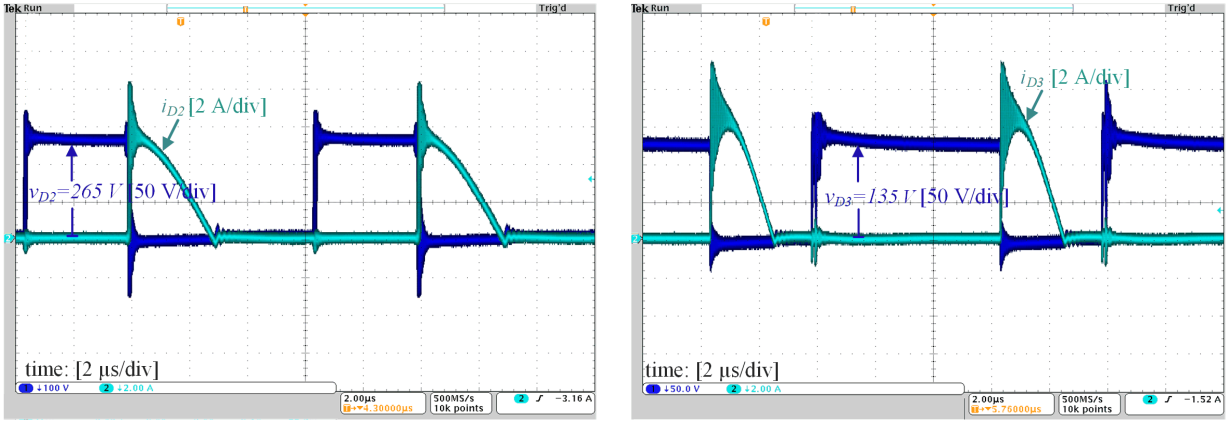
(**a**) (**b**)

Figure 7. (**a**) Voltages and currents on the input and output; (**b**) Voltages on capacitors C_1, C_2 and C_3.



(**a**) (**b**)

Figure 8. Voltage and current on (**a**) switch *S*; (**b**) diode D_1.



(**a**) (**b**)

Figure 9. Voltage and current on (**a**) diode D_2; (**b**) diode D_3.

Efficiency measurements were taken using the power precision analyzer Yokogawa WT500 and are presented in Figure 10. Tests under three different situations were performed to create conditions in accordance with the specifications of 250–400 W solar modules. Figure 10a presents the efficiency curve versus output power considering input and output voltages fixed at 48 V and 400 V, respectively. A maximum efficiency of 96.9% was measured at 60% of rated output power, while the full-load efficiency was 96.46%. Efficiency versus input voltage variation, maintaining the output power fixed at 400 W, is shown in Figure 10b. It is evident that the efficiency is considerably reduced at low input voltage due to increased current levels. A more realistic situation is when the output power decreases as the input voltage is reduced. Figure 10c shows the efficiency versus input voltage considering an output power variation of 250–400 W. Although an efficiency reduction is also observed as the input voltage decreases, the impact is not as severe as that verified in the test with P_o fixed at 400 W.

Finally, closed-loop operation with the output voltage fixed at 400 V is demonstrated in Figure 11. Steps in the input current reference from 4.25 A to 8.75 A and from 8.75 A to 4.25 A were applied, and the response demonstrates the proper operation of the converter using the control strategy depicted in Figure 5. In the tests, the output voltage was regulated at 400 V by the electronic load NHR9430 operating in the constant voltage mode to emulate the behavior of a grid-tied inverter stage. It is also noteworthy that the input current was

measured before the filter capacitor C_{in}, and hence its ripple is lower than the theoretical prediction depicted in the waveform of i_{Lk} (c.f., Figure 3).

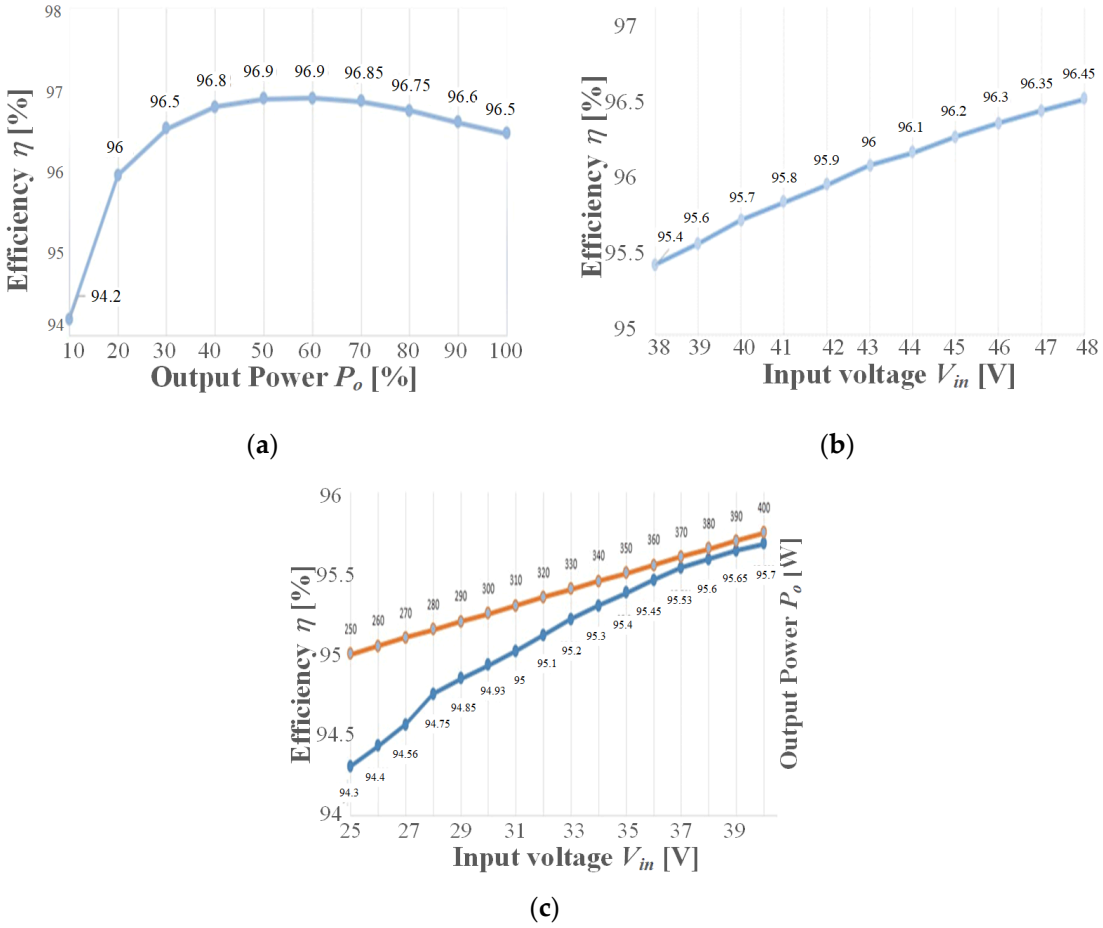


Figure 10. Efficiency curves: (**a**) as a function of the output power with V_{in} = 48 V and V_o = 400 V; (**b**) as a function of the input voltage (V_{in} = 38–48 V) with P_o = 400 W; and (**c**) as a function of the input voltage (V_{in} = 25–40 V) with variable output power (P_o = 250–400 W).

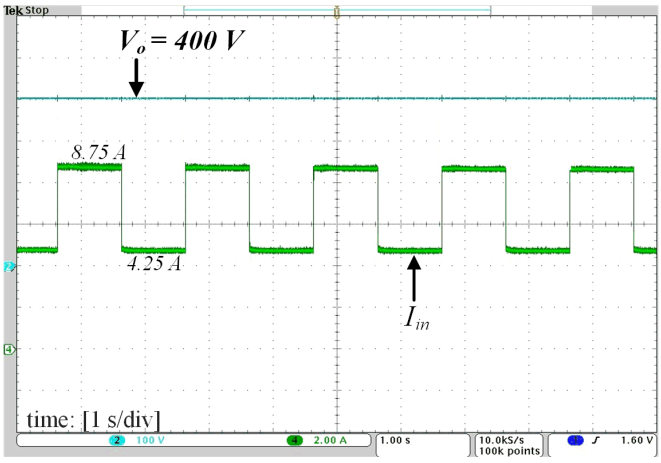


Figure 11. Closed-loop response for steps in the input current reference from 4.25 A to 8.75 A and from 8.75 A to 4.25 A. The output voltage is imposed by the electronic load NHR9430 operating in the constant voltage mode to emulate the behavior of a grid-tied inverter stage.

Comparative Analysis

The proposed converter is compared with the high-voltage-gain topologies proposed in [5,6,13–17], as summarized in Table 3. In this comparative analysis, only circuits containing a single active switch and one coupled inductor with two windings are considered. In addition, it is assumed that the leakage inductance of the coupled inductor is much smaller than its magnetizing inductance. As can be concluded from Table 3, both the voltage gain M and the voltage stresses on the semiconductors are usually related to the number of diodes and capacitors contained in the circuits. The circuits proposed in [5,13] contain only two diodes and two capacitors, although in [5] the voltage stress on the switch and on the diode D_2 is equal to the entire output voltage level. As a result, higher conduction and switching losses are expected. The converters introduced in [15,17] exhibit the higher voltage gains, but more diodes and capacitors are employed. The boost-flyback converter proposed in [13] presents the lower voltage conversion ratio, and also requires the use of an auxiliar snubber to prevent potentially destructive voltage spikes on D_3. As a consequence, if the same duty cycle is adopted, a higher number of turns ratio is required to reach the same voltage gain, and therefore weight and cost of the coupled inductor are also increased. It is also noteworthy that the snubber required for proper operation increases the losses of the circuit, which has an impact on the overall system efficiency. The converters proposed in [6,14,16] present similar constructive and operational characteristics. The highest efficiencies are verified in the proposed converter and in the circuit introduced in [6]. However, the proposed converter has a higher voltage gain and was tested with a higher switching frequency.

Table 3. Comparison between boost-based high-step-up DC–DC converters using a single active switch and one coupled inductor with only two windings.

Reference	Voltage Gain (V_o/V_{in})	Voltage Stress on the Switch	Voltage Stress on the Diodes			Number of Capacitors	Number of Diodes	Efficiency η
			V_{D1}	V_{D2}	V_{D3}			
Proposed	$\frac{2+n}{1-D}$	$\frac{V_{in}}{1-D}$	$\left(\frac{1+n}{1-D}+n\right)V_{in}$	$\left(\frac{1+n}{1-D}+n\right)V_{in}$	$\frac{V_{in}}{1-D}$	3	3	96.5% @400 W, 100 kHz, n = 1
[5]	$\frac{1+n}{1-D}$	$\frac{1+n}{1-D}V_{in}$	$\left(\frac{1+n}{1-D}-n+1\right)V_{in}$	$\frac{1+n}{1-D}V_{in}$	-	2	2	94% @300 W, 100 kHz, n = 3
[6]	$\frac{1+n}{1-D}$	$\frac{V_{in}}{1-D}$	$\frac{V_{in}}{1-D}$	$\frac{nV_{in}}{1-D}$	$\frac{nV_{in}}{1-D}$	3	3	96.5% @400 W, 90 kHz, n = 1.72
[13]	$\frac{1+nD}{1-D}$	$\frac{V_{in}}{1-D}$	$\frac{V_{in}}{1-D}$	Limited by the RCD snubber [1]	Voltage stress on the snubber diode [1]	3	3	93% @35 W, 38 kHz, n = 2
[14]	$\frac{1+n}{1-D}$	$\frac{V_{in}}{1-D}$	$\frac{V_{in}}{1-D}$	$\frac{nV_{in}}{1-D}$	$\frac{nV_{in}}{1-D}$	3	3	Not reported, 20 kHz, n = 1
[15] [2]	$\frac{1+n}{1-D}+n$	$\frac{V_{in}}{1-D}$	$\frac{V_{in}}{1-D}$	$\frac{nV_{in}}{1-D}$	$\frac{nV_{in}}{1-D}$	4	4	94.3% @400 W, 50 kHz, n = 1
[16]	$\frac{1+n}{1-D}$	$\frac{V_{in}}{1-D}$	$\frac{V_{in}}{1-D}$	$\frac{nV_{in}}{1-D}$	$\frac{nV_{in}}{1-D}$	3	3	94% @300 W, 100 kHz, n = 6
[17] [3]	$\frac{2+n}{(1-D)^2}$	$\frac{V_{in}}{(1-D)^2}$	$\frac{V_{in}}{1-D}$	$\frac{DV_{in}}{(1-D)^2}$	$\frac{V_{in}}{(1-D)^2}$	4	5	91.1% @500 W, 40 kHz, n = 1.86

[1] Voltage stresses were not reported in the paper. [2] Voltage stress on the fourth diode is similar to D_2 and D_3. [3] Voltage stresses on D_{r1} and D_o are not included.

5. Conclusions

A novel high-step-up DC–DC converter based on the boost converter employing one coupled inductor and voltage multiplier cells was proposed in this paper. The circuit contains a single active switch, three diodes and three capacitors, and is capable of achieving a high conversion ratio even when a low number of turns ratio is adopted. It was demonstrated that using a low number of turns ratio minimizes the influence of the leakage inductance on the voltage gain. In addition, the resonant characteristic of the circuit provides ZCS operation for two of its diodes, thus reducing the switching losses and improving the system efficiency. A detailed efficiency analysis was performed in the laboratory, and the results demonstrate that the proposed converter is a viable solution for applications with a power rating on the order of a few hundred watts, since it is capable of providing high voltage gain with a reduced number of components.

Author Contributions: Conceptualization, G.L.S. and C.B.N.; software, G.L.S.; validation, G.L.S., E.A.J. and C.B.N.; formal analysis, G.L.S., E.A.J. and C.B.N.; investigation, G.L.S.; data curation, G.L.S.; writing—original draft preparation, C.B.N.; writing—review and editing, E.A.J.; supervision, C.B.N.; project administration, C.B.N.; funding acquisition, E.A.J. and C.B.N. All authors have read and agreed to the published version of the manuscript.

Funding: This research was funded in part by the Coordination for the Improvement of Higher Education Personnel (CAPES)–Financing Code 001.

Data Availability Statement: No new data were created in this work.

Conflicts of Interest: The authors declare no conflict of interest.

Nomenclature

Abbreviations

AC	Alternate Current
DC	Direct Current
FC	Fuel Cell
MPPT	Maximum Power Point Tracking
PI	Proportional–Integral
PV	Photovoltaic
VMC	Voltage Multiplier Cell
ZCS	Zero Current Switching

Symbols

ΔI_{Lm}	Current ripple on L_m
Δt_i	Interval of the i-th operating stage
ΔV_{C1}, ΔV_{C2}, ΔV_{C3}	Voltage ripple on C_1, C_2 and C_3
λ	Inductance factor 1
ω_o	Resonant angular frequency
A	Simplifying term
C_{eq1}	Equivalent capacitance
D	Duty cycle
f_o	Resonant frequency
f_s	Switching frequency
i_{C1}, i_{C2}, i_{C3}	Instantaneous current on C_1, C_2 and C_3
i_{in}	Instantaneous input current
i_{Lk}	Instantaneous current on L_k
$I_{Lk}(s)$	Laplace transform of i_{Lk}
I_{Lk1}	Current on L_k at $t = t_1$
I_{Lk2}	Current on L_k at $t = t_4$
I_{Lm}	Average value of the current on L_m
I_o	Average value of the output current
k	Inductance factor 2
M	Voltage gain
M_{C1}, M_{C2}, M_{C3}	Partial voltage gains on C_1, C_2 and C_3
n	Number of turns ratio
R_{DSon}	On-resistance of the MOSFET
T_s	Switching period
v_{C1}, v_{C2}, v_{C3}	Instantaneous voltage on C_1, C_2 and C_3
V_{D1}, V_{D2}, V_{D3}	Maximum voltage stress on diodes D_1, D_2 and D_3
V_{in}	Input voltage
V_{GS}	Gate-to-source voltage on the MOSFET
v_{Lk}	Instantaneous voltage on L_k
V_o	Output voltage
V_S	Maximum voltage stress on switch S

References

1. Shubbak, M.H. Advances in solar photovoltaics: Technology review and patent trends. *Renew. Sustain. Energy Rev.* **2019**, *115*, 109383. [CrossRef]
2. Li, Z.; Ma, T.; Yang, H.; Lu, L.; Wang, R. Transparent and colored solar photovoltaics for building integration. *Solar RRL* **2021**, *5*, 2000614. [CrossRef]
3. Premkumar, M.; Subramaniam, U.; Haes Alhelou, H.; Siano, P. Design and Development of Non-Isolated Modified SEPIC DC-DC Converter Topology for High-Step-Up Applications: Investigation and Hardware Implementation. *Energies* **2020**, *13*, 3960. [CrossRef]
4. Zheng, Y.; Smedley, K.M. Analysis and design of a single-switch high step-up coupled-inductor boost converter. *IEEE Trans. Power Electron.* **2020**, *35*, 535–545. [CrossRef]
5. Hass, E.S.; Nascimento, C.B. A simple self-clamped high step-up DC-DC converter employing coupled inductor. *Braz. Power Electron. J.* **2019**, *24*, 204–213.
6. Rosas, I.P.; Agostini, E.; Nascimento, C.B. Single-switch high-step-up DC-DC converter employing coupled inductor and voltage multiplier cell. *IEEE Access* **2022**, *10*, 82626–82635. [CrossRef]
7. Wu, Y.-E.; Wu, Y.-L. Design and Implementation of a High Efficiency, Low Component Voltage Stress, Single-Switch High Step-Up Voltage Converter for Vehicular Green Energy Systems. *Energies* **2016**, *9*, 772. [CrossRef]
8. Rahimi, T.; Islam, M.R.; Gholizadeh, H.; Mahdizadeh, S.; Afjei, E. Design and Implementation of a High Step-Up DC-DC Converter Based on the Conventional Boost and Buck-Boost Converters with High Value of the Efficiency Suitable for Renewable Application. *Sustainability* **2021**, *13*, 10699. [CrossRef]
9. Pereira, A.V.C.; Cavalcanti, M.C.; Azevedo, G.M.; Bradaschia, F.; Neto, R.C.; Santos de Carvalho, M.R. A Novel Single-Switch High Step-Up DC–DC Converter with Three-Winding Coupled Inductor. *Energies* **2021**, *14*, 6288. [CrossRef]
10. Li, W.; He, X. Review of nonisolated high-step-up DC/DC converters in photovoltaic grid-connected applications. *IEEE Trans. Ind. Electron.* **2011**, *58*, 1239–1250. [CrossRef]
11. Liu, H.; Hu, H.; Wu, H.; Xing, Y.; Batarseh, I. Overview of high-step-up coupled-inductor boost converters. *IEEE J. Emerg. Sel. Top. Power Electron.* **2016**, *4*, 689–704. [CrossRef]
12. Forouzesh, M.; Siwakoti, Y.P.; Gorji, S.A.; Blaabjerg, F.; Lehman, B. Step-up DC–DC converters: A comprehensive review of voltage-boosting techniques, topologies, and applications. *IEEE Trans. Power Electron.* **2017**, *32*, 9143–9178. [CrossRef]
13. Tseng, K.C.; Liang, T.J. Novel high-efficiency step-up converter. *IEE Proc. Electr. Power Appl.* **2004**, *151*, 182–190. [CrossRef]
14. Baek, J.-W.; Ryoo, M.-H.; Kim, T.-J.; Yoo, D.-W.; Kim, J.-S. High Boost Converter Using Voltage Multiplier. In Proceedings of the 31st Annual Conference of IEEE Industrial Electronics Society (IECON), Raleigh, NC, USA, 6–10 November 2005.
15. Hsieh, Y.-P.; Chen, J.-F.; Liang, T.-J.; Yang, L.-S. A novel high step-up DC–DC converter for a microgrid system. *IEEE Trans. Power Electron.* **2011**, *26*, 1127–1136. [CrossRef]
16. Wai, R.-J.; Duan, R.-Y. High step-up converter with coupled inductor. *IEEE Trans. Power Electron.* **2005**, *20*, 1025–1035. [CrossRef]
17. Hu, X.; Gong, C. A High Voltage Gain DC–DC Converter Integrating Coupled-Inductor and Diode–Capacitor Techniques. *IEEE Trans. Power Electron.* **2014**, *29*, 789–800.
18. Abbasian, S.; Farsijani, M. A single-switch high step-up Zero Current Switching DC-DC converter based on three-winding coupled inductor and voltage multiplier cells with quasi resonant operation. *Int. J. Circ. Theory Appl.* **2022**, *50*, 4419–4433. [CrossRef]
19. Schmitz, L.; Martins, D.C.; Coelho, R.F. Generalized high step-up DC-DC boost-based converter with gain cell. *IEEE Trans. Circ. Syst. I Reg. Papers* **2017**, *64*, 480–493. [CrossRef]
20. Lee, H.-S.; Yun, J.-J. Quasi-resonant voltage doubler with snubber capacitor for boost half-bridge DC–DC converter in photovoltaic micro-inverter. *IEEE Trans. Power Electron.* **2019**, *34*, 8377–8388. [CrossRef]
21. Hasanpour, S.; Baghramian, A.; Mojallali, H. A modified SEPIC-based high step-up DC–DC converter with quasi-resonant operation for renewable energy applications. *IEEE Trans. Ind. Electron.* **2019**, *66*, 3539–3549. [CrossRef]
22. Roshandel, E.; Mahmoudi, A.; Kahourzade, S.; Emami, H.D. DC-DC High-Step-Up Quasi-Resonant Converter to Drive Acoustic Transmitters. *Energies* **2022**, *15*, 5745. [CrossRef]

Disclaimer/Publisher's Note: The statements, opinions and data contained in all publications are solely those of the individual author(s) and contributor(s) and not of MDPI and/or the editor(s). MDPI and/or the editor(s) disclaim responsibility for any injury to people or property resulting from any ideas, methods, instructions or products referred to in the content.