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Research on a Modeling and Control Strategy for Interleaved Boost Converters with Coupled Inductors

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Abstract: Interleaved DC–DC converters have significant advantages in improving the capability of power converters, and coupling the filtering inductor of the converter could further increase the power density. However, existing modeling and controller designs are complex and require multiple sensors to be involved in the control, which is not conducive to engineering implementation and reducing production costs. In view of this problem, taking a two-phase interleaved boost converter with a coupled inductor as an example, the small-signal models of the converter are derived for the resistive load and constant voltage source load using the state averaging method. The total inductor current is engaged in the control as a feedback signal, avoiding the coupling effect of the inductor on increasing the complexity of the controller. Based on this, a double closed-loop controller is designed, and a prototype of the two-phase interleaved boost converter with coupled inductor is built. Only one current sensor and one voltage sensor are required to participate in the control. The effectiveness of the analysis and design in this paper are verified by experiments.

Keywords: coupled inductors; interleaved boost; small-signal model; DC–DC converters; controller design

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1. Introduction

High-power, high-efficiency DC–DC converters are essential to the development process of modern industry. DC–DC converters efficiently convert and regulate DC voltage levels to suit the needs of electronic applications and are widely utilized in electric vehicles, aviation, navigation, renewable energy generation, etc., where the requirements for their power density are becoming increasingly demanding [1,2]. Traditional DC–DC converters, such as synchronous boost and buck converters, have the advantages of lower cost, lower complexity, and ease of implementation [3]. However, the limitations of the voltage and current capacity of the power semiconductors make it difficult to apply them to high-power applications [4–7].

To solve this problem, the original high-power system is divided into multiple low-power systems using interleaved technology to reduce the current stress of the power semiconductors. The interleaved parallel technique is achieved using N power converter modules in parallel, each with the same drive signal frequency and duty cycle but staggered in phase by an angle of $2\pi/N$. This technology makes it possible to meet the needs of high-power applications while maintaining the power level of the original devices. Interleaved DC–DC converters also offer the following advantages [8–10]: first, they could reduce voltage and current ripple, lower converter losses, and reduce filter size; second, they increase the equivalent switching frequency, which improves the dynamic response of the system. In addition, magnetic integration technology could be used to reduce the number of magnetic components by replacing the discrete inductors of each phase bridge arm with coupled inductors, which further improves the power density and reduces the cost [11–13]. A reasonable selection of the coupling inductor parameters can also achieve better dynamic and static performances [14].

However, the interleaved technique increases the number of circuit elements and makes the operating modes more complex than single-phase converters because of the misalignment of the two phases' ON-time [15]. In addition, the coupling effect of the inductors results in the phase currents not being independent, making it challenging to analyze the transient and steady-state characteristics of the converter. Consequently, to improve the dynamic and static performances of an interleaved DC–DC converter with a coupled inductor and to maximize its operational capability, it is necessary to analyze its mechanism of operation thoroughly, establish the mathematical model, and design a control strategy on this basis.

The actual operation of the converter is inevitably affected by the external environment. An appropriate control strategy and compensation network are essential for the stability and reliability of the system. In order to design a converter with a reasonable control performance, it is necessary to conduct small-signal analysis and transfer function derivation. The state-space averaging method is a popular approach for DC–DC converter modeling [16–18]. For interleaved DC–DC converters, the process of small-signal modeling has been proposed in [19–23]. A small-signal model of the interleaved boost using the state-space averaging method was developed by D. Maksimovic and A. Davoudi et. al., and an analog PID controller was designed [19,20]. H. M. M. Swamy et. al. used the state-space averaging method to analyze the operation of a two-phase interleaved buck converter in a high-power, high-intensity discharge lamp supply [21]. However, the above literature used discrete inductors, which differ from the small-signal modeling process of DC–DC converters with coupled inductors. N. Jantharamin et al. derived a complete small-signal model of a two-phase interleaved boost converter with a reverse-coupled inductor in a continuous–conduction mode (CCM) and a discontinuous–conduction mode (DCM), which was then verified by a sweeping experiment [22]. A. C. Schittler et al. compared the small-signal models of a two-phase interleaved boost converter using discrete inductors, direct-coupled inductors, and reverse-coupled inductors [23]. The paper verified that the reverse-coupled inductor has a high bandwidth and a high-quality factor in the closed-loop system. However, in both [22,23], separate current loop controllers were designed for each phase based on the duty cycle to a single-phase inductor current transfer function. As the number of phases increases, this strategy increases the complexity of the controller and requires more current sensors for the inductor current feedback.

As can be seen from this discussion, while there are many models of both discrete inductor and coupled-inductor multiphase boost converters, little research has been presented on the simplified small-signal model and single current sensor control strategy when utilizing a coupled inductor. In view of the above problems, this paper modeled an interleaved boost converter with a coupled inductor operating in the CCM and designed the controller based on the duty cycle to the total inductor current transfer function. To ensure the accuracy of the model, the ESR of the inductors and capacitors were considered. The following content of this paper is organized as follows. In Section 2, the small-signal model and transfer function of the converter for the resistive load are derived, and the case where the load degrades to a constant voltage source is considered. Based on the transfer function in Section 2, a closed-loop control strategy for the interleaved boost converter with a coupled inductor is designed in Section 3. The voltage and a current double closed-loop control are adopted for the resistive load, a single-current closed-loop control is used for the voltage source load, and the PI parameters are designed for both cases. In Section 4, the effectiveness of the modeling and control is verified using a 2 kW interleaved boost converter with a coupled inductor prototype.

2. Modeling of Interleaved Boost Converter with Coupled Inductor

The topology of the two-phase interleaved boost converter with a coupled inductor is shown in Figure 1. The synchronous rectification topology is used here to help reduce losses while ensuring that the converter can still operate in the CCM when a negative inductor current is generated during one switching cycle. In the interleaved boost topology,

two phases share the input and output ports, and the filtering inductor at the input port uses a reverse-coupled inductor. In Figure 1, L_1 and L_2 form the coupled inductor, with self-inductance $L_1 = L_2 = L$; the mutual inductance is M; R_L and R_C are the equivalent series resistance (ESR) of the inductor and output capacitor, respectively; v_s and v_o are the input and output voltages, respectively; i_{L1}, i_{L2}, and i_L are the currents corresponding to each inductor branch and the total input current, respectively; Q_1~Q_4 are the MOSFETs; and C is the output capacitance. The load can be a resistive load or a constant voltage source. The following content mainly analyzes the resistive load, and the analysis process is similar when the load is a constant voltage source. Therefore, the key conclusions are given without further elaboration.

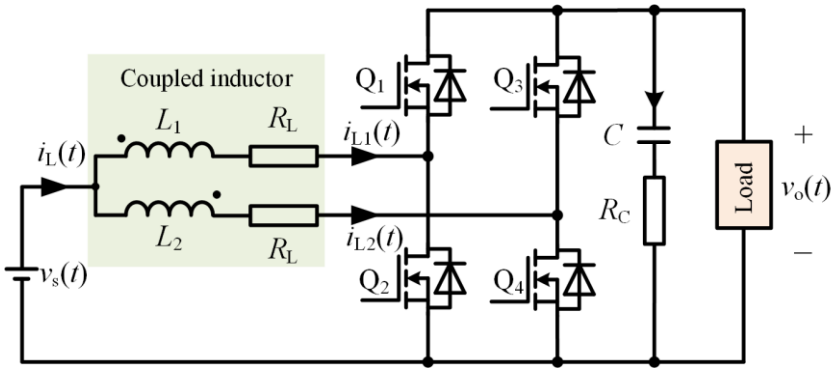


Figure 1. Two-phase interleaved boost topology with a coupled inductor.

2.1. Large-Signal Model

The converter operates in the CCM, and the energy flow is mainly controlled by Q_2 and Q_4, whose duty cycle can be continuously adjusted within a specific range. Q_1 and Q_2 are 180° complementary, Q_3 and Q_4 are 180° complementary, and Q_2 and Q_4 are 180° phase-shifted conduction. The drive and inductor current waveforms at steady state are shown in Figure 2, where v_{gs2} and v_{gs4} represent the gate drive signals of Q_2 and Q_4, respectively, shifted by half of a switching cycle. Without considering the dead band, there are four operating modes in one switching cycle. The equations established for each operating mode are as follows.

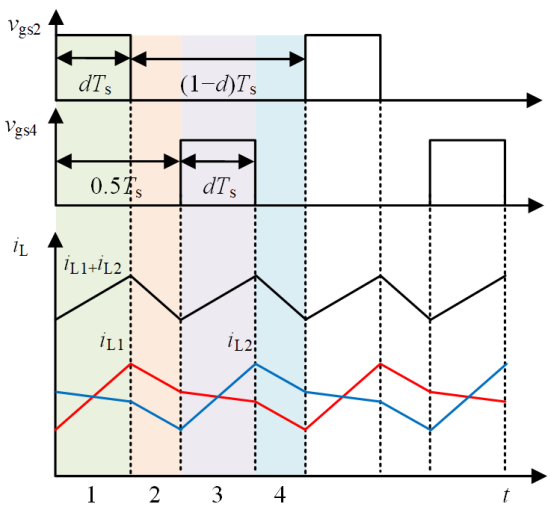


Figure 2. Drive waveforms and inductor current waveforms.

Operating mode 1 [0, dT_s], where switch Q_2 is turned on, and switch Q_4 is turned off. The input voltage source charges the inductor L_1 through Q_2, and the current i_{L1} increases linearly. The inductor L_2 discharges to the output port together with the input voltage source through Q_3, and the current i_{L2} decreases linearly. The state-space equation at this time is shown in Equation (1):

$$\begin{cases} L_1\dfrac{\mathrm{d}i_{L1}(t)}{\mathrm{d}t} - M\dfrac{\mathrm{d}i_{L2}(t)}{\mathrm{d}t} = v_s(t) - i_{L1}(t)R_L \\ L_2\dfrac{\mathrm{d}i_{L2}(t)}{\mathrm{d}t} - M\dfrac{\mathrm{d}i_{L1}(t)}{\mathrm{d}t} = v_s(t) - i_{L2}(t)R_L - v_o(t) \\ C\dfrac{\mathrm{d}v_c(t)}{\mathrm{d}t} = i_{L2}(t) - \dfrac{v_o(t)}{R} \end{cases} \tag{1}$$

Operating mode 2 [dT_s, $0.5T_s$], where the switches Q_2 and Q_4 are turned off. The inductor L_1 discharges to the output port together with the input voltage source through Q_1, and the inductor L_2 discharges to the output port together with the input voltage source through Q_3. Both of currents i_{L1} and i_{L2} decrease linearly. The state-space equation at this time is shown in Equation (2):

$$\begin{cases} L_1\dfrac{\mathrm{d}i_{L1}(t)}{\mathrm{d}t} - M\dfrac{\mathrm{d}i_{L2}(t)}{\mathrm{d}t} = v_s(t) - i_{L1}(t)R_L - v_o(t) \\ L_2\dfrac{\mathrm{d}i_{L2}(t)}{\mathrm{d}t} - M\dfrac{\mathrm{d}i_{L1}(t)}{\mathrm{d}t} = v_s(t) - i_{L2}(t)R_L - v_o(t) \\ C\dfrac{\mathrm{d}v_c(t)}{\mathrm{d}t} = i_{L1}(t) + i_{L2}(t) - \dfrac{v_o(t)}{R} \end{cases} \tag{2}$$

Operating mode 3 [$0.5T_s$, $(0.5 + d)T_s$], where switch Q_2 is turned off and switch Q_4 is turned on. The inductor L_1 discharges to the output port together with the input voltage source through Q_1, and the current i_{L1} decreases linearly. The input voltage source charges the inductor L_2 through Q_4, and the current i_{L2} increases linearly. The state-space equation at this time is shown in Equation (3):

$$\begin{cases} L_1\dfrac{\mathrm{d}i_{L1}(t)}{\mathrm{d}t} - M\dfrac{\mathrm{d}i_{L2}(t)}{\mathrm{d}t} = v_s(t) - i_{L1}(t)R_L - v_o(t) \\ L_2\dfrac{\mathrm{d}i_{L2}(t)}{\mathrm{d}t} - M\dfrac{\mathrm{d}i_{L1}(t)}{\mathrm{d}t} = v_s(t) - i_{L2}(t)R_L \\ C\dfrac{\mathrm{d}v_c(t)}{\mathrm{d}t} = i_{L1}(t) - \dfrac{v_o(t)}{R} \end{cases} \tag{3}$$

Operating mode 4 [$(0.5 + d)T_s$, T_s], where the switches Q_2 and Q_4 are turned off. The energy flow process at this time is the same as that of Operating mode 2, and we obtain:

$$\begin{cases} L_1\dfrac{\mathrm{d}i_{L1}(t)}{\mathrm{d}t} - M\dfrac{\mathrm{d}i_{L2}(t)}{\mathrm{d}t} = v_s(t) - i_{L1}(t)R_L - v_o(t) \\ L_2\dfrac{\mathrm{d}i_{L2}(t)}{\mathrm{d}t} - M\dfrac{\mathrm{d}i_{L1}(t)}{\mathrm{d}t} = v_s(t) - i_{L2}(t)R_L - v_o(t) \\ C\dfrac{\mathrm{d}v_c(t)}{\mathrm{d}t} = i_{L1}(t) + i_{L2}(t) - \dfrac{v_o(t)}{R} \end{cases} \tag{4}$$

The state-space averaging equation is obtained by averaging the state-space variables over one switching period and is called the large-signal model, which is shown in (5):

$$\begin{cases} L_1 \dfrac{\mathrm{d}\langle i_{\mathrm{L1}}(t)\rangle_{Ts}}{\mathrm{d}t} - M\dfrac{\mathrm{d}\langle i_{\mathrm{L2}}(t)\rangle_{Ts}}{\mathrm{d}t} = \langle v_{\mathrm{s}}(t)\rangle_{Ts} - \langle i_{\mathrm{L1}}(t)\rangle_{Ts} R_{\mathrm{L}} - (1-d)\langle v_{\mathrm{o}}(t)\rangle_{Ts} \\ L_2 \dfrac{\mathrm{d}\langle i_{\mathrm{L2}}(t)\rangle_{Ts}}{\mathrm{d}t} - M\dfrac{\mathrm{d}\langle i_{\mathrm{L1}}(t)\rangle_{Ts}}{\mathrm{d}t} = \langle v_{\mathrm{s}}(t)\rangle_{Ts} - \langle i_{\mathrm{L2}}(t)\rangle_{Ts} R_{\mathrm{L}} - (1-d)\langle v_{\mathrm{o}}(t)\rangle_{Ts} \\ C\dfrac{\mathrm{d}\langle v_{\mathrm{c}}(t)\rangle_{Ts}}{\mathrm{d}t} = (1-d)(\langle i_{\mathrm{L1}}(t)\rangle_{Ts} + \langle i_{\mathrm{L2}}(t)\rangle_{Ts}) - \dfrac{\langle v_{\mathrm{o}}(t)\rangle_{Ts}}{R} \end{cases} \tag{5}$$

where $< >_{Ts}$ means the averaging operation performed on the variables over switching period T_{s}.

2.2. Small-Signal Model

After obtaining the state-space averaging equation, Equation (5) is locally linearized near the static operating point, and the Laplace transform is applied to the state equation. The small-signal model is obtained as (6), where $D' = 1 - D$:

$$\begin{cases} sL_1\hat{i}_{\mathrm{L1}}(s) - sM\hat{i}_{\mathrm{L2}}(s) = \hat{v}_{\mathrm{s}}(s) - \hat{i}_{\mathrm{L1}}(s)R_{\mathrm{L}} - D'\hat{v}_{\mathrm{o}}(s) + V_{\mathrm{o}}\hat{d}(s) \\ sL_2\hat{i}_{\mathrm{L2}}(s) - sM\hat{i}_{\mathrm{L1}}(s) = \hat{v}_{\mathrm{s}}(s) - \hat{i}_{\mathrm{L2}}(s)R_{\mathrm{L}} - D'\hat{v}_{\mathrm{o}}(s) + V_{\mathrm{o}}\hat{d}(s) \\ sC\hat{v}_{\mathrm{c}}(s) = D'(\hat{i}_{\mathrm{L1}}(s) + \hat{i}_{\mathrm{L2}}(s)) - (I_{\mathrm{L1}} + I_{\mathrm{L2}})\hat{d}(s) - \dfrac{\hat{v}_{\mathrm{o}}(s)}{R} \end{cases} \tag{6}$$

It can be seen from (6) that there is a coupling relationship between the inductor currents of the two phases, which complicates the transient analysis. To avoid the added complexity of the coupling effect on the control analysis, two currents are combined into the total input-port current i_{L} ($i_{\mathrm{L}} = i_{\mathrm{L1}} + i_{\mathrm{L2}}$). Equation (6) is further reduced as (7):

$$\begin{cases} \dfrac{L-M}{2}\hat{i}_{\mathrm{L}}(s) = \hat{v}_{\mathrm{s}}(s) - \hat{i}_{\mathrm{L}}(s)R_{\mathrm{L}} - D'\hat{v}_{\mathrm{o}}(s) + V_{\mathrm{o}}\hat{d}(s) \\ sC\hat{v}_{\mathrm{c}}(s) = D'\hat{i}_{\mathrm{L}}(s) - I_{\mathrm{L}}\hat{d}(s) - \dfrac{\hat{v}_{\mathrm{o}}(s)}{R} \end{cases} \tag{7}$$

It can be concluded that the small-signal equation for an interleaved boost converter with a coupled inductor is similar in form to the small-signal equation for a traditional single-phase boost converter. The only difference lies in the inductance. Therefore, the small-signal model of the two-phase interleaved boost converter with a coupled inductor could be equated to the small-signal model of a single-phase boost converter with equivalent inductance $L_{\mathrm{eff}} = (L - M)/2$ and a doubled switching frequency. The analysis of the single-phase boost converter can be used in the subsequent analysis. Figure 3a shows the small-signal AC equivalent circuit of a two-phase interleaved boost converter with coupled inductor for the resistive load. When the load is a constant voltage source, the charging and discharging process of the output capacitor can be neglected due to the constant output voltage. The system is changed from a second-order system to a first-order system, at which point the AC equivalent circuit is shown in Figure 3b.

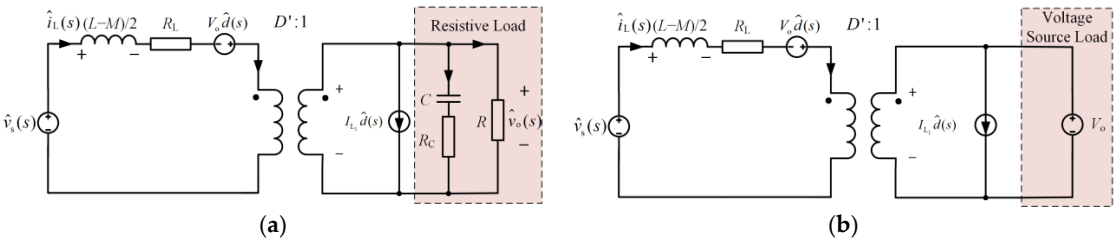


Figure 3. (**a**) Small-signal AC equivalent circuit for the resistive load; (**b**) small-signal AC equivalent circuit for the voltage source.

2.3. Transfer Functions

According to the derivation in the previous section, the open-loop transfer functions of the two-phase interleaved boost converter with a coupled inductor can be obtained. The transfer functions for the resistive load are shown in Table 1.

From the above table, it can be seen that the two-phase interleaved boost converter with a coupled inductor still has a right half-plane zero, whose frequency can be calculated using the following formula:

$$f_{\mathrm{RHPZ}} = \frac{D'^2R - R_{\mathrm{L}}}{2\pi L_{\mathrm{eff}}} \tag{8}$$

The reduction in the equivalent inductance causes the right half-plane zero to appear in the higher frequency band, ensuring that the converter can achieve a higher bandwidth.

Table 1. Transfer functions of the interleaved boost converter with a coupled inductor.

Item	Expression
$G_{\mathrm{vd}}(s) = \frac{\hat{v}_{\mathrm{o}}(s)}{\hat{d}(s)}$	$\frac{V_{\mathrm{o}}(D'^2R - R_{\mathrm{L}})}{D'(D'^2R + R_{\mathrm{L}})} \frac{-\frac{R_{\mathrm{C}}CL_{\mathrm{eff}}}{D'^2R - R_{\mathrm{L}}}s^2 + \frac{-L_{\mathrm{eff}} + R_{\mathrm{C}}CD'^2R - R_{\mathrm{L}}R_{\mathrm{C}}C}{D'^2R - R_{\mathrm{L}}}s + 1}{\frac{RL_{\mathrm{eff}}C + R_{\mathrm{C}}L_{\mathrm{eff}}C}{D'^2R + R_{\mathrm{L}}}s^2 + \frac{L_{\mathrm{eff}} + RCR_{\mathrm{L}} + CR_{\mathrm{C}}R_{\mathrm{L}} + RCR_{\mathrm{C}}D'^2}{D'^2R + R_{\mathrm{L}}}s + 1}$
$G_{\mathrm{id}}(s) = \frac{\hat{i}_{\mathrm{L}}(s)}{\hat{d}(s)}$	$\frac{2V_{\mathrm{o}}}{D'^2R + R_{\mathrm{L}}} \frac{(R/2 + R_{\mathrm{C}})Cs + 1}{\frac{RL_{\mathrm{eff}}C + R_{\mathrm{C}}L_{\mathrm{eff}}C}{D'^2R + R_{\mathrm{L}}}s^2 + \frac{L_{\mathrm{eff}} + RCR_{\mathrm{L}} + CR_{\mathrm{C}}R_{\mathrm{L}} + RCR_{\mathrm{C}}D'^2}{D'^2R + R_{\mathrm{L}}}s + 1}$
$G_{\mathrm{vi}}(s) = \frac{\hat{v}_{\mathrm{o}}(s)}{\hat{i}_{\mathrm{L}}(s)}$	$\frac{(D'^2R - R_{\mathrm{L}})}{2D'} \frac{-\frac{R_{\mathrm{C}}CL_{\mathrm{eff}}}{D'^2R - R_{\mathrm{L}}}s^2 + \frac{-L_{\mathrm{eff}} + R_{\mathrm{C}}CD'^2R - R_{\mathrm{L}}R_{\mathrm{C}}C}{D'^2R - R_{\mathrm{L}}}s + 1}{(R/2 + R_{\mathrm{C}})Cs + 1}$
$G_{\mathrm{vs}}(s) = \frac{\hat{v}_{\mathrm{o}}(s)}{\hat{v}_{\mathrm{s}}(s)}$	$\frac{D'R}{D'^2R + R_{\mathrm{L}}} \frac{R_{\mathrm{C}}Cs + 1}{\frac{RL_{\mathrm{eff}}C + R_{\mathrm{C}}L_{\mathrm{eff}}C}{D'^2R + R_{\mathrm{L}}}s^2 + \frac{L_{\mathrm{eff}} + RCR_{\mathrm{L}} + CR_{\mathrm{C}}R_{\mathrm{L}} + RCR_{\mathrm{C}}D'^2}{D'^2R + R_{\mathrm{L}}}s + 1}$
$G_{\mathrm{is}}(s) = \frac{\hat{i}_{\mathrm{L}}(s)}{\hat{v}_{\mathrm{s}}(s)}$	$\frac{1}{D'^2R + R_{\mathrm{L}}} \frac{(R + R_{\mathrm{C}})Cs + 1}{\frac{RL_{\mathrm{eff}}C + R_{\mathrm{C}}L_{\mathrm{eff}}C}{D'^2R + R_{\mathrm{L}}}s^2 + \frac{L_{\mathrm{eff}} + RCR_{\mathrm{L}} + CR_{\mathrm{C}}R_{\mathrm{L}} + RCR_{\mathrm{C}}D'^2}{D'^2R + R_{\mathrm{L}}}s + 1}$
$Z_{\mathrm{p}}(s) = \frac{\hat{v}_{\mathrm{o}}(s)}{\hat{i}_{\mathrm{o}}(s)}$	$\frac{RR_{\mathrm{L}}}{D'^2R + R_{\mathrm{L}}} \frac{R_{\mathrm{C}}L_{\mathrm{eff}}C/R_{\mathrm{L}}s^2 + (L_{\mathrm{eff}}/R_{\mathrm{L}} + R_{\mathrm{C}}C)s + 1}{\frac{RL_{\mathrm{eff}}C + R_{\mathrm{C}}L_{\mathrm{eff}}C}{D'^2R + R_{\mathrm{L}}}s^2 + \frac{L_{\mathrm{eff}} + RCR_{\mathrm{L}} + CR_{\mathrm{C}}R_{\mathrm{L}} + RCR_{\mathrm{C}}D'^2}{D'^2R + R_{\mathrm{L}}}s + 1}$
$Z_{\mathrm{q}}(s) = \frac{\hat{i}_{\mathrm{L}}(s)}{\hat{i}_{\mathrm{o}}(s)}$	$-\frac{D'R}{D'^2R + R_{\mathrm{L}}} \frac{R_{\mathrm{C}}Cs + 1}{\frac{RL_{\mathrm{eff}}C + R_{\mathrm{C}}L_{\mathrm{eff}}C}{D'^2R + R_{\mathrm{L}}}s^2 + \frac{L_{\mathrm{eff}} + RCR_{\mathrm{L}} + CR_{\mathrm{C}}R_{\mathrm{L}} + RCR_{\mathrm{C}}D'^2}{D'^2R + R_{\mathrm{L}}}s + 1}$

When the load is a constant voltage source, the duty cycle to total inductor current transfer function is as follows, which is characterized as a first-order inertia process:

$$G_{\mathrm{id}}(s) = \left.\frac{i_{\mathrm{L}}(s)}{\hat{d}(s)}\right|_{\hat{v}_s(s)=0} = \frac{V_{\mathrm{o}}}{sL_{\mathrm{eff}} + R_{\mathrm{L}}} \tag{9}$$

The derivation of the transfer function helps in the analysis and design of the control loop, which is discussed in detail in the next section.

3. Controller Design for Converter

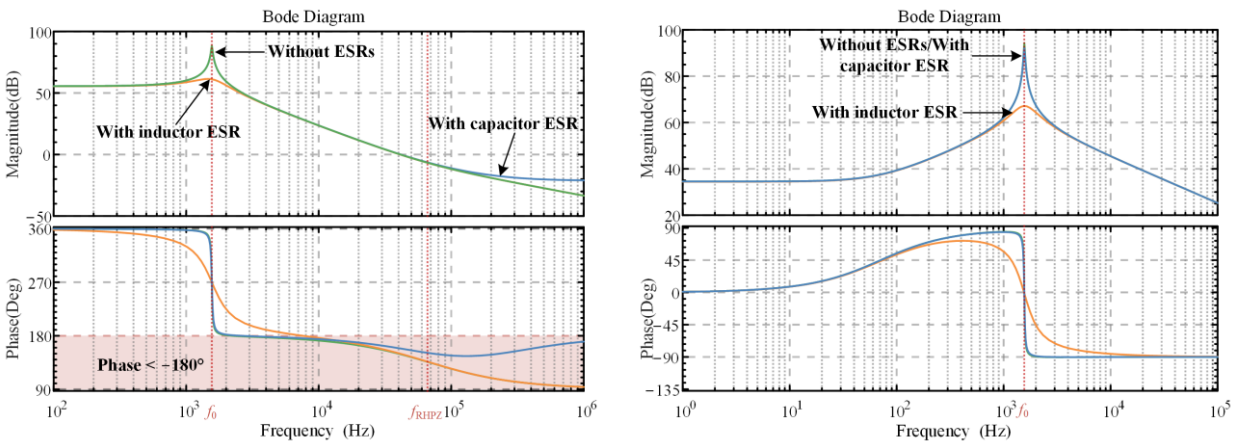
This section proposes a controller design method for the two-phase interleaved boost converter with a coupled inductor based on the mathematical model derived from the previous derivation. This approach considers the influence of ESR of the energy storage component on the frequency domain analysis and designs the controller through the total

inductor current, which has the advantage of a simple control structure and achieves a high control accuracy and a fast response speed. The design parameters of the two-phase interleaved boost converter with a coupled inductor in this paper are summarized in Table 2.

Table 2. The parameters of the two-phase interleaved boost converter with a coupled inductor.

Parameter	Value
Rated Power (kW)	2
Input Voltage (V)	150
Output Voltage (V)	300
Switching Frequency (kHz)	40
Self-Inductance (μH)	76
Mutual Inductance (μH)	24
Output Capacitor (μF)	100
ESR of Inductor (mΩ)	126
ESR of Capacitor (mΩ)	6.5

The system orders are different when the converter output is connected to a resistive load and a voltage source load, so the controller was designed separately for them. Figure 4 shows a Bode diagram of the open-loop transfer functions G_{vd} and G_{id} for the resistive load, taking into account the effect of the ESRs of the inductor and capacitor on the system. It can be seen that the system resonates at 1.56 kHz (f_0). The ESRs help to mitigate the resonant effect by reducing the resonant peak and slowing down the phase delay. In this design case, the ESR of the inductor is relatively larger than that of the capacitor, for which its effect is more noticeable. As can be observed from the high-frequency band of the G_{vd}'s Bode diagram, the right half-plane zero causes a 90° phase delay to the system and increases the gain. The ESR of the capacitor reduces the hysteresis effect of this right half-plane zero but further increases the gain in the high-frequency band. According to (8), the right half-plane zero frequency f_{RHPZ} = 68 kHz, and the phase remains close to or lower than −180° from the middle to the high frequency. According to the above analysis, the unfavorable amplitude and phase characteristics of the duty cycle to the output voltage transfer function G_{vd} make it difficult to obtain a satisfactory closed-loop performance with single voltage-loop compensation. As a result, a voltage and current double closed-loop control strategy is considered.



(**a**) (**b**)

Figure 4. (**a**) Duty cycle to the output voltage transfer function G_{vd}; (**b**) duty cycle to the total inductor current transfer function G_{id}.

3.1. PI Parameter Design for Resistive Load

According to the above analysis, a double closed-loop control was used to improve the transient characteristics of the converter for the resistive load. A control block diagram of the dual closed-loop control is shown in Figure 5, where $F_m = 1/V_m$ is the transfer function of the PWM modulation; $V_m = 1$; $H_i(s)$ and $H_v(s)$ are the feedbacks; G_{cv} and G_{ci} are the voltage loop PI controller and current loop PI controller, respectively; and the transfer functions are as follows:

$$G_{cv}(s) = \frac{K_{vp}s + K_{vi}}{s} \tag{10}$$

$$G_{ci}(s) = \frac{K_{ip}s + K_{ii}}{s} \tag{11}$$

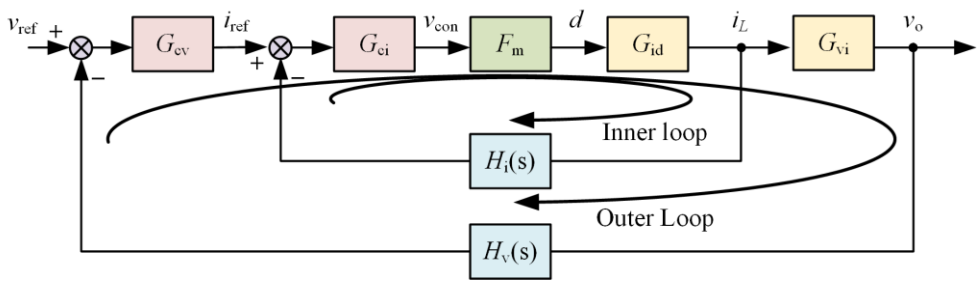


Figure 5. Block diagram of the double closed-loop control.

The feedback of the voltage and current loops are both low-pass filters with a cut-off frequency of 20 kHz, and the transfer function is shown in (12):

$$H_v(s) = H_i(s) = \frac{1}{\frac{1}{2\pi \cdot 20000}s + 1} \tag{12}$$

Considering the delay caused by the digital control, the delay process is introduced and the first-order approximation is made to the first-order inertia process with the following transfer function:

$$G_d(s) \approx \frac{1}{T_s s + 1} \tag{13}$$

Bode diagrams of the current inner-loop compensation and voltage outer-loop compensation are shown in Figure 6. As shown in Figure 6a, the crossover frequency of the current inner loop is too high, and the gain margin and phase margin are negative, which is not conducive to system stability. When selecting the crossover frequency, a variety of factors should be taken into consideration, both to reduce the high-frequency noise caused by the switching frequency and to meet the dynamic performance requirements. At the same time, the crossover frequency should be significantly higher than the resonant frequency to provide enough gain at the peak to eliminate resonance. On balance, the control parameters of the current inner loop were selected as $K_{ip} = 0.0034$ and $K_{ii} = 10$, at which point the crossing frequency of the current inner loop was reduced from 60 kHz to 5 kHz, with a phase margin of $PM = 42°$. On the basis of the determination of the parameters of the current inner loop, a Bode diagram of the voltage outer loop was drawn, as shown in Figure 6b. In order to ensure that the current loop can track the current reference output by the voltage outer-loop controller in time, the response speed of the current inner loop needs to be significantly higher than that of the voltage outer loop. Therefore, the crossover frequency of the outer loop is usually designed to be approximately one-fifth of that of the inner loop [24]. As can be seen from Figure 6b, the crossover frequency of the voltage loop is too low, which is also not conducive to the fast response of the system. Finally, the control parameters of the voltage loop are selected as $K_{vp} = 1.57$ and $K_{vi} = 101$, which increases

the crossover frequency, and the crossover frequency is f_c = 1 kHz and the phase margin is PM = 90°. The total PI controller parameters for the resistive load are shown in Table 3.

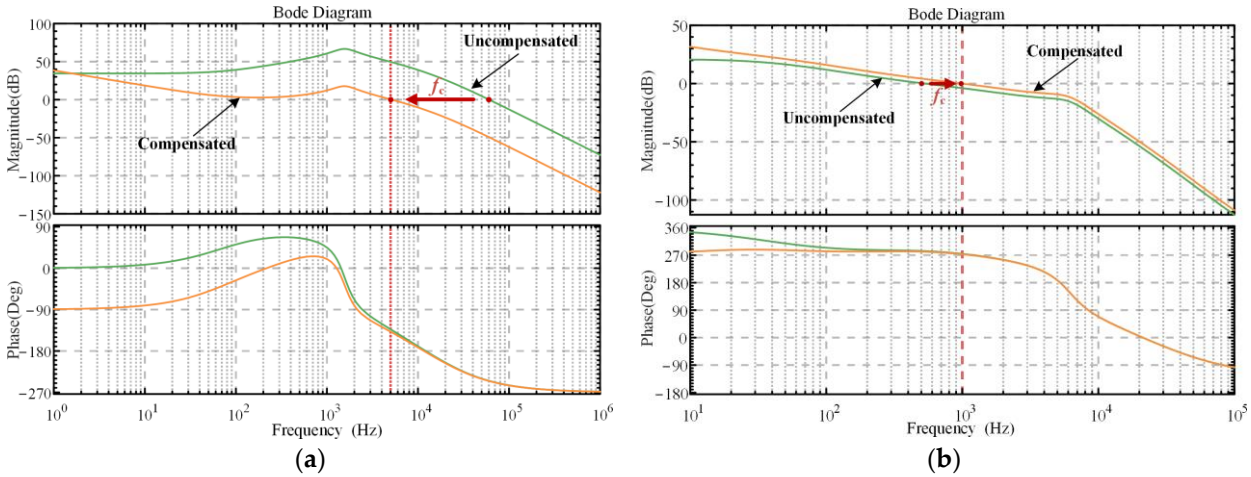


Figure 6. (**a**) Compensation of the current inner loop; (**b**) compensation of the voltage outer loop.

Table 3. The total PI controller parameters for the resistive load.

Item	Proportional Coefficient	Integral Coefficient
Current Inner Loop	0.0034	10
Voltage Outer Loop	1.57	101

The small-signal block diagram when using a double closed-loop control is shown in Figure 7, where $\hat{v}_s$ and $\hat{i}_o$ represent the input voltage small-signal disturbance and load current small-signal disturbance, respectively. The transfer functions in Figure 7 have been given above. The audio sensitivity and the closed-loop output impedance represent the suppression capability of the converter for input noise and load fluctuation, respectively. Taking the closed-loop output impedance as an example, the change in the output voltage after the system is disturbed is determined by the product of the magnitude of the step load change and the peak value of the output impedance together, as shown in Equation (14). It can be seen that the smaller the output impedance, the more stable the output voltage of the converter. Therefore, it is necessary to minimize the audio sensitivity and output impedance to obtain a constant output voltage.

$$v_o(t)_{pp} = I_{step} 10^{|Z_o|_{peak}/20} \tag{14}$$

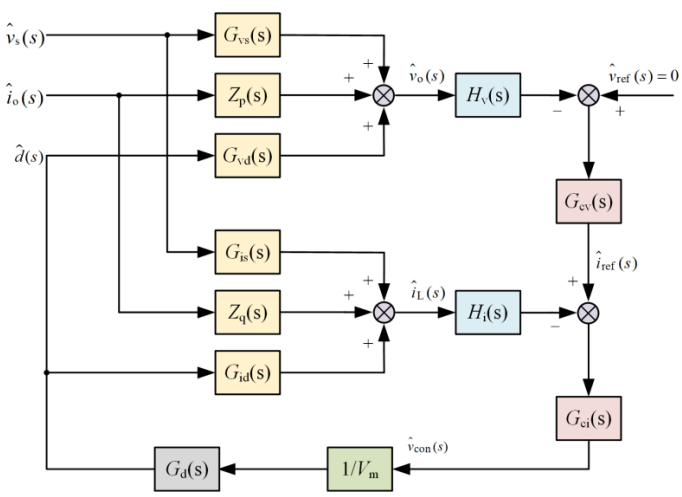


Figure 7. Small-signal block diagram of the double closed-loop control.

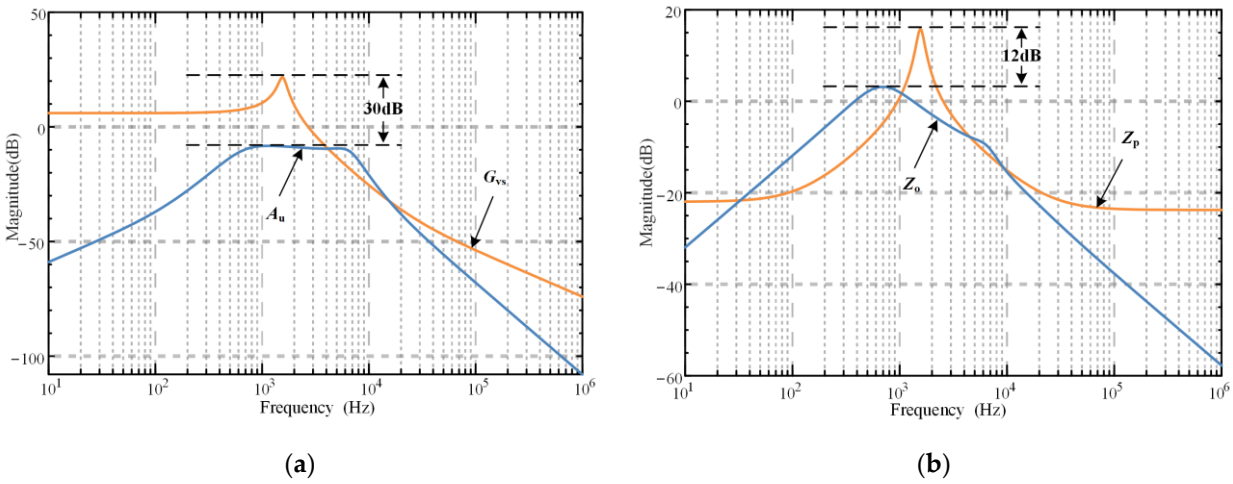
Combined with the above figure, the audio sensitivity is calculated according to the Mason gain formula as (15):

$$A_{\mathrm{u}} = \left.\frac{\hat{v}_{\mathrm{o}}}{\hat{v}_{\mathrm{s}}}\right|_{\mathrm{closed}} = \frac{G_{\mathrm{vs}}H_{\mathrm{v}}V_{\mathrm{m}} + G_{\mathrm{vs}}H_{\mathrm{v}}H_{\mathrm{i}}G_{\mathrm{ci}}G_{\mathrm{id}}G_{\mathrm{d}} - G_{\mathrm{is}}H_{\mathrm{i}}G_{\mathrm{ci}}G_{\mathrm{d}}G_{\mathrm{vd}}H_{\mathrm{v}}}{V_{\mathrm{m}} + G_{\mathrm{cv}}G_{\mathrm{ci}}G_{\mathrm{d}}G_{\mathrm{vd}}H_{\mathrm{i}} + G_{\mathrm{ci}}G_{d}G_{\mathrm{id}}H_{\mathrm{i}}} \tag{15}$$

The closed-loop output impedance is calculated as follows:

$$Z_{\mathrm{o}} = \left.\frac{\hat{v}_{\mathrm{o}}}{\hat{i}_{\mathrm{o}}}\right|_{\mathrm{closed}} = \frac{Z_{\mathrm{p}}H_{\mathrm{v}}V_{\mathrm{m}} + Z_{\mathrm{p}}H_{\mathrm{v}}H_{\mathrm{i}}G_{\mathrm{ci}}G_{\mathrm{id}}G_{\mathrm{d}} - Z_{\mathrm{q}}H_{\mathrm{i}}G_{\mathrm{ci}}G_{\mathrm{d}}G_{\mathrm{vd}}H_{\mathrm{v}}}{V_{\mathrm{m}} + G_{\mathrm{cv}}G_{\mathrm{ci}}G_{\mathrm{d}}G_{\mathrm{vd}}H_{\mathrm{i}} + G_{\mathrm{ci}}G_{d}G_{\mathrm{id}}H_{\mathrm{i}}} \tag{16}$$

Figure 8 shows a Bode diagram comparison between the closed-loop transfer function and the open-loop transfer function. Figure 8a compares the Bode diagram of the audio sensitivity with the input–output transfer function, and the peak of the magnitude decreases by 30 dB. From Figure 8b, it can be observed that the peak of the magnitude curve of the audio sensitivity is 12 dB lower than the open-loop output impedance. The decrease in the peak ensures the output voltage is as constant as possible despite changes in the external conditions.



(**a**) (**b**)

Figure 8. (**a**) Audio sensitivity; (**b**) output impedance.

3.2. PI Parameter Design for the Voltage Source Load

When the load is a voltage source, the current at the input port is the control target, and a single-current closed loop can be used. The control block diagram is shown in Figure 9.

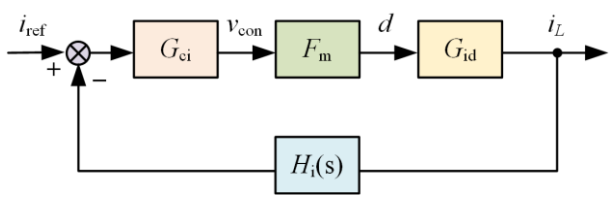


Figure 9. Block diagram of the single-current closed-loop control.

According to (9), the open-loop Bode diagram of the current loop is shown in Figure 10. It can be seen that the crossover frequency of the current loop is too high to meet the dynamic response requirements of the system. At this time, the phase margin is negative, indicating that the system is unstable. After adding the PI controller, the system traverses 0 dB with a slope of −20 dB/dec and has a slope of −40 dB/dec in both the low- and high-frequency bands, taking into account the dynamic response performance and the ability to suppress noise. The controller parameters at this time are chosen as K_{ip} = 0.002, K_{ii} = 1, crossover frequency f_{c} = 4 kHz, and phase margin PM = 60°.

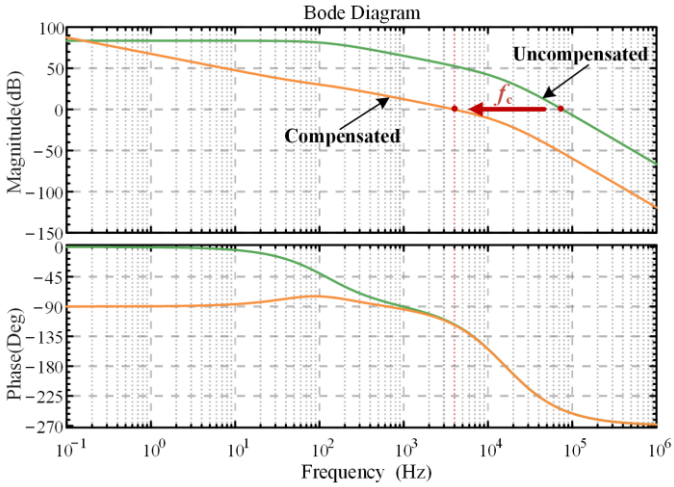


Figure 10. Single-current loop Bode diagram.

4. Experiments—Results and Analysis

To verify the effectiveness of the small-signal model and its controller parameters, a two-phase interleaved boost converter with a coupled inductor experimental platform was constructed in this paper. As shown in Figure 11, the main parameters of the circuit were consistent with Table 2. An LCR (IM3533-01) meter was used to measure the self-inductance, mutual inductance (indirectly measured), and ESR of the inductors and capacitors. The power semiconductor was a SiC MOSFET (FF6MR12W2M1P_B11) from Infineon, the output capacitor was a film capacitor with low ESR, and the coupled inductor was made from a customized core of DMR95 material wound with Litz wire. The controllers of the platform included controllers based on DSP TMS320C28346 and FPGA EP3C80F484I7. The DSP was responsible for executing algorithms, and the FPGA was responsible for the sampling control signals and generating the driving signals.

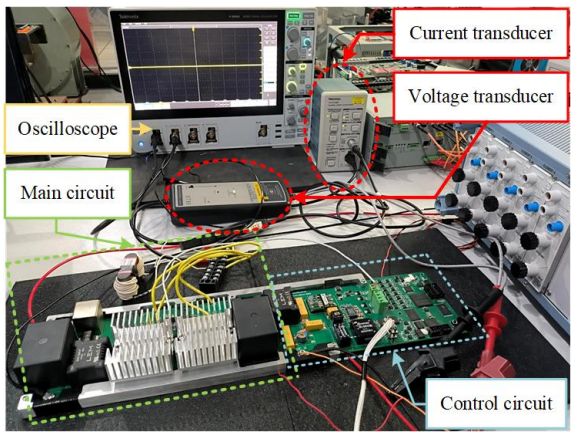


Figure 11. Experimental platform.

The experiment considered two cases where a constant voltage source and a resistive load are connected to the output port. Figure 12 shows the steady and transient response waveforms of the converter for the resistance load. The steady-state waveforms at D < 0.5 and D > 0.5 are depicted in Figures 12a and 12b, respectively. Notably, the current waveform no longer exhibits a triangular shape under the coupling effect. Figure 12c shows the steady-state voltage and current waveforms of the converter, with a single inductor current ripple of approximately 13 A and a total input current ripple of less than 1 A. It is clear that the interleaved structure effectively reduced the input current ripple. The output voltage and current transient response waveforms when the input voltage was quickly adjusted from 150 V to 160 V are shown in Figure 12d. The graphic shows that the output voltage can still

be kept steady at 300 V. Figure 12e shows the change in the output voltage caused by the step change in the load current. When the load resistor was adjusted to make the system load jump from 75% to a full load, the output voltage waveform temporarily dropped to approximately 300 V, with a drop of 4 V. Figure 12f is the response waveform of the voltage and current when the output voltage command was adjusted by the upper computer. When the voltage instruction was modified from 290 to 300 V, there was no visible overshoot, and the voltage response was quick. Figure 13 is the start-up process and the current waveform of the dynamic adjustment of the current command when the output was a constant voltage source. The waveforms show that the current loop control had a fast dynamic response and good steady-state performance. Moreover, the efficiency of the converter is depicted in Figure 14. Figure 14a represents the efficiency curve in the full output power range, and the power was modified by adjusting the input current. Figure 14b shows the efficiency measured near the rated power, which is 98.031%.

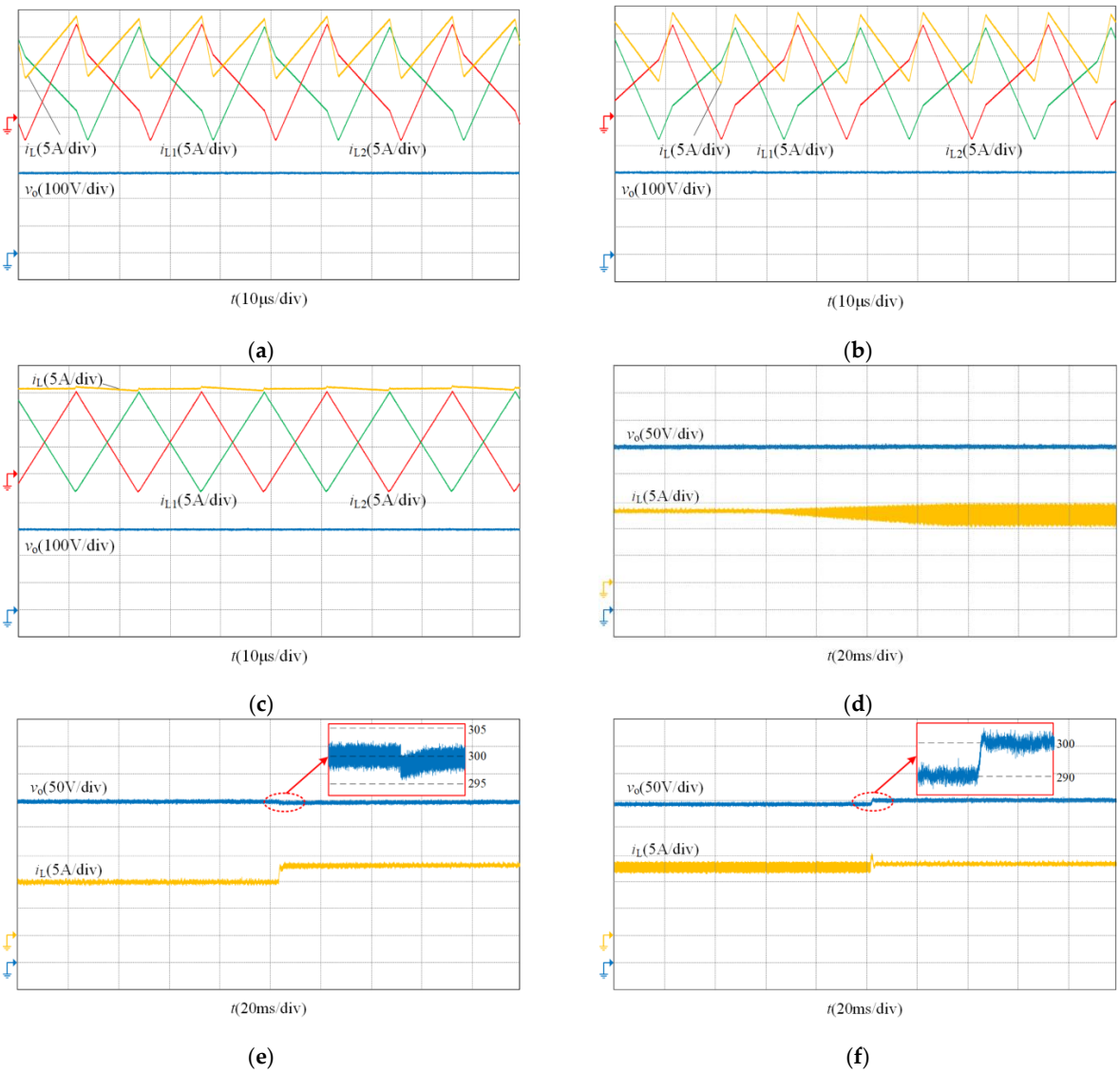
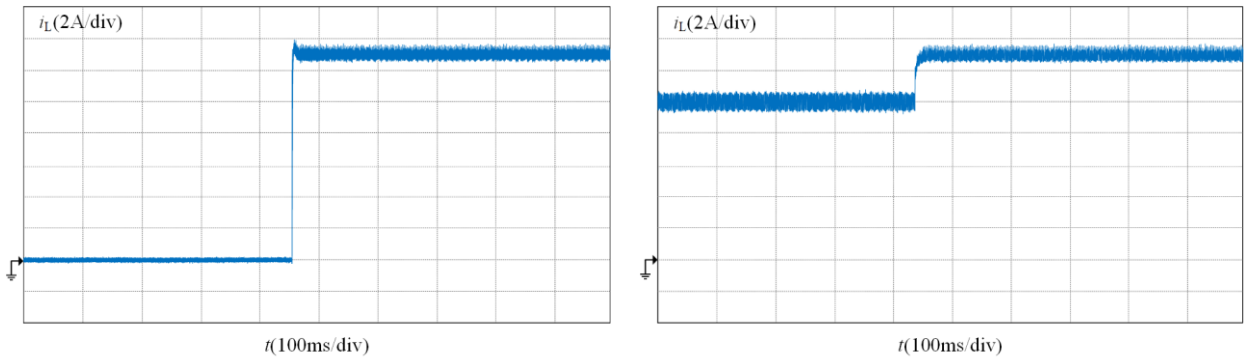
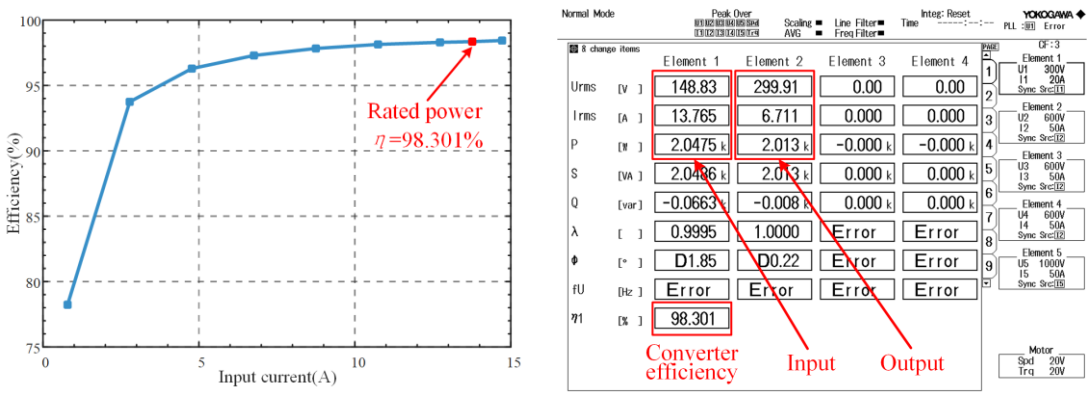


Figure 12. Experimental waveforms of the resistive load: (**a**) steady-state waveform at D < 0.5; (**b**) steady-state waveform at D > 0.5; (**c**) steady-state waveform at D = 0.5; (**d**) step input response; (**e**) step load response; (**f**) regulation of the voltage command.



(**a**) (**b**)

Figure 13. Experimental waveforms of the constant voltage source load; (**a**) start-up process; (**b**) regulation of the current command.



(**a**) (**b**)

Figure 14. (**a**) Experimental efficiency of the two-phase interleaved boost converter with a coupled inductor; (**b**) efficiency measurement of the rated power.

5. Conclusions

In this paper, a small-signal model of a two-phase interleaved boost converter with a coupled inductor operating in the CCM was developed using the state-space averaging method. The model was based on the duty cycle to the total inductor current transfer function and considered the effect of the ESRs of the inductors and capacitors on the accuracy of the model. A dual closed-loop control system consisting of a current inner-loop controller and a voltage outer-loop controller was designed and implemented for the resistive load, while a single-current loop was used to realize the control for the voltage source load. To validate the proposed controller, a 2 kW interleaved boost converter prototype was built and tested. The experimental results demonstrate that the modeling and controller design are effective and ensure good dynamic and steady-state performance while simplifying the control structure.

Because one current sensor is utilized, diagnosing potential current unevenness and faults is challenging. Therefore, future research will focus on diagnosing and resolving the potential issue of current unevenness without increasing the number of circuit sensors and complexity. On the other hand, special focus must be given to the problem of controller optimization by adjusting the structure and parameters of the controller to achieve the optimum performance of the converter. Another future research is aimed at integrating a magnetics design, which has a positive effect on increasing the efficiency and power density of the system.

As mentioned, future work should focus further on efficiency and power density improvements, fault detection, and also on controller optimization.

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