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A Dynamic Multi-Cell FCL to Improve the Fault Ride through Capability of DFIG-Based Wind Farms

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Abstract: Endowing wind farms (WFs) with fault ride through (FRT) capability is crucial to their continuous availability under various operating conditions. This paper proposes a dynamic adaptive multi-cell fault current limiter (MCFCL) topology to enhance the FRT capability of grid connected WFs. The proposed MCFCL consists of one transient cell (TC) and multi resistive cells (RCs) directly connected to the grid's high voltage without using any series injection transformers nor any series connection of semiconductor switches. The transient cell of the MCFCL includes two transient limiting reactors (TLRs) to mitigate the transient fault current and limit the rate of change of the currents of the semiconductor switches during fault occurrence. The number of RCs in the MCFCL is determined based on voltage sag level. These latter are inserted in the fault path to provide an adaptive voltage sag compensation mechanism according to the voltage sag level. Assessment of the MCFCL under various sag conditions, showed that the MCFCL is able to effectively compensate for a wide range of voltage sags without any over voltage at the WF's terminal. Comparison analysis with the conventional single-cell bridge-type FCL (SBFCL) showed the superior performance of the proposed MCFCL.

Keywords: wind farms (WFs); multi-cell fault current limiter (MCFCL); fault-ride through (FRT)

1. Introduction

To facilitate the integration of an increased number of wind turbines into the power grid, many countries have adopted new grid codes [1]. These latter aim at specifying the electrical performance that generation units must comply with in order to ensure the safe and reliable operation of power grids. Fault ride-through (FRT) capability which aims at mitigating the adverse effects of grid faults is among the aspects covered by grid codes [1,2]. This capability helps to WFs to remain connected to the grid for a certain time, under faulty conditions [2]. This measure prevents the widespread tripping of WTs due to grid disturbances and thwarts local or system wide instabilities [1,2].

Doubly fed induction generators (DFIGs) are widely used in modern WTs because of their variable speed operation, partially rated power converters and ability to decouple the control of the active and reactive powers [3]. A major drawback of DFIGs, however, is their high sensitivity to grid disturbances such as short circuit faults and voltage sags or short duration voltage variations.

These latter may lead to high transient over-currents in the rotor circuit and over-voltage in the DC link capacitor [3]. This problem can either be mitigated using software [4–6] or hardware [7–20] approaches. The software-type solutions are based on modifications of the DFIG converters, especially the rotor side converter (RSC). Among the drawbacks of the software-based approaches are limited RSC capacity and capacitor voltage limitation in severe voltage sags. The above-mentioned problems can be overcome using hardware approaches [3]. These latter encompass (1) shunt flexible ac transmission systems (FACTS) controllers which include STATCOM devices [7]; (2) series hardware schemes, which include dynamic voltage restorers (DVR) [8], unified inter-phase power controllers (UIPC) [9], and series braking resistors (SBR) [10]; (3) energy storage systems (ESS) [11]; and (4) fault current limiters (FCLs) [12–20].

Though hardware schemes such as static synchronous compensators (STATCOM), dynamic voltage restorers (DVR), unified interphase power controllers (UIPC) and energy storage systems (ESS) are reliable interfaces that can fulfil the FRT requirements of WFs; they require high capacity and accordingly high-cost power converters, thus making these solutions costly and impractical. Among the hardware schemes, FCLs were found to be effective FRT protection schemes [3,4]. Various FCL technologies have been proposed and developed in the literature to mitigate fault currents. They are generally classified into superconducting FCLs (SFCLs) [12,13], and solid-state FCLs (SSFCLs) [14,15]. Employing SFCLs in WFs provides a feasible interconnection mechanism to enhance FRT. However, they require high-cost superconducting materials and cooling systems when used in high voltage systems [14].

Recently, the bridge-type FCLs (BFCLs), which are classified as SSFCLs are receiving more attention as an effective measure to meet the WF requirements [15]. Though various BFCL topologies have been proposed and documented in the literature, they were reported to be used for FRT enhancement for the first time in [14]. In this topology, the discharging resistor (DR) was located in the DC side and the DR was used to consume the excess active power of the WF generators and improve their FRT capability. Firouzi *et al*. proposed a sliding mode controller-Based BFCL for Fault Ride-Through Performance Enhancement of DFIG-Based Wind in [15]. The authors further proposed a transformer-type BFCL with multi-resistors instead of a single DR to improve the DFIG FRT performance in [16]. Using a three-phase coupling transformer, however, was shown to reduce the efficiency of the BFCL under asymmetrical faults and increase its cost. The DR in the DC side was transferred into the AC side and implemented in parallel with the BFCL in [17]. Hossain used a BFCL with a series inductor and resistor to improve the transient stability of DFIG-based WTss [18]. A series capacitor and a resistor were used in [19], as limiting impedance to support the interconnection point voltage by supplying the necessary reactive power. Kartijkolaie *et al*. proposed to place the resistor in the DC side of the BFCLto consume the DFIG's active power and improve its FRT capability [20].

All the above mentioned BFCL-based techniques are based on single-cell FCLs. Their components and limiting impedance are designed considering the system voltage level and worst voltage sag condition, respectively. Additionally, they place the limiting impedance in series with the faulty line path, which can cause destructive over voltage at the WF's interconnection point for lower voltage sag level. Also, the limiting impedance switching in the single-cell BFCL (SBFCL) increases the failure rate and voltage stress of the semiconductor switches.

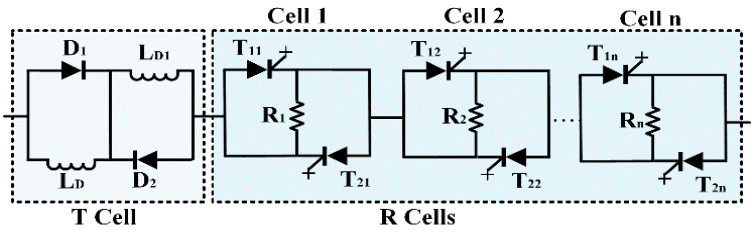
To mitigate the above problems, we propose in this paper a dynamic multi-cell FCL (MCFCL) topology. Its main contributions are as follows:

- A multi-cell FCL that has a resistor in each cell and is directly connected to the power grid without using the series transformer, thus reducing the volume and cost of the MCFCL.
- A FCL topology that puts the suitable number of cells in the fault path in accordance with the voltage sag level, thus providing an adaptive voltage sag compensation mechanism.
- A design that is able to effectively mitigate voltage sag conditions ranging from low to severe and prevent the occurrence of over-voltages in the WF terminals.

The remainder of the paper is organized as follows. The proposed MCFCL power circuit is detailed in Section 2. An analytical study of the proposed topography is provided in Section 3. The proposed topology is implemented to a DFIG-based WF and its performance is assessed under various voltage sag conditions in Section 4. Some concluding remarks are provided in Section 5.

2. Proposed Multi-Cell Fault Current Limiter (MCFCL) Topology

The proposed MCFCL configuration is illustrated in Figure 1a. The MCFCL consists of two main parts, including a transient cell (TC) and n resistive cells (RC) coupled in series arrangement to meet high voltage operation requirements. The TC of the MCFCL include two diodes (D_1 and D_2) and two transient limiting reactors (TLRs) to limit the transient fault current at the fault occurrence instant. Each RC of the MCFCL consists of two gate-turn off (GTO) semiconductor switches and one limiting resistor.



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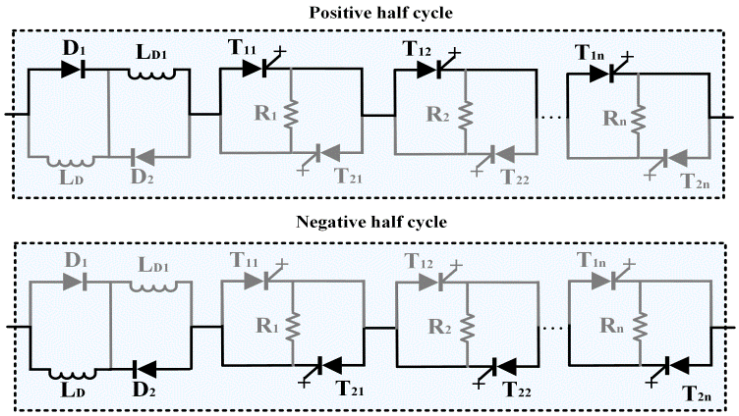

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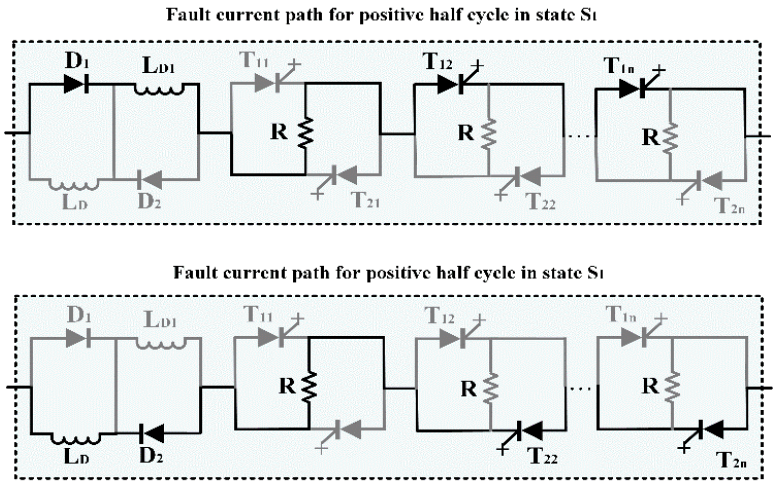

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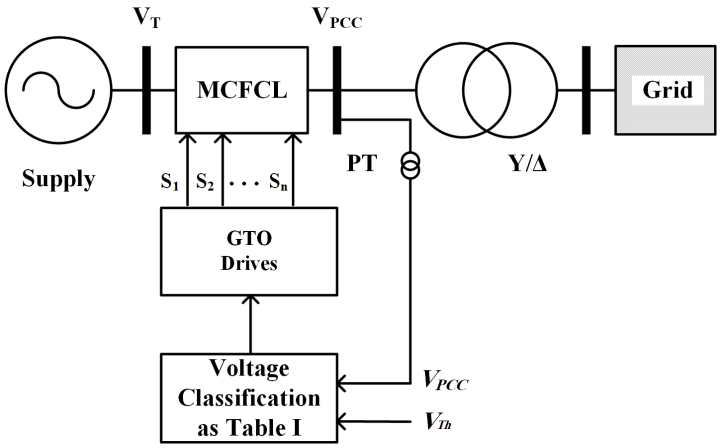
Figure 1. *Cont.*



(**d**)

Figure 1. (**a**) Schematic diagram of the MCFCL, (**b**) MCFCL with three cells and resistors as limiting impedance, (**c**) Current path of the MCFCL for all steps according to Table 1, (**d**) MCFCL control system.

Table 1. Switching strategy.

Switching Sequence				Cell Resistance	Voltage Range (pu)
S_1	S_2	S_{n-1}	S_n		
0	0	0	0	0	$V_{Th} < V_{PCC}$
1	0	0	0	R	$V_{Th} - V_T^{max} < V_{PCC} < V_{Th}$
1	1	0	0	$2R$	$V_{Th} - 2V_T^{max} < V_{PCC} < V_{Th} - V_T^{max}$
1	1	1	1	nR	$V_{Th} - nV_T^{max} < V_{PCC} < V_{Th} - (n-1)V_T^{max}$

2.1. MCFCL Operation

The basic operating principle of the MCFCL is divided into normal and faulty operating conditions. Under normal conditions, all the RCs' GTO switches are closed. Therefore, the limiting resistors of RCs (R_1–R_n) are bypassed. The AC line current (i_L) passes through the D_1-L_{D1}-T_{11}-T_{1n} path and charges the L_{D1} to the peak value of the current i_L. Also, for the negative half cycle of operation, the current i_L flows through the D_2-L_{D2}-T_{21}-T_{2n} path and charges the L_{D2} to the peak value of the line current. Figure 1b illustrates the line current flow path under normal conditions for the positive and negative half cycle of operation, respectively. After several cycles, the L_{D1} and L_{D2} act as a DC current source. Thus, diodes D_1 and D_2 are freewheeling and result in a zero voltage drop under normal conditions.

Note however, that under normal conditions, the flowing line current from TLRs and the semiconductor switches results in some power and voltage losses. However, the latter can be ignored in HV systems. When a short circuit fault occurs in the downstream of the MCFCL, the raising rate of the fault current is suppressed by the TLRs of the TC. Then, considering the coupling voltage level; the MCFCL control system will turn off the GTO switches. Therefore, the MCFCL inserts the combinational of limiting resistors according to Table 1, in fault path to restrict the fault current and compensate the voltage sag at the acceptable level. Figure 1c represents the fault current path under faulty operating conditions for the state S1 according to Table 1.

S_1–S_n represent the pair GTO switches' states of each cell. 1 and 0 represent the ON and OFF states of GTO switches, respectively. Also, V_T^{max} represents the maximum acceptable voltage of each cell. V_{PCC} and V_{Th} are the measured coupling voltage and the threshold value. After fault period, the coupling voltage starts to recover to pre-fault level. Once the coupling voltage exceeds the threshold value, the semiconductor switches are closed with sequenced arrangements.

2.2. MCFCL Control System

The control system of the MCFCL is illustrated in Figure 1d. Note that the grid coupling voltage succeeding the MCFCL location is used to detect the fault and control the MCFCL operation. First, the voltage at coupling point (V_{PCC}) and the threshold value (V_{Th}) are compared. If $V_{PCC} < V_{Th}$, the adaptive control circuit detects the fault. Following this, the control system determines the suitable number of cells, which should be inserted in fault path according to Table 1. When the fault is cleared, the V_{PCC} return back to the pre-fault voltage. When the V_{PCC} becomes greater than the V_{Th}, the MCFCL control circuit opens the GTO switches with sequenced arrangements, respectively.

2.3. Procedure to Determine the Number of MCFCL Cells

The number of MCFCL cells is selected based on the voltage rating of the semiconductor switches of each RC. The maximum acceptable voltage of each cell is represented by V_T^{max}, which is the voltage rating of each GTO switch in each cell. The maximum voltage drop on each cell is obtained by:

$$V_m = \frac{V_g}{nR + Z_g} \tag{1}$$

where V_g and Z_g represent the grid voltage and impedance, respectively. To ensure that the voltage drop of each cell is within acceptable ranges, the following inequality: $V_T^{max} > V_m$ should be satisfied. Hence, Equation (1) can be re-written as follows:

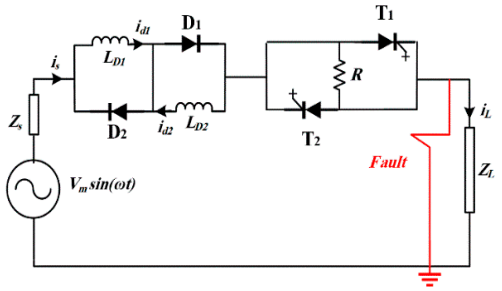
$$V_T^{max} > \frac{V_g}{nR + Z_g} \tag{2}$$

The number of cells is obtained from (2) as follows:

$$n > \frac{V_g - V_T^{max} Z_g}{R V_T^{max}} \tag{3}$$

3. Analytical Study of the Proposed MCFCL Topology

The configuration of a single phase MCFCL is illustrated in Figure 2a. To simplify the analysis, we consider a MCFCL with two cells, including one TC and one RC, which are located between the power source and the load. *Vs* and *Zs* represent the voltage and impedance source, respectively. Z_L represents the sum of the load and line impedance in this system. V_D and V_F are the diodes and GTO switches forward voltages, respectively. Based on the grid operation condition, the MCFCL is divided into two conditions: normal and faulty.



(**a**)

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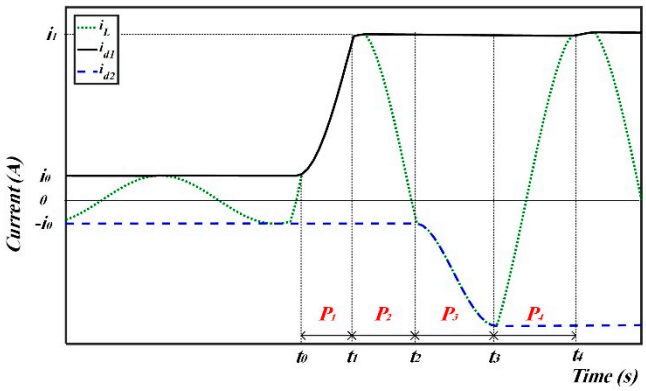


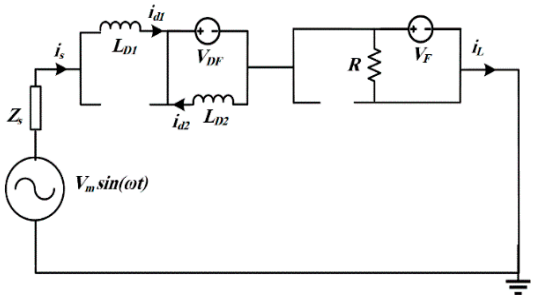
(**b**)

Figure 2. (**a**) Configuration of the single phase MCFCL under study, (**b**) MCFCL performance under normal and faulty conditions.

Figure 2b shows the MCFCL performance under both normal and faulty conditions. Under normal conditions, both TLRs currents (i_{d1} and i_{d2}) are charged to the positive and negative peak values of line current, respectively. Considering $V = L\ di/dt$, the voltage drop on these reactors is low and has no effect on the system performance in this case. The MCFCL operation under faulty condition is represented by periods P_1–P_4. When the short circuit fault occurs at $t = t_0$, the line currents (i_L) and i_{d1} start to increase. The period P_1 ($t_0 < t < t_1$), represents the MCFCL performance under this condition. Figure 3a represents the equivalent power circuit of the MCFCL for the period P_1. Note that during P_1, the line current (i_L) flows through the D_1-L_{D1}-T_1 path and charges the DC reactor (L_{D1}). The line current can be expressed by:

$$V_m \sin(\omega t) = L\frac{di_L}{dt} + Ri_L + V_D + V_F \tag{4}$$

where $R = r_{d1} + R_s$ and $L = L_{D1+}L_s$.



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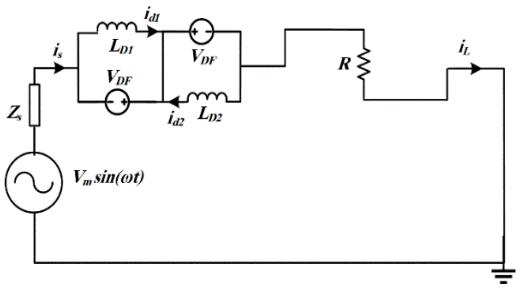

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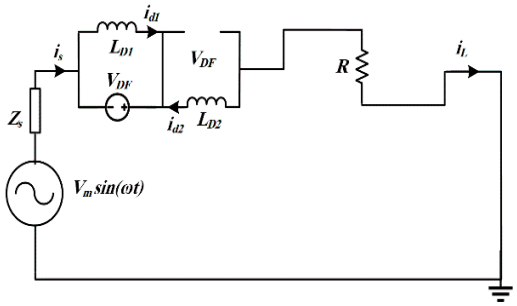

(**c**)

Figure 3. Equivalent circuit of MCFCL for (**a**) P_1, (**b**) P_2, and P_4 (**c**) P_3.

Solving (4), yields the following expression for i_L:

$$i_L(t) = \left[i_0 - \frac{V_m}{|Z|}\sin(\omega t_0 - \varphi) + \frac{V_D + V_F}{R}\right]e^{-\frac{R}{L}(t-t_0)} + \frac{V_m}{|Z|}\sin(\omega t - \varphi) - \frac{V_D + V_F}{R} \quad (5)$$

At $t = t_2$, the control system of the MCFCL detects the fault and turns the GTO switches (T_1 and T_2) off. The period P_2 ($t_1 < t < t_2$), represents the MCFCL performance under this condition.

Figure 3b represents the equivalent power circuit of the MCFCL for the period P_2. Note that during P_2, the current i_L is less than its counterpart i_{d1} and the diodes D_1 and D_2 are in freewheeling state. Considering Figure 3b, the line current is derived as follows:

$$V_m \sin(\omega t) = L\frac{di_L}{dt} + Ri_L \quad (6)$$

Using (6), we can express the current i_L as follows:

$$i_L(t) = \left[i_1 - \frac{V_m}{|Z|}\sin(\omega t_1 - \varphi)\right] \quad (7)$$

where $R = R_s + R$ and $L = L_s$. In period P_3 ($t_2 < t < t_3$), the i_L flows through D_2-L_{D2}-R path and charges the DC reactor (L_{D2}). Figure 3c represents the equivalent power circuit of the MCFCL for the period P_3. The voltage equation in this period is expressed by:

$$V_m \sin(\omega t) = L\frac{di_L}{dt} + Ri_L + V_D \quad (8)$$

Considering (8), the line current is expressed by:

$$i_L(t) = \left[i_0 - \frac{V_m}{|Z|}\sin(\omega t_0 - \varphi) + \frac{V_D}{R}\right]e^{-\frac{R}{L}(t-t_2)} + \frac{V_m}{|Z|}\sin(\omega t - \varphi) - \frac{V_D}{R} \quad (9)$$

where $R = r_{d1} + R_s + R$ and $L = L_{D1} + L_s$. In period P_4 ($t_2 < t < t_3$), the i_L is less than the i_{d2} and the diodes D_1 and D_2 are freewheeling state. Note that the equivalent power circuit of the MCFCL for period P_4 is the same as the one depicted in Figure 3b. Accordingly, the line current equation in this period is expressed using Equation (7).

4. Implementation to a DFIG-Based WF

To assess the performance of the proposed MCFCL topology, we implemented it to the single line diagram depicted in Figure 4a and simulated it using PSCAD/EMTDC software. The simulated WF is connected to the grid through the MCFCL and a 0.7 kV/20 kV transformer. A 20 MW aggregated DFIG-type WT is used to model the WF. Three short circuit faults with different fault impedances are considered to assess the performance of the MCFCL under three voltage sag ranges. Additionally,

a comparison analysis with a SBFCL scheme [17] is carried over. In this case we swapped the MCFCL in the system shown in Figure 4a by a SBFCL and compared their performance. The values of R_D = 30 Ω and L_D = 10 mH are considered in this study. Figure 4b represents the SBFCL power circuit. The parameters of the system under study are provided in Table 2. The dynamics of the wind turbine, DFIG, and its control system are briefly described in the next section.

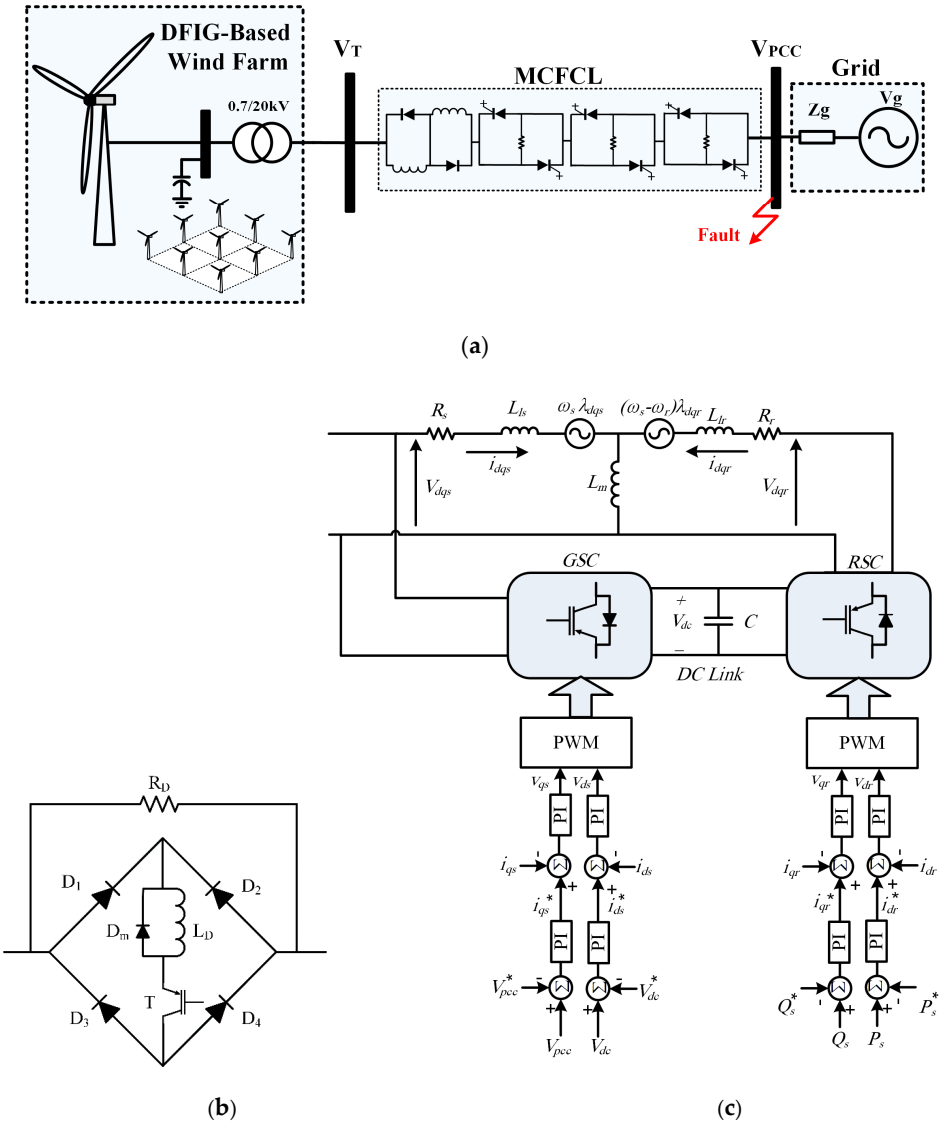

Figure 4. (**a**) Single diagram of the study system, (**b**) Power circuit of the SBFCL, (**c**) Control system of the DFIG converters.

Table 2. System Data.

	Parameters	Value
Grid	Rated voltage	20 kV
	Frequency	50 Hz
DFIG	Nominal power	2 MW
	Nominal voltage	690 V
	Nominal frequency	50 Hz
	Inertia constant	1 s
	Stator resistance	0.0057 Ω
	Stator leakage reactance	0.078 Ω
	Rotor resistance	0.0159 Ω
	Rotor leakage reactance	0.1022 Ω
	Mutual reactance	2.434 Ω
MCFCL	TLR inductance	0.01 H
	Resistance of each RC	10 Ω

4.1. DFIG-Based Wind Turbine Model

The mechanical power (P_m) of the wind turbine can be expressed as [21,22]:

$$P_m = 0.5\ \rho\pi R^2 C_p(\lambda,\beta)v_w^3 \tag{10}$$

where P_m (10) P_{wt} represents the mechanical power extracted from the wind energy, ρ, v_w and λ are the air density, the wind speed, and the tip speed ratio, respectively. R is the blade radius, and C_P (β, λ) as follows:

$$C_p(\lambda,\theta) = 0.22\left(\frac{116}{\lambda_c} - 0.4\beta - 5\right)e^{-12.5\lambda_c} \tag{11}$$

$$\lambda_c = \left(\frac{1}{\frac{1}{\lambda+0.08\beta} - \frac{0.035}{\beta^3-1}}\right) \tag{12}$$

The drive train system is modelled using the two-mass system detailed in [21].

Figure 4c shows the DFIG connected to the WT. The RSC and grid side converter (GSC) control systems are also depicted in this figure. The DFIG stator and rotor power circuit voltage and flux relations in the *d-q* synchronous reference frame are expressed by the following Equations (5) and (6):

$$V_{qs} = R_s\ i_{qs} + \frac{d\varphi_{qs}}{dt} - \omega_s\varphi_{ds} \tag{13}$$

$$V_{ds} = R_s\ i_{ds} + \frac{d\varphi_{ds}}{dt} - \omega_s\varphi_{qs} \tag{14}$$

$$V_{dr} = R_r\ i_{dr} + \frac{d\varphi_{dr}}{dt} - (\omega_s - \omega_r)\varphi_{qr} \tag{15}$$

$$V_{qr} = R_r\ i_{qr} + \frac{d\varphi_{qr}}{dt} - (\omega_s - \omega_r)\varphi_{dr} \tag{16}$$

$$\lambda_{qs} = L_s\ i_{qs} + L_m\ i_{qs} \tag{17}$$

$$\lambda_{ds} = L_s\ i_{ds} + L_m\ i_{ds} \tag{18}$$

$$\lambda_{qr} = L_s\ i_{qr} + L_m\ i_{qr} \tag{19}$$

$$\lambda_{dr} = L_s\ i_{dr} + L_m\ i_{dr} \tag{20}$$

Indices *s*, *r*, *q* and *d* represent the stator, rotor, *q-axis* and *d-axis* components of stator and rotor voltage and flux. L_m is the magnetizing inductance. The RSC of the DFIG controls the output active and reactive power. Also, the GSC of the DFIG controls the DC link capacitor voltage and the grid coupling voltage (V_{PCC}). Additional details concerning the DFIG control system can be found in [5,6].

4.2. Simulation Results

To assess the performance of the proposed FRT scheme, we apply three short circuit faults with different fault impedances to the PCC bus at t = 5 s for 150 ms as shown in Figure 4a. In these conditions the PCC voltage drops to 0.01 pu, 0.35 pu and 0.75 pu, respectively. This enables us to analyze the performance of the proposed SBFCL scheme under low, medium, and severe voltage sag conditions, respectively.

The SBFCL resistance is R_D = 30 Ω and each RC resistance of the MCFCL is R = 10 Ω. The wind speed is considered 14 m/s in this study. Considering system voltage, the MCFCL has four cells, include one TC and three RCs. Also, the voltage sag is divided into three range as demonstrated in Table 3. The switching states and voltage sag ranges are represented as Table 3. S_1–S_3 represents the pair GTO switches states of RC_1–RC_3 cell. Simulations are performed as follows:

- Scenario A: No FRT devices.

- Scenario B: Using the SBFCL.
- Scenario C: Using the MCFCL.

Table 3. Switching states of MCFCL for three cell.

States			Cell Resistance	Voltage Sag Range (pu)
S_1	S_2	S_3		
ON	ON	ON	0	$V_{PCC} > 0.9$ pu
OFF	ON	ON	R	0.6 pu $< V_{PCC} <$ 0.9 pu
OFF	OFF	ON	$2R$	0.3 pu $< V_{PCC} <$ 0.6 pu
OFF	OFF	OFF	$3R$	$0 < V_{PCC} <$ 0.3 pu

4.2.1. Low Voltage Sag Condition

In this condition, the fault resistance is set to be $R_f = 0.5\ \Omega$, which results in a 0.25 voltage sag at PCC. The conventional SBFCL inserts the $R_D = 30\ \Omega$ in the fault path. However, the MCFCL control circuit turns off the S_1 and puts the $R = 10\ \Omega$ in series with line in scenario C, considering Table 2. Figure 5 demonstrates the MCFCL performance for this condition.

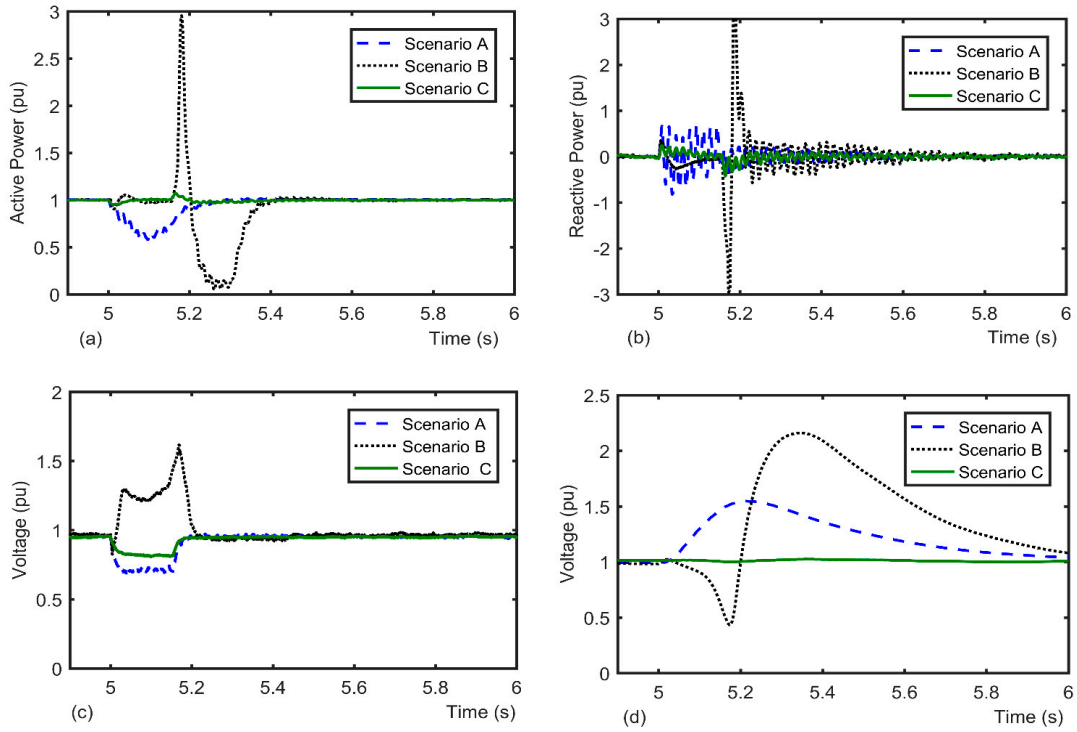

Figure 5. Low voltage sag, (**a**) Active power, (**b**) Reactive power, (**c**) Terminal voltage (**d**) DC link voltage.

It can be observed from Figure 5a, that the output active power from WF drops to 0.55 pu for scenario A. In scenario B, the active power remains constant during fault occurrence, however; it's post-fault dynamics show a sharp increase to 3 pu followed by a sudden decrease to near zero, which is harmful for the generator. However, *scenario* C reveals that using the MCFCL results in lower oscillations in the active power during the fault period and after fault clearance, which provides faster stabilization under faulty conditions. Figure 5b depicts the dynamics of the WF's reactive power. Note noticeable fluctuations of the WF's reactive power during post-fault in scenario B. However, with the MCFCL in scenario C, the reactive power fluctuations are lowest, and it quickly returns back to its pre-fault value. Figure 5c shows the dynamics of the terminal voltage for three scenarios under low voltage condition. Considering this figure, the terminal voltage drops to 0.75 pu in scenario A.

In scenario B, it raises to 1.5 pu and the DFIG stator experiences transient over-voltage. However, in scenario C, the terminal voltage is 0.9 pu and remains in acceptable range by using the MCFCL.

Figure 5d shows the DC link voltage of DFIG. Considering this figure, it increases to 1.5 pu in this condition for scenario A. In scenario B, it gradually decreases during fault period and then raises to 2.2 pu after fault clearance. However, by using the MCFCL, the DC link voltage remains constant.

4.2.2. Medium Voltage Sag Condition

For this condition, the fault resistance is decreased, and the PCC voltage is decreased to 0.35 pu. The control circuit of the MCFCL opens switches S_1 and S_2 to insert two cells resistance in the fault path in scenario C, considering Table 2. Figure 6 shows the MCFCL performance for this condition. Figure 6a shows the output active power from WF for this voltage sag level. In this voltage sag level, the output active power from WF drops to 0.15 pu for scenario A. In scenario B, the active power in fault period remains constant, however; it increases to 2.5 pu and then drops after fault period. However, the MCFCL provide the lowest active power fluctuation during and after fault. Figure 6b shows the WF reactive power. Considering this figure, the MCFCL in scenario C has the lowest reactive power fluctuation. Figure 6c shows the terminal voltage for three scenarios in this condition. In scenario A, the terminal voltage drops to 0.4 pu. In scenario B, the terminal voltage raises to 1.2 pu during fault period in this condition. But, in scenario C, it is 0.9 pu and remains in acceptable range by using the MCFCL. Figure 6d shows the DC link voltage for all scenarios. It increases to 2 pu in scenario A. In scenario B, the DC link voltage increases after fault clearance to 1.5 pu and then recovers to its pre-fault value. However, in scenario C, it remains constant during and after fault.

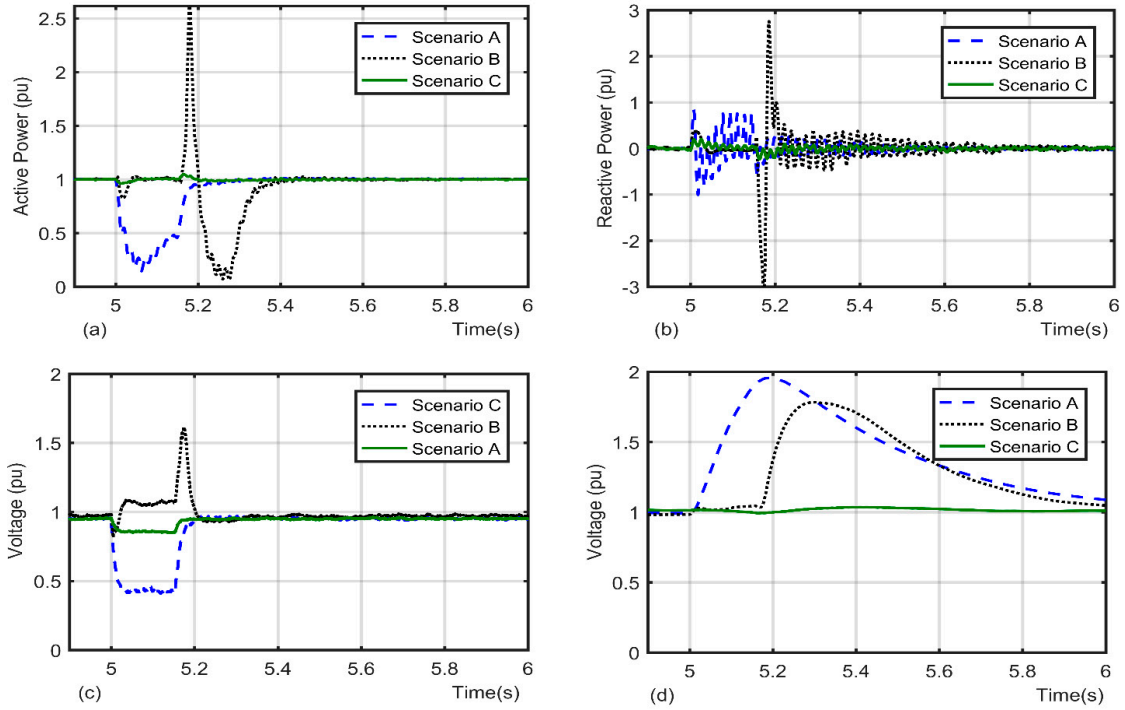

Figure 6. Medium voltage sag, (**a**) Active power, (**b**) Reactive power, (**c**) Terminal voltage, (**d**) DC link voltage.

4.2.3. Severe Voltage Sag Condition

Figure 7 depicts the MCFCL performance under severe voltage sag condition for the above mentioned three scenarios. In this condition, the control circuit of the MCFCL opens S_1, S_2, and S_3 and inserts three RCs resistances in series with a line like the SBFCL.

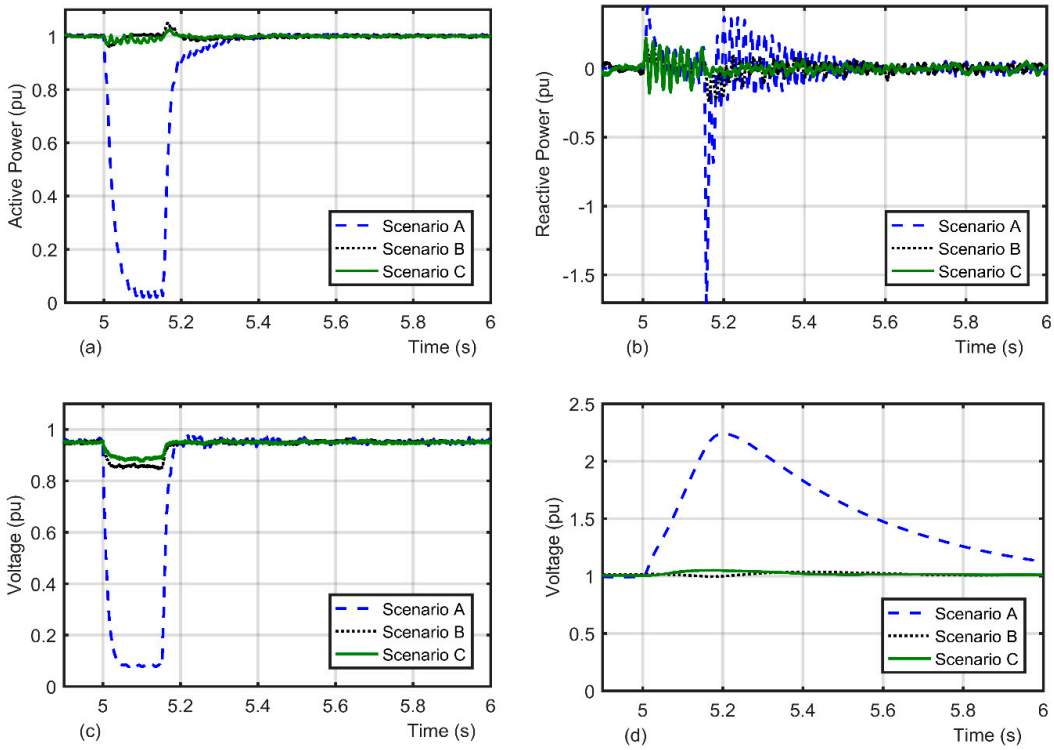

Figure 7. Severe voltage sag conditions, (**a**) Active power, (**b**) Reactive power, (**c**) Terminal voltage, (**d**) DC link voltage.

Figure 7a–d present the active power, reactive power and terminal and DC link voltages responses to this severe voltage sag condition. It can be seen from these figures that both MCFCL and SBFCL have similar responses in terms of voltage sag, active power drop, reactive power oscillations, and DC link overvoltage under this condition.

Based on the above results, we can confirm that:

- Using the SBFCL produces high transient over voltage under low and medium voltage sag conditions, which is harmful for the DFIG under short circuit fault current.
- The proposed MCFCL scheme is able to properly mitigate a wide range of voltage sag levels without producing any transient over voltage.
- The MCFCL outperforms the SBFCL in terms of FRT performance and transient over-voltage under medium and low voltage sag levels.
- Response and performance of both SBFCL and MCFCL are the same under severe voltage sag levels.

5. Conclusions

This paper proposed a novel MCFCL topology to mitigate voltage sags and facilitate the integration of DFIG-based WFs into the high voltage power grid. The proposed scheme includes one TC and multiple RCs directly connected to the grid without using the series transformer, which reduces the cost and volume of the MCFCL. It also inserts a suitable number of RCs in the fault path to provide an adaptive voltage sag compensation mechanism in accordance with the voltage sag level. Assessment of the proposed approach under various sag conditions, showed that the MCFCL is able to effectively compensate for a wide range of voltage sags and prevent the occurrence of over-voltages in the WF terminal. A major advantage of the proposed MCFCL scheme is its ability to insert a suitable number of cells in the fault path to provide the adequate voltage sag compensation in accordance with the severity of the voltage sag. A comparison analysis with the conventional single-cell bridge-type FCL (SBFCL) showed that, although the performance of the MCFCL is similar to that of SBFCL under severe

voltage sag conditions, it outperforms the latter in terms of FRT capability transient over-voltage under lower and medium voltage sag levels.

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