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A Hybridization of Cuk and Boost Converter Using Single Switch with Higher Voltage Gain Compatibility

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Abstract: In the current era, the desire for high boost DC-to-DC converter development has increased. Notably, there has been voltage gain improvement without adding extra power switches, and a large number of passive components have advanced. Magnetically coupled isolated converters are suggested for the higher voltage gain. These converters use large size inductors, and thus the non-isolated traditional boost, Cuk and Sepic converters are modified to increase their gain by adding an extra switch, inductors and capacitors. These converters increase circuit complexity and become bulky. In this paper, we present a hybrid high voltage gain non-isolated single switch converter for photovoltaic applications. The proposed converter connects the standard conventional Cuk and boost converter in parallel for providing continuous current mode operation with the help of a single power switch, which gives less voltage stress on controlled switch and diodes. The proposed hybrid topology uses a single switch with a lower component-count and provides a higher voltage gain than non-isolated traditional converters. The converter circuit mode of operation, operating performance, mathematical derivations and steady-state exploration and circuit parameters design procedures are deliberated in detail. The proposed hybrid converter circuit components, voltage gain and performance, were compared with other topologies in the literature. The MATLAB/Simulink simulation study and microcontroller-based experimental laboratory prototype of 150 W were implemented. The simulation study and experimentation results were confirmed to be a satisfactory agreement with the theoretical analysis. This topology produced non-inverting output in continuous input current mode using a single switch with high voltage gain (≈5.116 gain) with a maximum efficiency of 92.2% under full load.

Keywords: DC-to-DC converter; single switch high voltage gain converter; non-isolated DC-to-DC converter; low voltage stress; higher voltage gain

1. Introduction

Due to the increase in energy demand, large amounts of conventional energy have been consumed, which is very dangerous due to their CO2 emissions. For example, all countries are keen on replacing conventional energy sources with non-conventional sources. Researchers are currently exploring power converters and interfacing circuits to meet out-migration. Non-conventional sources such as wind energy [1,2], photovoltaic (PV) [3,4] and hydrogen-powered fuel cells (FC) [5,6] are leading sources for meeting commercial and industrial demands. A PV-powered power system consists of PV modules coupled in a series as well as parallel combinations that are fed to the required DC voltage through the DC-to-DC converter, which is then converted as a DC-to-AC source through the inverter [7]. The controller development of DC-to-DC converters using a fuzzy logic controller and sliding mode control has recently gained attention. Those converters are used in a microgrid that minimizes the instability effects in [8,9]. For optimizing the performance of the converter, an optimization algorithm was used to tune the controller's coefficients [9]. A constant power load in a shipboard DC microgrid was investigated for the finite time by adopting the finite-time disturbance observer method [10]. The estimated load power was then received by the fixed-time terminal sliding mode controller to stabilize the entire marine power grid as well as tracking the reference voltage of the DC bus in a fixed time independent of initial conditions. For a high-efficiency PV system, a dual-power stage micro-inverter (high voltage gain DC-to-DC converter + DC-to-AC inverter) was issued in the market. In many industrial applications such as those found in the automotive, telecommunication and shipping industries, systems need higher voltage gain DC-to-DC converters with large input current [11–13]. These converters typically boost the range from 24–60 V to 100–300 V. For example, automotive headlamps need 48/100/120 V range, but the vehicle battery capacity can only deliver 12/24/48 V. For these situations, high voltage converters are suggested with high voltage gain [14,15]. According to the theoretical calculations, the conventional boost converter can offer a high duty ratio with infinite voltage gain. However, in a practical case, it is limited due to the inductor saturation limits. Besides, any DC-to-DC converter, which needs to provide a high output voltage and high power conversion, draws large input current; hence, the power switches metal-oxide-semiconductor field-effect transistor (MOSFET) and diode) are needed to handle the voltage stress.

Topologies have presented numerous single switch converters in the literature to provide the high step-up voltage conversion [14–20]. These converters have some limitations for their voltage gain, which is mainly because of the inductors, power semiconductor switches and the parasitic elements of those converters. Hence, a researcher has recommended using a step-up transformer with a converter to overcome this issue (flyback converter) [21]. It may be achieved with a high current for high power uses, which is not the most efficient. Other attempts have been made by using a single switch with a forward and tapped inductor connected converters are proposed for high voltage gain [22–24]. Though these converters have a controlled degree of freedom through the transformer turns ratio adjustment, considering the transformer size, the converter is large. The high voltage gain quadratic converters are the next choice in this group [25,26]. However, a quadratic converter has high voltage stress across the first semiconductor, resulting in it being more efficient than the classical converter. The impedance (using two inductors and two capacitors) source-based converter handles the buck-boost voltage conversion with high gain; however, it needs a high voltage-handling power switch to operate shoot-through and not shoot-through operation. A high voltage gain integrated boost and flyback converter is proposed by [27] using the leakage inductor energy recirculation in the switch-off period; however, this method suffered from pulsating input currents.

The converter topology accumulated with a coupled inductor produces a high step-up conversion with high efficiency [28,29]. Here, the voltage gain is dealt with by changing the converter switch turns ratio like isolated type converters. Though this topology obtains a high gain, due to the coupled inductor-leakage inductance, the switch may suffer a high voltage spike. The passive and active clamping approaches have been established [30] by adding a coupled inductor for the high voltage conversion ratio; however, this converter is inefficient in terms of cost and size. The other choice

is adapting a switched capacitor in the switching-mode converter for the high voltage gain [28,29]. Due to the pulse shape, the input current of the converter leads to a weak load and line regulation problems. The voltage-doubler concept in converters [30–34] can provide a high voltage gain with the coupled inductor. Here, the switching frequency is less than an inductor magnetizing current frequency, which is not suitable for reliable operation. Recently, using the single switch in DC-to-DC power converters, various research papers have been published to derive high voltage gain without using a higher duty ratio [35–40]. The authors in [33] proposed a 2D/1-D voltage gain single switch buck–boost converter with low input current ripple and appropriate voltage gain. Nevertheless, it has the discontinuous current in the input side. In paper [37], a transformerless high voltage gain buck–boost was proposed with a voltage gain of 3D/1-D; though this converter has a discontinuous input current. A quadratic DC–DC buck–boost converter with single-switch topology is presented in [39] for widespread voltage conversion. The high step-up single switch converter is recommended for PV-based grid applications [30]. However, in this converter, the low-level input voltage habitually roots massive input current and higher current ripples. This large amount of current affects the power switch during the higher duty ratio operation, causing a large conduction loss. Recently, Banaei et al. proposed a converter using a single switch with less switching voltage stress. Even though the converter can maintain the continuous input current for all duty ratios, the primary power switch voltage stress is strictly equal to the converter output voltage, which caused high conduction losses [38]. In [40,41], the single switch Cuk topology uses an extra inductor and capacitor to provide the extra voltage. However, in this topology, when diodes are operating with higher current and voltage, the diode reverse recovery current is predominant, which increases the switching losses. Among all converter topology, the cascade boost converter type is proficient in obtaining a higher gain with minimal duty ratio for the full range of voltage gain [19]. Nevertheless, the main switch has higher voltage stress in this topology.

Based on this discussion, and although several single switch boost converter topologies are proposed in the literature, their major approaches are concerned with the use of less magnetic elements, size, weight, conduction losses and cost-savings for the inductors. These approaches have higher voltage stresses on their switch (nearly the same as their output voltage). Therefore, these converters still have significant challenges, such as high step-up requirements for the larger duty ratio, output diode reverse recovery complication, higher switching voltage stress and satisfactory efficiency. Integrating the classical DC-to-DC converter is a better choice than modifying an existing converter. However, while cascading those classical converters with additional boosting capability, reducing the power switches and passive elements leads to an appropriate converter circuit size as well as cost reductions. With that aim, in this paper, we propose a DC–DC converter topology by integrating the conventional boost and Cuk converters with high voltage gain. Our proposed topology uses only one power switch with higher static voltage gain when compared to other conventional converters. Our proposed converter delivers voltage using two series-connected identical capacitors connected in parallel with the converter circuit. In this paper, we also deal with the maintenance of the capacitor balancing. The detailed converter mode operation, analysis, design, small-signal analysis and analytical switching losses were deliberated. The MATLAB/Simulink simulation and PIC microcontroller-based experimentation results for the integrated converter shows the advantages and practicality of the proposed converter.

The paper is organized as follows: Section 2 describes the proposed hybrid converter design and its mode of operation. Section 3 describes the converter components design and small-signal analysis. Section 4 explains the design procedure and components. The simulation, experimentation and comparison with other similar topologies are discussed in Sections 5 and 6. The conclusion is given at the end of Section 7.

2. Topology and Operation of Proposed Hybrid DC–DC Converter

The proposed integrated hybrid converter combines the conventional boost converter and classical Cuk DC-to-DC converter. The method used for the design of the proposed hybrid converter topology is illustrated in Figure 1. Figure 1a,b shows the typical conventional boost converter and classical Cuk converter, respectively. In both of these converters, the input inductor, power switches and input source are organized in the same way. Hence, there is an opportunity to merge these two converters by keeping the power switch and input inductor commonly on the input side. Except for the input side boost inductor (L_1) and the power switch T, the rest of the circuit is connected precisely in parallel with each other. Hence, the output side two capacitors (C_1 and C_3) are placed across the load. This hybrid structure increases the voltage gain by complementing the benefits of boost and Cuk converters. The converter provides continuous current mode operation with the help of a single power switch, which provides less voltage stress on the controlled switch and diodes.

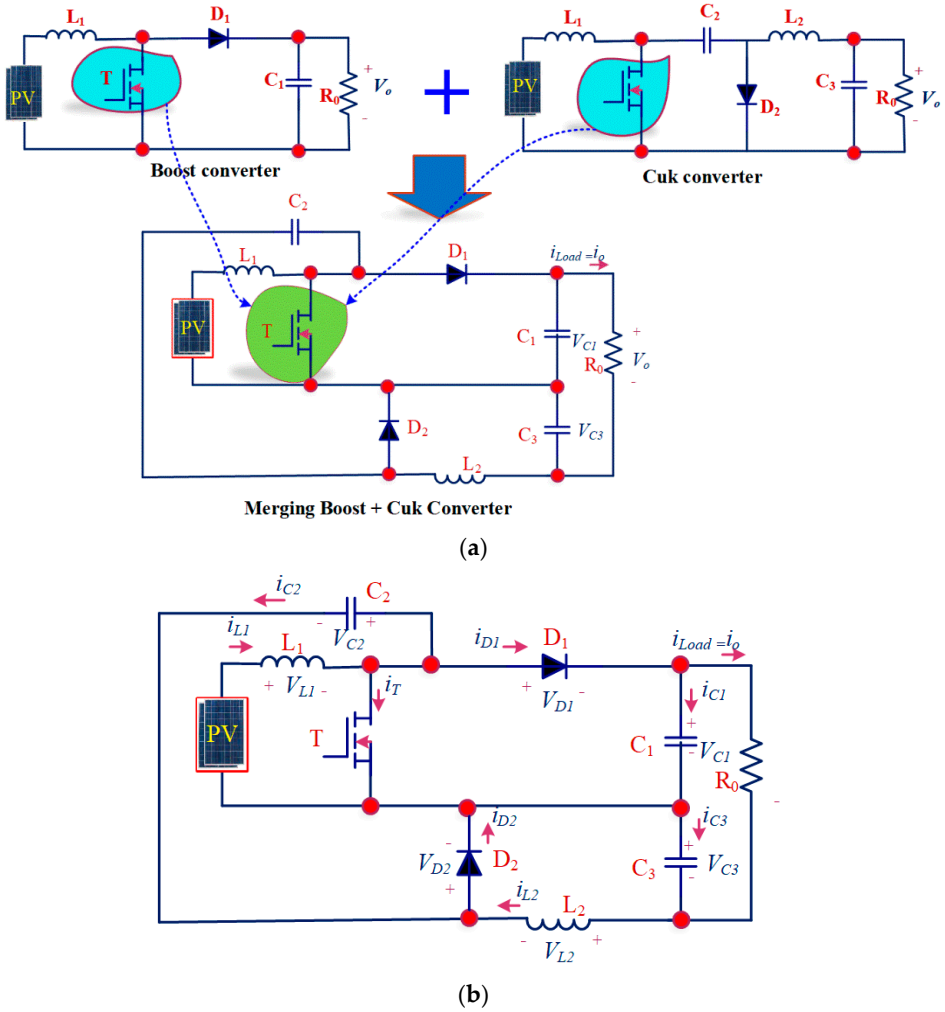


Figure 1. (**a**) Proposed converter integration; (**b**) proposed single switch hybrid DC–DC converter.

Operation of Hybrid DC–DC Converter

The proposed hybrid DC–DC converter mode operations, their capacitors (C_1, C_2 and C_3) and inductors (L_1 and L_2) charging and discharging analysis derivations were considered as follows. The two assumptions were taken for this analysis: (1) all the components are ideal; (2) the converter works under continuous conduction. Figure 3a illustrates the continuous conduction operating mode waveforms of the proposed converter. This advanced hybrid DC–DC converter mode operation has three modes of operation.

- Mode-I [t_a–t_b], presented in Figure 2a. During mode-1, when t = t_a, the power switch T is turned ON and inductors (L_1 and L_2) are charging until t_b. In the same interval, the capacitor C_2 is discharging through T, and inductor L_2 as the diodes (D_1 and D_2) are blocking concerning V_{C1} and V_{C2}.
- Mode-II [t_b–t_c], illustrated in Figure 2b. During mode-1, when t = t_b, the power switch T is in the OFF state. Now the capacitor C_1 voltage (V_{C1}) is higher than V_{C2}. Hence, after t_b interval, the C_2 is charging and inductors L_1 and L_2 are discharging. It is happening throughout t_b to t_c. In the course of this period, diode D_2 is continuously conducting since diode D_1 is still in reverse bias.
- Mode-III [t_c–t_d], presented in Figure 2c. During this mode, the power switch T remains OFF as well as the V_{C1} is equal or lesser than V_{C2}. Here, both the inductors L_1 and L_2 are discharging, and C_1 and C_2 are charging via L_1. Hence the diode D_1 and D_2 are conducting and delivering the current to load.

The proposed hybrid DC-to-DC converter operation mode waveforms are presented in Figure 3. In mode-I, the power switch T is 'ON' and turned 'OFF' in mode-II as well as mode-III. The proposed converter duty ratio versus voltage gain performance was compared to boost and Cuk converters. Figure 3b displays the voltage gain versus duty ratios for boost, Cuk and the proposed hybrid converter. Based on the plot, it can be seen that the proposed hybrid converter has a better voltage gain ratio when compared with the boost and Cuk converter, respectively. In addition to the extended voltage static gain, the proposed topology achieves lower voltage stress across the power switch and diodes, when compared to a boost converter.

The power switch voltage stress is equal to the peak voltage across the capacitor C1. Hence, voltage stress across the power switch T was lower than the total output voltage. The voltage stress of D1 and D2 is equal to the voltage across the power switch T in the OFF state. Hence, the diodes' current rating requirement was lower than power switch T. In the classical boost converters for both Cuk and boost, the power switch and diode need an equal rating. In the higher gain operations, the classical converter needs a higher duty cycle than the proposed converter. Therefore, the voltage stress for switch and diode are higher. Hence, the proposed converter efficiency in the higher gain operation is better than the conventional boost converter.

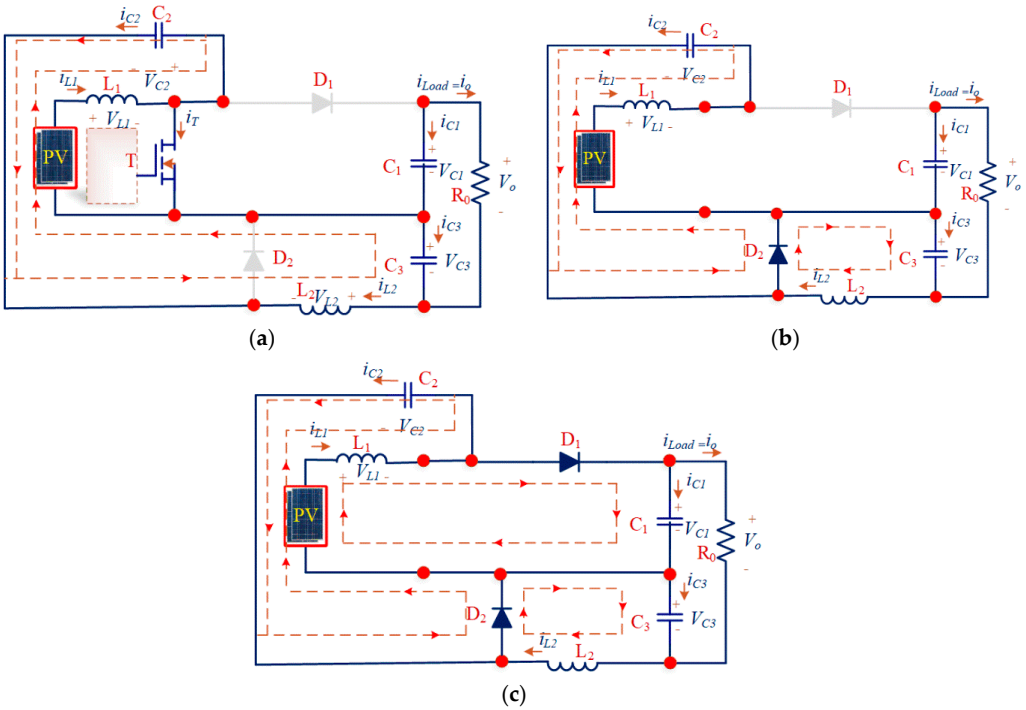


Figure 2. Modes of operation of the proposed hybrid DC-to-DC converter: (**a**) Mode-I [t_a–t_b]; (**b**) Mode-II [t_b–t_c]; (**c**) Mode-III [t_c–t_d].

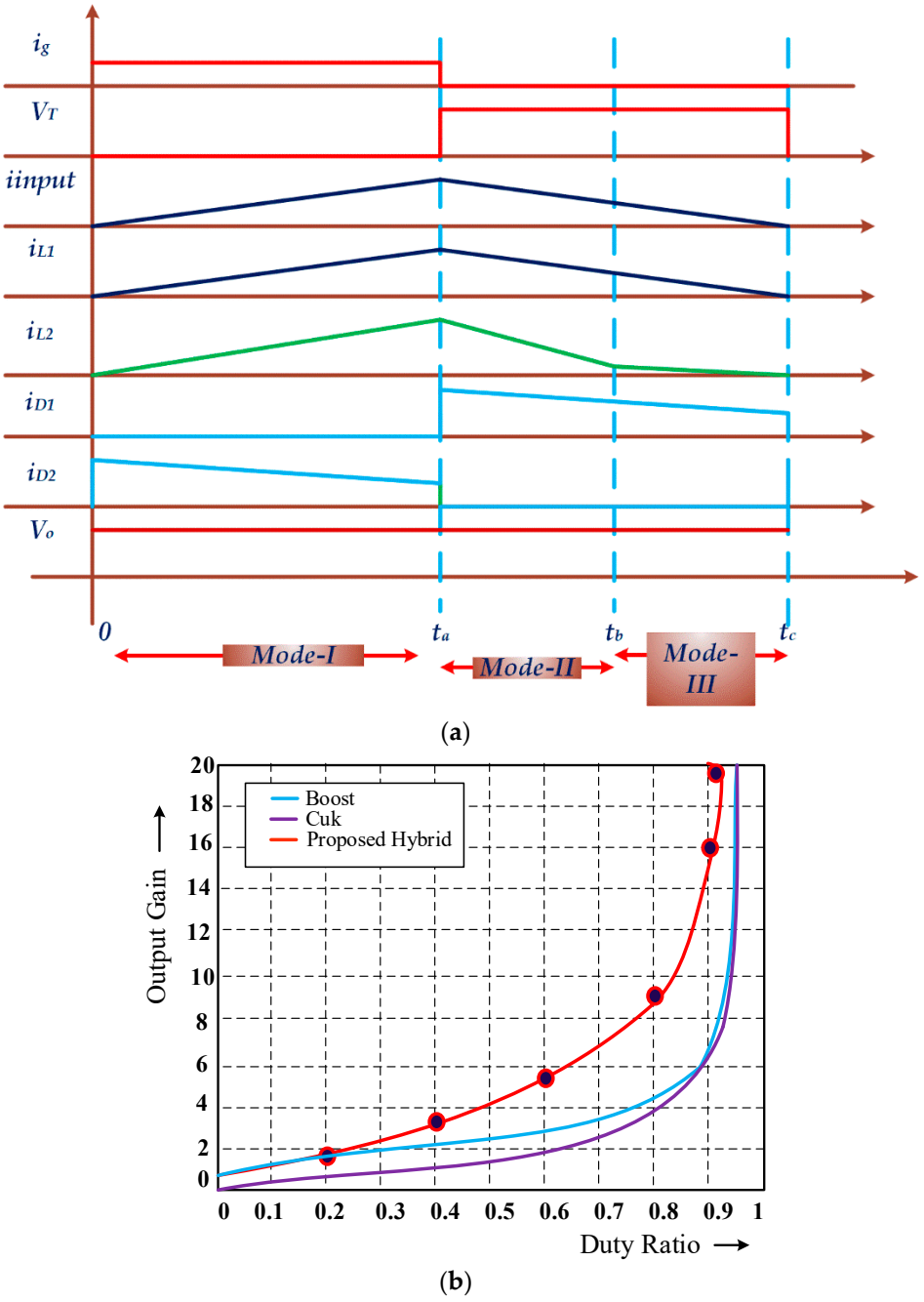


Figure 3. (**a**) Mode diagram of the proposed circuit; (**b**) voltage gain versus duty ratio for boost, Cuk and proposed hybrid converter.

In general, for any DC-to-DC converter, the input inductor selection is carried out depending on the converter conduction mode, load current requirement, and it is desirable to confirm the least output current ripple. Hence, the input inductor L_1 value was chosen with minimal current ripple Δ_{iL}. The inductor current, i_L for the proposed converter is supplied from either a PV or DC source (V_{PV} or V_{in}). When the converter receives a supply voltage from the input source, the converter power switch T is turned ON, and inductor current i_{L1} is derived as follows. Applying Kirchhoff's voltage law in mode-I [t_a–t_b], the capacitors current i_{C1} and i_{C2} are derived as

$$\begin{aligned} -V_{PV} + v_{L1} = 0 \Rightarrow v_{L1} = V_{PV} \\ -v_{C2} + v_{L2} + v_{C3} = 0 \Rightarrow v_{L2} = -v_{C3} + v_{C2} \end{aligned} \quad (1)$$

$$\begin{aligned} -i_T + i_{L1} - i_{C2} &= 0 \\ i_O - i_{L2} - i_{C3} &= 0 \end{aligned} \tag{2}$$

$$\begin{aligned} i_{C2} &= -i_{L2} \\ i_{C1} &= -i_O \end{aligned} \tag{3}$$

During mode-II [t_b–t_c], when the power switch T is in OFF, the coil transfers energy to the capacitors C_1 and C_3. As a result, from loop 1 and loop 2, it can verify that

$$\begin{aligned} &-V_{PV} + v_{L1} + v_{C2} = 0 \Rightarrow v_{L1} = -v_{C2} + V_{PV} \\ &v_{L2} + v_{C3} = 0 \Rightarrow v_{L2} = -v_{C3} \\ &v_{C2} = v_{C1} \end{aligned} \tag{4}$$

From loop 1 and loop 2 (mode-II Figure 2b), the capacitor current i_{C1} and i_{C2} are derived as follows,

$$\begin{aligned} i_{C1} &= i_{D1} - i_O \\ i_{C2} &= i_{L1} - i_{D1} = i_{D2} - i_{L2} \end{aligned} \tag{5}$$

$$I_C = \frac{1}{T}\int_0^T i_C dt = \frac{C}{T}\int_0^T dv_C(t) = \frac{C}{T}(v_C(T) - v_C(0)) \tag{6}$$

during steady-state condition $V_{C(T)} = V_{C(0)}$. Hence, the average value of the current capacitors is null. Also, the inductor coils average voltage is zero, since $v_L(t) = L\frac{di_L(t)}{dt}$. The currents in the inductors and voltage in the capacitors tend to be approximately constant. The power switch is in the ON state for a percentage of the period (δT) and OFF during the next state (δT-T). Here, T is the total switching time. Therefore, the average value inductor voltage V_{L1} and capacitor's current i_{C1} are illustrated in Figure 4 and Figure 7.

$$V_{L1} = \frac{1}{T}\left[\int_O^{\delta T} V_{PV} dt + \int_{\delta T}^{T} (V_{PV} - V_{C1}) dt\right] = 0 \tag{7}$$

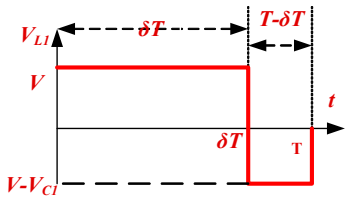


Figure 4. Inductor voltage V_{L1}.

Replacing the voltage on the calculation, we obtain the capacitor voltage V_{C1}

$$V_{C1} = \frac{1}{1-\delta} V_{PV} \tag{8}$$

The inductor L_2 voltage is illustrated in Figure 5, and inductor average voltage value is

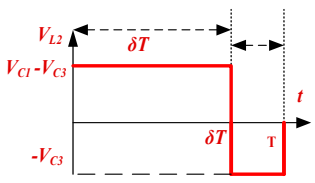


Figure 5. Inductor voltage V_{L2}.

$$V_{L2} = \frac{1}{T}\left[\int_0^{\delta T}(V_{C1} - V_{C3})dt + \int_{\delta T}^{T} -V_{C3}dt\right] = 0 \tag{9}$$

The voltage across the capacitor C_3 can be written as

$$V_{C3} = \frac{\delta}{1-\delta}V_{PV} \tag{10}$$

Hence, the converter output voltage can be calculated as

$$V_O = \frac{1+\delta}{1-\delta}V_{PV} \tag{11}$$

By equating the converter input power and output power, the input inductor current is derived as

$$V_{PV}I_{L1} = V_O I_O \Rightarrow I_{L1} = \frac{1+\delta}{1-\delta}I_O \tag{12}$$

When the Kirchhoff's current law is applied in the loop

$$i_{C3} + i_O - i_{L2} = 0 \Rightarrow i_{L2} = i_{C3} + i_O \tag{13}$$

The capacitor C_3 charge and discharge current is shown in Figure 6. Here the capacitor current average value observed is zero, and the average current in the inductor is similar to the average output current, as the inductor tends to retain that average value.

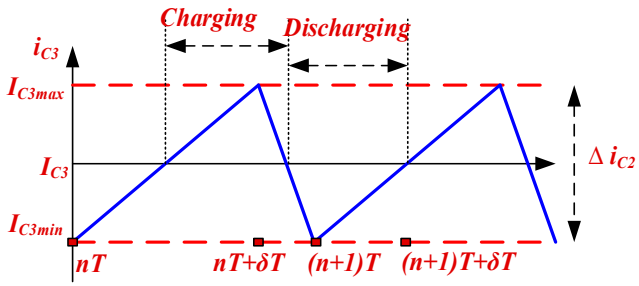


Figure 6. Capacitor current i_{C3}.

Assuming that $i_0 = i_{l2}$

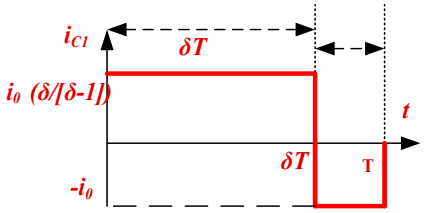


Figure 7. Capacitor current C_1.

The mean value of the capacitor C_1 current (i_{C1}) is displayed in Figure 7. From the capacitor current interval zero to δT and δ to T time, the i_{C1} is calculated as

$$I_{C1} = \frac{1}{T}\left[\int_0^{\delta T}(-i_O)dt + \int_{\delta T}^{T}(i_{D1} - i_O)dt\right] = 0 \tag{14}$$

$$i_{D1} - i_O = i_O\frac{\delta}{1-\delta} \tag{15}$$

When the power switch T is turned ON, the diode D_1 current is calculated as

$$i_{D1} = \frac{I_O}{1-\delta} \tag{16}$$

Similarly, when the power switch T is turned OFF, the diode D_2 current is calculated as

$$i_{L1} - i_{D1} = i_{D2} - i_{L2} = I_O \frac{\delta}{1-\delta} \tag{17}$$

$$i_{D2} = \frac{I_O}{1-\delta} \tag{18}$$

The current of the power switch T can be written as

$$i_T = i_{L1} - i_{C2} = \frac{2I_O}{1-\delta} \tag{19}$$

3. Scaling Converter Components Design

The proposed hybrid converter reactive components, inductors coil (L_1 and L_2) and capacitors (C_1, C_2 and C_3), are calculated for maximum values as the power switch T should support both the converter voltage and current.

3.1. Design of Inductors

The inductor coil (L_1 and L_2) values calculation and current limitation analysis are observed by precise variation concerning the average value shown in Figure 8. The differential equation of inductor voltage V_L is shown as

$$v_L(t) = L\frac{di_L(t)}{dt} \tag{20}$$

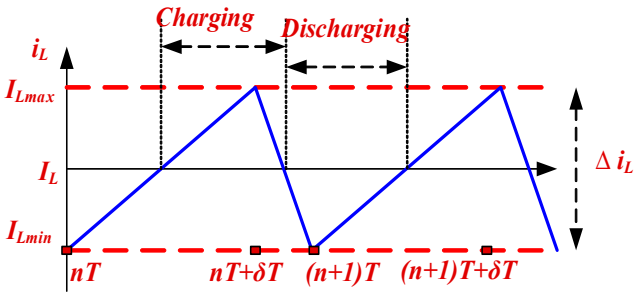


Figure 8. Evolution of the inductor current.

By assuming inductor voltage V_L nearly constant, the current equation inductor is calculated as follows

$$i_L(t) = \frac{v_L}{L}\Delta t_L + i_L(t0) \tag{21}$$

Thus, $v_L(t) = L\frac{di_L(t)}{dt}$ it becomes

$$\frac{\Delta i_L}{\Delta t_L} = \frac{v_L}{L} \tag{22}$$

Using the instantaneous inductor voltage equation, the inductor voltage will be

$$v_{L1} = \begin{cases} V_{PV}, & nT < t < nT + \delta T \\ V_{PV} - V_{C1}, & nT + \delta T < t < (n+1)T \end{cases} \tag{23}$$

During 'ON' state of the power switch, $\Delta t_L = \delta T$

$$L_1 = \frac{V_{PV}\delta T}{\Delta i_{L1}} \tag{24}$$

$$v_{L2} = \begin{cases} V_{C1} - V_{C3,} & nT < t < nT + \delta T \\ -V_{C3,} & nT + \delta T < t < (n+1)T \end{cases} \tag{25}$$

For the 'OFF' state of the power switch, it has $\Delta t_L = (1-\delta)T$

$$L_2 = \frac{v_{C3}(1-\delta)T}{\Delta i_{L2}} \tag{26}$$

3.2. Design of Capacitors

The calculation of capacitor values C_1, C_2 and C_3 are given below. The changing and discharging variation around the average value is shown in Figure 9.

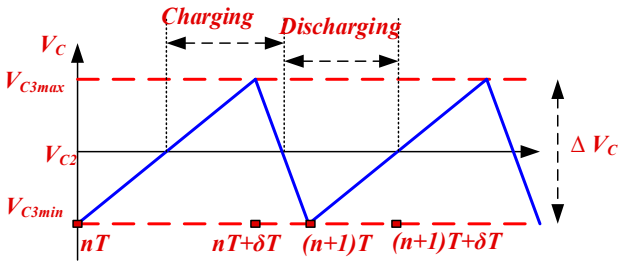


Figure 9. Evolution of the current in the coil.

The differential equation of the capacitor

$$i_c(t) = C\frac{dv_c(t)}{dt} \tag{27}$$

Similar to the calculation of inductors, the capacitor variation is calculated using Equation (27) after linearization of $i_c(t) = C\frac{dv_c(t)}{dt}$ becomes,

$$\frac{\Delta v_c}{\Delta t_c} = \frac{i_C}{C} \tag{28}$$

With the instantaneous value of the capacitor current over a certain period, the value of the capacitor can be calculated. For capacitor C_1, the current is given by:

$$i_{C1} = \begin{cases} -I_0, & nT < t < nT + \delta T \\ I_0\frac{\delta}{1-\delta}, & nT + \delta T < t < (n+1)T \end{cases} \tag{29}$$

During the first-time interval, for $\Delta t_c = \delta T$, C_1 is

$$C_1 = \frac{I_0\delta T}{\Delta v_{C1}} \tag{30}$$

The capacitor current C_2 is given by

$$i_{C2} = \begin{cases} -I_0, & nT < t < nT + \delta T \\ I_0\frac{\delta}{1-\delta}, & nT + \delta T < t < (n+1)T \end{cases} \tag{31}$$

During the time interval, when $\Delta t_c = \delta T$

$$C_2 = \frac{I_0 \delta T}{\Delta v_{C2}} \tag{32}$$

For capacitor C_3, the current does not show instantaneous values and is nearly constant during the switching state. The behavior of capacitor C_3 is opposite capacitors C_1 and C_2. When controlling the power semiconductor switch for the driving load variation, capacitor charge ΔQ is related to the inductor current $\Delta i_{L2}/2$ and time is taken T/2.

$$Q = Cv_c \Rightarrow C = \frac{Q}{v_c},\ C_3 = \frac{\Delta Q}{\Delta v_{c3}} \tag{33}$$

$$\text{At load variation, } \Delta Q = \frac{\frac{T}{2}\frac{\Delta i_2}{2}}{2} = \frac{T\Delta i_{L2}}{8} \tag{34}$$

$$\text{The capacitor } C_3\text{value is calculated as } C_3 = \frac{T\Delta i_{L2}}{8\Delta v_{c3}} \tag{35}$$

In the dynamic condition, capacitors C_1 and C_3 values are deliberate in this section. The calculation is computed by including the sudden change in drive load resistance. Output voltage in the dynamic operating region is determined using the equivalent circuit (Figures 10 and 11), assuming that the current passes zero to its steady-state value, Δt_1, the settling time of the current in the inductor L_1.

$$i_{C1} = C_1 \frac{dv_{C1}}{dt} = -i_0 \quad \Rightarrow v_{C1}(t) = \frac{1}{C_1}\int_0^t (-i_0)dt + v_{C1}(0) \tag{36}$$

$$v_{C1}(\Delta t_1) = \frac{1}{C_1}\int_0^t (-i_0)dt + v_{C1}(0) = -\frac{1}{C_1}\frac{P_0}{V_0}\Delta t_1 + v_{C1}(0) \tag{37}$$

Thus, capacitor voltage VC_1 is calculated using Equation (37)

$$v_{C1}(\Delta t_1) = \frac{1}{C_1}\int_0^t (-i_0)dt + v_{C1}(0) = \frac{1}{C_1}\frac{P_0}{V_0}\Delta t_1 \Rightarrow C_1 = \frac{1}{\Delta v_{C1}}\frac{P_0}{V_0} \tag{38}$$

In a dynamic case, while changing the converter duty ratio, the inductor current increases coil rapidly. Hence, the Δt_1 value needs to calculate, in detail, from the response of $i_{LI}(s)$, which displays the input current of the response when rapid changes occur in output current $i_o(s)$. At time Δ_{t2}, the current flow through the capacitor C_3 is calculated as

$$i_{C3} = C_2 \frac{dv_{C3}}{dt} = -i_0 \tag{39}$$

$$C_3 = \frac{1}{\Delta v_{C3}}\frac{P_0}{V_0}\Delta t_2 \tag{40}$$

For calculation straightforwardness, it is assumed that the current has equal settling times.

In terms of the energetic properties, the proposal converter is similar to the boost and Cuk converters. The proposed converter input inductor, power switches and input source are organized the same way as the classical boost and Cuk converters. Except for the input side boost inductor (L_1) and the power switch T, the rest of the proposed converter circuit elements are connected precisely in parallel with each other and on the output side, two capacitors (C_1 and C_3) are placed across the load. Therefore, the proposed converter increases the voltage gain by combining the benefits of boost and Cuk converters.

3.3. Small Signal Analysis of Hybrid DC–DC Converter

The average equivalent circuit model of the proposed hybrid DC–DC converter was derived and is presented in Figure 10. The circuit analysis was derived for the switch in both the ON and OFF period. The initial conditions were an approach to obtain the average value of the coil; the current remained the same.

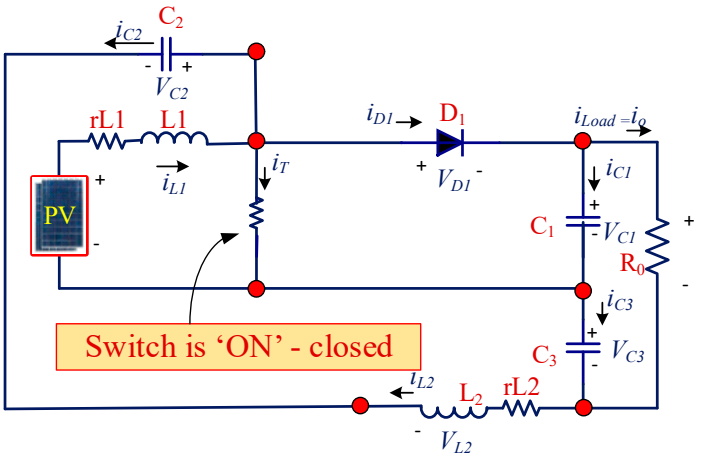


Figure 10. Equivalent circuit of the converter with losses in the mode-1 operation.

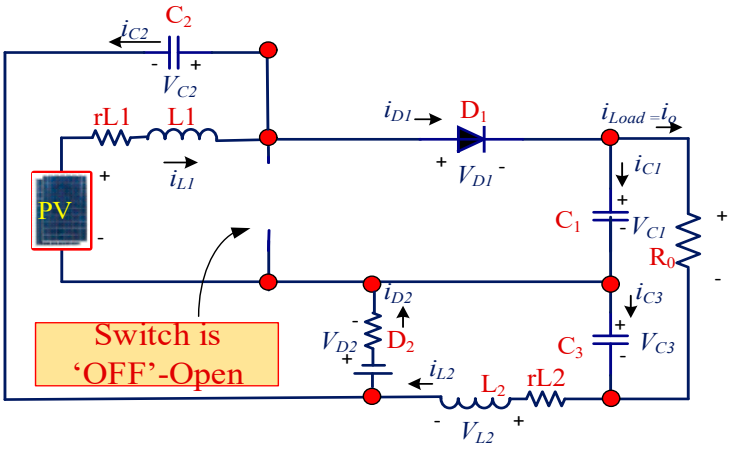


Figure 11. Equivalent circuit of the converter with losses in mode-2 and mode-3 operation.

By the application of mesh law to the circuit in Figure 10, we can verify that

$$\begin{cases} -V_{PV} + v_{L1} + r_{L1}I_{L1} + R_{DSon}i_T = 0 \\ v_{C2} - v_{L2} - R_{DSon}i_T - vc3 - r_{L2}I_{L2} = 0 \end{cases} \Rightarrow \begin{cases} v_{L1} = -V_{PV} - r_{L1}I_{L1} - R_{DSon}i_T \\ v_{L2} = v_{C2} - R_{DSon}i_T - v_{C3} - r_{L2}I_{L2} \end{cases} \quad (41)$$

$$\begin{cases} -V_{PV} + v_{L1} + r_{L1}I_{L1} + v_{C2} + V_{D2} + R_{D2}i_{D2} = 0 \\ v_{L2} + r_{L2}I_{L2} + v_{C3} + V_{D2} + R_{D2}i_{D2} = 0 \end{cases} \Rightarrow \begin{cases} v_{L1} = -V_{PV} - r_{L1}I_{L1} - v_{C2} - V_{D2} - R_{DSon}i_T \\ v_{L2} = -r_{L2}I_{L2} - v_{C3} - V_{D2} - R_{D2}i_{D2} \end{cases} \quad (42)$$

$$-V_{PV} + v_{L1} + r_{L1}I_{L1} + v_{C1} + v_{D1} + R_{D1}i_{D1} = 0 \quad (43)$$

$$v_{D1} = v_{D2},\ R_{D1}i_{D1} = R_{D2}i_{D2},\ v_{C2} = v_{C1}$$

From the waveform v_{L1} and v_{L2},

$$V_{L1A} = V_{PV} - R_{Dson}I_T - r_{L1}I_{L1} \quad (44)$$

$$V_{L1B} = V_{PV} - r_{L1}I_{L1} - V_{C1} - V_{D2} - R_{D2}I_{D2} \quad (45)$$

$$V_{L2A} = V_{C1} - R_{DSON}I_{SC} - V_{C3} - r_{L2}I_{L2} \tag{46}$$

$$V_{L2B} = -r_{L2}I_{L2} - V_{C3} - V_{D2} - R_{D2}I_{D2} \tag{47}$$

The analysis of converter input to output relation is calculated with losses and approximated with ideal semiconductor devices. The output voltage expressions of the converter were derived and are given below.

$$V_{L1} = 0 \Rightarrow V_{C1} = \frac{V_{PV} - r_{L1}I_{L1}}{1-\delta} \tag{48}$$

$$V_{L2} = 0 \Rightarrow V_{C3} = \frac{\delta}{1-\delta}(V_{PV} - r_{L1}I_{L1}) - r_{L2}I_{L2} \tag{49}$$

From the expressions V_{C1} and V_{C2}, the voltage gain converter is calculated as

$$\frac{V_0}{V_{PV}} = \frac{1+\delta}{1-\delta + \frac{r_{L1}}{R_0}\frac{(1+\delta)^2}{1-\delta} + \frac{r_{L2}}{R_0}(1-\delta)} \tag{50}$$

where $r_{L1}/R_0 = r_{L2}/R_0$.

Figure 12 illustrates the voltage output gain versus the duty cycle for the proposed hybrid converter. The Figure indicates the ideal condition ($r_{L1}/R_0 = 0$), where losses need to be introduced in the circuit (the gain for unit value goes to zero, as expected) and other operating conditions $r_{L1}/R_0 = r_{L2}/R_0 = 0.0001$ to 0.76, where near 0.76 duty cycle, the converter gain approaches six times boosting ($V_0 = 6V_{in}$).

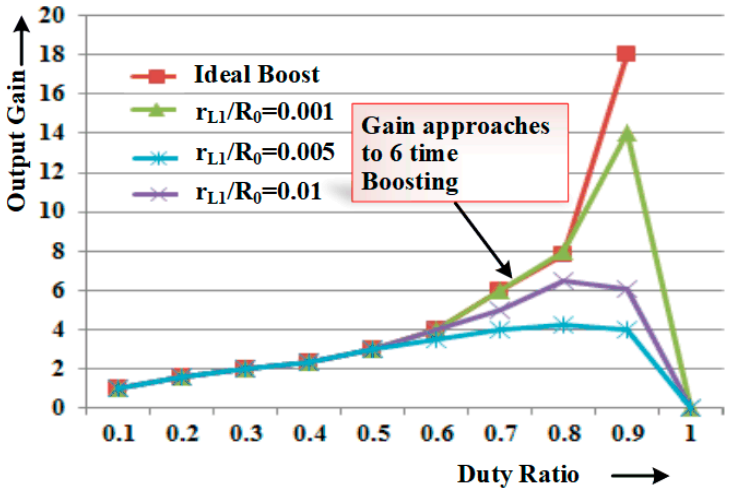


Figure 12. Voltage output gain versus duty cycle.

3.4. Analysis of Losses

The losses of each indictor L_1 and L_2 are denoted from internal resistors r_{L1} and r_{L2}, respectively. Thus, the losses in r_{L1}

$$P_{\rightleftarrows r_{L1}} = p_{1\rightleftarrows}\, P_{i\rightleftarrows} = r_{L1}I_{L1rms^2} \Leftrightarrow r_{L1} = \frac{p_1 P_i}{I_{L1rms}{}^2} \tag{51}$$

The sufficient value is given as

$$I_{L1rms} = \sqrt{I_{L1}{}^2 + \left(\frac{\Delta i_{L1}}{2\sqrt{3}}\right)^2} = \sqrt{I_{L1}{}^2 + \left(\frac{0.1I_{L1}}{2\sqrt{3}}\right)^2} = I_{L1}\sqrt{1 + \left(\frac{0.1}{2\sqrt{3}}\right)^2}$$

$$\Delta i_{L2} = 0.1I_{L2} \tag{52}$$

$$\text{Since both the inductors are identical, } \Delta i_{L1} = 0.1I_{L1} \tag{53}$$

Two kinds of losses in the semiconductor are driving and switching.

3.5. Conduction Losses in the Diodes

The losses in the diode are given as

$$P_D = \frac{1}{T}\int_0^T v_D(t) i_D(t) dt = V_D I_D + R_D I_{Drms}^2 \tag{54}$$

$$v_D(t) = V_D + R_D i_D(t) \tag{55}$$

Specific to the case of the diode, for mode-2 operation:

$$i_{D1}(\delta T < t < T) = \frac{I_0}{(1-\delta)} \tag{56}$$

$$I_{D1} = \frac{1}{T}\int_0^T i_{ak1}(t) dt = I_0 \tag{57}$$

$$I_{D1rms} = \sqrt{\frac{1}{T}\int_0^T i_{D1}^2(t) dt} = \frac{I_0}{\sqrt{(1-\delta)}} \tag{58}$$

Thus, resistance is calculated as

$$P_{D1} = \frac{p_3}{2} P_i = V_{D1} I_0 + R_{D1}\left(\frac{I_0}{\sqrt{(1-\delta)}}\right)^2 \Leftrightarrow R_{D1} = \left(\frac{p_3}{2} P_i - V_{D1} I_0\right)\frac{(1-\delta)}{I_0^2} \tag{59}$$

The same can be applied to D_2, resulting in the same results for this diode

$$R_{D2} = \left(\frac{p_3}{2} P_i - V_{D2} I_0\right)\frac{(1-\delta)}{I_0^2} \tag{60}$$

4. Design Procedure

The component selections and other design parameters of the proposed converter at the power range of 150 W were calculated and are presented. The input power was considered a DC-fixed source. The general diagram of the converter design flow chart is shown in Figure 13.

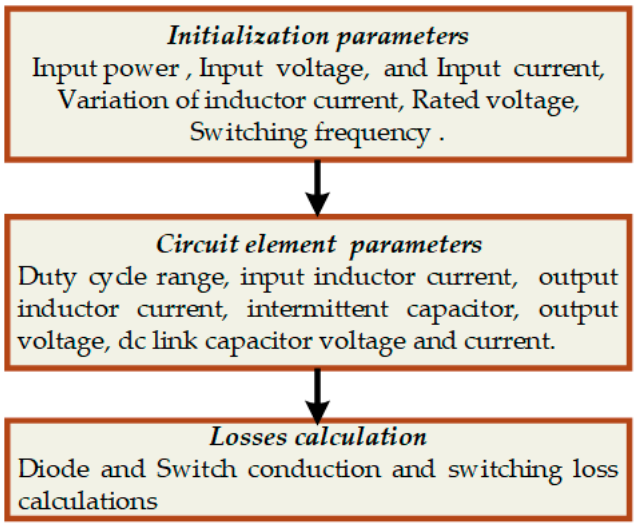


Figure 13. Design setup of converter parameter selections.

To illustrate the numerical values of converters, capacitor and inductors, the below parameters were fixed for the converter design.

i. The input power P_{in} = 150 W, for V_{in} = 24 V, I_{in} = 6.2 A;
ii. Power of the converter, P_i = 150 W;
iii. Input voltage converter V_{in} = 24 V;
iv. Duty cycle is fixed as δ = 0.8;
v. The converter output voltage, V_o = 104 V;
vi. The output current and inductor current were expected to be I_0 = 1.11 A and I_{L1} = 4.25 A, respectively;
vii. The capacitor C_1 and C_3 voltages were calculated as V_{C1} = 110 V and V_{C3} = 104 V;
viii. The general typical value sizing of capacitor C_1, C_3 and L_1, L_2 was calculated as Δi_{L1} = 10% I_{L1}, hence for L_1 = 1 mH, the change in this was Δi_{L1} = 0.425 A. The same changes can be seen for Δi_{L2} = 10% I_{L2}, L_2 = 1 mH and Δi_{L2} = 0.14 A;
ix. When the change in the capacitor ΔV_{C1} was 1% V_{C1}, the capacitor C_1 value was 100 µF and ΔV_{C1} = 1.10 V. Similarly, for ΔV_{C2} = 1% V_{C2}, C_2 = 100 µF, ΔV_{C2} = 1.04V and ΔV_{C3} = 1% V_{C3}, C_3 = 2 µF,ΔV_{C3} = 0.08 V;
x. For the power semiconductor switch, the maximum open-circuit voltage was Vs_{max} = 100 V, Vs_{max} = 95 V;
xi. Diodes D_1 and D_2, Vs_{max} = 100 V, Vs_{max} = 95 V.

The D_1 and D_2 can ensure a voltage of 100V, which ensures the safety factor of the converter. The converter can support a maximum current of six amps. When using six amps, the current safety factor is reduced to 60%–65%. Hence, the semiconductor must be selected to withstand the converter to provide maximum currents and voltages with a safety factor around 50%. The n-type reinforcing MOSFET is better chosen for providing the safety factor, and the proposed converter design uses the same [35]. The diodes (D_1 and D_2), and MOSFET switching losses and conduction losses were calculated and given in Equations (61)–(73).

Conduction losses of the diode D_1 and D_2:

$$P_D = \int V_{ak}\,(t)\; i_{ak}\,(t)dt = V_D i_{ak+} R_D I_{akrms}^2 \tag{61}$$

$$R_{D1} = \left(\frac{p3}{2} p_i - V_{D1} I_o\right) \frac{(1-\delta)}{I_o^2} \tag{62}$$

$$R_{D1} = \left(\frac{p3}{2} p_i - V_{D2} I_o\right) \frac{(1-\delta)}{I_o^2} \tag{63}$$

$$P_{D1} = V_{D1} i_{ak1+} R_{D1} I_{akrms1}^2 \tag{64}$$

$$P_{D2} = V_{D2} i_{ak2+} R_{D2} I_{akrms2}^2 \tag{65}$$

Switching losses of the Diode D_1 and D_2:

$$P_{SD1} = \frac{t_{rr} - t_s}{T} V_{ak1} i_{ak1} \tag{66}$$

$$P_{SD2} = \frac{t_{rr} - t_s}{T} V_{ak2} i_{ak2} \tag{67}$$

Conduction losses of the MOSFET:

$$P_{\text{MOSFET Conduction Loss}} = R_{DS\_ON} i_{\text{MOSFET rms}} \tag{68}$$

$$i_{MOSFET} = \frac{2I_0}{(1-\delta)} \tag{69}$$

$$P_{P_{MOSFET\ switcing\ loss}} = \frac{t_{ON} + t_{OFF}}{T}(V_{MOS} i_{MOS}) + \frac{1}{2T}(C_{MOS} V_{MOS})^2 \tag{70}$$

Total switching losses for the proposed converter is:

$$P_{total\ switcing\ losses} = \frac{t_{ON} + t_{OFF}}{T}(V_{MOS} i_{MOS}) + \frac{1}{2T}(C_{MOS} V_{MOS})^2 + 2\frac{t_{rr} - t_s}{T} V_{ak} i_{ak} \tag{71}$$

$$t_{ON} = t_r(i_{MOS}) + t_f(V_{MOS}) \tag{72}$$

$$t_{OFF} = t_f(i_{MOS}) + t_r(V_{MOS}) \tag{73}$$

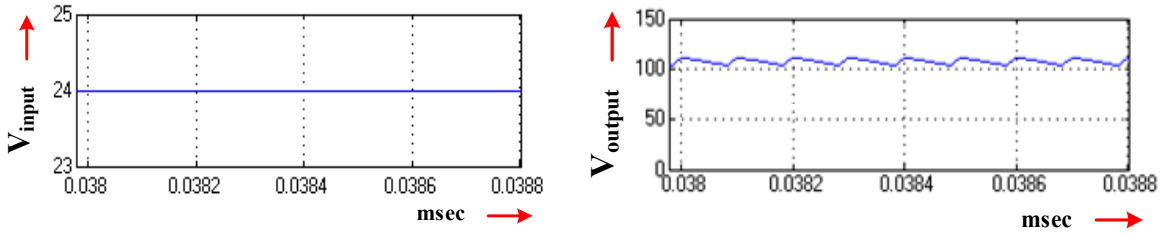
The efficiency of the proposed converter is found using

$$\eta = \left(\frac{p_o}{p_i}\right) = \frac{P_i - \sum P_T}{P_i} \tag{74}$$

where P_i = input power and $\sum P_T$ = Total losses ($P_{Diode2\ Con.Losses}$ + $P_{Diode2\ Con.Losses}$ + $P_{MOSFET\ switching\ loss}$ + $P_{MOSFET\ Conduction\ Loss}$).

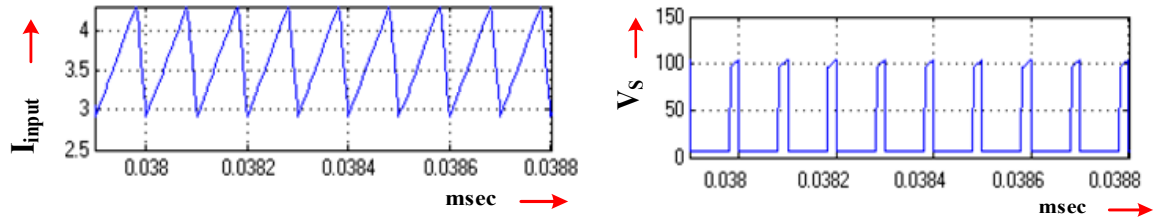
5. Simulation Results

The hybrid DC–DC converter operation and performance estimation were modeled in the MATLAB/Simulink simulation platform and waveforms were presented. The simulation specification and parameter were as follows: The input power = 150 W, input voltage of the converter (V_{in}) = 24 V, maximum duty cycle δ = 0.8 and switching frequency f_s = 10 kHz. The converter input and output inductors were L_1 = 1 mH and L_2 = 1 mH receptivity. The capacitors were C_1 = 100 µF, C_2 = 100 µF and C_3 = 2 µF. Figures 14–17 show the proposed converter simulation results for 10 kHz switching frequency and 80% duty cycle, and the results confirm the theoretical values. The converter duty cycle was fixed to be equal to or less than 0.8 to minimize the conduction losses. From Figure 14, when the converter duty cycle was fixed at 0.8 with 24V input voltage, the converter delivered an output voltage of 124 V (5.166 times higher than the input voltage). During the continuous conduction mode, the inductance L1 current was limited within the saturation limit in the range of 3 to 4.5 A and maintained the converter input current. Figure 15 displays the input current, as well as voltage across the power switches, and Figure 17 shows D_1 and D_2 voltages, V_{D1} and $V_{D2,}$ respectively, during the switching period. From the results, it could be seen that during the time of switching, the switches (MOSFET and diode) were maintained with their maximum allowable voltage as 100 V. It was verified that the voltage across the switches was less than that of the converter. From the i_{L2} and V_{D2} simulation results, it can be seen that the proposed converter maintains a continuous current capability. Figure 16 shows the simulation waveforms for the inductor current i_{L1} and inductor current i_{L2}. From this waveform, it is seen that the inductors were charging uniformly and delivering the current in the continuous conduction. Figure 17 illustrates the voltage across the power diode, V_{D1} and V_{D2}. When the duty cycle was reduced to 0.6, the converter performance, switching reliability and continuous current capability were linear. Hence, the proposed converter has a wide range of controllability with a controlled degree of freedom to avail wider voltage outputs. The simulation was also performed in transient conditions (changing load and sudden change in the duty cycle). During this transient period, the output voltage and current through i_{L1} changed with a small transient period and after reaching the continuous conduction and maintaining the constant output voltage.



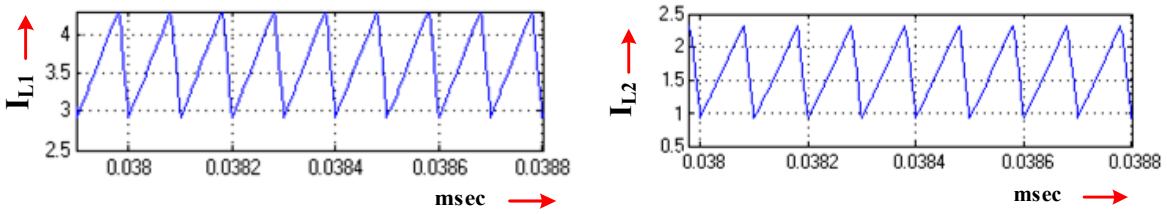
(**a**) (**b**)

Figure 14. Simulation waveforms for input voltage 24V DC and 0.8 duty cycle; (**a**) input voltage waveform (voltage scale: 1 V/div and t: 20 μs/div) and (**b**) input voltage waveform (voltage scale 50 V/div and t: 20 μs/div).



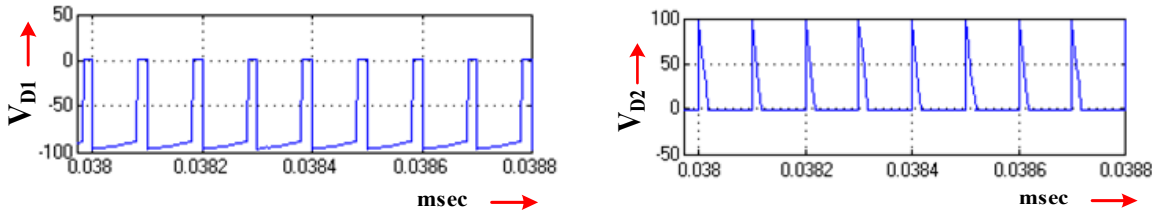
(**a**) (**b**)

Figure 15. Simulation waveforms for input voltage 24V DC and 0.8 duty cycle; (**a**) input current waveform (current scale: 0.5 A/div and t: 20 μs/div) and (**b**) voltage across the power switch waveform (voltage scale 50 V/div and t: 20 μs/div).



(**a**) (**b**)

Figure 16. Simulation waveforms for input voltage 24 V DC and 0.8 duty cycle; (**a**) inductor current i_{L1} waveform (current scale: 0.5 A/div and t: 20 μs/div) and (**b**) inductor current i_{L2} waveform (current scale: 0.5 A V/div and t: 20 μs/div).



(**a**) (**b**)

Figure 17. Simulation waveforms for input voltage 24V DC and 0.8 duty cycle; (**a**) voltage across the power diode, V_{D1} waveform (voltage scale: 50 V/div and t: 20 μs/div) and (**b**) voltage across the power diode, V_{D2} waveform (voltage scale: 50 V/div and t: 20 μs/div).

The proposed single switch hybrid DC–DC converter is compared with conventional converters (boost and Cuk) for different duty cycles from the range zero to one. The switching frequency and other circuit components for this evaluation were taken as being the same as the proposed converter values are given in the design (see Table 1). As expected, the proposed converter voltage gain was more than the boost and Cuk converter duty cycle. Figure 18 shows the voltage gain comparison of boost and Cuk with the proposed converter.

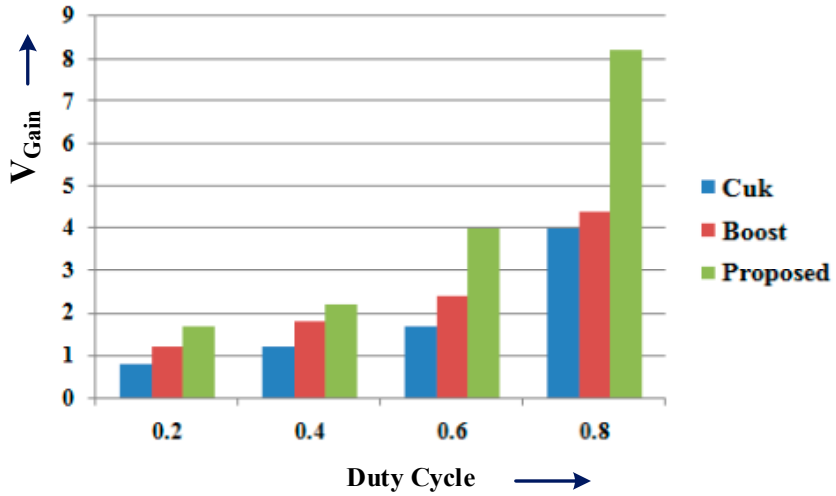


Figure 18. Voltage gain comparison of boost and Cuk with the proposed converter.

6. Experimental Results

To confirm the experimental performance of the proposed hybrid DC–DC converter, the experimental laboratory setup was developed in collaboration with a Peripheral Interface Controller (PIC) microcontroller, as shown in Figure 19. To verify the theoretical and simulation results, the experimentations were conducted with similar values considered in the simulation studies. The converter was a 150 W circuit with parameters as listed in Table 1.

Similar to the simulation verification, the converter duty cycle was fixed as equal to or less than 0.8 to minimize the conduction losses. While testing the converter, the input DC source was fixed to generate constant input voltage and power as 24 V and 150 W range. As seen in Figure 20, while the converter duty cycle was fixed as 0.8, the corresponding output voltage was observed to be 122 V (closer to the simulation results). Figure 21 shows the converter input current and output voltage.

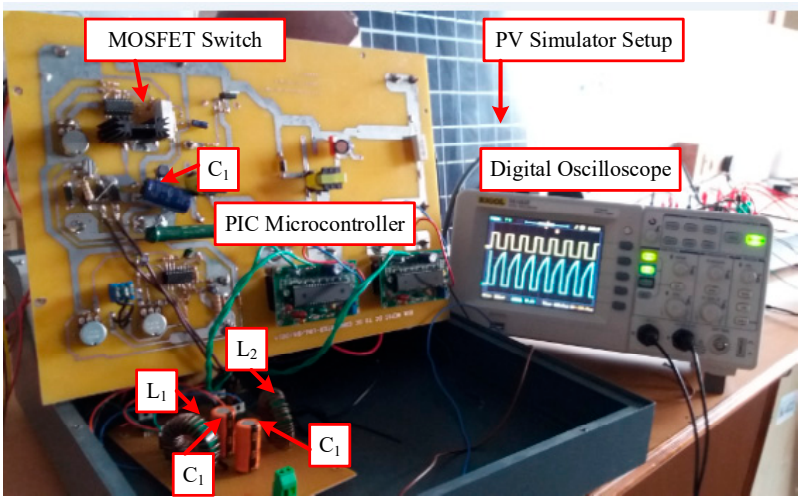


Figure 19. Prototype setup of the proposed converter.

Table 1. Parameter of components of the proposed converter.

Components	Parameter
Input power P_{input}	150 W
Input voltage V_{in}	24 V
Output power P_0	112 W
Switching frequency f_s	10 KHz
Power MOSFET	SiHB30N60E
Diode D_1 and D_2	VS-15EWX06FN-M3
Inductance L_1 and L_2	1 mH
Capacitor C_1,C_2 and C_3	100 µF, 100 µF and 2 µF
The output of Diode V_{D1} and V_{D2}	100 V and 95 V
Output Capacitor V_{C1},V_{C2} and V_{C3}	104 V, 110 V and 8 V

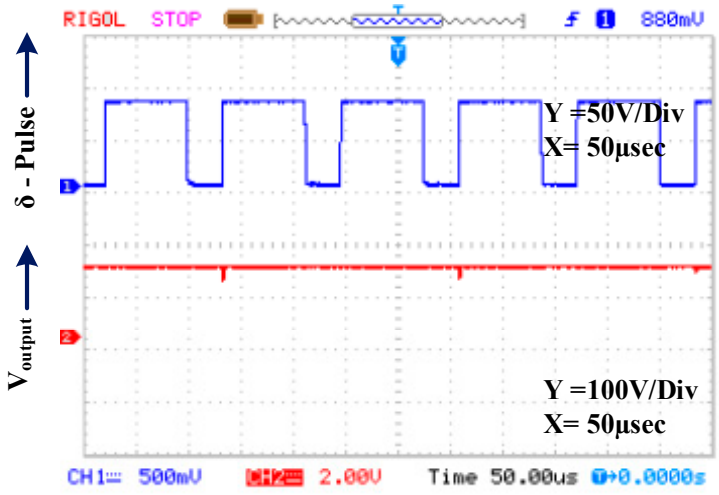


Figure 20. The experimental waveform of the duty cycle and input voltage.

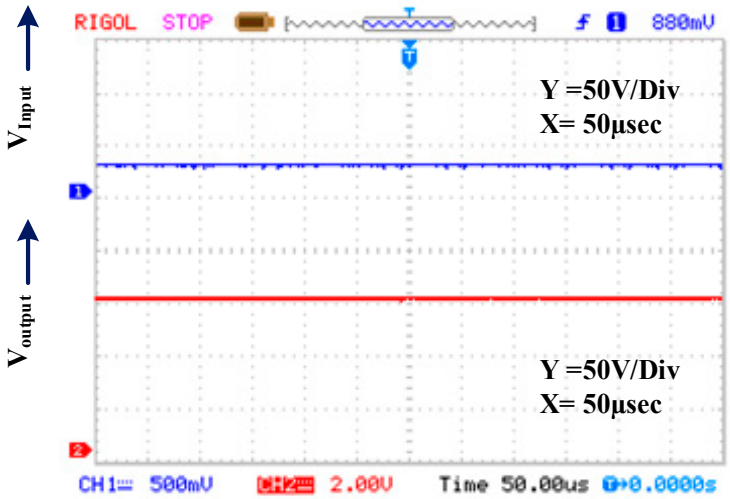


Figure 21. The experimental waveform of input voltage and output voltage for input voltage 24 V and 0.8 duty cycle.

During the DC-to-DC conversion period, the converter maintained the continuous conduction with the inductance L_1 current saturation limit range of 3 to 4.5 A, as depicted in Figure 22. Hence, the power switch was secured against the high rising current by maintaining the converter input current inductance L_1 current saturation limit, which ensures the converter reliability against the input source. Similarly, from Figures 23 and 24, during the time of switching, the MOSFET and diode were maintained with their maximum allowable voltage as 100 V, which was smaller than the converter output voltage (102 V). Here, during the switching period, the voltage across the main power switch was 100 V, and diode D_1 and D_2 were equal to V_{D1} = 100 V and V_{D2} = 95 V, respectively. During the entire mode of operation, the inductor current i_{L1} and i_{L2} maintained the identical current profile, which maintains the voltage balance between C_1 and C_2. Figure 25 shows the experimental waveform of the input inductor current, i_{L1} and voltage across i_{D2} the power switch for input voltage 24 V and 0.8 duty cycle.

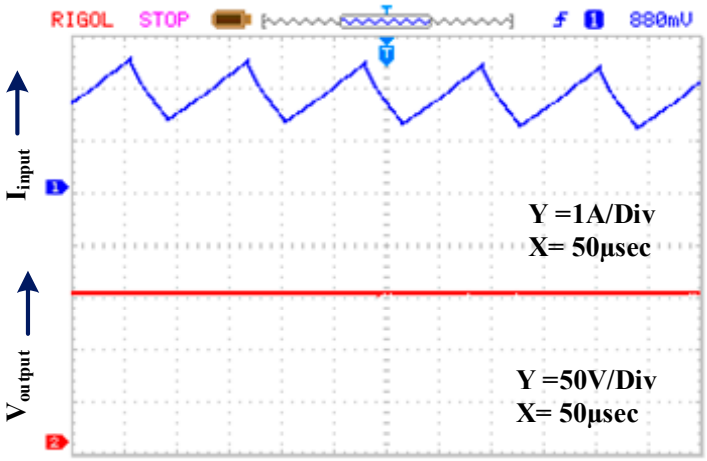


Figure 22. The experimental waveform of input current and output voltage for input voltage 24 V and 0.8 duty cycle.

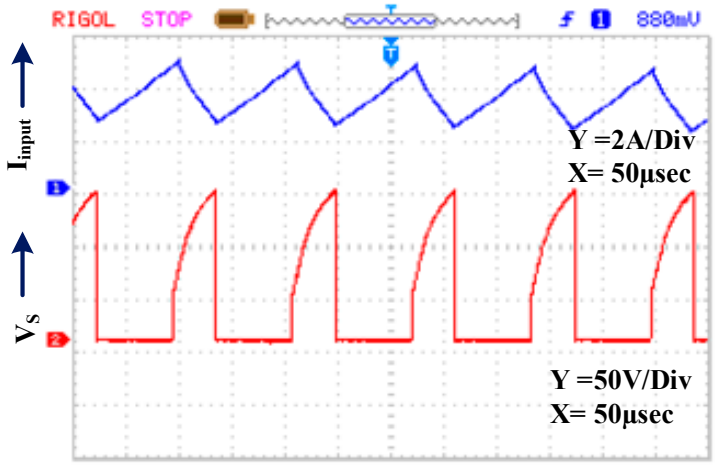


Figure 23. The experimental waveform of input current and voltage across the power switch for input voltage 24 V and 0.8 duty cycle.

Next, the converter was operated by changing the duty ratio to observe transient operation behaviour. For the period of transient operation, the converter load was kept constant as the previous value. During the trial, the switching duty-cycle varied from 0.8 to 0.5. During this period, likely the output voltage decreased and stabilized after a few milliseconds. A similar response happened in the inductor current i_{L1} and preserved in the converter in continuous conduction.

To validate the comparison of the theoretical and experimental results, the converter continuous conduction mode(CCM) state voltage gain was plotted concerning the variation duty ratio from 0.2 to 0.8 (see Figure 26a). From the results, it can be seen that the experimental values are very close to the theoretical calculations. Finally, the efficiency of the proposed converter was found under full load. The calculated experimental maximum efficiency of the proposed converter at 0.8 duty cycle is 92.2%. The calculated experimental maximum efficiency of the proposed converter is 92.2%. Figure 26b shows experimental power loss distribution operating at the rated condition. During duty ratio $\delta = 0.8$, the semiconductors (D_1, D_2 and MOSFET) switching losses were calculated as 0.4 W, 0.5 W and 1.2 W using equations (61)–(74). Hence, the total switching losses for the converter was 2.1 W. Similarly, the conduction of the power switches and other circuit parameters losses were observed. In the overall power distribution losses, the MOSFET switching loss and conduction loss alone are about 52%. As presented in Figure 26b, the I^2R losses in the MOSFET, diode and the snubber circuitry losses were accounted for as significant losses. Nevertheless, the proposed converter voltage stress reduction helps to choose the lower voltage-rating switch, and hence conduction losses are expected to reduce.

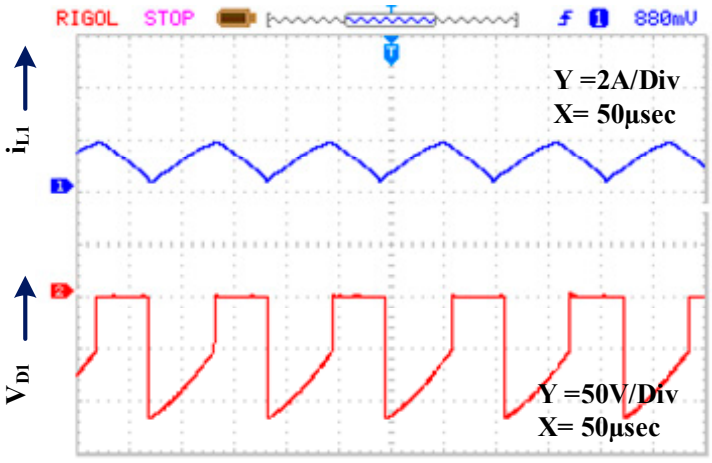


Figure 24. The experimental waveform of the input inductor current, i_{L1} and voltage across i_{D1} the power switch for input voltage 24 V and 0.8 duty cycle.

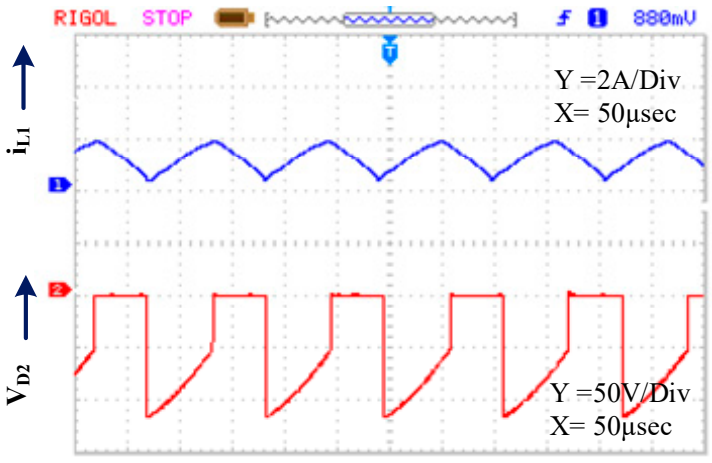


Figure 25. The experimental waveform of the input inductor current, i_{L1} and voltage across i_{D2} the power switch for input voltage 24 V and 0.8 duty cycle.

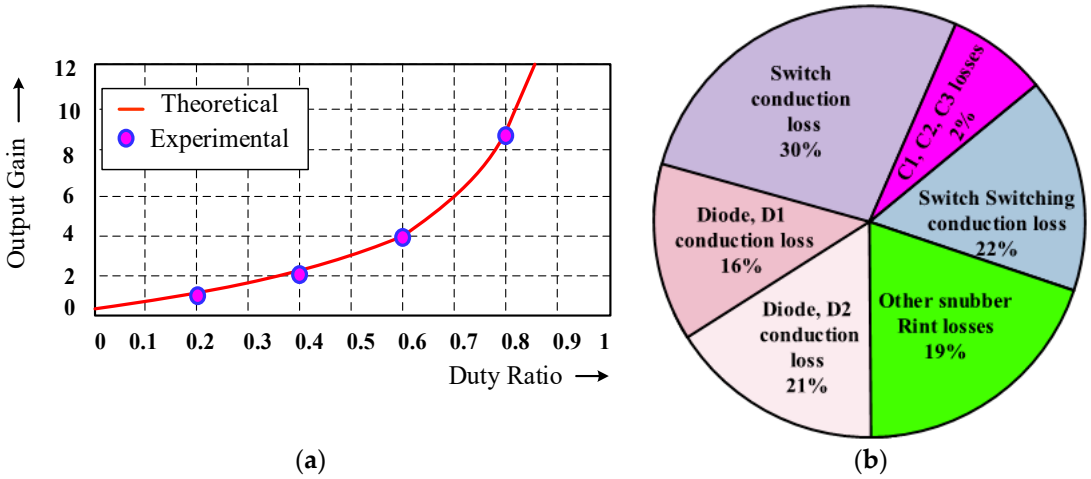


Figure 26. (**a**) Theoretical and experimental results comparison. (**b**) Experimental power loss distribution operating at rated condition (duty ratio from 0.8).

Key Performance Comparison

For validating the proposed converter performance, Table 2 shows the comparison with other similar converters. According to the table, the proposed converter provides a better voltage gain with a single active switch, and normalized voltages stress of semiconductor devices is less when compared to other converters. Based on the presented analysis and discussions, results and comparisons confirm the functionality and advantages of the proposed converter.

Table 2. Performance comparison of similar converter topology.

Similar Converter Topology	Converter [39]	Converter [9]	Converter [30]	Converter [40]	Converter [36]	Proposed Converter
Switches used	1	2	1	1	1	1
Diodes used	5	2	2	3	1	2
No. of Inductors used	3	2	2	3	2	2
No. of capacitors used	3	2	3	3	3	3
Continuous input current	Yes	No	Yes	Yes	No	Yes
Voltage gain, V_O	$\frac{(\delta)^2}{(1-\delta)^2}$ Vin	$\frac{2(1+\delta)}{(1-\delta)}$ Vin	$\frac{1}{1-\delta}$ Vin	$\frac{\delta}{(1-\delta)^2}$ Vin	$\frac{2\delta}{(1-\delta)}$ Vin	$V_O = \frac{1+\delta}{1-\delta} V_{PV}$
Efficiency	91%	90%	91%	90%	92%	92.2%
The voltage stress on the active switch	Moderate	Less	High	Less	High	Moderate

7. Conclusions

The high voltage gains and highly efficient single switch hybrid non-isolated DC–DC converter is shown in this paper. The proposed topology was derived by integrating conventional boost and Cuk converters. This topology produced a non-inverting output in continuous input current mode with a single switch having high voltage gain (≈5.116 gain). When compared with the classical boost and Cuk converters, the proposed topology facilitates a substantial voltage gain with comparable lower switching stress. The steady-state analysis under the CCM condition and design calculation for the proposed hybrid was discussed in detail.

Finally, the validation test done with the proposed converter privileges, the voltage gain, power switch voltage stress and elements used in the circuit simulation studies were presented. Characterize the proposed topology for its obtained performances, PIC microcontroller based real-time experimental setup was realized under the power rating of 150 W with an efficiency of 92.2%. Experimental results confirmed the practicability in real-time applications needs.

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