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Editorial

Special Issue "Building Three-Dimensional Integrated Circuits and Microsystems"

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With the further innovation of chip technology, semiconductor integrated circuits have made irreplaceable contributions to the development of microelectronic systems. Three-dimensional (3D) integration technology achieves a vertical interconnection at the package level by relying on wire bonding and chip flip–chip in the vertical direction to achieve multi-layer circuit bonding. Complex microsystems can be achieved at a low cost while still maintaining a high performance and integration. Compared with the traditional two-dimensional integration, 3D integration is being increasingly widely used in semiconductor and microelectronic fields, such as high-end computing, servers and data centers, military and aerospace, and medical equipment. Therefore, in order to meet the needs of the development of the times, more in-depth and extensive research on 3D integration is indispensable.

The performance of the 3D integrated system is closely related to the process technology route. The 3D stacking technology for wafer bonding satisfies the chip's demands for an increased bandwidth and reduced power consumption through the process of wafer bonding and an interconnection hole, which is of a great significance for future 3D integrated processing. In addition, the performance of the 3D stacking system is greatly improved by TSV (through silicon vias) interconnection technology. Thus, TSV technology has gained significant importance in the realm of 3D integrated circuit applications. When the three-dimensional integrated hardware technology encounters bottlenecks, the focus is shifted to the combination with artificial intelligence algorithms, which also effectively improves the overall performance of the system. The application of three-dimensional integration in microelectronics involves all aspects. The combination of bumps in micro-nano processing technology, high-density through-hole manufacturing and wafer bonding, and the continuous improvement of technology also poses high requirements for materials, components, and circuits for 3D integration.

In order to overcome these problems, the most recent advancements in 3D integration have been shared in order to enhance its functional capabilities and adapt it to diverse applications. This Special Issue of "Building Three-Dimensional Integrated Circuits and Microsystems" aims to collect excellent research results and comprehensive reports related to 3D integrated circuits and microsystems. The Special Issue is available online at https://www.mdpi.com/journal/processes/special_issues/TDIC.

This Special Issue covers a variety of theoretical and experimental research on 3D integration, focusing on the process and technology route of 3D integrated systems and the combination of artificial intelligence algorithms with different application fields.

One significant contribution of 3D integration lies in optical interconnected technology. The new generation data center is further developing in the direction of a high speed and intelligence, which suggests a great demand for the iteration of optical interconnection technology. Three-dimensional integration based on active photonic interposers can achieve the advantages of a high integration, high bandwidth, and low power consumption, which

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has become the main direction for next-generation optical module technology. For example, the author designed and verified the fabrication of optical transceivers and the 3D assembly of the modules integrated with edge couplers and RDL-TSV-RDL in [1], achieving ideal high frequency characteristics and extremely low optical coupling loss and the compatibility challenge of TSV and edge coupler fabrication. Different manufacturing processes are selected, verified, and optimized. Finally, the manufacturing and 3D assembly of the active inserter are realized, while the co-manufacturing problem of the TSV and the edge coupler is solved, which ascertains the perfect electrical and optical characteristics. It lays a solid foundation for further research and large-scale application of 3D optical modules in the future.

Another contribution of 3D integration lies in the application of parameter extraction. The author proposed an improved RF small-signal equivalent circuit model and the corresponding parameter extraction method [2]. The external parasitic effects caused by ground–signal–ground (GSG) layout are evaluated by a three-dimensional full-wave electromagnetic simulation method, and an improved five-step analytical parameter extraction method is proposed. The model parameters of the inherent device are determined analytically by using the nonlinear rational function fitting method. By comparing the device simulator and the electromagnetic simulator, the effectiveness of the proposed small-signal equivalent circuit model and the corresponding extraction method is verified.

The technology has piqued the curiosity of researchers who are exploring its potential applications, including its use in radiation detectors. At present, the commonly used integration methods of silicon PIN radiation detectors are faced with the challenges of a complex process, poor reliability, and dead layer thickness. In order to reduce metal signal crosstalk, the package volume and weight, a new integration method based on metal bonding technology was proposed to realize the integration of thick and thin detectors [3]. Based on existing works, the authors aimed to achieve a good bonding strength at a low bonding temperature and pressure, which is important for the future of 3D-integrated processing and the performance optimization of silicon PIN detectors [3]. The deep learning algorithm can quickly simulate complex physical correlations by training a large amount of data to enhance the efficiency. The deep learning classification model was used to determine the adhesion strength of the wafer by analyzing the surface morphology without using any tensile strength test equipment, thus effectively reducing the cost of instrument testing [4]. The authors used an artificial intelligence algorithm to establish a two-dimensional warranty decision model integration model, and used a grid search algorithm, PSO algorithm, and PSO-based algorithm to obtain the optimal EW scheme of the gearbox of the electric multi-unit (EMU) system. The analysis results show that the model established has a good practicability and effectiveness [5].

TSV is one of the most advanced technologies in the semiconductor manufacturing industry. Due to its superior electrical properties, reduced power consumption, increased bandwidth, higher density, smaller form factor, and lighter weight, it has emerged as a promising area for future advancement. The selection of a crucial parameter for achieving the TSV process is linked to the selection of process technology, which ultimately dictates the TSV performance to a significant degree. The proposed scheme achieves an obvious improvement in reducing system noise and area and provides a learning idea for future related research [6].

In this Special Issue, the application of 3D integration in a warranty decision model, parameter extraction in a circuit model and a metal detector, and the optical interconnection was studied. The technology of the 3D integration process route, such as TSV and wafer bonding, is discussed. Today, with the development of semiconductors and microelectronics, it is essential to fully understand the design and manufacturing of three-dimensional integrated packaging for a complex system-level interconnection density enhancement and new interlayer interconnection processes. This Special Issue presents new concepts and methodologies for advancing 3D integration. The combination of hardware upgrades,

algorithmic improvements, and process techniques has been experimentally tested and validated, providing a valuable reference for future research in this field.

Finally, we hope that the content of this Special Issue can provide valuable information for researchers involved in 3D integration in different fields.

Conflicts of Interest: The authors declare no conflict of interest.

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