energies

MDPI

Article

Sampling Rate and Performance of DC/AC Inverters with Digital PID Control—A Case Study

Marian Blachuta *, Robert Bieda and Rafal Grygiel

Department of Automatic Control and Robotics, Silesian University of Technology, 16 Akademicka Str., 44-100 Gliwice, Poland; robert.bieda@polsl.pl (R.B.); rafal.grygiel@polsl.pl (R.G.)
* Correspondence: marian.blachuta@polsl.pl

Abstract: The huge influence of the sampling rate on the performance of the digital PID control of a voltage source inverter (VSI) is revealed. It is shown that an appropriately chosen continuous-time model of a digital controller with the PWM power converter behaves like the actual discrete-time system, which allows for a simple controller analysis and design. The variable structure nature of the inverter with both the RC rectifier and an abruptly changing resistive load with two modes of operation within the sampling period is directly taken into account. Two simulation models, a discrete-time PWM and a continuous-time, of an inverter are presented, which are used to tune the PID controller and to evaluate the control performance. The behavior of the system in both modes is explained on the basis of the root loci and frequency characteristics. The results obtained for three sampling rates: 12.8, 25.6, and 51.2 kHz, are presented and compared with an actual VSI experiment. A comparison with other results obtained for this VSI shows that properly tuned PID control outperforms the more sophisticated solutions based on the coefficient diagram method (CDM) and the passivity based control (PBC).

Keywords: VSI; PID control; PWM; carrier frequency; variable structure; THD; performance evaluation; modeling; simulation

Citation: Blachuta, M.; Bieda, R.; Grygiel, R. Sampling Rate and Performance of DC/AC Inverters with Digital PID Control—A Case Study. *Energies* **2021**, *14*, 5170. https://doi.org/10.3390/en14165170

Academic Editors: Jung-Wook Park and Nicu Bizon

Received: 29 June 2021
Accepted: 17 August 2021
Published: 21 August 2021

1. Introduction

DC/AC inverters, also called voltage source inverters (VSI), are commonly used as a basic component of uninterruptible power supply units (UPS) which provide emergency power to a load when the mains power fails. They convert the DC energy contained in batteries into the appropriate AC voltage. Sinusoidal output of switching power inverters consisting of passive conservative components and semiconductor devices operated as switches is achieved by the pulse-width modulated (PWM) signal.

The performance of the inverter is usually measured as the value of the total harmonic distortion (THD) of the output voltage under the the standard non-linear RC rectifier load. Another measure of performance is the distortion of the output voltage caused by a sudden decrease or increase in the resistive load. We apply both performance indices irrespective of the source of the distortion.

Since the performance of simple inverters without feedback control is usually not satisfactory, a plenitude of control schemes were proposed in the literature. They can be classified into two main categories: single-loop control and multiple input controllers, including multi-loop structures. Multi-loop architectures usually consist of two loops. The external loop is based on a resonant (R), proportional resonant (PR), or repetitive controller (RC), and the inner loop, for the filter capacitor current control, is based on a proportional or more complex controller [1–3]. The outer loop is responsible for reference signal following while the inner loop for fast disturbance attenuation. Even more complicated multi-loop structures with the DC-bus voltage decoupling and load current compensation are presented and discussed in [4]. Another sophisticated solution based on multiple inputs

is the passivity based control (PBC) [5–7] which uses three input variables: the output voltage, and the inductor and output currents [8]. These structures require not only additional sensors and data conditioning channels but also reasonable knowledge of system parameters and involve high computational overheads.

Despite having excellent capability of reference following at constant resistive load, single-loop control based on a resonant (R), proportionally resonant (PR) [9,10], or repetitive controller (RC) [2] have poor disturbance rejection properties [11]. Therefore, single-loop solutions focused on disturbance rejection rather than on the reference following. The latter can be compensated by the appropriate modification of the reference signal. One of the latest approaches belonging to this category is the coefficient diagram method (CDM) which leads to dynamical controllers of higher order [12–14].

It should be noted that the results presented in numerous publications refer to inverters exhibiting diverse values of inductance L and capacitance C that constitute the LC filter, and of the sampling frequency f_s. The voltages and rating powers of the inverters are also different. The sampling frequency varying in various publications between 1.8–20 kHz is treated as imposed and its value remains beyond any discussion. Therefore, a fair comparison of the results of various solutions obtained in these case studies is very difficult if not impossible. There are also papers, e.g., [2,4], that totally neglect digital data processing and treat inverters as continuous-time systems, or, e.g., [3,9], which use sampling rate just for discretization of continuous-time controllers designed neglecting the effect of sampling.

For more overall results, comparisons should be made for inverters with the same parameters. The best way to have some flexibility in parameter choice is the possession of a theoretical model that allows the design to be made, and a simulation model that takes the basic parameters of the PWM system into account to verify the results.

The main novelty of the paper is the disclosure of the huge impact of sampling rate on the performance of the controlled inverter. The article focuses on the results of the proportional-integral-differential (PID) control tuned for the case of RC rectifier load via a method based on both mathematical model and simulation, which is an alternative to the one presented in recent research [14,15]. Contrary to the popular approach to load current as an independent disturbance, our approach is based on the variable structure nature of the inverter where there are two operating modes during the period of the output voltage: load mode and no-load mode.

2. Description of the Test Bed

In order to compare our results with experiments and prior results [14,15], we refer to the setup whose simplified schematic diagram is depicted in Figure 1.

It is assumed that the inverter feeds the load whose model is presented in Figure 2. Due to the EN6240 standard stating that for the UPS below 3 kW the most typical is rectifier load, we pay main attention to non-linear load adopted from reference [14]. The parameters of this load fulfil the requirement that its power factor is about 0.7.

The output voltage is rectified prior to its measurement, with its sign delivered separately to the microprocessor. This increases the analog-to-digital resolution from 12 to 13 bit. A galvanic isolation is provided both in the path of the output voltage measurement system and in the path of discrete control PWM output. The analog isolation amplifier with capacitor coupling that uses signal switching at the frequency of 500 kHz produces a significant high-frequency output ripple with peak-to-peak values of 20 mV. Therefore, an additional low pass filter is used in the measurement path designed according to the guidelines of the Texas Instruments Data Sheet. Its dynamics are much faster than the sampling period and they are neglected when modeling the dynamics of the control loop. The value of the measurement path gain $k_D = [V_{out}]/V_{out}$, where $[V_{out}]$ is the integer output from the ADC, was determined experimentally as $k_D = 110.8\ \mathrm{V}^{-1}$.

It is also assumed that the nominal value of the DC-bus voltage is $V_{DC}^{nom} = 40$ V.

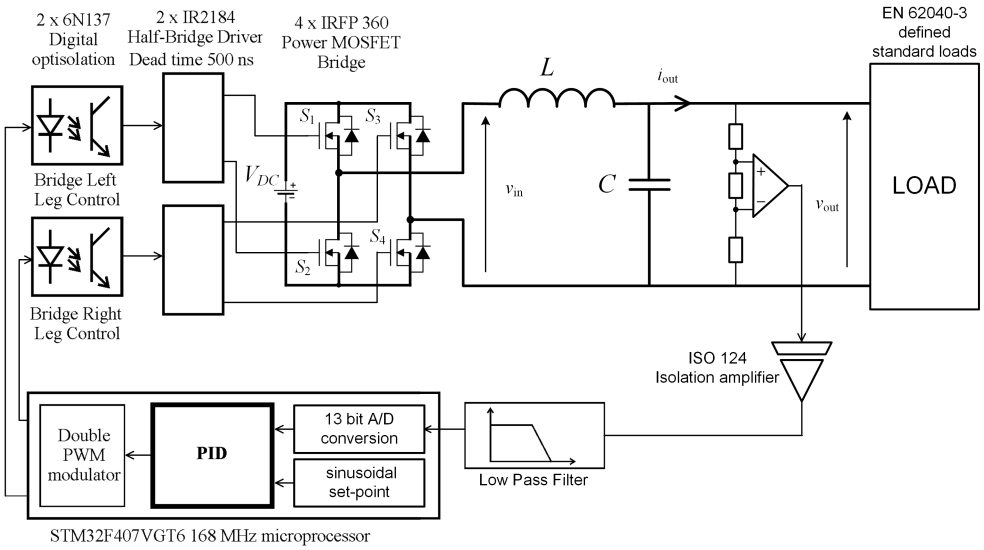
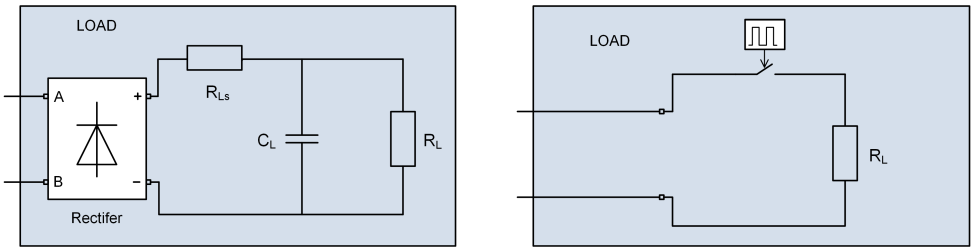


Figure 1. Schematic of the experimental rig. LC filter components: a torroidal core coil with nominal inductance $L_F = 1$ mH made of alloy-powder Super-MSS material and MKP type metallized polypropylene capacitor with nominal capacitance $C_F = 50$ µF. Further details and photo can be found in [14].



(**a**) (**b**)

Figure 2. Models of the loads. (**a**) Non-linear rectifier RC load, $R_{Ls} = 1\ \Omega$, $R_L = 100\ \Omega$, $C_L = 430$ µF (**b**) Periodically switched resistive load, $R_L = 50\ \Omega$.

The control system is based on the STM32F407VGT6 microprocessor with 168 MHz clock. The input frequency of the counters of the PWM modulator equal to 84 MHz. The inverter is designed for the carrier frequency f_s = 25,600 Hz providing 512 switching cycles within the period 20 ms resulting from the output voltage frequency of 50 Hz. As a result, the PWM period h equals to 20 ms/512 $\approx$ 39 µs.

The reference sine wave is constructed from a quarter of the period represented by 128 values, expressed in machine units, and stored in an array. For a sampling rate of 51.2 kHz there are 256 values but for 12.8 kHz the sine wave is represented by only 64 values. It is the largest source of quantization in this system.

The maximum value that can be reached by the comparator within one PWM period is 84,000,000/25,600 = 3281. This means that the maximum value of duty cycle $d = 1$ is reached for the value of control signal $[u] = 3280$ machine units. As a result, the relationship between the duty cycle d and control signal $[u]$ expressed in machine units, or u expressed in volts is determined by

$$d = \text{sat}\{k_M[u]\} = \text{sat}\{k_M k_D u\}, \tag{1}$$

where $k_D = 110.8\ \text{V}^{-1}$, $k_M = 1/3280$. For f_s = 12,800 Hz there is $k_M = 1/6560$, and for f_s = 51,200 Hz, $k_M = 1/1640$. Observe that

$$k_{PWM} = k_M k_D. \tag{2}$$

Then

$$d = \text{sat}\{k_{PWM}u\} \tag{3}$$

and the mean value of the PWM modulated signal on the input to the LC filter is determined by

$$v_{in} = V_{DC}d = V_{DC}\text{sat}\{k_{PWM}u\}. \tag{4}$$

3. Simulation and Controller Tuning

Both the rectifier load and jump-wise switching of the load resistance make the system a variable structure one. Therefore, a part of the system consisting of the LC filter and the load is modeled as an electric circuit, while the rest is modeled using standard SIMULINK blocs. The interface between them is accomplished with `measurement` and `controlled voltage source` blocks.

Although a real controller works on variables expressed in machine units related to the physical ones by the coefficient k_D, we use physical units in simulation models. For the sake of simplicity, in the conceptual phase we neglect signal quantization introduced by the ADC and PWM modulator. There are, however, no obstacles to include quantization at the realization step. It should be noticed that the elements of the electric circuits are just models of the electronic components depicted in Figures 1 and 2. In particular, the equivalent serial resistance R_F characterizes the power losses on switches, e.g., static power losses on the resistances of the switches and the dynamic switching power losses, the power losses on the serial resistances of the filter inductor winding together with the resistances of serial inverter connections and the power losses of the filter core, which are dependent on the material of the filter coil core. This resistance is a non-linear function of the switching frequency and the inductor current. It is not possible to calculate R_F analytically and it should be determined experimentally, e.g., using methods described in [16,17]. Similarly, R_{Ls} in the rectifier load model in Figure 2 is supposed to model a non-linear diode characteristic, which is hardly acceptable for small voltages. For these and another reasons, such as imperfections in the sensor circuits, switching rise and fall times, and discrepancies of transistor and diode characteristics, simulation and experimental results may differ in some detail in the practical implementation.

3.1. Simulation Model of the PWM Modulated Inverter

The organization of the controller is as follows. At the beginning of the PWM pulse, a program interrupt is generated that triggers the sampling of the output voltage, AD conversion, and computation of the control signal $[u(i)]$ stored in the registers of the two PWM comparators to determine the duty ratio $d(i)$ in the next sampling period. This program organization results in a one-step delay in the controller. Therefore, the one step delayed realization of the classical discrete-time PID control law

$$H_c(z) = k_r[1 + \frac{h}{T_i}\frac{1}{1-z^{-1}} + \frac{T_d}{h}(1-z^{-1})] \tag{5}$$

$$= k_c\frac{b_0 + b_1z^{-1} + b_2z^{-2}}{1-z^{-1}} \tag{6}$$

is modeled by the following expressions

$$w(i) = w(i-1) + k_ak_c[b_0e(i) + b_1e(i-1) + b_2e(i-2)], \tag{7}$$

with the control signal

$$u(i) = w(i-1) \tag{8}$$

and the control error

$$e(i) = r(i) - v_{out}(i), \;\; r(i) = V_m\sin(2\pi f \times ih). \tag{9}$$

Here, h is the sampling period, i is the number of sampling instant, f is the AC frequency, $r(i)$ is the sinusoidal set-point, $v_{out}(i)$ is the output voltage, V_m is the amplitude of the reference sinusoid, $e(i)$ is the control error, k_c is the controller gain. The coefficient k_a is an additional controller gain enabling fine tuning, or adaptation to changes of DC-bus voltage V_{DC} as follows

$$k_a = V_{DC}^{nom} / V_{DC}, \tag{10}$$

where V_{DC}^{nom} means the nominal voltage of the DC bus for which the controller is designed, while V_{DC} is its current value. In theoretical considerations it will be $k_a = 1$.

From (1) the relationship between the duty cycle $d(i)$ and the control signal $u(i)$ reads

$$d(i) = \text{sat}\{k_M k_D u(i)\} = \text{sat}\{k_{PWM} u(i)\}. \tag{11}$$

This allows the construction of a simulation model that includes a PWM modulator, an LC filter, and a discrete-time controller, as depicted in Figure 3. The power stage of the inverter consisting of the PWM modulator and inverter bridge is modeled by a custom SIMULINK procedure which enables the choice of the modulation type and quantization or its lack. The coefficients b_0, b_1 and b_2 of (5) are determined from c_1, c_2 and k_c defined in Section 3.2 and obtained by an optimization procedure described in Section 3.3. They are expressed as follows:

$$b_0 = \frac{1}{8}(2 + c_1 h)(2 + c_2 h),\ b_1 = -\frac{1}{8}\left(8 - 2c_1 c_2 h^2\right),\ b_2 = \frac{1}{8}(2 - c_1 h)(2 - c_2 h). \tag{12}$$

Since the controller is designed for nominal conditions then it is assumed that $V_{DC} = V_{DC}^{nom}$, and then $k_a = 1$. If this is not the case then the adaptation coefficent k_a given in Equation (8) should be applied to preserve the optimal controller settings also for V_{DC} changed.

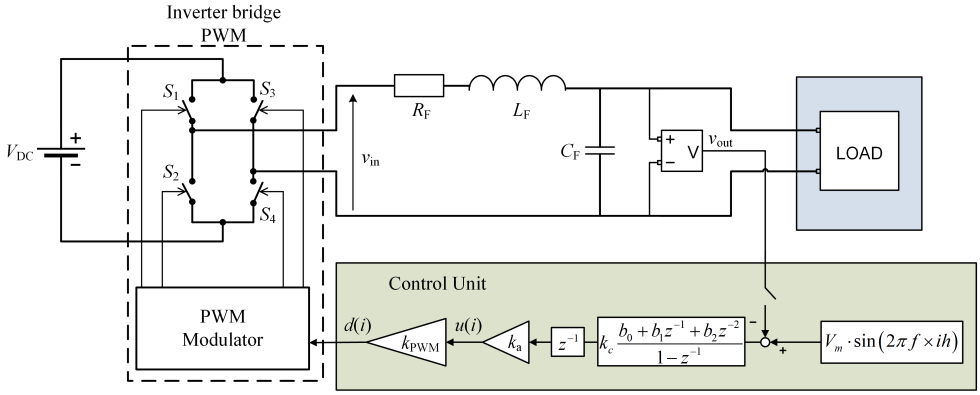


Figure 3. Schematic diagram of a PWM based simulation model of the discrete-time control system.

3.2. Quasi-Continuous-Time Simulation Model

Simulations based on the PWM model are very time-consuming. Therefore, an alternative approach to the PWM controlled system is adopted, which assumes its approximation by a delayed continuous time system whose parameters depend on the sampling period. The QCT approach requires a discrete-time controller to be approximated by a continuous-time one. It has been shown that these approximations give exceptionally exact results compared to those based on the PWM model.

From (4) it follows that the mean value of the input voltage from the PWM modulator can be expressed as $v_{in}(i) = V_{DC} d(i)$. From (11) there is

$$v_{in}(t) = V_{DC} \text{sat}\{k_{PWM} u(t)\}, \tag{13}$$

where $u(t) = u(i)$ for $ih < t \leq (i+1)i$. When using the QCT approach $u(t)$ is treated as a continuous time variable.

The passage of the PWM signal through a dynamical system exhibits a delay of $h/2$. Therefore, assuming that the control path does not saturate, the modulator plus inverter bridge transfer function $K_{PWM}(s)$ can be expressed as

$$K_{PWM}(s) = V_{DC}k_{PWM}\mathrm{e}^{-s\frac{h}{2}} = k_P\mathrm{e}^{-s\frac{h}{2}}, \tag{14}$$

with

$$k_P = V_{DC}k_{PWM} \tag{15}$$

being the gain of the power module. From (5)–(9) the transfer function of the controller plus one step delay caused by information processing is

$$z^{-1}H_c(z^{-1}) = z^{-1}k_c\frac{b_0 + b_1z^{-1} + b_2z^{-2}}{1 - z^{-1}}. \tag{16}$$

Its quasi-continuous-time counterpart bases on the substitution

$$z^{-1} = \frac{\frac{2}{h} - s}{\frac{2}{h} + s} = \frac{1 - s\frac{h}{2}}{1 + s\frac{h}{2}} \approx \mathrm{e}^{-sh} \tag{17}$$

leading to a function

$$k_c\frac{(s + c_1)(s + c_2)}{s(s + \frac{2}{h})}\mathrm{e}^{-sh}. \tag{18}$$

Absorption of the transfer function of the power module in (14) finally gives

$$k_Pk_c\frac{(s + c_1)(s + c_2)}{s(s + \frac{2}{h})}\mathrm{e}^{-s\frac{3}{2}h}. \tag{19}$$

The resulting simulation model is displayed in Figure 4.

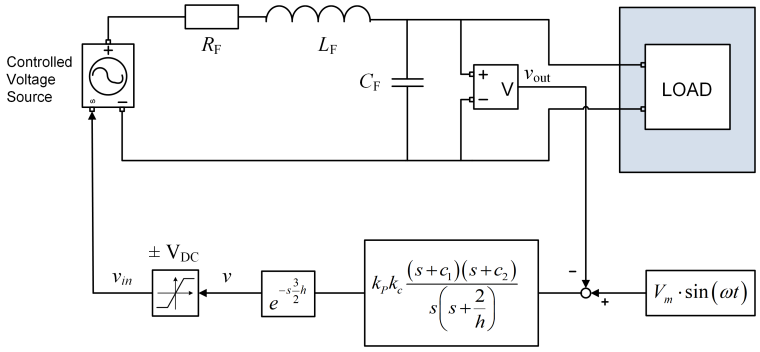


Figure 4. Schematic diagram of the QCT based simulation model of the control system $v_{in} = V_{CD}\mathrm{sat}\{v/V_{CD}\}$.

3.3. Controller Tuning for Non-Linear RC Load

The LC filter with the transfer function $K(s)$ determined in (33), which can also be written as

$$K(s) = \frac{s_1s_2}{(s + s_1)(s + s_2)},\ s_{1,2} = \sigma(1 \pm j\theta) \tag{20}$$

plays the role of the plant to be controlled, whose output is supposed to follow the reference sinusoid $V_m \sin \omega t$ in spite of the variable load. Since $v_{out}(t)$ is an unbiased periodic function then it can be presented as

$$v_{out}(t) = \sum_{k=1}^{\infty} A_k \sin(k\omega t + \varphi_k). \tag{21}$$

Denoting the distortion function $\psi(t)$ as

$$\psi(t) = \frac{v_{out}(t) - A_1 \sin(\omega t + \varphi_1)}{A_1} = \frac{1}{A_1} \sum_{k=2}^{\infty} A_k \sin(k\omega t + \varphi_k), \tag{22}$$

the quality of the produced output voltage can be expressed by the value of THD_H defined as

$$\mathrm{THD}_H = \frac{1}{A_1} \sqrt{\sum_{k=2}^{H} A_k^2} \tag{23}$$

for H high enough.

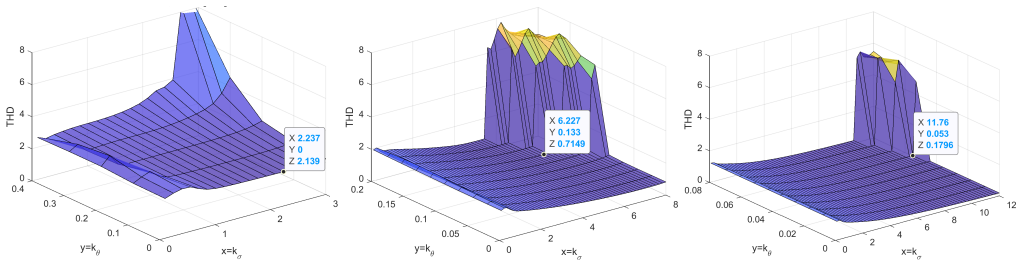
In order to choose the best controller parameters for the case of rectifier load, the values of THD were computed based on simulated outputs. Since simulations based on the PWM model are time consuming they were replaced by faster simulations based on the QCT model. The QCT counterpart of $H_c(z)$ determined in (5) is

$$K_c(s) = k_c \frac{(s + c_1)(s + c_2)}{s(s + \frac{2}{h})}. \tag{24}$$

The parameters $c_{1,2}$ of the controller were assumed complex, such that

$$c_{1,2} = k_\sigma \times \sigma(1 \pm k_\theta \times j\theta). \tag{25}$$

The THD values are calculated on a dense mesh of values of both variables k_σ and k_θ, with the loop gain $k = k_p k_c$ selected so that the gain margin ΔA of the no-load system has some assumed value. The choice of k is performed based on the Nyquist plot using the MATLAB function `margin`. This ensures stability of the systems taken into account when computing THD on the mesh of remaining controller parameters. The resulting values of THD as functions of variables k_σ and k_θ computed for selected k are shown in Figure 5 for three values of f_s, from which a pair (k_σ^0, k_θ^0) ensuring minimum value of THD is chosen.

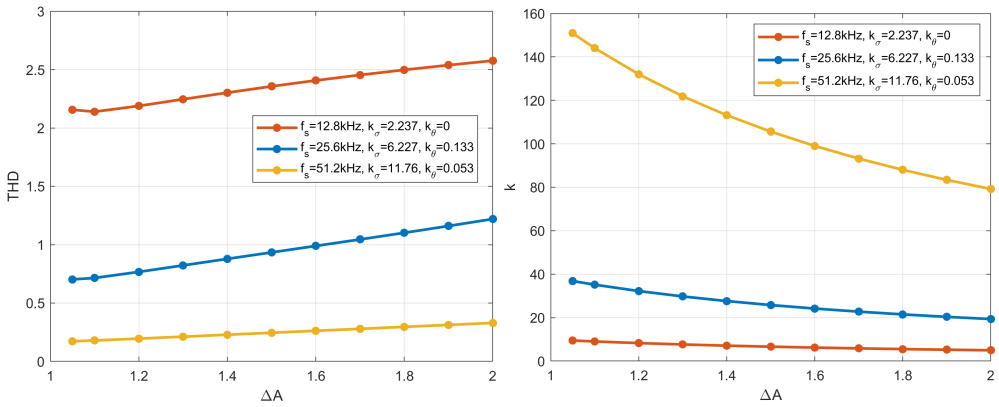


(**a**) (**b**) (**c**)

Figure 5. Surfaces of THD values as functions of k_θ and k_σ for three sampling rates: (**a**) $f_s = 12.8$ kHz, (**b**) $f_s = 25.6$ kHz and (**c**) $f_s = 51.2$ kHz. The optimum values (k_σ^0, k_θ^0) are denoted by dots.

Finally, based on $c_{1,2}$ calculated from (25), the values b_0, b_1 and b_2 of the discrete-time controller $H_c(z)$ of (6) can be found from the formulas in (12). The gain k_c is calculated from $k_c = k/k_p$.

The resulting values of THD and k as functions of ΔA are depicted in Figure 6.



(**a**) (**b**)

Figure 6. Dependence of (**a**) THD and (**b**) loop gain k from the gain margin ΔA for various sampling frequencies f_s. High frequencies f_s enable big values of k leading to small values of THD.

One should notice that very small values of the gain margin $\Delta A \simeq 1.1$ that give minimum value of THD would not be acceptable for an ordinary control system. However in the VSI the loss of stability can only result from the change of the DC bus voltage V_{DC}. The variability of V_{DC} can be compensated by an additional gain $k_a = V_{DC}^{nom}/V_{DC}$ in the controller realization defined in Equations (7)–(9). Otherwise, when the variability of V_{DC} is small and we do not wish to adapt to its changes, a greater gain margin can be chosen by selecting the gain $k_a < 1$.

In Figure 7, the output signal $v_{out}(t)$ along with load current are displayed for three sampling frequencies and the optimally tuned PID controllers under assumption of the gain margin $\Delta A = 1.1$ More detailed information can be obtained from Figure 8 where the distortion function $\psi(t)$ defined in (22) and THD defined in (23) obtained from both the PWM and QCT models are shown for the uncontrolled and optimally controlled inverter at three sampling rates. The excellent match of the results of both models is noticeable. The control signal $u(t)$ along with a function $\chi(t)$ determining the deviation of $u(t)$ from a no-load sine wave, defined as

$$\chi(t) = \frac{u(t) - B_1 \sin(\omega t + \phi_1)}{B_1}, \tag{26}$$

where B_1 is the amplitude of the first harmonic of $u(t)$, is presented in Figure 9. The PWM simulation model reveals some asymmetric "ringing" of the controller with average values represented by the results of the QCT simulation model. Dependence of the THD and the loop gain k on the assumed value of the gain margin ΔA is presented in Figure 6. From Figure 10, it can be seen that close to the stability border obtained from the QCT model, and outside of it, the QCT model gives results different than the PWM one returning perfectly stable results. This means that the results presented in Figure 6 are conservative, and the controllers can be experimentally fine tuned in the real inverter by increasing the value of k_a in (7). Certain measures of control performance, i.e., amplitude A_1 of the first harmonic, THD, and minimum and maximum value of distortion of actual output from the first harmonic are collected in Table 1. Except for $f_s = 12.8$ kHz, almost ideal A_1 stabilization is to be noticed due to the presence of integration in the controller transfer function.

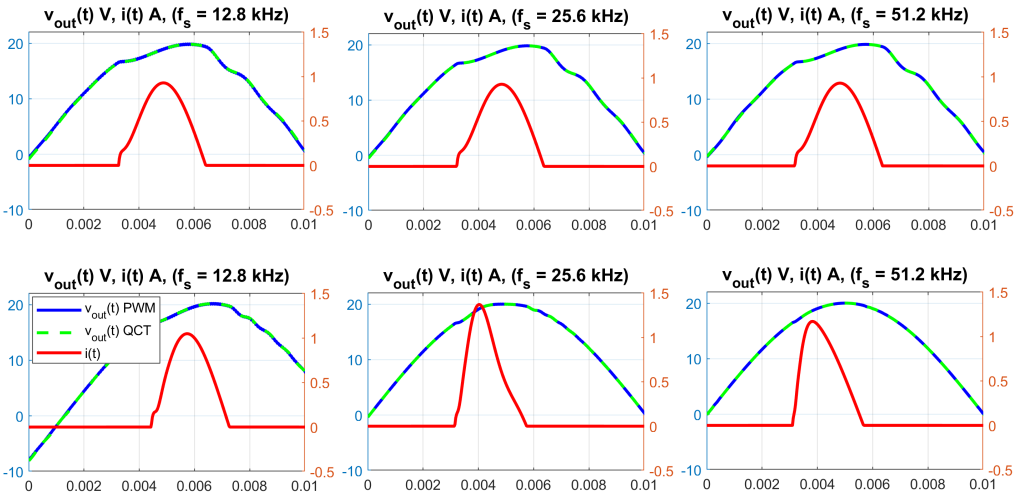


Figure 7. Output voltages $v_{out}(t)$ and load currents $i(t)$ under rectifier load for three sampling rates. Top row: uncontrolled system; bottom row: optimally tuned PID controlled systems with $\Delta A = 1.1$. Blue lines: output from PWM simulation, green lines: output from QCT simulation.

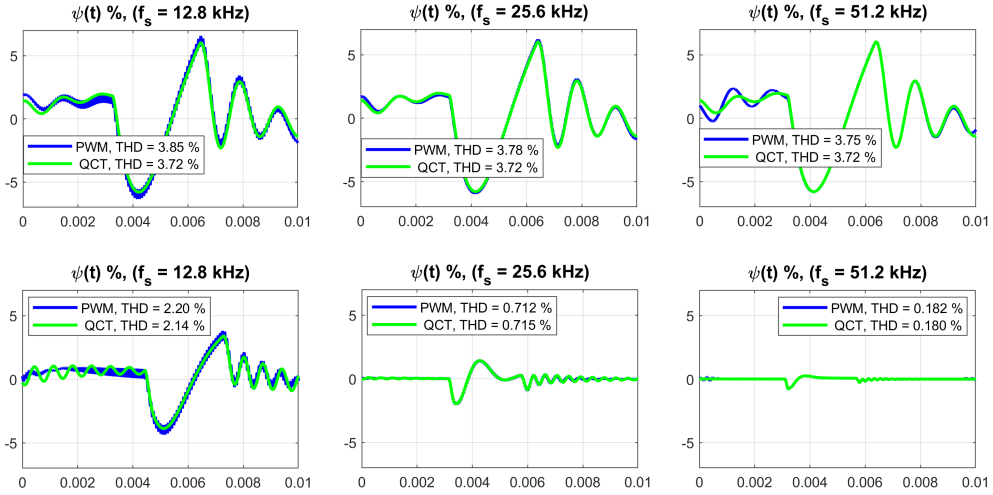


Figure 8. The distortion function ψ and THD values obtained from QCT and PWM simulation models. Top row: uncontrolled system, bottom row: PID controlled system. Green lines: QCT simulation, blue lines: PWM simulation.

Table 1. Amplitude A_1, THD, and the extremum values of the distortion function $\psi(t)$.

f_s (kHz)	A_1 (V)	THD (%)	ψ_{min} (%)	ψ_{max} (%)
Open Loop				
25.6	19.6964	3.78	−5.986	6.212
Closed Loop				
12.8	19.921	2.20	−4.366	3.794
25.6	20.002	0.712	−2.060	1.496
51.2	20.005	0.182	−0.790	0.268

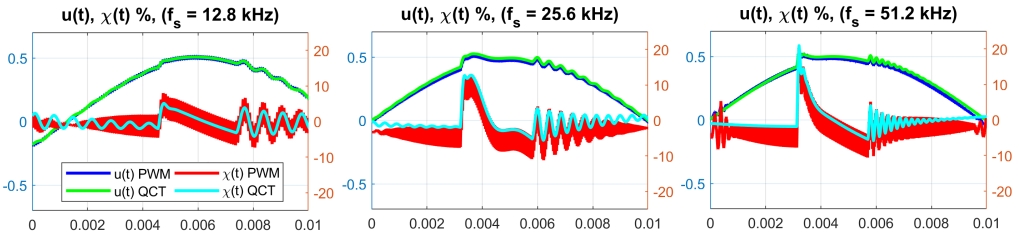


Figure 9. Control signal $u(t)$ and deviation function $\chi(t)$ obtained from the QCT simulation and PWM simulation.

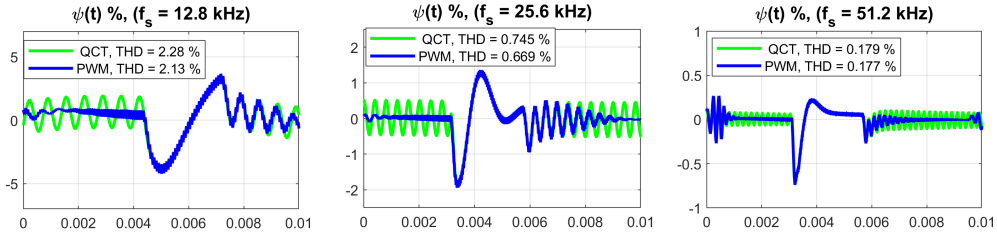


Figure 10. Distortion function $\psi(t)$ on the QCT stability boarder $\Delta A = 1.0$ vs $\psi(t)$ delivered by the PWM simulation model. The PWM system remains stable—the QCT stability criterion is conservative.

4. Theoretical Analysis of the Control System

The aim of this section is to explain the phenomena observed during simulation and to discuss, based on the analysis of closed-loop characteristics, the influence of delays caused by digital data processing. This is performed using the QCT approach.

An important feature of the inverter with the rectifier RC load is that it has a variable structure depending on the current state of the Graetz rectifier bridge. Two periods can be distinguished: the no-load idle period when the diodes of the Graetz bridge do not conduct and the load period when the diodes do conduct and current is drawn from the inverter. Therefore, unlike virtually every bibliography source where the load current is treated as an independent variable, we analyze the system as a variable structure one.

4.1. QCT Controller Model

For the convenience of analytic considerations, the controller model should be described by a rational transfer function We assume that the controller does not saturate during VSI operation and that the QCT model of the power module given in (13)–(15) is absorbed by the equation of the QCT controller.

$$C(s) = k_P k_c \frac{(s+c_1)(s+c_2)}{s(s+\frac{2}{h})} \times \frac{1-s\frac{h}{2}}{1+s\frac{h}{2}} \times (1-s\frac{h}{2}) \tag{27}$$

$$= k\frac{(s+c_1)(s+c_2)}{\frac{2}{h}s} \times \frac{(1-s\frac{h}{2})^2}{(1+s\frac{h}{2})^2} \tag{28}$$

with $k = k_P k_c$ being the loop gain. Equation (27) can be reordered as follows:

$$C(s) = C^*(s) \times \left(\frac{1-s\frac{h}{2}}{1+s\frac{h}{2}}\right)^2 \tag{29}$$

with an ideal no-delay continuous-time PID

$$C^*(s) = k\frac{h}{2}\frac{(s+c_1)(s+c_2)}{s}. \tag{30}$$

4.2. Open Loop System

The dynamics of the inverter can be represented by transfer functions related to particular modes of operation. Let $Z_L(s)$ denote the impedance of the load in each of them. Then the LC filter has the transfer function:

$$K(s) = \frac{1}{L_F C_F s^2 + [\frac{L_F}{Z_L(s)} + R_F C_F]s + 1 + \frac{R_F}{Z_L(s)}} \tag{31}$$

In the no-load mode there is $Z_L(s) = \infty$. In the resistive load mode $Z_L(s) = R_L$, while in the non-linear RC mode

$$Z_L(s) = \frac{R_{Ls} + R_L + R_{Ls} R_L C_L s}{1 + R_L C_L s} \tag{32}$$

As a result, for the idle period there is

$$K(s) = \frac{1}{L_F C_F s^2 + R_F C_F s + 1} \tag{33}$$

for the resistive load

$$K(s) = \frac{1}{L_F C_F s^2 + [\frac{L_F}{R_L} + R_F C_F]s + 1 + \frac{R_F}{R_L}} \tag{34}$$

and for the conducting rectifier mode

$$K(s) = \frac{b_1 s + b_0}{a_3 s^3 + a_2 s^2 + a_1 s + a_0} \tag{35}$$

with $a_3 = R_{Ls} R_L C_L L_F C_F$, $a_2 = R_{Ls} C_F (L_F + R_F R_L C_L) + R_L L_F (C_F + C_L)$, $a_1 = R_{Ls}(R_F C_F + R_L C_L) + R_L R_F (C_F + C_L) + L_F$, $a_0 = R_{Ls} + R_L + R_F$, $b_1 = R_{Ls} R_L C_L$, $b_0 = R_{Ls} + R_L$. The characteristics of these transfer functions are presented in Figure 11.

4.3. Closed Loop System

For the analysis of control systems with controllers optimized in the previous section for the non-linear LC load, four types of their characteristics are applied: root loci, Nyquist plots, Bode diagrams, sensitivity $S(j\omega)$, and complementary sensitivity $T(j\omega)$ functions. These characteristics are considered for both modes: the load mode and the no-load one. It is clear from the performed simulations that the no-load period is characterized by weakly damped high-frequency oscillations, which are prone to instability. The transients in the load period are much less oscillatory.

In this section, the properties of both modes will be examined separately, as if the system was running in one of them all the time.

4.3.1. No-Load Mode

This mode is particularly sensitive to system delays and, as such it limits the values of controller gains that determine the control quality. In Figure 12, root loci of the no-load system $C(s)K(s)$ with controllers tuned in the previous section are plotted at three different sampling frequencies. The circles on the positive axis represent pairs of zeros at $2/h$ introduced due to sampling. They attract loci as the controller gain increases. Circles in the left hand plane denote controller zeros, while crosses denote the open loop poles: the one in the origin is due to controller integration part, the complex conjugate pair is due to LC filter poles.There are also crosses on the left real axis at $-2/h$ denoting double poles due to sampling. The resulting closed-loop poles are denoted by stars. It is clear that except for $f_s = 12.8$ kHz the complex pair with relatively high imaginary part dominates over the remaining real roots. This pair is responsible for fast oscillations observed in Figures 8–10.

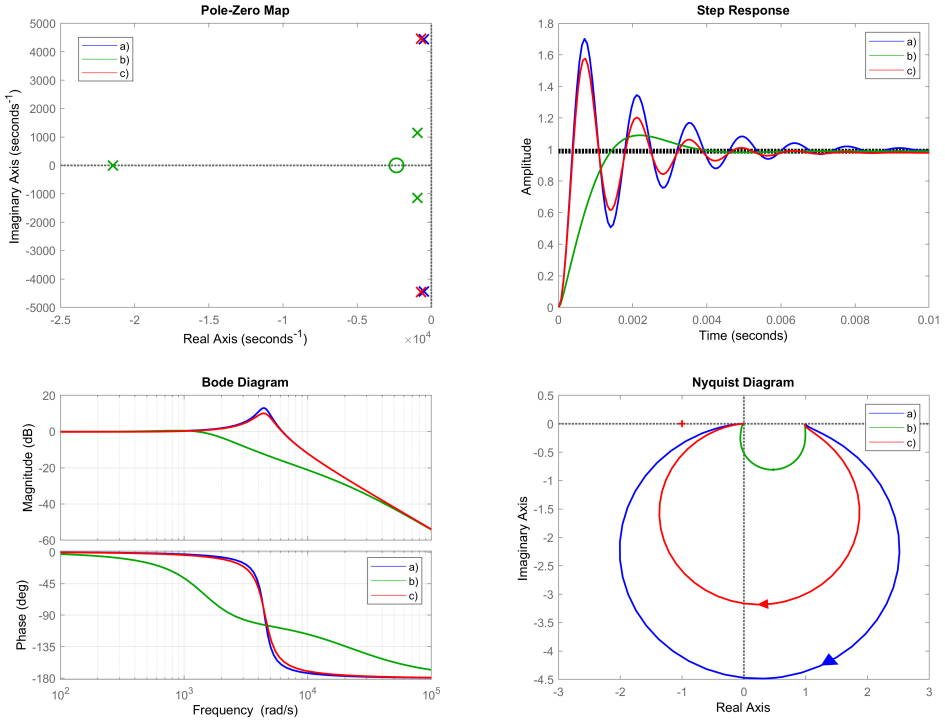
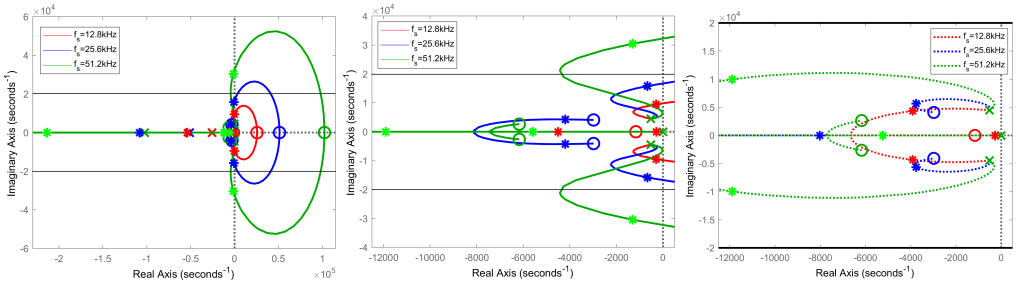


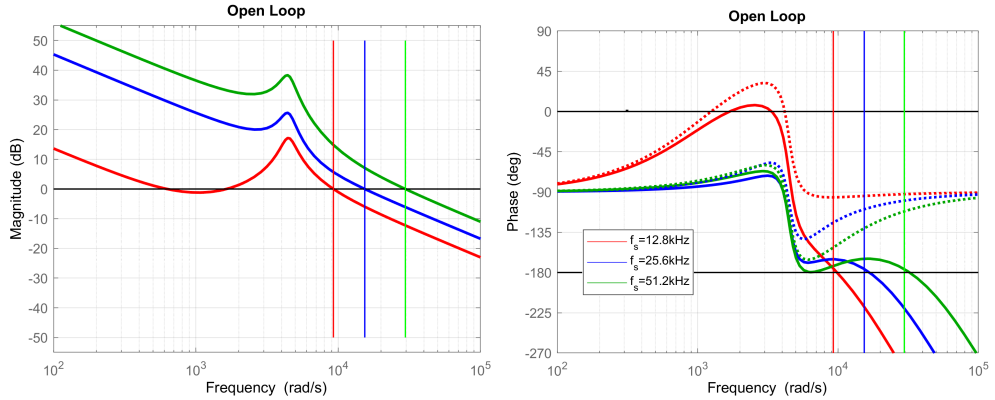
Figure 11. Poles and zero, step responses, Bode and Nyquist plots of the open loop system in two modes. (a) no-load, (b) RC load, (c) resistive load $R_L = 50\ \Omega$. Notice small differences between characteristics of the no-load and the resistive load system, and a large discrepancy between the no-load and RC load system.



(**a**) (**b**) (**c**)

Figure 12. Root loci for the no-load system. Crosses—open loop poles, circles—zeros, dots—closed loop poles under assumption $\Delta A = 1.1$. The gains are as follows: $f_s = 12.8$ kHz: $k = 9$, $f_s = 25.6$ kHz: $k = 35$; $f_s = 51.2$ kHz: $k = 144$ (**a**) general view (**b**) dominant poles (zoom), (**c**) system with no-delay controller $C^*(s)$ (zoom). Notice a large impact of delays on the position of roots.

Bode diagrams of the no-load systems are depicted in Figure 13. The left plot displays magnitudes while the right phases. Dotted lines denote the phase characteristics for a hypothetical system without any delays, i.e., for hypothetical controller $C^*(s)$. It is clearly seen that the phase characteristics for the actual controller $C(s)$ with a double phase shifting element strongly deviate from the no-delay ones. The vertical lines mark the frequencies where $|C(j\omega)K(j\omega)| = 1$. It is interesting to notice that the optimal values of controller phases are then close to 0, and after that they become negative. The resulting open loop phases are -180 deg + $\Delta\phi$, where the phase margin $\Delta\phi$ is a small positive number. Another representation of frequency response characteristics are the Nyquist plots presented in Figure 14. They provide more insight into the phase and gain margin. In particular, for the gain margin $\Delta A = 1.1$ the phase margin is around 4 deg for the actual system and around 80 deg for the hypothetical no-delay one.



(**a**) (**b**)

Figure 13. Bode plots (**a**) magnitudes for the LC filter with PID controllers, (**b**) phases of the LC filter with PID controllers. Solid lines are for $C(s)$, dotted lines—for $C^*(s)$, Vertical lines mark the frequencies, such that $|C(j\omega)K(j\omega)| = 1$. It is seen that there is only a small phase margin $\Delta\phi$ at these frequencies, and a quite large for the fictitious system $C^*(s)K(s)$ without any delays caused by discrete-time data processing.

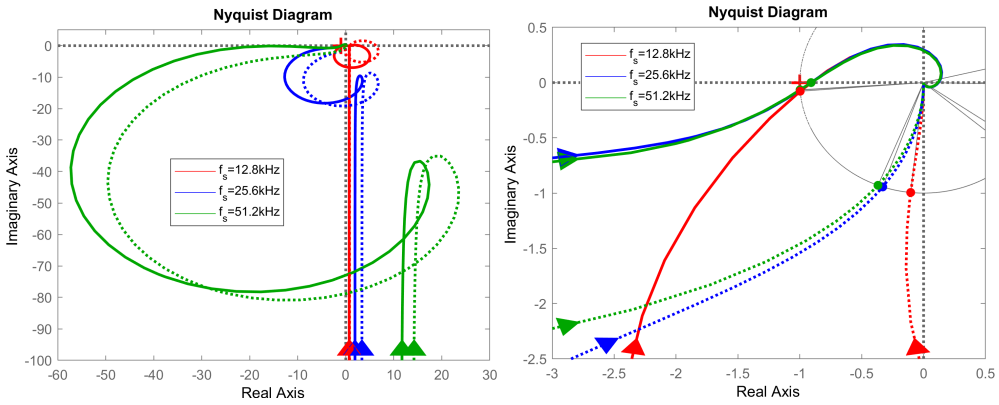


Figure 14. Solid lines: Nyquist plots for the systems depicted in Figure 13 with $\Delta A = 1.1$: $f_s = 12.8$ kHz: $k = 9$, $\Delta\phi = 4.48$ deg, $f_1 = 1473$ Hz, $f_\pi = 1566$ Hz; $f_s = 25.6$ kHz: $k = 35$, $\Delta\phi = 3.86$ deg, $f_1 = 2447$ Hz, $f_\pi = 2665$ Hz; $f_s = 51.2$ kHz: $k = 144$, $\Delta\phi = 3.75$ deg, $f_1 = 4721$ Hz, $f_\pi = 5142$ Hz; Dotted lines: for the system with the hypothetical no-delay controller $C^*(s)$: $f_s = 12.8$ kHz: $\Delta\phi = 84$ deg, $f_s = 25.6$ kHz: $\Delta\phi = 70.7$ deg, $f_s = 51.2$ kHz: $\Delta\phi = 68.4$ deg.

Finally, the closed loop characteristics given by the sensitivity $S(\omega)$ and complementary sensitivity $T(\omega)$ functions, where

$$S(\omega) = \left|\frac{1}{1+C(s)K(s)}\right|_{s=j\omega}, \quad T(\omega) = \left|\frac{C(s)K(s)}{1+C(s)K(s)}\right|_{s=j\omega} \tag{36}$$

are presented in Figure 15. As a result of small values of ΔA and $\Delta\phi$ both $S(\omega)$ and $T(\omega)$ feature high resonant peaks. The hypothetical systems with no-delay controllers do not have such extrema.

Characteristic frequencies and closed-loop roots determining the properties of the system in the no-load mode are collected in Table 2, where σ_0, ϕ_0 and θ characterize a pair of complex roots as follows

$$s_{1,2} = -\sigma_0 \pm j\omega_0 = -\sigma_0(1 \pm j\theta), \text{ where } \theta = \frac{\omega_0}{\sigma_0}, \text{ and } \omega_0 = 2\pi f_0. \tag{37}$$

Close proximity of f_0 to the resonance frequency f_r, and sandwiching of f_r between f_1 and f_π is to be noticed. High values of the degree of oscillability θ indicate large numbers of

slowly decreasing oscillations. High values of the degree of stability σ_0 indicates relatively fast extinguishing of their envelope.

Table 2. Characteristic frequencies and closed-loop roots in the no-load mode.

f_s (kHz)	f_1 (Hz)	f_r (Hz)	f_0 (Hz)	f_π (Hz)	$-\sigma_0 \pm j\omega_0$	θ
12.8	1473	1508	1509	1566	$-289 \pm j9480$	33
25.6	2447	2514	2516	2665	$-664 \pm j1581$	24
51.2	4721	4842	4847	5141	$-1296 \pm j30{,}453$	23

It should be noticed that, due to high values of θ, neither the very small values of the gain margin ΔA and phase margin $\Delta\phi$ nor high peaks in the closed-loop frequency characteristics of Figure 15 would be accepted in an ordinary control system. However, it is no problem for the VSI since the frequency of the reference signal is several orders of magnitude lower than the resonance frequencies of the closed loop system so that the reference itself does not trigger fast oscillations. They are, however, triggered by initial conditions resulting from the previous load period.

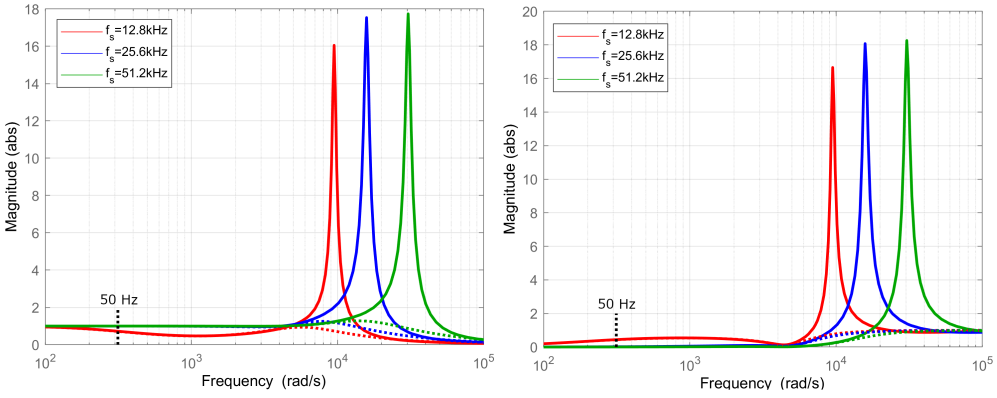


Figure 15. (**a**) Complementary sensitivity $T(\omega)$ and (**b**) sensitivity $S(\omega)$ of the closed-loop no-load systems; $f_s = 12.8$ kHz: $f_r = 1508$ Hz; $f_s = 25.6$ kHz: $f_r = 2514$ Hz; $f_s = 51.2$ kHz: $f_r = 4842$ Hz.

Unfortunately, the optimal gain for the case $f_s = 12.8$ kHz is so small that the root -286 on the real axis does not sufficiently depart from the origin on the s-plane so that it can affect the transients to the same extent as a pair $-289 \pm j9480$ closest to the imaginary axis. As a result the output signal is not able to follow the reference properly, which can be seen from Figure 15, where $f = 50$ Hz is marked. Moreover from Figures 7 and 8 the optimal control is quite poor and the values of THD do not differ greatly from those of the uncontrolled system. In Figures 13–19, it is seen that the case $f_s = 12.8$ kHz deviates greatly from those for $f_s = 25.6$ kHz and $f_s = 51.2$ kHz. One can conclude that $f_s = 12.8$ kHz is too small a frequency for the system considered.

It is interesting to compare the roots of a hypothetical no-delay system with the controller $C^*(s)$ whose root loci close to imaginary axis are plotted in Figure 12b with the actual ones plotted in Figure 12c. For the ascending order of f_s they are as follows -286, $-289 \pm j9480$; (-278), $-664 \pm j15,808$; $(-3764 \pm j5657)$ and $-1296 \pm j30,453$; (-5230), where the numbers in parentheses are for no-delay system. Except for $f_s = 12.8$ kHz the remaining roots have larger values of σ and much smaller of θ. As a result, the transients are much less oscillatory and fade away faster. A comparison of the results obtained by a hypothetical no-delay controllers $C^*(s)$ and the actual ones are presented in Figure 16. It is clear that the quality of the disturbance suppression depends mainly on the controller gain, the value of which is limited due to oscillations resulting from the delays in the loop.

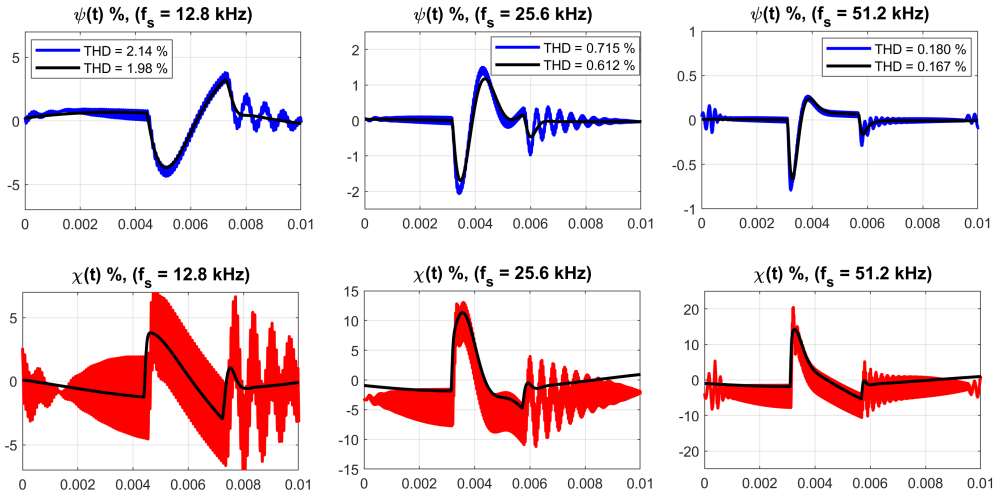
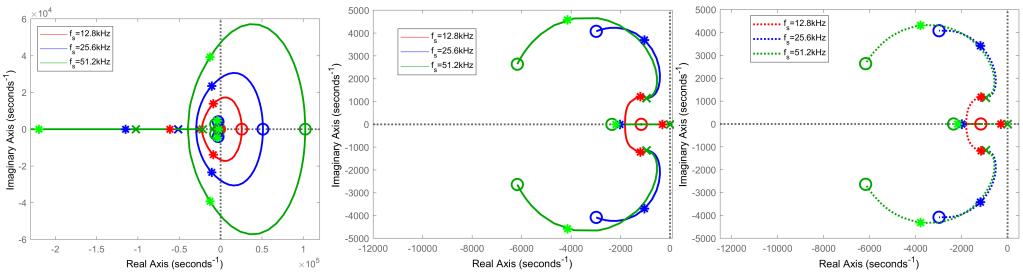


Figure 16. Effect of sampling on control performance. The black lines represent responses with the fictitious controller $C^*(s)$ without any delay, and colored lines with the real controller $C(s)$ optimized for THD. The higher the gain the lower the values of $\psi(t)$ during the load period constituting the main contribution to THD. However, the still possible gain increase is restricted by oscillations of $\psi(t)$ due to data processing delay important in the no-load period.

4.3.2. Load Mode

Current draining from the VSI in the load period is the fundamental cause of the distortion of the output voltage V_{out}. Once finished, it triggers oscillations in the no-load period. Root loci, Bode diagrams, and Nyquist plots for $C(j\omega)K(j\omega)$ in the load period are displayed in Figures 17 and 18 for three sampling frequencies. Root loci show that there are two groups of oscillatory roots—the faster and the slower ones collected in Table 2. From Figure 17 and Table 2 it is clear that the influence of delays on the roots closes to the imaginary axis in the no-load mode is much smaller than in the load mode. The character of responses depends on the slow roots whose imaginary parts, depending of f_s in increasing order, equal to 193 Hz, 589 Hz, and 1200 Hz. They are marked on Figure 19, along with frequencies 2214, 3743, 6235 Hz of faster roots to show how they reflect in the extrema of $S(\omega)$ and $T(\omega)$. The case $f_s = 12.8$ kHz differs from the remaining ones through the relatively slow real root -305. This root is responsible for the qualitative deviation of both frequency response and time response characteristics of the system at $f_s = 12.8$ kHz. In particular, from Figure 18, it is clear that the control system is not able to follow the 50 Hz sinusoid exactly enough. When comparing the remaining no-load mode roots with the load mode ones, the latter have much greater σ values and much lower θ values. This means that the transients in the load mode are much less oscillatory and vanish faster. High values of both stability margins, i.e., gain margin, ΔA, and phase margin, $\Delta\phi$ seen in Figure 18 and meagre extrema seen in Figure 19 confirm this in the frequency domain. As a result, sampling has a negligible effect on transients in this mode. This is clearly seen from Figure 16 where the no-delay responses and the delay ones practically overlap and explained by Table 3 showing very low influence of f_s on the slow roots.



(**a**) (**b**) (**c**)

Figure 17. Root loci for the load mode. (**a**) general view, (**b**) dominating poles with $C(s)$ (zoom), (**c**) dominating poles with no-delay $C^*(s)$ (zoom). Crosses—open loop poles, circles—zeros, dots—closed loop poles. Controller optimized under assumption of $\Delta A = 1.1$ for the no-load mode. Note that, unlike the other roots, the roots for $f_s = 12.8$ kHz do not depart significantly from the open loop poles. As a result, the real root close to zero dominates the closed-loop dynamics Note the weak effect of delays on the poles positions.

Table 3. Roots in the load mode First row: with $C(s)$, second row with $C^*(s)$.

f_s (kHz)	Fast Roots			Slow Roots		
	$-\sigma \pm j\omega$	θ	f_0 (Hz)	$-\sigma$, $-\sigma \pm j\omega$	θ	f_0 (Hz)
12.8	$-8791 \pm j13{,}909$	1.58	2214	-305, $-1194 \pm j1216$	1	193
	$-27{,}803$	0	0	-296, $-1154 \pm j1180$	1.02	188
25.6	$-10{,}660 \pm j23{,}519$	2.21	3743	$-1029 \pm j3696$	3.59	588
	$-33{,}511$	0	0	$-1180 \pm j3417$	2.9	544
51.2	$-12{,}879 \pm j39{,}175$	3.04	6235	$-4143 \pm$ j4575	1.1	728
	$-41{,}600$	0	0	$-3780 \pm j4307$	1.14	686

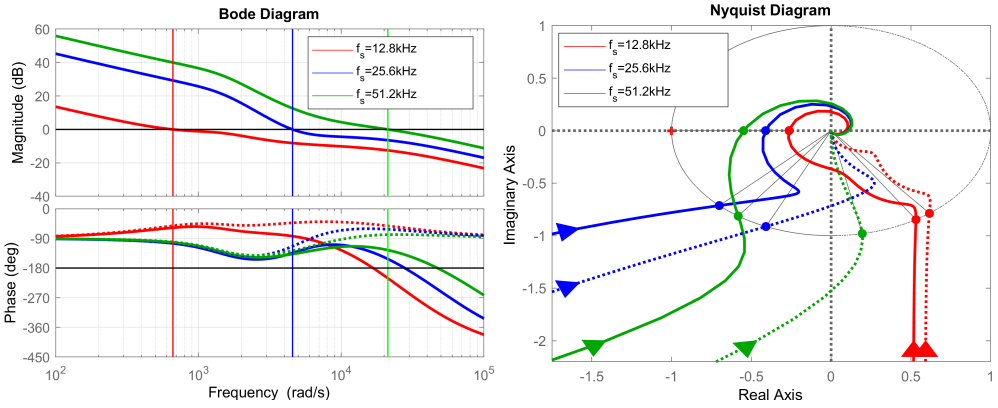


Figure 18. Bode and Nyquist plots for the load mode. Large stability margins ΔA and $\Delta\phi$ are to be noticed. $f_s = 12.8$ kHz: $\Delta\phi = 122$ deg, $f_1 = 106$ Hz, $\Delta A = 3.79$, $f_\pi = 2658$ Hz; $f_s = 25.6$ kHz: $\Delta\phi = 45$ deg, $f_1 = 727$ Hz, $\Delta A = 2.44$, $f_\pi = 4440$ Hz; $f_s = 51.2$ kHz: $\Delta\phi = 54$ deg, $f_1 = 3379$ Hz, $\Delta A = 1.82$, $f_\pi = 7512$ Hz.

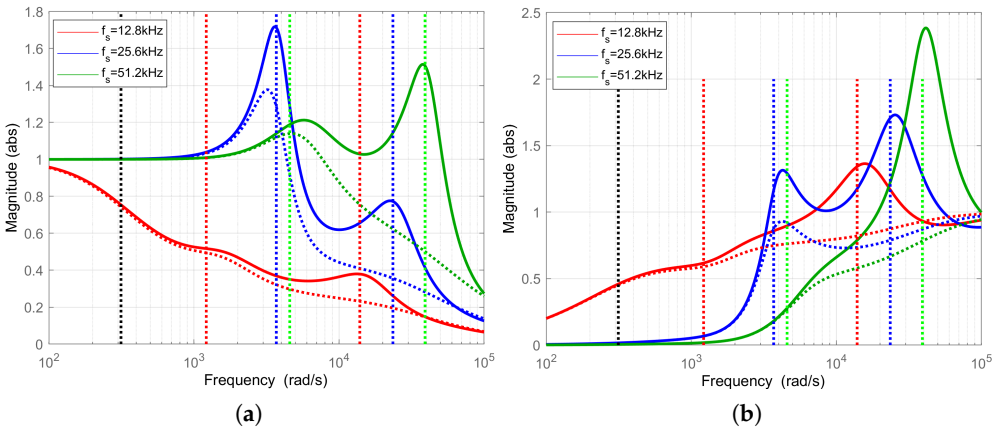


Figure 19. (**a**) Complementary sensitivity $T(\omega)$ and (**b**) $S(\omega)$ of the closed-loop for the load mode.

5. Remarks on Abruptly Changing Resistive Load

If the controller settings are optimized for the RC rectifier load they can be far from the optimum for another loads. Application of the controllers obtained in previous sections to the resistive load of Figure 2 give results presented in Figures 20–22 with the results summarized in Table 4. The controller can be tuned to provide the smallest value of THD (or of max $\psi(t)$ also for this type of load using our optimization methodology. Then, in turn, the settings will not be optimal for RC rectifier load. It is also possible to formulate a weighted performance index to find a compromise solution.

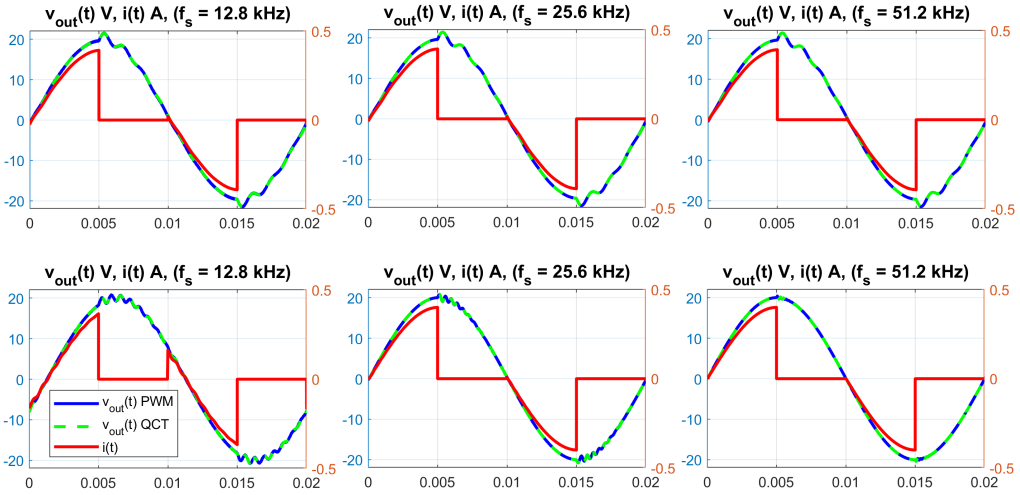


Figure 20. Output voltages $v_{out}(t)$ and load currents $i(t)$ under abruptly changing resistive load for three sampling rates. Top row: uncontrolled system; bottom row: PID control tuned to the rectifier load with $\Delta A = 1.1$ Blue lines: PWM simulation, Green lines: QCT simulation.

Table 4. Amplitude A_1, THD, and the extreme values of distortion $\psi(t)$ for the abruptly changing resistive load.

f_s (kHz)	A_1 (V)	THD (%)	ψ_{min} (%)	ψ_{max} (%)
		Open Loop		
25.6	19.8883	3.02	−4.6683	8.1171
		Closed Loop		
12.8	19.991	2.32	−4.2378	6.0307
25.6	20.002	1.39	−4.3515	4.0724
51.2	20.005	0.321	−1.5179	1.9826

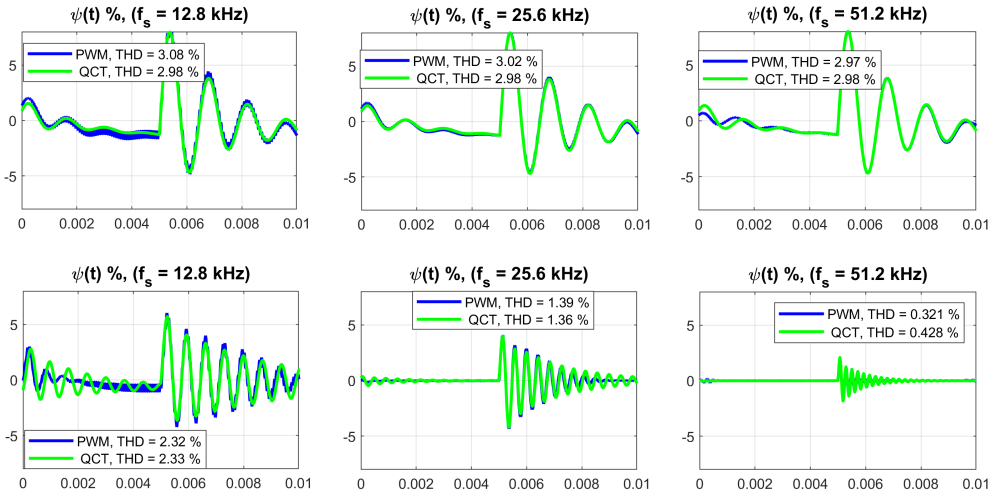


Figure 21. Values of the $\psi(t)$ and THD functions obtained from QCT and PWM simulation models. Upper row: uncontrolled system, lower row: PID controlled system. Green lines: QCT simulation, blue lines: PWM simulation.

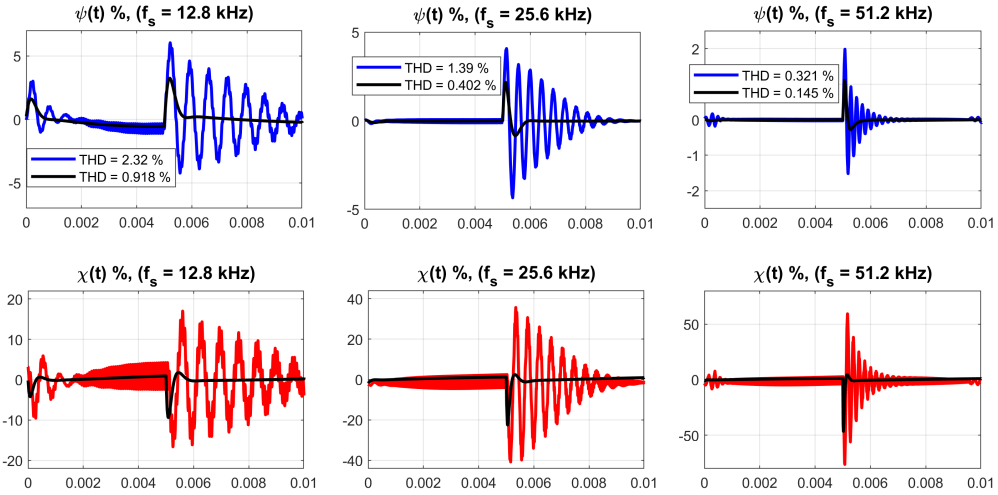


Figure 22. Effect of sampling on control performance. The black lines represent responses with the fictitious no-delay controller $C^*(s)$, and the colored lines with the real controller $C(s)$. The higher the gain the lower the values of $\psi(t)$ during the no-load period with with the fictitious no-delay controller $C^*(s)$.

6. Remarks on Raising the Sampling Rate

Figures 16 and 22 show how destructive the data processing delays are for the control performance.

From the frequency plots in Figures 13 and 14 it can be seen that the no-load system with the no-delay controller $C^*(s)$ is stable for all positive gains. Similar conclusion apply to the load system whose frequency plots are depicted in Figures 18 and 19. This is reinforced by root loci for systems with relative order equal to 1, which both no-load and load systems belong to. They have the property that branches starting at $k = 0$ in open system poles tend to zeros as $k \to \infty$ except for one branch travelling along real axis to $-\infty$. As a result, increasing the sampling rate to infinity, $f_s \to \infty$, would result in possibility of raising the controller gain to infinity, $k_c \to \infty$ making the discrepancy function $\psi(t) \to 0$ and THD$\to 0$.

Therefore, the pursuit of extremely good control suggests the use of high sampling rates or the realization of the controller algorithm as a continuous-time based on operational amplifiers.

7. Note on THD Computation

The aim of this note is the determination of the minimum number of harmonics H necessary to find the value of THD. To this end we calculated the function THD_H defined in (23) for both the open and the closed loop system with both rectifier and abruptly changing resistive loads. The results presented in Figure 23 show that for the open-loop system $H = 30$ is sufficient regardless of the type of load, while for closed-loop system $H = 200$ is necessary. This is due to the resonance frequencies depicted in Figures 11 and 15, which are the highest harmonics affecting the value of the THD. In the paper $H = 500$ was used.

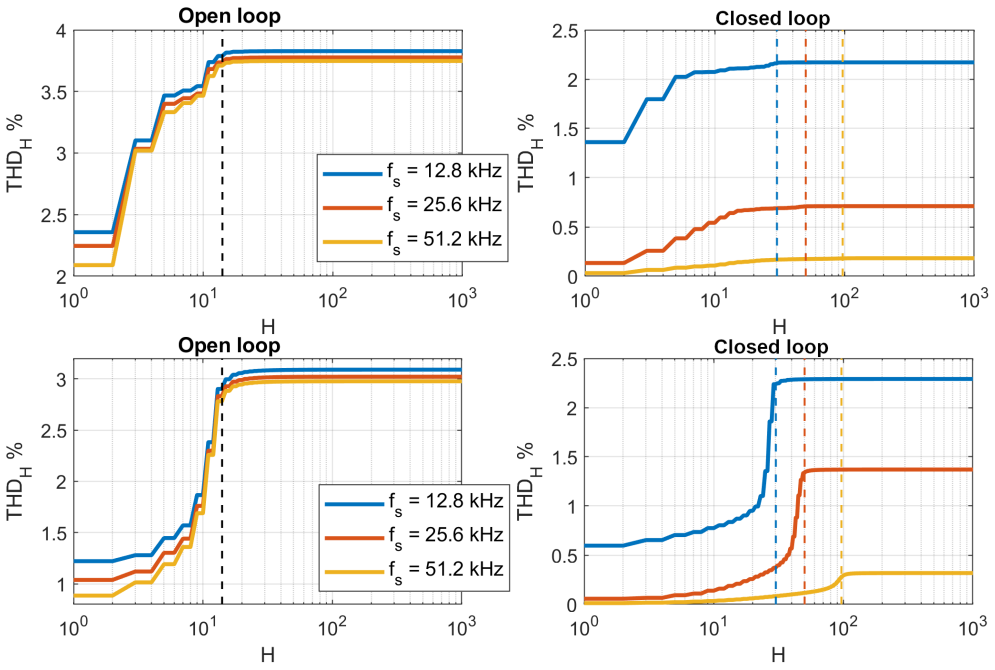


Figure 23. THD_H as a function of H. Top row—rectifier load, bottom row—abruptly changing resistive load.Vertical colored dashed lines indicate resonant frequencies f_r for no-load closed-loop systems from Table 2 depicted in Figure 15, and black line for $f_r = 702.81$ Hz for the open-loop system depicted in Figure 11.

8. Comparison with Other Results

A series of various experiments and simulations were performed and reported in [14,15] for the experimental VSI considered in this paper. The Authors put much attention to the modulation index $M = V_m/V_{DC}$. They reported using $M = 0.3$ in simulations and $M = 0.8$ in the experimental system, but without commenting on its impact on the result. No simulation schema or V_{DC} value was provided, and no comparison was made between simulation and experiment. Therefore, our results can only cautiously be compared with the outcomes of these papers. In [14], a comparison of three control systems working at sampling rate of 25.6 kHz is presented. It appears that there is little to choose between the THD values when using PID, coefficient diagram method (CDM), and passivity based control (PBC). The results were $\mathrm{THD}_{30} = 1.78\%$ for PID, 1.88% for CDM, and 1.33% for PBC, and 4.17% for the open loop (OL) case. These results are, however, much worse than our simulation result of 0.71% that uses the controller

$$H_c(z^{-1}) = 13.0\frac{0.5678 - 0.9908z^{-1} + 0.4413z^{-2}}{1 - z^{-1}} \tag{38}$$

with the THD value 3.78% in OL. The main reason of this discrepancy is a smaller value $\Delta A = 1.1$ used in this paper compared with $\Delta A = 1.5$ used in [6]. Moreover, no optimization procedure was applied to PID tuning in [6].

An important conclusion is that a properly tuned PID control outperforms more sophisticated CDM and PBC algorithms. A radically better result with THD = 0.18% is obtained when increasing the sampling frequency to 51.2 kHz.

We have also checked the possible influence of M on control performance raised in [14]. Although the value of M affects the instantaneous values of $\frac{di_L}{dt}$ within the sampling period, we have established that it does not affect the performance of output voltage control. The simulation results confirming this finding for $0.3 \leq M \leq 0.8$ are displayed in Figure 24. Thus we have shown that as far as control is concerned, not M affects its properties, but V_{DC} which determines the gain k_P of the power module in (15). As a result, changing V_m changes M but does not affect the closed loop dynamics, while changing V_{DC} changes both M and the dynamics of the closed loop. The latter can be counteracted by the gain correction specified in (10).

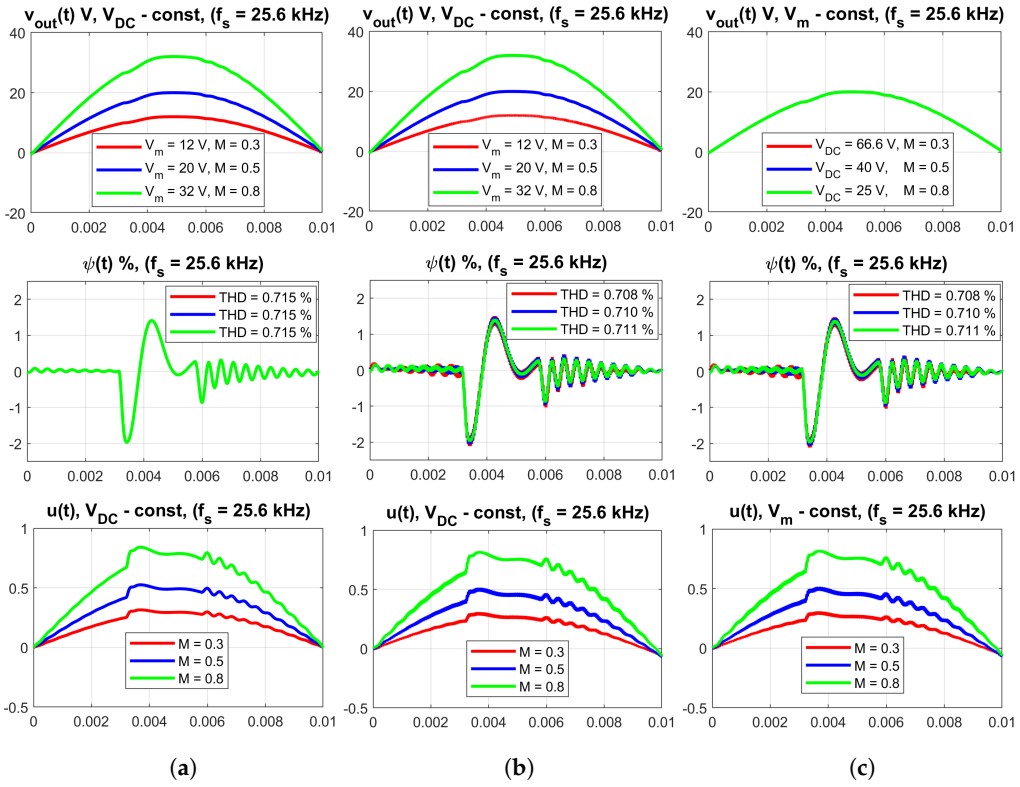


Figure 24. Comparison of simulated control results at various values of the modulation index M. (**a**) QCT simulation, $V_{DC} = 40$ V, different values of V_m; (**b**) PWM simulation, data the same as in (**a**); (**c**) PWM simulation, $V_m = 20$ V, various values of V_{DC} with the gain adjusted. Notice that the distortion function $\psi(t)$ is practically the same in all cases, hence the quality of control does not depend on M.

In order to show possible discrepancies between the model and the physical reality a comparison of an experimental result obtained on real inverter of Figure 1 with the simulation result obtained using the simulation model of Figure 3 is presented in Figure 25. The results of experiment and simulation for the PID controlled system of [14] are presented, and the values of THD_{500} are computed. They are slightly greater than THD_{30} quoted in [14,15]. The main difference between the simulation result and the experiment is presence of the ripple visible in functions $\psi(t)$ and $\chi(t)$ which influences to certain extent both $u(t)$ and v_{out}. Nevertheless, the simulated results match very well the experimental ones. This proves the validity of our models in predicting the behavior of a real inverter.

Unfortunately, for a switching frequency of $f_s = 51.2$ kHz, the computational capabilities of the controller were not sufficient to execute necessary operations within the sampling period.

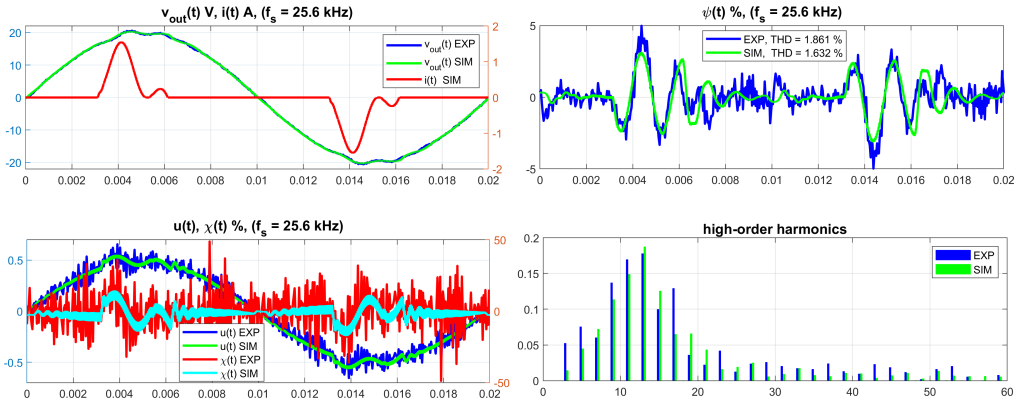


Figure 25. Experiment (EXP) vs simulation (SIM). Notice residual ripple in $\chi(t)$ and $\psi(t)$. The experiment was carried out before installing the output filter to the separation amplifier. Despite of these imperfections, a close proximity of theoretical and experimental results can be observed. This proves the validity of our models in predicting the behavior of a real inverter.

9. Conclusions

The effects pertinent to discrete-time data processing and PWM signal modulation were analyzed using the quasi-continuous-time (QCT) approach which approximates a discrete-time system by a continuous-time one. This enabled rapid simulations of the disturbed system and extensive analysis of system characteristics, including root loci and frequency plots.

The variable dynamic structure of the inverter with a rectifier load was used for both model building and controller tuning. To this end, two simulation models were presented: the PWM model and the QCT model. QCT approach has proven to be an effective PID controller tuning tool that minimizes the value of THD for the UPS inverter with the rectifier load.

Comparison of simulation results of the PWM controlled system and the approximating continuous-time one showed that there was almost no difference between them in the terms of the shape of the response and resulting THD. Comparison of the actual inverter experiment with the simulation confirmed validity of the method. A comparison with other results obtained in [14] for this VSI showed that a properly tuned PID controller outperformed the more sophisticated passivity based (PBC) and coefficient diagram method (CDM) controllers.

The most important conclusion is that the sampling rate is the major factor determining the VSI control performance. Therefore, from the control performance point of view, either possibly highest frequency of digital control system should be applied, perhaps using dedicated hardware solutions proposed in [18], or an analog solution for control algorithm could be considered.

Author Contributions: Conceptualization, M.B.; methodology, M.B., R.B. and R.G.; software, R.B. and R.G.; validation, R.B. and R.G.; formal analysis, M.B., R.B. and R.G.; writing—original draft preparation, M.B.; writing—review and editing, M.B.; visualization, R.B., R.G., M.B.; supervision, M.B.; project administration, M.B.; All authors have read and agreed to the published version of the manuscript.

Funding: Work was financed by the grant from the Silesian University of Technology—subsidy for maintaining and developing the research potential in 2021.

Institutional Review Board Statement: Not applicable.

Informed Consent Statement: Not applicable.

Data Availability Statement: Not applicable.

Acknowledgments: The Authors are grateful to Zbigniew Rymarski for providing the test bench in order to conduct experiments.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Abdel-Rahim, N.; Quaicoe, J. Analysis and design of a multiple feedback loop control strategy for single-phase voltage source UPS inverter. *IEEE Trans. Power Electron.* **2003**, *18*, 1176–1185. [CrossRef]
2. Razi, R.; Karbasforooshan, M.-S.; Monfared, M. Multi-loop control of UPS inverter with a plug-in odd-harmonic repetitive controller. *ISA Trans.* **2017**, *67*, 496–506. [CrossRef] [PubMed]
3. Woo, Y.-T.; Kim, Y.-C. Digital Control of a Single-Phase UPS Inverter for Robust AC-Voltage Tracking. *Int. J. Control Autom. Syst.* **2005**, *3*, 620–630.
4. Ryan, M.; Brumsickle, W.; Lorenz, R. Control Technology Options for Single-Phase UPS Inverters. *IEEE Trans. Ind. Appl.* **1997**, *33*, 493–501. [CrossRef]
5. Komurcugil, H. Improved passivity-based control method and its robustness analysis for single-phase uninterruptible power supply inverters. *IET Power Electron.* **2015**, *8*, 1558–1570. [CrossRef]
6. Rymarski, Z.; Bernacki, K.; Dyga, Ł.; Davari, P. Passivity-Based Control Design Methodology for UPS Systems. *Energies* **2019**, *12*, 4301. [CrossRef]
7. Serra, F.M.; De Angelo, C.H.; Forchetti, D.G. IDA-PBC control of a DC–AC converter for sinusoidal three-phase voltage generation. *Int. J. Electron.* **2017**, *104*, 93–110. [CrossRef]
8. Rymarski, Z.K.; Bernacki, K. Different Approaches to Modelling Single-phase Voltage Source Inverters for Uninterruptible Power Supply Systems. *IET Power Electron.* **2016**, *9*, 1513–1520. [CrossRef]
9. Parvez, M.; Elias, M.; Abd Rahim, N.; Blaabjerg, F.; Abbot, D.; Al-Sarawi, S. Comparative Study of Discrete PI and PR Controls for Single-Phase UPS Inverter. *IEEE Access* **2020**, *6*, 45584–45595. [CrossRef]
10. Yepes, A.; Freijedo, F.; Doval-Goy, J.; Lopez, O.; Malvar, J.; Fernes-Comesana, P. Effects of discretization methods on the performance of resonant controllers. *IEEE Trans. Power Electron.* **2010**, *25*, 1692–1712. [CrossRef]
11. Wang, X.; Loh, P.C.; Blaabjerg, F. Stability Analysis and Controller Synthesis for Single-Loop Voltage-Controlled VSIs. *IEEE Trans. Power Electron.* **2017**, *32*, 7394–7404. [CrossRef]
12. Hamamci, S.E.; Kaya, I.; Koksal, M. Improving performance for a class of processes using coefficient diagram method. In Proceedings of the 9th Mediterranean Conference on Control and Automation, MED'01, Dubrovnik, Croatia, 27–29 June 2001; pp. 1–6.
13. Manabe, S. Coefficient diagram method. In Proceedings of the 14th IFAC Symposium on Automatic Control in Aerospace 1998, Seoul, Korea, 24–28 August 1998; Volume 31, pp. 211–222.
14. Rymarski, Z.; Bernacki, K. Different Features of Control Systems for Single-Phase Voltage Source Inverters. *Energies* **2020**, *13*, 4100. [CrossRef]
15. Blachuta, M.; Rymarski, Z.; Bieda, R.; Bernacki, K.; Grygiel, R. Continuous-Time Approach to Discrete-Time PID Control for UPS Inverters—A Case Study. In *Intelligent Information and Database Systems, ACIIDS 2020*; Lecture Notes in Computer Science; Springer: Cham, Switzerland, 2020; Volume 12033.
16. Bernacki, K.; Rymarski, Z.; Dyga, Ł. Selecting the coil core powder material for the output filter of a voltage source inverter. *Electron. Lett.* **2017**, *53*, 1068–1069. [CrossRef]
17. Rymarski, Z.; Bernacki, K.; Dyga, Ł. Measuring the power conversion losses in voltage source inverters. *AEU Int. J. Electron. Commun.* **2020**, *124*, 153359. [CrossRef]
18. Maksimovic, D.; Zane, R.; Erickson, R. Impact of digital control in power electronics. In Proceedings of the 16th International Symposium on Power Semiconductor Devices and ICs, Kitakyushu, Japan, 24–27 May 2004.