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# Modeling of Average Current in Ideal and Non-Ideal Boost and Synchronous Boost Converters

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**Abstract:** This paper provides a modeling approach for average current control (ACC) operating in open-loop configuration. The converters chosen are non-ideal boost and synchronous boost converters operating in continuous conduction mode (CCM). Initially, these converters are mathematically modeled considering all the non-idealities using volt-sec and amp-sec balance equations and simulated using MATLAB and Simulink. The open-loop transfer function of the switch current or inductor current ($G_{id}$) to the duty ratio is derived using the state space averaging (SSA) technique and analyzed using MATLAB/Simulink. It is observed that the $G_{id}$ of the converters is highly stable in open loop. A larger magnitude resonance is observed in ideal boost and synchronous boost converters than the non-ideal converters. However, the low frequency gain and the crossover frequency remained the same. With the increase in the load resistance, higher resonance and lower low frequency gain is observed in non-ideal boost and non-ideal boost synchronous boost converters. The derived transfer function is validated against the standard switch model using LTSpice software.

**Keywords:** average current control; DC-DC converters; low frequency gain; MATLAB; non-ideal converters; Simulink; stability



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## 1. Introduction

ACC is one of the popular current control techniques employed in power factor correction (PFC) circuits. In ACC, the transfer function of $G_{id}$ is mathematically modeled using various control techniques such as small signal analysis and state space averaging (SSA), etc., and its features such as stability, cut-off frequency, etc., in open loop are analyzed. Although ACC cannot provide quick control, it offers high noise immunity. Figure 1 shows an open-loop ACC for a non-ideal DC-DC converter.

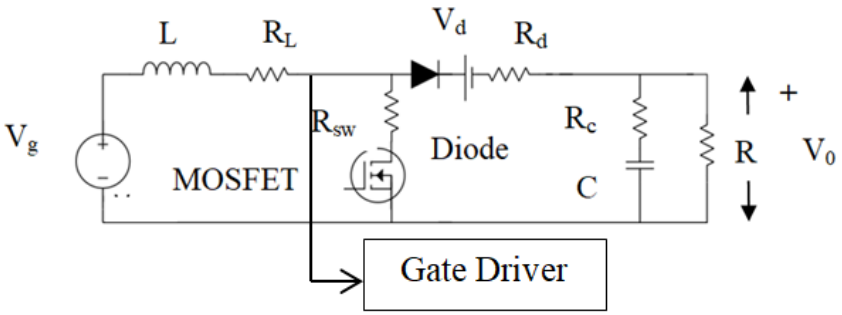


**Figure 1.** Open-loop ACC in a non-ideal converter.

In the past, several attempts were made to determine the $G_{id}$ for different converters operating in CCM and DCM operations. ACC for an ideal boost converter was determined by selecting an appropriate controller, shown in [1], based on small signal modeling (SSM)

approach for CCM. The non-idealities such as the switch resistance and equivalent series resistances (ESR) of the inductor and capacitor were not considered during ACC modeling.

As the switching frequency ($f_s$) increases, the overall converter size decreases. In [2], ACC for a buck converter operating in CCM is presented for different frequencies, namely wide frequency (WF), high frequency (HF), and low frequency considering a single loop as shown in Figure 1. The transfer function was derived using the SSM approach. The presence of ESRs plays a vital role in the WF and LF ranges. From simulation and experimental results, it was noted that the WF transfer function is of second order and has a zero. The zero frequency was lesser than that of the complex poles. The HF transfer function was first order due to a pole zero cancellation. These dynamics were studied for a non-ideal buck converter in CCM.

In [3], a comparative analysis of various control techniques for achieving low total harmonic distortion (THD) and high power factor (PF) is shown. Some of the techniques for increasing the PF are peak current mode (PCM) control, average current control (ACC), hysteresis control, borderline control, and fuzzy logic. It was concluded that to obtain a high PF and low THD, fuzzy controllers are best-suited. The traditional PI controller provided a PF of around 0.98, whereas the fuzzy controller provided a PF of 0.99. The closed control was achieved for the boost converter topology operating in CCM. However, the modeling of the converter under an open and closed loop for ideal and non-ideal conditions was not discussed.

In [4,5], a new technique called circuit averaging is introduced to analyze $G_{vd}$ (perturbed output voltage to duty cycle) without deriving the actual transfer function using LTSpice software. This method provides a shorter computation time and lesser modeling effort. The bode plots derived using SSA from MATLAB/Simulink and circuit averaging from LTSpice software matched perfectly. However, the ACC for the converters was not proposed using circuit averaging techniques.

In [6], ACC for boost converter operating in CCM using SSM is modeled and simulated for two conditions of the load, namely resistive load and current sink. The zero frequency decreased by a factor of two and the damping decreased to 14% in the case of a current sink load. However, no comments on the low frequency gain were provided. The behavior of the synchronous boost converter under such conditions was not studied.

ACC is mainly used for PFC in DC-DC converters in order to make the output voltage from the rectifier in phase with the output current. To achieve this, the rectifier should consider the DC-DC converter as a resistive load. An application of ACC using a boost converter operating in CCM is presented in [7]. The power factor was greater than 0.9 for 120 V and 230 V. Though ACC was used, the modeling and comparative analyses of boost and synchronous boost converters considering the non-idealities were not shown.

In [8], mathematical modeling for transformerless DC-DC converters is presented and simulated using MATLAB/Simulink. The converters were modeled using 'commonly used blocks' and analyzed by deriving the volt-sec and amp-sec balance equations. This type of modeling provided both the transient and steady-state responses. The converters that were modeled were buck, boost, buck-boost, and cuk operating in CCM under ideal conditions. In [9], similar converters along with SEPIC operating in CCM are modeled; however, 'Mux' and 'fcn' blocks were used instead of 'commonly used blocks'. Along with DC-DC converters, a controlled three-phase rectifier was modeled considering an inductive load.

The modeling for isolated DC–DC converters such as ideal flyback and forward converter was performed and simulated using MATLAB/Simulink [10]. The closed-loop modeling of the converters was performed using PI controllers. It was concluded that the flyback converter for the selected specifications was better-suited than the forward converter considering the response time. The ideal flyback converter showed lesser (a) duty ratio and (b) filter inductance and, hence, the conduction losses were reduced.

Modeling of DC-DC converters is extremely important to understand the dynamics of the converter and design inductor and capacitor. The steady-state modeling of DC-

DC converters was simulated using MATLAB/Simulink. Three different approaches for modeling buck, boost and buck-boost converters were considered. In practice, the DC-DC converters possess various parameters such as diode drop ($V_d$), MOSFET drop ($R_{sw}$), and ESRs of inductor and capacitor ($R_L$ and $R_c$, respectively), which in turn cause a decrease in the output voltage. The behavior of converters changes when modeled considering non-idealities. Mathematical modeling considering the non-ideality (inductor ESR) for these converters was investigated. The DC transfer functions for the converters were also derived using the state space averaging approach [11].

In [12], the transfer functions for the constant voltage operation ($G_{vd}$) for ideal buck, boost, and buck-boost converters operating in CCM are derived using various methods, namely SSM, SSA, and circuit averaging techniques. It was shown that the ideal boost and buck-boost converters were unstable in open-loop mode due to the presence of right-half-plane (RHP) zeroes. In achieving closed-loop control in DC-DC converters, the design of controllers plays an extremely critical role, especially during phase reversal. The various steps to be taken while designing a controller are shown in [13].

The primary aim of this paper w to identify the optimal choice of DC-DC converters between boost and synchronous boost for ACC in open loop. Since the converters designed are for similar output voltage and current ratings, their performances were compared. The $G_{id}$ for ideal and non-ideal boost converters was derived using state space averaging technique and was compared with that of synchronous boost converters. The behavior in terms of low frequency gain, resonant frequency, and crossover frequency though the modeling approach is studied in this paper. Increased low frequency gain is one of the important features of using a non-ideal synchronous boost converter. This feature, in turn, provides an improved steady state response compared to the non-ideal boost converter.

In Sections 2 and 3, mathematical models for the non-ideal converters assuming CCM operation are derived using volt-sec and amp-sec balance equations and modeled using MATLAB/Simulink software. Section 4 shows the derivation of $G_{id}$ using the SSA technique for the converters. The specifications of the converters are shown in Section 5. Results and discussions of the analyses of $G_{id}$ for the mentioned converters are provided in Section 6.

## 2. Mathematical Model for Boost Converter

Figure 2 shows a schematic of an ideal boost converter operating in CCM. The various drops across the switch S (MOSFET), diode D, and various ESRs are ignored. When the switch S is closed, the inductor is charged as it is connected in series with the supply voltage. The diode becomes reverse-biased and the capacitor becomes charged due to the load current.

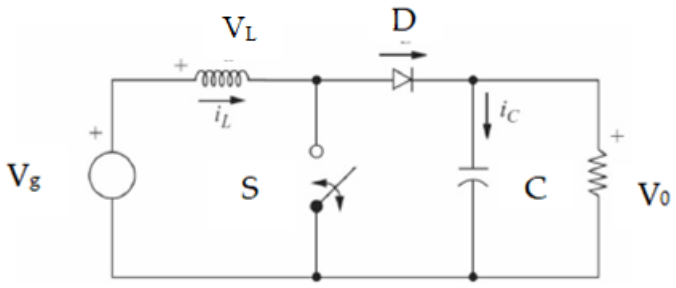


**Figure 2.** Schematic of an ideal boost converter.

When the switch S is opened, the charged inductor changes its polarity resulting in the diode becoming forward-biased. Similarly, the previous charged capacitor becomes discharged through the load resistor R.

The mathematical model for the converter is shown in [9].

$$V_L = L\frac{di_L}{dt} = V_g - V_0(1-s) \quad (1)$$

$$i_c = C\frac{dV_0}{dt} = i_L(1-s) - \frac{V_0}{R} \quad (2)$$

The working of the non-ideal boost converter is similar to that of the ideal converter. However, the drops associated with the switch, diode and the ESRs of inductor and capacitor are considered in the non-ideal condition.

Figure 3 shows a schematic of a non-ideal boost converter operating in CCM.

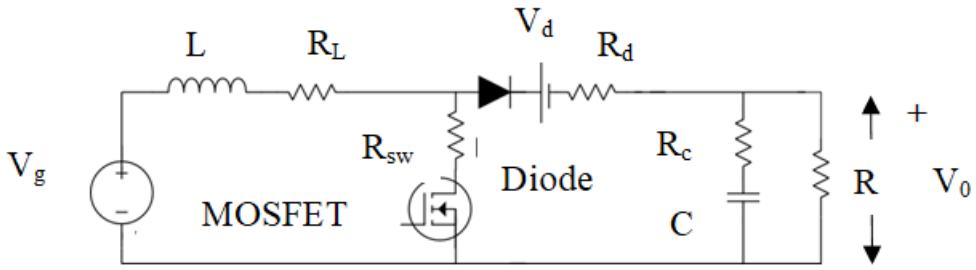


**Figure 3.** Schematic of a boost converter.

The operation of the converter involves two stages of the switch: (a) switch OFF and (b) switch ON.

When the switch MOSFET1 is closed,

$$V_L = V_g - i_L(R_L + R_{sw}) \quad (3)$$

$$i_c = -V_c/(R + R_c) \quad (4)$$

where $V_L$ is the voltage drop across the inductor (V), $V_g$ is the supply voltage (V), $i_L$ is the current in the inductor (A), $R_L$ is the equivalent series resistance (ESR) of the inductor (Ω), $R_{sw}$ is the switch resistance (Ω), $i_c$ is the capacitor current (A), $V_c$ is the voltage across the capacitor (V), $R$ is the load resistance (Ω), $R_c$ is the capacitor ESR (Ω), and $V_0$ is the output voltage (V).

When the switch MOSFET1 is opened and MOSFET2 is closed,

$$V_L = V_g - i_L(R_L + R_d + RR_c/(R + R_c)) - V_d - RV_c/(R + R_c) \quad (5)$$

$$i_c = i_L R/(R + R_c) - V_c/(R + R_c) \quad (6)$$

where $V_d$ is the diode drop (V) and $R_d$ is dynamic resistance of the diode (Ω).

The mathematical model for the converter can be obtained by combining (3) and (5) with (4) and (6).

$$V_L = \frac{di_L}{dt} = (V_g - i_L(R_L + R_{sw})) * s + (1-s) * ((V_g - i_L(R_L + R_d + RR_c/(R + R_c)) - V_d - RV_c/(R + R_c))) \quad (7)$$

where $s$ is the instantaneous duty cycle.

$$i_c = C\frac{dV_c}{dt} = (-V_c/(R + R_c))s + (1-s) * ((i_L R/(R + R_c) - V_c/(R + R_c))) \quad (8)$$

Equations (7) and (8) were modeled using MATLAB/Simulink and the dynamics of $i_L$ and $V_c$ were captured.

## 3. Mathematical Model for Synchronous Boost Converter

Figure 4 shows an ideal synchronous boost converter operating in CCM. By comparing Figures 1 and 3, it is noted that in Figure 3, diode D is replaced by the MOSFET S2. The drop across MOSFET would be lesser than that of the diode. This provides a lower duty ratio to achieve the specified output voltage. Such converters are referred to as point-of-load (POL) converters and are used as power supplies for micro-controllers and processors.

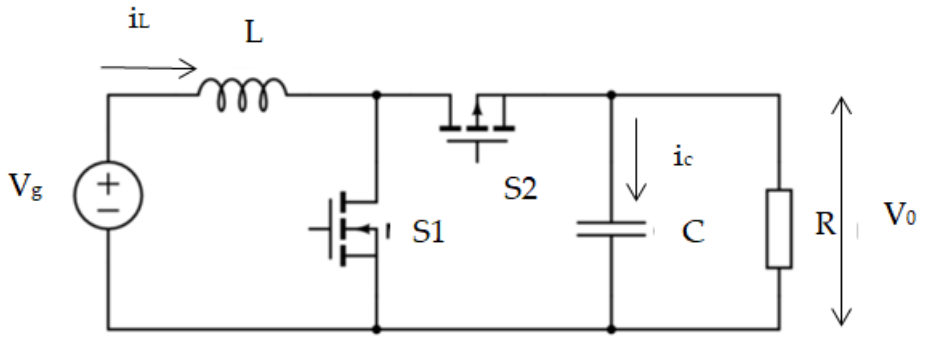


**Figure 4.** Schematic of ideal synchronous boost converter.

Initially, the switch S1 is closed and S2 is open. The inductor L is charged due to the supply current. Similarly, the capacitor is also charged due to the load current. At this point of time, switch S1 is opened and S2 is closed.

The charged inductor changes the polarity and the current $i_L$ flows in switch S2. The charged capacitor is discharged to the resistive load R.

The mathematical model for the converter is shown below.

$$V_L = L\frac{di_L}{dt} = V_g - V_0(1-s) \tag{9}$$

$$i_c = C\frac{dV_0}{dt} = i_L(1-s) - \frac{V_0}{R} \tag{10}$$

It can be observed that the equations are similar to that of ideal boost converter. However, in order to observe the difference between the converter, non-idealities have to be considered, which is presented in this paper. Figure 5 shows a non-ideal synchronous boost converter operating in CCM.

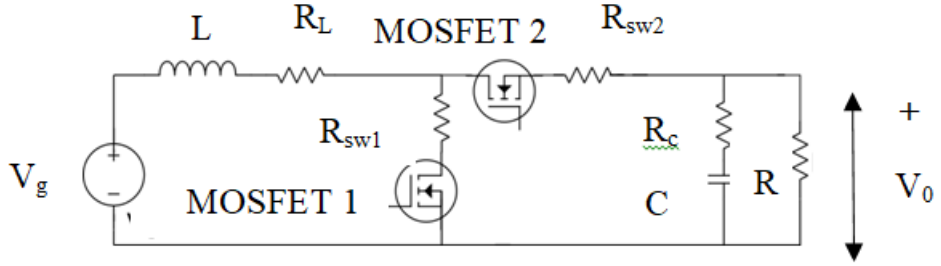


**Figure 5.** Schematic of a synchronous boost converter.

When switch MOSFET 1 is closed,

$$V_L = V_g - i_L(R_L + R_{sw1}) \tag{11}$$

$$i_c = -V_c/(R + R_c) \tag{12}$$

When switch MOSFET 1 is opened and MOSFET 2 is closed,

$$V_L = V_g - i_L(R_L + R_{sw2} + RR_c/(R + R_c)) - RV_c/(R + R_c) \tag{13}$$

$$i_c = \frac{i_L R}{R + R_c} - \frac{Vc}{R + R_c} \tag{14}$$

The mathematical model for the converter can be obtained by combining (11) with (13) and (12) with (14),

$$V_L = L\frac{di_L}{dt} = (V_g - i_L(R_L + R_{sw1}))s + (1-s) * (V_g - i_L(R_L + R_{sw2} + RR_c/(R+R_c)) - RV_c/(R+R_c)) \quad (15)$$

$$i_c = C\frac{dV_c}{dt} = (-V_c/(R+R_c))s + (1-s) * ((i_L R/(R+R_c) - V_c/(R+R_c))) \quad (16)$$

where $R_{sw1}$ and $R_{sw2}$ ($\Omega$) are the resistances of MOSFET 1 and 2, respectively.

**4. Average Current Modeling of Non-Ideal Boost Converter**

As shown above, the operation of the converters can be described when the switch is closed and later opened. The state variables were selected as $i_L$, $V_c$, and the output as $i_L$. With respect to Figure 3, the output voltage $V_0$ can be expressed as

$$V_0 = V_c + i_c R_c \quad (17)$$

Substituting (11) in (12),

$$V_0 = RV_c/(R+R_c) \quad (18)$$

Substituting (18) in (11),

$$i_c = -V_c/(R+R_c) \quad (19)$$

The state-space representation is defined as

$$\overset{0}{X} = AX + BU \quad (20)$$

$$Y = CX + EU \quad (21)$$

The state-space matrices were constructed and are shown below.

$$\begin{bmatrix} di_L/dt \\ dV_c/dt \end{bmatrix} = \underbrace{\begin{bmatrix} -(R_L+R_{sw})/L & 0 \\ 0 & -1/C(R+R_c) \end{bmatrix}}_{A_1} \begin{bmatrix} i_L \\ V_c \end{bmatrix} + \underbrace{\begin{bmatrix} 1/L & 0 \\ 0 & 0 \end{bmatrix}}_{B_1} \begin{bmatrix} V_g \\ V_d \end{bmatrix} \quad (22)$$

When the switch is closed,

$$V_0 = V_c + i_c R_c \quad (23)$$

From the circuit,

$$i_c = i_L - V_0/R \quad (24)$$

Substituting (18) in (19),

$$V_0 = R(V_c + i_L R_c)/(R+R_c) \quad (25)$$

Hence,

$$V_L = V_g - i_L(R_L + R_d + RR_c/(R+R_c)) - V_d - RV_c/(R+R_c) \quad (26)$$

$$i_c = i_L(1 - R_c/(R+R_c)) - V_c/(R+R_c) \quad (27)$$

$$\begin{bmatrix} di_L/dt \\ dV_c/dt \end{bmatrix} = \underbrace{\begin{bmatrix} -(R_d+R_L)/L + RR_c/(R+R_c))/L & -R/L(R+R_c) \\ R/C(R+R_c) & -1/C(R+R_c) \end{bmatrix}}_{A_2} \begin{bmatrix} i_L \\ V_c \end{bmatrix} + \underbrace{\begin{bmatrix} 1/L & -1/L \\ 0 & 0 \end{bmatrix}}_{B_2} \begin{bmatrix} V_g \\ V_d \end{bmatrix} \quad (28)$$

Averaging the equations,

$$A = A_1 D + A_2 D' \quad (29)$$

$$\begin{aligned} A &= \begin{bmatrix} a_{11} & a_{22} \\ a_{21} & a_{22} \end{bmatrix} \\ a_{11} &= -(DR_{sw} + R_L + R_d D' + D'RR_c/(R+R_c))/L \\ a_{12} &= -RD'/L(R+R_c) \\ a_{21} &= -D'R/C(R+R_c) \\ a_{22} &= -1/C(R+R_c) \\ \hat{i_L}/\hat{d} &= C[sI - A]^{-1}B \end{aligned} \tag{30}$$

$$C = [1\ 0] \tag{31}$$

where the input is

$$U = \begin{bmatrix} V_g \\ V_d \end{bmatrix} X = \begin{bmatrix} iL \\ Vc \end{bmatrix} \tag{32}$$

$$\frac{\hat{i_L}}{\hat{d}} = \frac{(1) + \frac{R^2(1-D)I_L}{LC(R+R_c)^2}}{\Delta} \tag{33}$$

where (1) is

$$(s + 1/C(R+R_c)) * ((I_L/L)(R_d - R_{sw} + RR_c/(R+R_c)) + RV_c/L(R+R_c) + V_d/L \tag{34}$$

$$\Delta = (1) + R^2 D'^2/(LC * (R+R_c)^2)$$

and (1) is

$$s + 1/C(R+R_c)) * (s + (DR_{sw} + R_L + R_d D' + RR_c D'/(R+R_c))/L$$

The state matrix E = 0 as it has no coefficient related to matrix U.

## 5. Average Current Modeling of Non-Ideal Synchronous Boost Converter

As shown for a non-ideal boost converter, the state space matrices A, B, C, and E were derived and are shown below.

$$A_1 = \begin{bmatrix} -(R_L + R_{sw1})/L & 0 \\ 0 & -1/C(R+R_c) \end{bmatrix} \tag{35}$$

$$A_2 = \begin{bmatrix} -(R_L + R_{sw2} + RR_c/(R+R_c))/L & -R/L(R+R_c) \\ R/C(R+R_c) & -1/C(R+R_c) \end{bmatrix} \tag{36}$$

$$A = \begin{bmatrix} -(D'R_{sw1} + D'R_{sw2} + D'RR_c/(R+R_c))/L & -RD'/L(R+R_c) \\ RD'/C(R+R_c) & -1/C(R+R_c) \end{bmatrix} \tag{37}$$

$$\frac{\hat{i_L}}{\hat{d}} = \frac{(1) * (s + \frac{1}{C(R+R_c)}) + \frac{R^2(1-D)I_L}{LC(R+R_c)^2}}{\Delta} \tag{38}$$

where (1) is

$$((-I_L/L)(R_{sw1} - R_{sw2} - \frac{RR_c}{R+R_c})) + \frac{RV_c}{L(R+R_c)} \tag{39}$$

$$\Delta = (2) + \frac{R^2(1-D)^2}{(LC * (R+R_c)^2)} \tag{40}$$

where (2) is

$$(s + (R_{sw}D + R_{sw2}D' + RR_c D'/(R+R_c))/L) * (s + 1/C(R+R_c)) \tag{41}$$

## 6. Converter Specifications

Table 1 shows the specifications of the converters.

**Table 1.** Specification of converters.

| SL.NO | Parameter | Value |
|---|---|---|
| 1 | Input Voltage, $V_g$ | 5 V |
| 2 | Output Voltage, $V_0$ | 12 V |
| 3 | Output Current, $I_0$ | 1 A |
| 4 | Inductor, L | 4.7 µH |
| 5 | Inductor ESR, $R_L$ | 0.071 Ω |
| 5 | Switch Resistance, $R_{sw}$ | 0.024 Ω |
| 6 | Diode Drop, $V_d$ | 0.555 V |
| 7 | Capacitor, C | 9.66 µF |
| 8 | Capacitor ESR, $R_c$ | 0.16 Ω |
| 9 | Duty Ratio, D | 0.6285 |
| 10 | Switching Frequency, $f_s$ | 500 kHz |

## 7. Results

Figures 6 and 7 show the variation in $i_L$ and $V_c$ for non-ideal boost and synchronous boost converters. As observed from Figure 6, the maximum values of $V_0$ and $i_L$ were around 16 V and 12.5 A, respectively. However, the steady-state values were 12 V and 2.6 A, respectively. Similar observations can be observed in Figure 7.

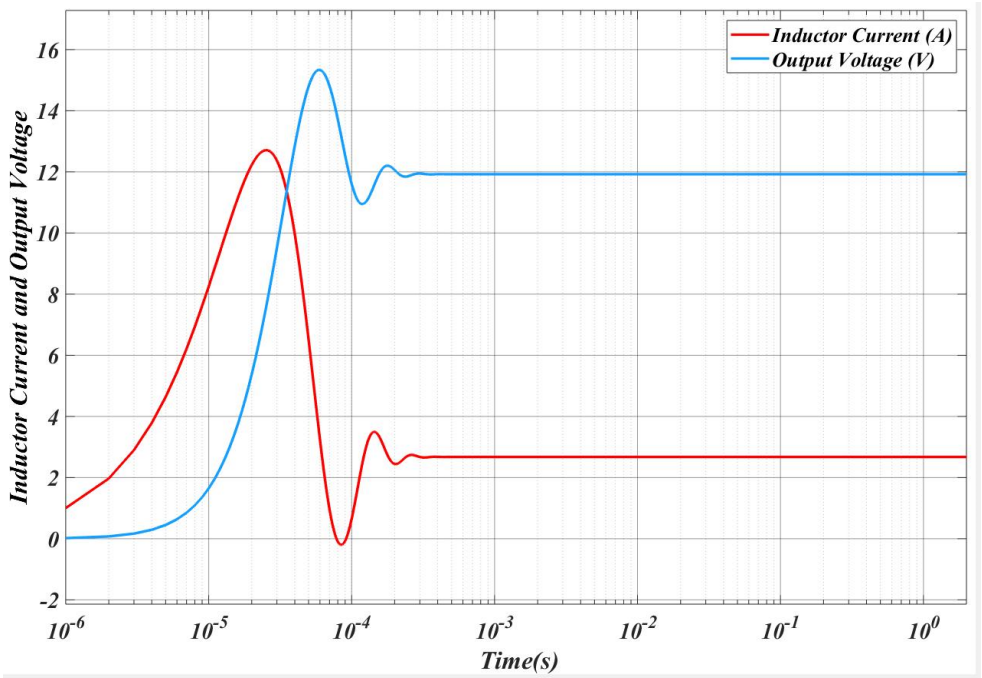


**Figure 6.** $i_L$ and $V_c$ vs. time.

Figure 8 shows the frequency response of $G_{id}$ for ideal and non-ideal boost converters. The ideal converter shows higher resonance than the non-ideal converter. However, no major change in low frequency gain and the cut-off frequency is seen.

Figure 9 shows frequency response of $G_{id}$ for ideal and non-ideal synchronous boost converters. Higher resonance is observed in the non-ideal synchronous boost converter. However, no change in the cut off frequency is observed.

Figure 10 shows frequency response of $G_{id}$ for non-ideal boost and synchronous converters. The non-ideal synchronous boost converter shows higher resonance than the other converter. However, no change is seen in the crossover frequency.

Figure 11 shows the open loop poles and zeros of $G_{id}$ for ideal and non-ideal boost converters. It can be observed that the poles in the non-ideal converter are separated from the right-hand side (RHS) of the s-plane due to which they possess more stability.

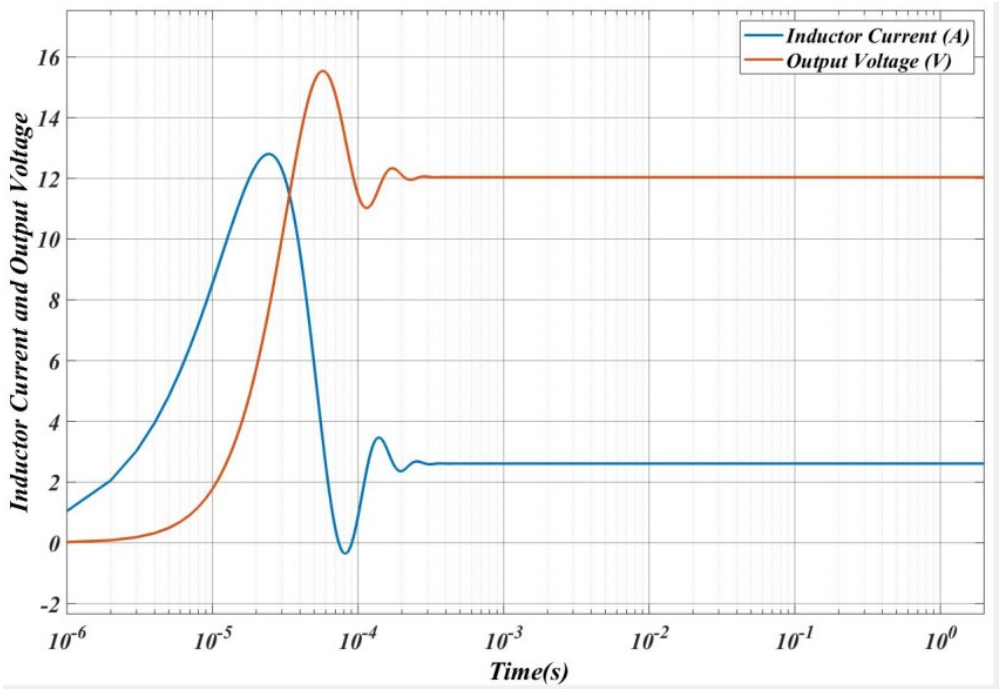


**Figure 7.** $i_L$ and $V_0$ vs. time.

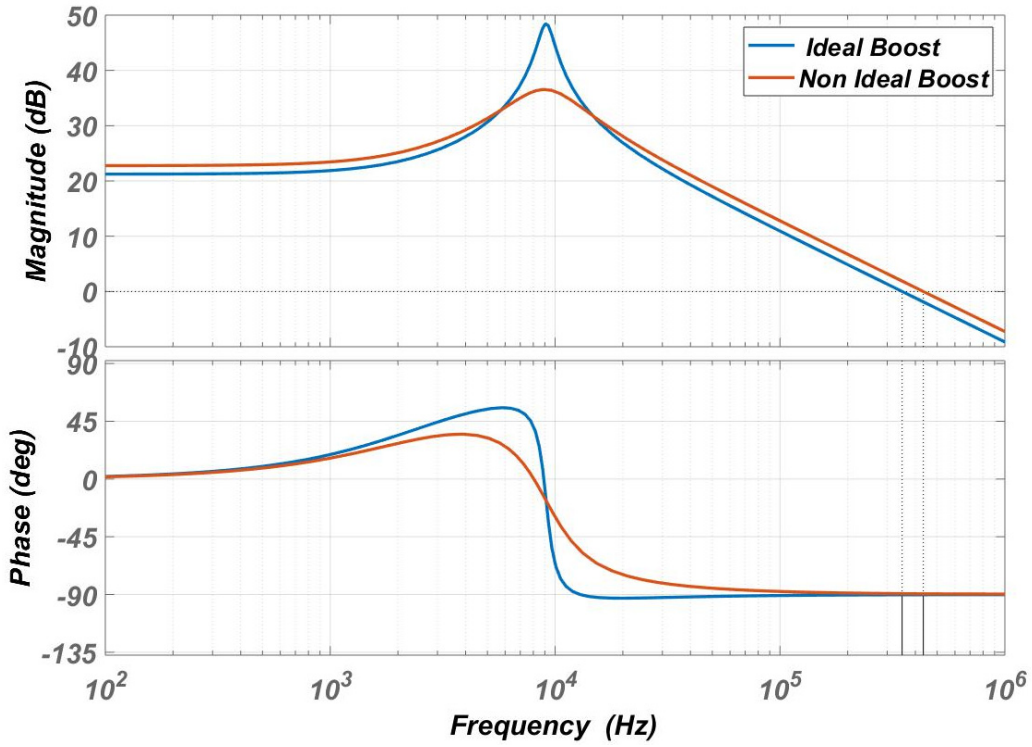


**Figure 8.** Frequency response of $G_{id}$ for ideal and non-ideal boost converters.

In Figure 12, the root loci for the same converters were analyzed by making $R_{C=}$ 0. It was observed that the zeros of the converters superposed.

The root loci of the Ideal and non-ideal synchronous boost converters were analyzed. Figure 13 shows the placement of the poles and zeros of $G_{id}$. It was observed that the non-ideal converter was more stable than the ideal converter. A similar observation was made on the synchronous boost converters shown in Figure 14. Changes in $R_c$ had a negligible effect on the position of poles and zeros.

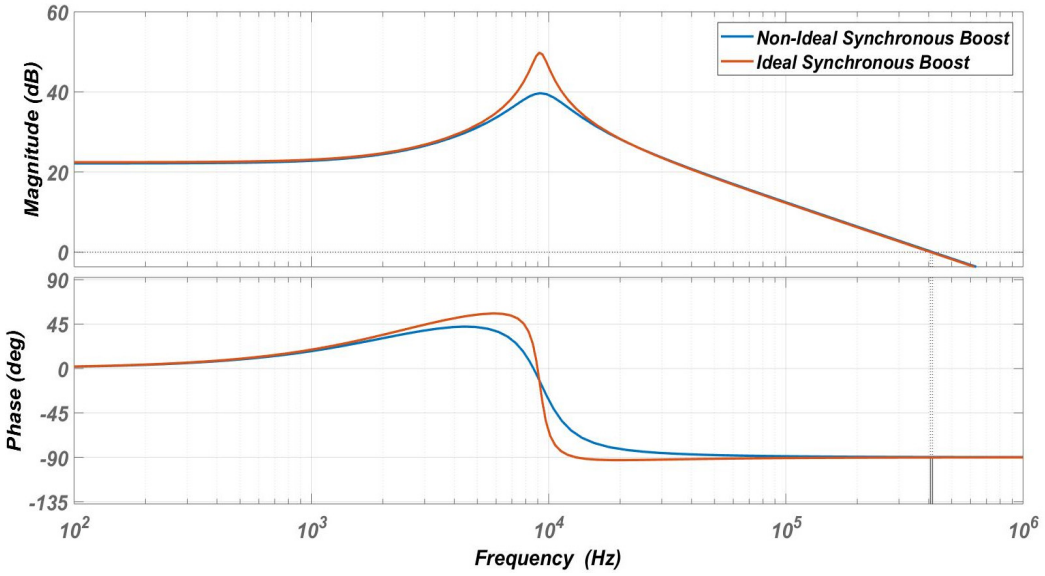


**Figure 9.** Frequency response of $G_{id}$ for ideal and non-ideal synchronous boost converters.

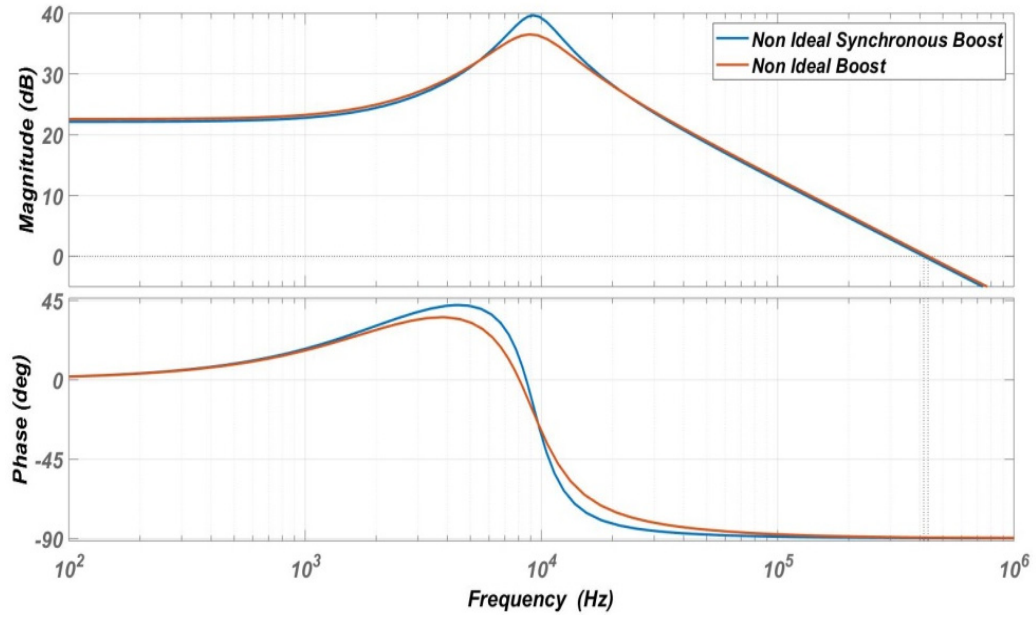


**Figure 10.** Frequency response of $G_{id}$ for non-ideal boost and synchronous converters.

Table 2 shows the features of the converters in terms of Gain Margin (GM), Phase Margin (PM) and Cross Over frequency ($f_c$)

**Table 2.** Features of $G_{id}$ for various converters.

| Type | GM | PM (Degrees) | $f_c$ (kHz) |
|---|---|---|---|
| Ideal Boost | Infinity | 89.8 | 349 |
| Non Ideal Boost | Infinity | 90.3 | 424 |
| Ideal Synchronous Boost | Infinity | 89.8 | 407 |
| non-ideal Synchronous Boost | Infinity | 90.3 | 425 |

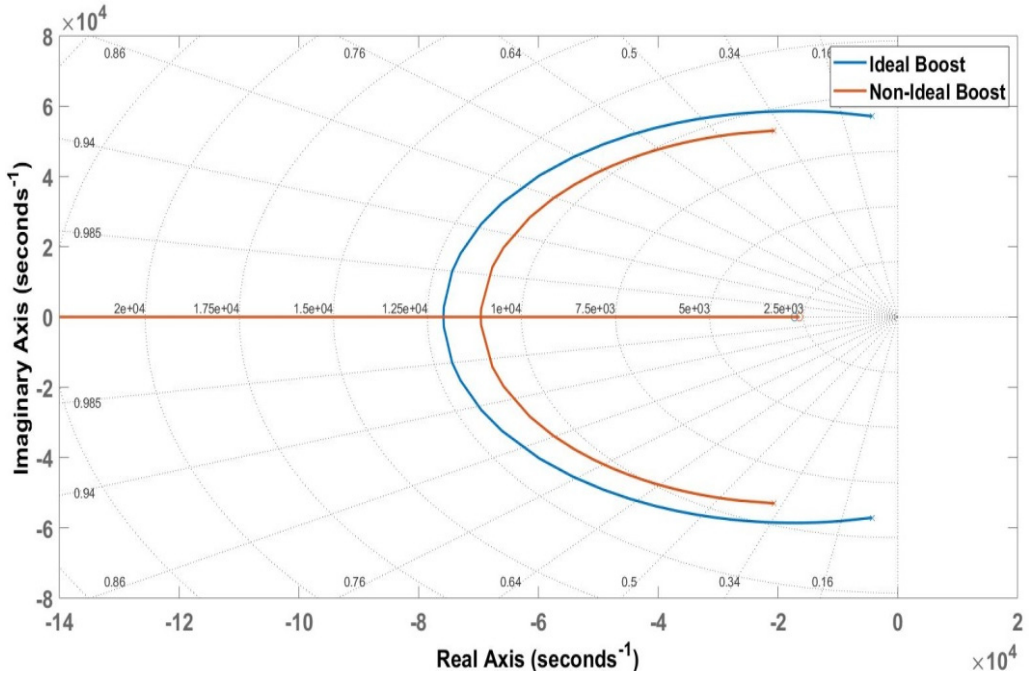


**Figure 11.** Root loci of the $G_{id}$.

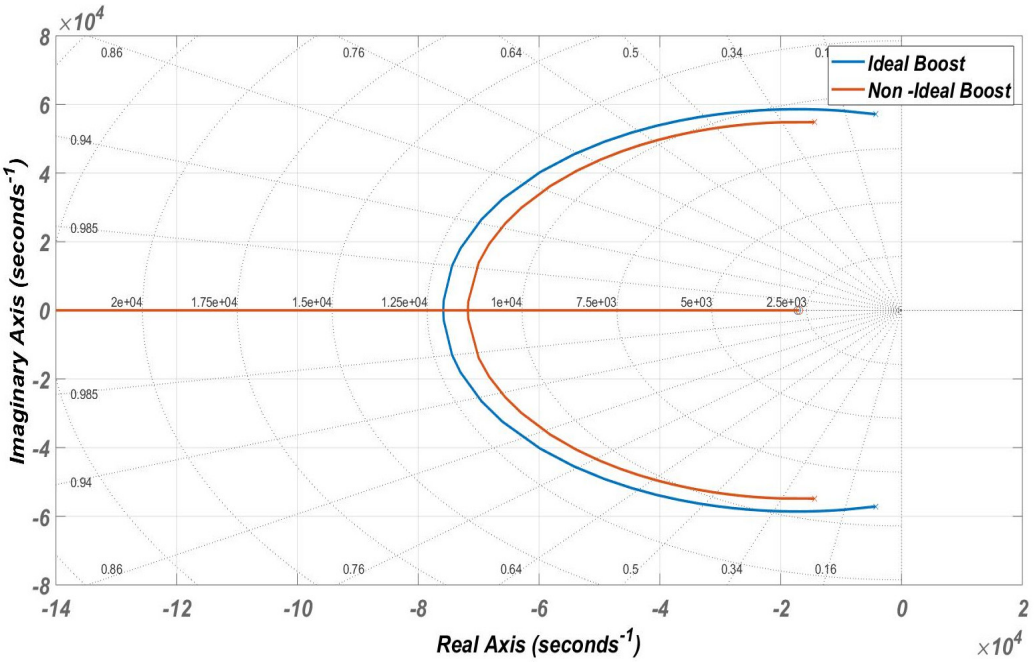


**Figure 12.** Root loci of the $G_{id}$ for $R_C = 0$.

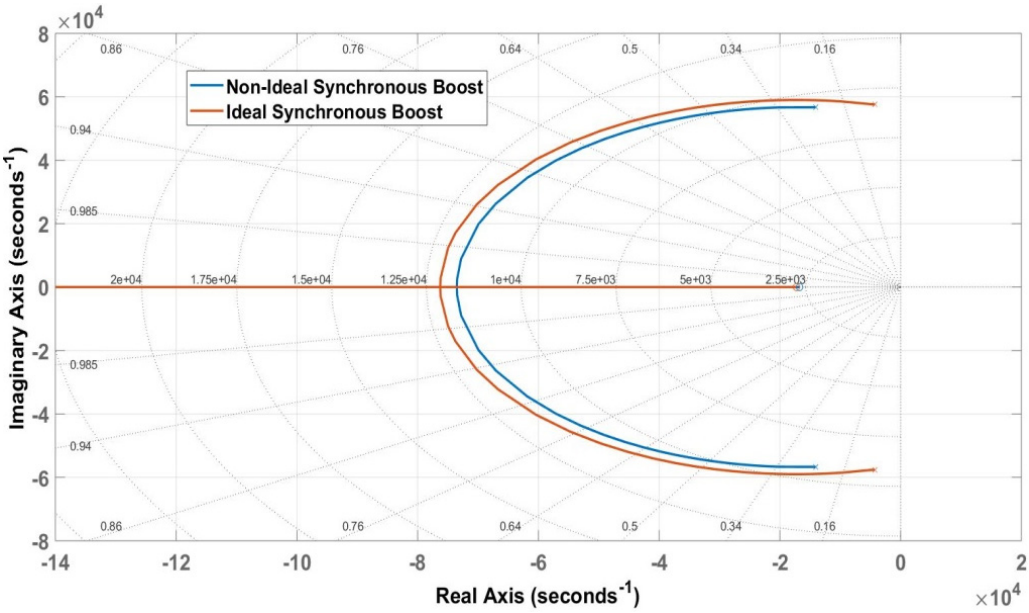


**Figure 13.** Placement of poles and zeros.

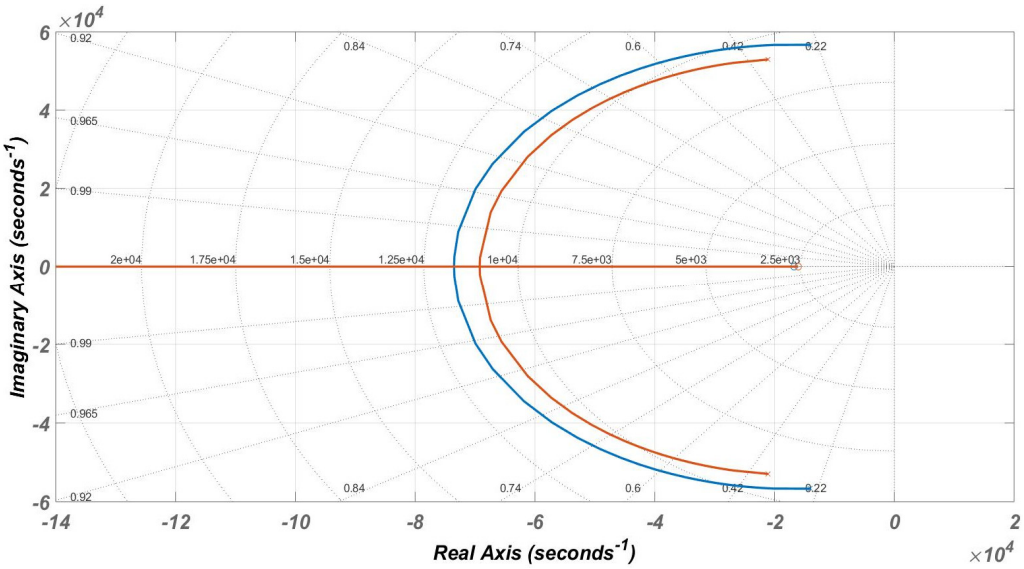


**Figure 14.** Placement of poles and zeros on the synchronous boost converters.

## 8. Validation

The derived transfer function was validated using the switch models provided in the LTSpice software tool. Figure 15 shows the switch model used for non-ideal boost and synchronous boost converters.

Figure 16 shows the $G_{id}$ obtained from the switch model. It is noted that Figures 15 and 16 show a perfect match in terms of the low frequency gain, phase margin (PM), and crossover frequency. The low frequency gain was 22 dB, PM was 424 kHz, and resonant frequency was 9 kHz.

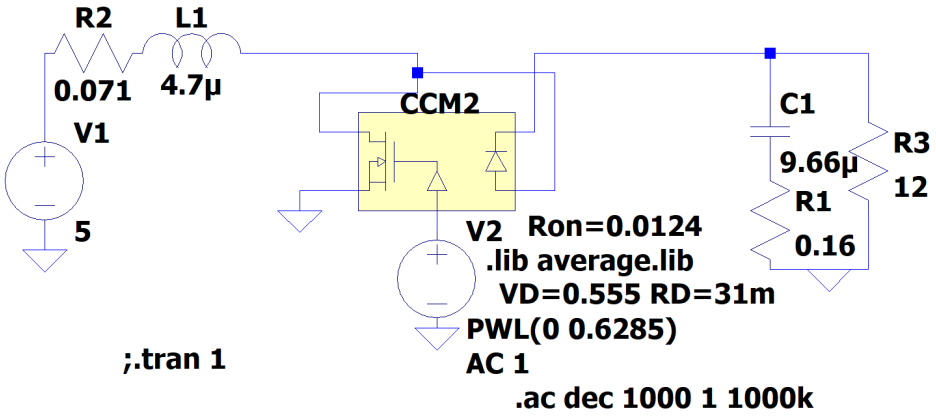


**Figure 15.** Switch model of ideal and non-ideal boost and synchronous boost converters.

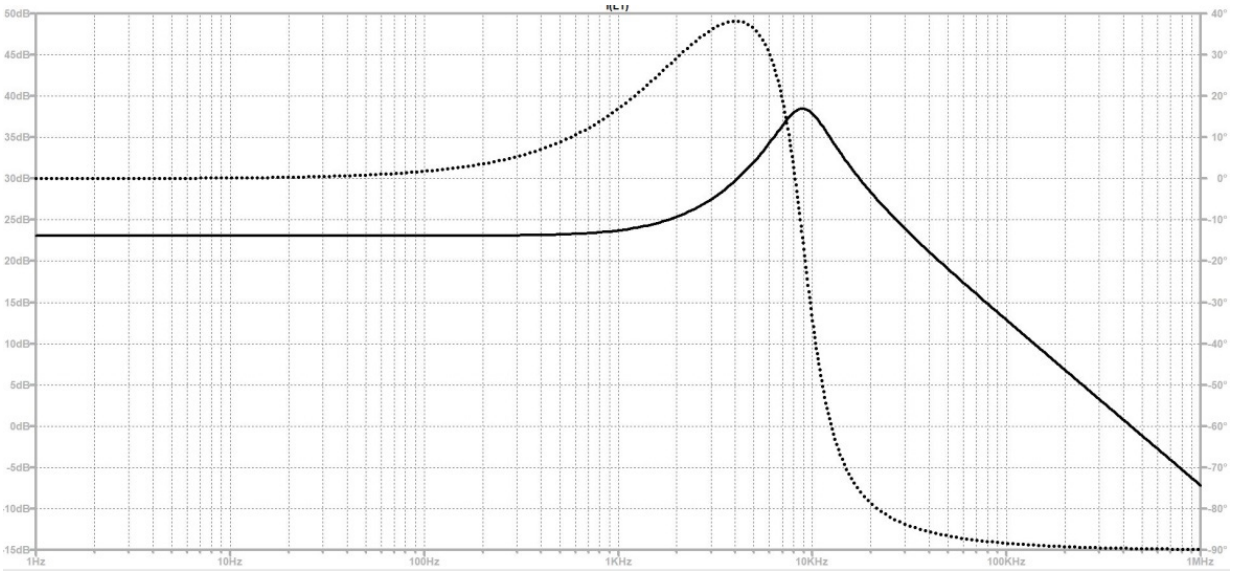

**Figure 16.** $G_{id}$ of a non-ideal boost converter from switch model.

In Figure 17, R varies from 12 to 36 Ω and the $G_{id}$ can be observed for a non-ideal boost converter. It is noted that the highest load resistance provided the lowest frequency gain and the highest resonant frequency.

Figures 18 and 19 show the effect of $G_{id}$ on varying L and C values. It is inferred that as the value of L increases, the resonant frequency shifts toward the lower frequency range and the resonant frequency gradually decreases. The lowest L provided the highest cut-off frequency. However, when C increased, the cut-off frequency remained the same.

Figure 20 shows the $G_{id}$ for a synchronous boost converter. By comparing Figures 10 and 20, the low frequency gain, PM and the cut-off frequency perfectly match. The low frequency gain was 22.1 dB, PM was 90.3°, cut-off frequency was 415 kHz, and resonant frequency was 9.38 kHz.

In Figures 21 and 22, R and L vary and the effect on $G_{id}$ was studied on a non-ideal synchronous boost converter. Similar observations to that of the non-ideal boost converter were made.

Figure 23 shows the $G_{id}$ for an ideal boost converter. The $G_{id}$ shown in Figure 23 perfectly matches that of Figure 8 in terms of the low frequency gain, PM, crossover frequency, and resonant frequency. The low frequency gain was 22.9 dB, PM was 90.3°, crossover frequency was 424 kHz, and resonant frequency was 9.12 kHz.

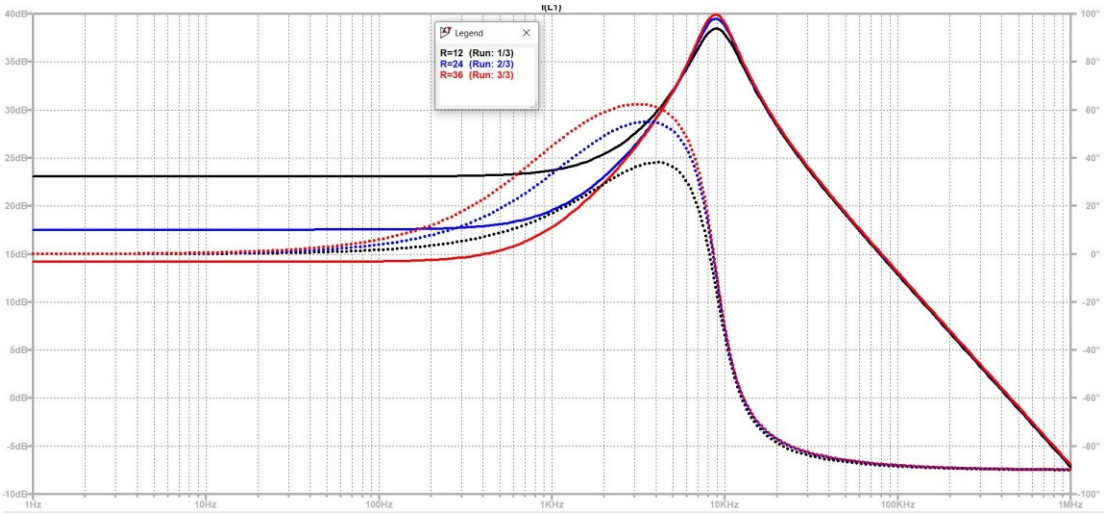


**Figure 17.** Variation in $G_{id}$ due to change in R.

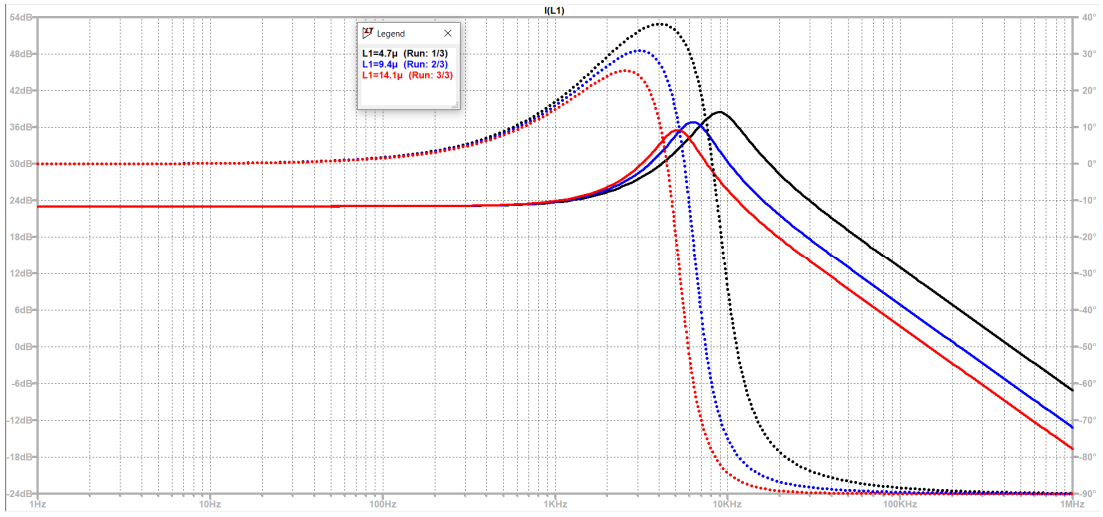


**Figure 18.** Variation in $G_{id}$ due to change in L.

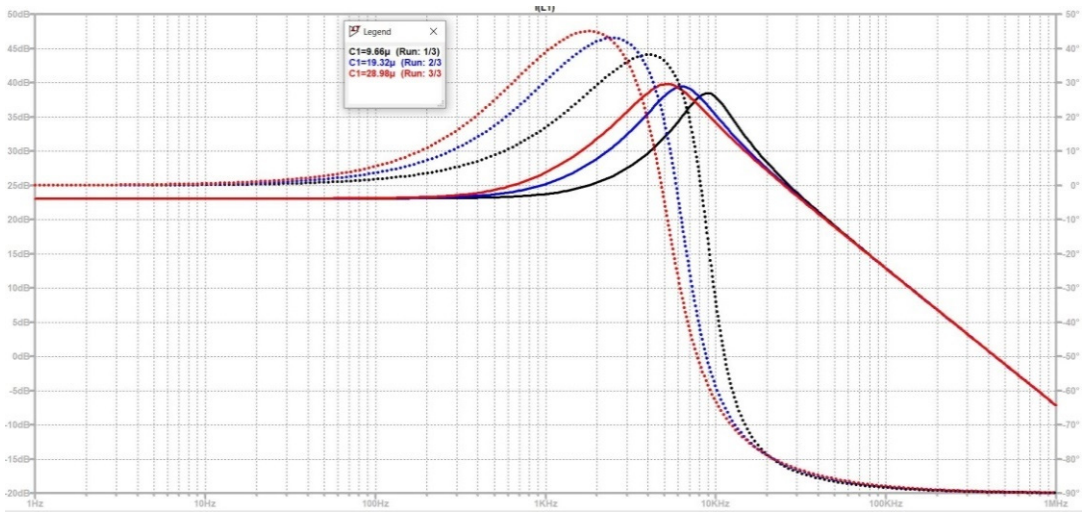


**Figure 19.** Variation in $G_{id}$ due to change in C.

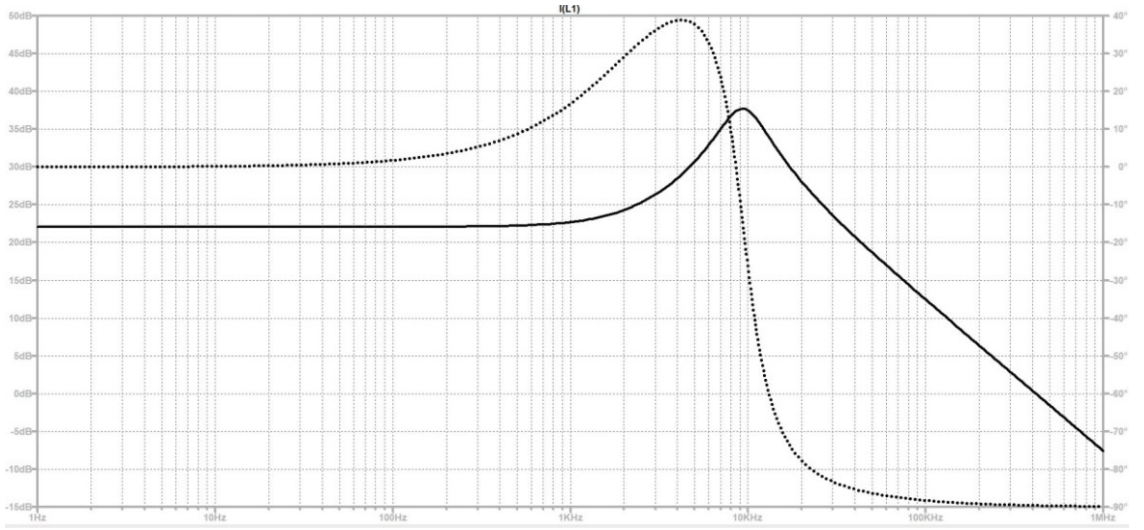


**Figure 20.** $G_{id}$ of a non-ideal synchronous boost converter from the switch model.

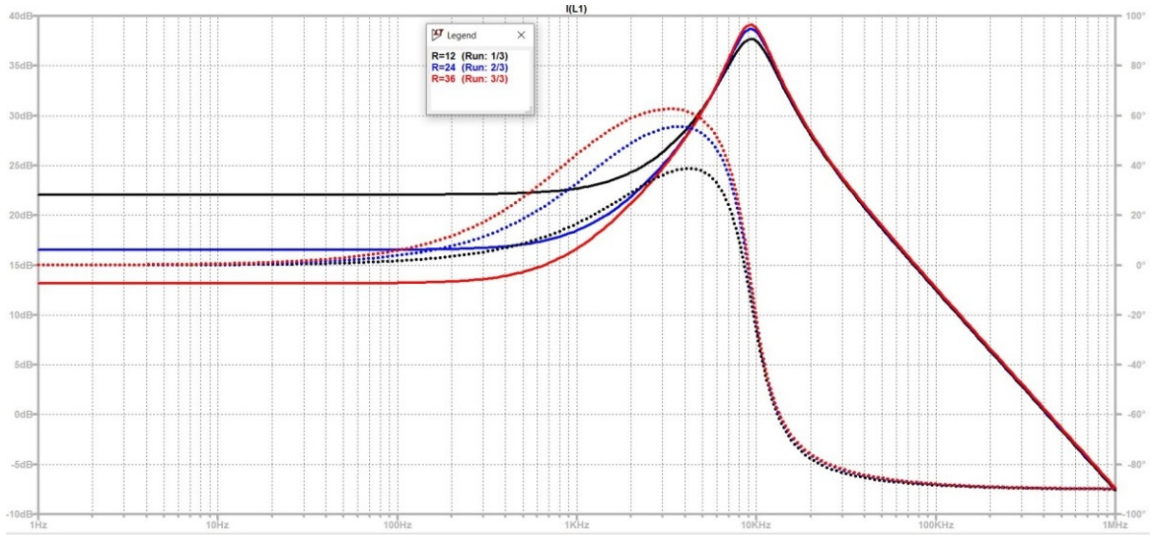


**Figure 21.** Variation in $G_{id}$ due to change in R on a non-ideal synchronous boost converter.

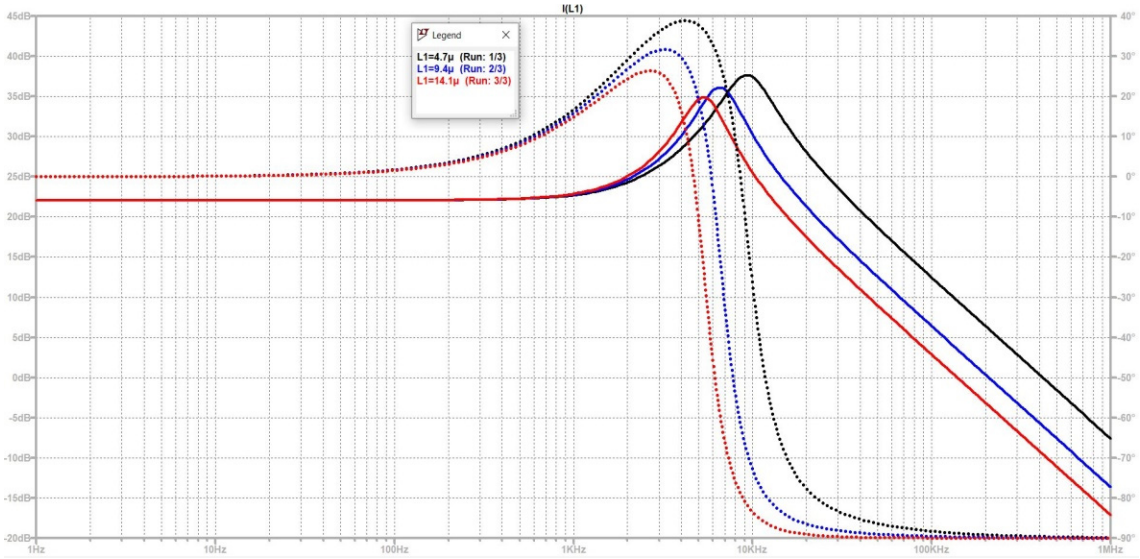


**Figure 22.** Variation in $G_{id}$ due to change in L on a non-ideal synchronous boost converter.

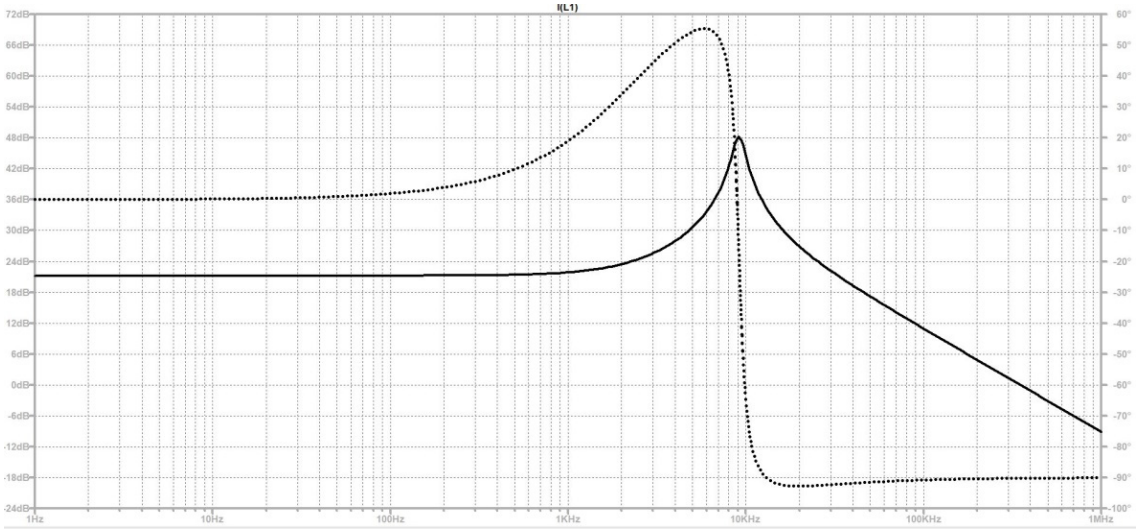


**Figure 23.** The $G_{id}$ of a non-ideal boost converter from the switch model.

## 9. Conclusions

The main aim of this work was to compare the differences between non-ideal boost and non-ideal synchronous boost converters for ACC. In this regard, a study on non-ideal boost and non-ideal synchronous boost converters operating in CCM was carried out. These converters were modeled using volt-sec and amp-sec balance equations. A simulation was performed using MATLAB/Simulink to observe the transients in the currents and voltages. Using a 'Mux' and a 'fcn' block, simulation was performed using a fixed-type solver. Using the SSA approach, $G_{id}$ was derived for the converters. The dynamics of these converters under various conditions were studied. It was found that the converters were highly stable in open loop. The $G_{id}$ for the non-ideal synchronous boost converter showed higher resonance than that for the non-ideal boost converter. However, the crossover frequency remained the same. The $G_{id}$ of the ideal boost and synchronous boost converters remained the same. With $R_c = 0$, the zeros of the ideal and non-ideal boost converters overlapped. However, this effect was not observed in synchronous converters.

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