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Improvement of DC Fault Current Limiting and Interrupting Operation of Hybrid DC Circuit Breaker Using Double Quench

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Abstract: In this paper, direct current (DC) fault current limiting and interrupting operation of hybrid DC circuit breaker (DCCB) using double quench, which consists of DCCB, a series resonance circuit, power electronic switch, surge arrestor, two separated current limiting reactor/resistor, and two superconducting elements, were suggested. The suggested hybrid DCCB can perform the interrupting operation after twice or once DC fault current limiting operation according to DC fault current amplitude. To verify the effective operation of the suggested hybrid DCCB, the modeling for the components of DCCB, the surge arrestor, and the SCE was carried out and its DC operational characteristics were analyzed. Through the analysis of the modeling results for the suggested hybrid DCCB, the suggested hybrid DCCB, the suggested hybrid DCCB, the suggested hybrid DCCB, the suggested hybrid DCCB were discussed.

Keywords: hybrid DC circuit breaker (DCCB); double quench; superconducting elements; DC fault current limiting and interrupting operation

1. Introduction

Recently, direct current (DC) grid, called as low voltage DC (LVDC), medium voltage DC (MVDC), or high voltage DC (HVDC) system, has been receiving attention due to the increase of DC load and DC distributed power source and thus the various protection devices for DC grid such as DC circuit breaker (DCCB) have been developed. One of the important technologies in DCCBs is that the increased DC current is to make rapid zero crossings. Another one is to effectively remove the arc in mechanic contact comprising the DCCB. To achieve these technologies in DCCB, the hybrid DCCBs or the modified DCCBs, which utilize the power electronic switches with higher ratings, have been introduced continuously [1–5].

Moreover, the DCCBs, which can achieve the fault current limiting operation shortly before the fault current interruption, have been suggested and the improvement of the DCCB's performance through the combination of the superconducting elements (SCEs) has been constantly reported [6–10].

In this paper, the hybrid DCCB using double quench of SCEs, which has a mechanical switch (MS), power electronic switch (PS), two SCEs, and two separated current limiting reactor/resistor (CLRs), were proposed and the effect of twice DC fault current limiting operations according to the amplitude of DC fault current on the interrupting operation of the DCCB was analyzed through the PSCAD/EMTDC (power system computer-aided design/electro-magnetic transient including direct current) simulation.

With the PSCAD/EMTDC modeling for the mathematical characteristic equation of each component, the double quench generation of the SCEs comprising the hybrid DCCB was confirmed to be contributed to the successful DC fault current interruption along with



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Copyright: © 2021 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (https:// creativecommons.org/licenses/by/ 4.0/). twice DC fault current limiting operation through the comparative analysis with the case of the hybrid DCCB without two SCEs and two separated CLRs.

2. Structure and Modeling of Hybrid Direct Current Circuit Breaker (DCCB) Using Double Quench

2.1. Structure of Hybrid Direct Current Circuit Breaker (DCCB) Using Double Quench

The structure of the hybrid DCCB using double quench consists of two CLRs and two SCEs as DC current limiting components, MS, LC series circuit and PS as DC current interrupting components, and surge arrestor (SA) as overvoltage prevention as shown in Figure 1. The series resonance circuit has a parallel connection with MS to induce zero current crossings in MS in case of the DC fault current occurrence. PS, connected in series the controller. The SCE₁ acts as both the fault detector and the initial DC fault current limiter. The quench occurrence in SCE_1 directly after the fault happens makes the CLR_1 act as the first fault current limiter through SCE₂. In case that the larger DC fault current flows into SCE_2 despite the quench occurrence of the SCE_1 , the quench in SCE_2 occurs sequentially and the second DC fault current limiting operation of the hybrid DCCB can be achieved. After the DC fault current limiting operation through single quench in SCE_1 or double quench in both SCE_1 and SCE_2 comprising the hybrid DCCB according to the amplitude of the DC fault current, the DC fault current interrupting operation through the MS is achieved by its opening operation and then, finally separated from the DC fault current path by the opening of PS. The SA pre-vents the over-voltage across the DCCB during the DC current limiting and the interrupting operation.



Figure 1. Structure of hybrid Direct Current (DC) circuit breaker using double quench; SCE: superconducting element; MS: mechanical switch; CLR: current limiting resistor/reactor; SA: surge arrestor; PS: power switch.

2.2. Modeling of Hybrid Direct Current Circuit Breaker (DCCB) Using Double Quench

To analyze the current limiting and the interrupting characteristics, the PSCAD/EMTDC modeling for the suggested hybrid DCCB using a double quench of two SCEs was carried out. MS, SCE, and SA were considered as the main modeling components.

For the MS's dynamic arc behavior, the arc conductance (GMS) was reflected into the PSCAD/EMTDC modeling from Mayr's arc model as expressed in Equation (1) and modeled to generate directly after the MS current (i_{MS}) exceeded 8 kA. In Equation (1), G_0 , Q_0 , and τ_a represent the conductance of insulation material between two conducting plates,

the heat energy, and the time constant of arc, respectively [11,12]. The resistance of each SCE, which generates in case that the current in SCM (i_{SCM1} , i_{SCM2}) exceeds the critical current (I_{C1} , I_{C2}), was reflected into its PSCAD/EMTDC modeling with the resistance equation, represented in Equation (2). R_N and τ_b in Equation (2) express the normal resistance and time constant of SCE, respectively [13,14].

In addition, the PSCAD/EMTDC modeling for the SA was considered with the resistance of Equation (3) derived from its voltage and current relation with the breakdown voltage (V_B) and the nonlinear index (γ) [15]. The current in the MS (i_{MS}) directly after the DC fault occurrence can be obtained as Equation (5) from the second differential equation for the current of the MS (i_{MS}) as shown in Equation (4). In Equations (5) and (6), n and k represent the cycle number of the zero current point in the current of MS and the ratio of the voltage variation induced in the MS (Δv_{MS}) over the current variation of MS (Δi_{MS}), respectively.

$$G_{\rm MS}(t) = G_0 \times \exp\left(\int_{t_1}^t \frac{v_{\rm MS}(\lambda)i_{\rm MS}(\lambda)}{Q_0} d\lambda\right) \times \exp\left(-\frac{t}{\tau_a}\right) \tag{1}$$

$$R_{\rm SCE}(t) = R_{\rm N} \times \sqrt{1 - \exp\left(-\frac{t}{\tau_{\rm b}}\right)} \tag{2}$$

$$R_{\rm SA}(t) = V_{\rm B}^{\gamma} v_{\rm SA}(t)^{1-\gamma} \tag{3}$$

$$\frac{d^2 i_{\rm MS}(t)}{dt^2} + \frac{k}{L} \frac{d i_{\rm MS}(t)}{dt} + \frac{1}{LC} i_{\rm MS}(t) = \frac{1}{LC} I_{\rm CB}$$
(4)

$$i_{\rm MS}(t) = I_{\rm CB} \left[1 - \frac{e^{-\alpha \frac{2n-1}{2}\pi}}{\sin \beta \frac{2n-1}{2}\pi} e^{\alpha t} \sin \beta t \right]$$
(5)

$$\alpha = -\frac{k}{2L} \qquad \beta = \sqrt{\frac{1}{LC} - \left(\frac{k}{2L}\right)^2} \tag{6}$$

To verify the merits of the suggested hybrid DCCB using double quench, the simulated DC system was constructed as shown in Figure 2. The specifications for the simulated DC system were listed in Table 1. For DC short-circuit simulation with different amplitude of DC fault current, SW_{21} or SW_{22} was closed individually for 0.01 s for larger DC fault current and lower DC fault current after SW_1 was closed. The values of the parameters, described in the modeling of MS, SCE_1 , SCE_2 , and SA comprising the hybrid DCCB, were listed in Table 2 together with CLR₁, CLR₂, and series resonance circuit.



Figure 2. Simulated DC system for the operation of hybrid DCCB using double quench; Z_1 : line impedance; Z_L : load impedance; R_{21} : small DC fault resistance; R_{22} : large DC fault resistance.

DC System Circuit	Parameters	Value	Unit
DC source voltage	V _{DC}	15	kV
Line impedance (Z_1)	R ₁	0.01	Ω
	X_1	0.377	Ω
Load impedance (Z _L)	R _L	0.6	Ω
Small DC Fault Resistance	R ₂₁	0.6	Ω
Large DC Fault Resistance	R ₂₂	1.2	Ω

Table 1. Specification of DC System for DC Short-Circuit Tests.

Table 2. Design Parameters of Components Comprising Hybrid DCCB using Double Quench.

Components	Description	Parameters	Value	Unit	
MS	Conductance of insulation material	G ₀	$5.5 imes10^{15}$	-	
	Heat energy	Q_0	15	-	
	Time constant of arc	$ au_{a}$	1	-	
Series Resonance	Series inductance	L	87	μH	
Circuit	Series capacitance	С	3.33	μF	
SCE1	Normal resistance of SCE ₁	<i>R</i> _{N1}	1	Ω	
	Normal resistance of SCE ₂	R_{N2}	20	Ω	
SCE_2	Time constant of $SCE_1 \& SCE_2$	$ au_{ m b}$	0.1	-	
	Critical current of SCE_1	I_{C1}	5	kA	
	Critical current of SCE ₂	I _{C2}	7	kA	
CLR ₁	Current limiting reactance	L _{CLR}	2	mH	
CLR ₂	Current limiting resistance	R _{CLR}	2	Ω	
SA	breakdown voltage	VB	20	1.37	
	nonlinear index	γ	8	ΚV	

3. Results and Discussion

The improvement of the DC current limiting and interrupting operations of the suggested hybrid DCCB was analyzed from the simulation results for the larger DC fault current and the lower DC fault current situations.

Figure 3 shows the DC fault current limiting and interrupting operation of the suggested hybrid DCCB in case of the larger DC fault current occurrence. With the arc conductance in Equation (1) calculated using the voltage and the current of the MS, the voltage ($v_{\rm MS}$) and the current ($i_{\rm MS}$) of the MS were displayed in Figure 3b,c, respectively.

The fault starting time is indicated with t_1 in Figure 3. After t_1 , the time for the current of the SCE₁ (i_{SCE1}) to arrive at the critical current (I_{C1}) is marked with t_{C1} . After that time, the voltage of the MS sharply increases and the arc starting time is notated with t_{Arc} as seen in Figure 3b. As t_{Arc} , the current of the MS (i_{MS}) as seen in Figure 3c increases with the parabola form together with the resonance due to the LC series resonance circuit. Though the increase of the MS's current, the current in the SCE₁ (i_{SCE1}) due to its quench occurrence decreases, which makes the current in the SCE₂ (i_{SCE2}) or the CLR₁ (i_{CLR1}) increase on the other way. The increased current of the SCE₂ is observed to approach its critical current (I_{C2}) at t_{C2} . The decrease of the SCE₂'s current due to its quench occurrence again causes the current of the CLR₂ to be increased as seen in Figure 3a. Through twice or double quench occurrence in two SCEs and the series resonance, the current of the MS (i_{MS}) smoothly increases with the series resonance frequency due to the series LC circuit and then, approaches the zero current point at t_{SA} . On the other hand, the voltage of the DCCB (v_{DCCB}) sharply starts to increase at the moment of the zero current point and exceeds the breaking voltage (V_B) as seen in Figure 3b. However, the operation of the surge arrestor, as seen in the current occurrence of the surge



arrestor (i_{SA}) from Figure 3a, is confirmed to be contributed to suppressing the overvoltage of the DCCB.

Figure 3. Cont.



Figure 3. DC fault current limiting and interrupting operation waveforms of the hybrid DCCB using double quench in case of the larger DC fault current occurrence. (a) Current waveforms of DCCB, SCE₁, SCE₂, CLR₁, CLR₂ and SA (i_{DCCB} , i_{SCE1} , i_{SCE2} , i_{CLR1} , i_{CLR2} , i_{SA}). (b) Voltage waveforms of DCCB, MS, SCE₁, SCE₂, CLR₁ (v_{DCCB} , v_{MS} , v_{SCE1} , v_{SCE2} , v_{CLR1}). (c) DC current limiting and interrupting waveforms of DCCB, MS, LC, SCE₁ (i_{DCCB} , i_{MS} , i_{LC} , i_{SCE1}).

After the MS opens, the current of the SCM₁ (i_{SCE1}) starts to decrease with the amplitude of the resonance frequency due to the series LC resonance circuit and then, finally approaches to zero value at t_2 . In the end, the current of DCCB of the hybrid DCCB reaches zero value at t_3 as seen in Figure 3a.

For the comparative analysis with the hybrid DCCB without the SCMs and the CLRs, the currents of the DCCB and the MS ($i_{DCCB}^{w/o}$, $i_{MS}^{w/o}$) and the voltage of the MS ($v_{MS}^{w/o}$) were included in Figure 3. As seen in Figure 3, the MS in the case of the hybrid DCCB without the SCMs and the CLRs can be seen to be not open or fail to be open.

In the case of the lower DC fault current occurrence, which was simulated by closing SW₂₂ after SW₁ was closed as shown in Figure 2, the DC fault current limiting and interrupting operations of the suggested hybrid DCCB were displayed in Figure 4. Both the time (t_{C1}) for the current of the SCE₁ (i_{SCE1}) to arrive at the critical current (I_{C1}) and the time (t_{Arc}) for the voltage of the MS (v_{MS}) rapidly to start to increase is seen to be a little longer compared to the larger DC fault current occurrence as analyzed in Figure 3. Furthermore, the second fault current limiting operation did not happen since the current of the SCE₂ (i_{SCE2}) did not exceed its critical current (I_{C2}) as seen in Figure 4a. After t_{Arc} , the current in the MS (i_{MC}), which kept zero value before t_{Arc} , starts to increase with the resonance frequency of series LC circuit and then, approaches zero point at t_{SA} by the increase of the current (i_{LC}) in series LC circuit as seen in Figure 4c. Simultaneously, as soon as the current of the MS approaches zero point at t_{SA} , the voltage of the MS (v_{MS}), as shown in Figure 4b, exceeds the breaking voltage (V_B), and then, the current of the surge arrestor (i_{SA}) starts to flow as displayed in Figure 4a.

After t_{SA} , the zero current time of the SCM₁ (t_2) and the zero current time of the DCCB (t_3) were accompanied. This time t_3 was called the complete opening time.

Due to the lower DC fault current, the voltage and current levels in components comprising the hybrid DCCB as analyzed in Figure 4 were observed to have a small scale compared to the larger DC fault current. Therefore, the complete opening time (t_3) in the case of the lower DC fault current occurrence seems to be shorter than the case of the larger DC fault current. To compare the hybrid DCCB without two SCMs and two separated CLRs, the DC fault current limiting and interrupting waveforms of the suggested hybrid DCCB were displayed in Figure 5 together. In the case of the larger DC fault current occurrence, as shown in Figure 5a, the complete opening operation at t_3 after the zero current in the MS through the series resonance of LC together with the twice DC fault current limiting operations of two SCMs was achieved. On the other hand, the DC fault current interrupting operation ($i_{MS}^{w/o}$, $i_{DCCB}^{w/o}$) in the case of the hybrid DCCB without two SCMs was not achieved.

To compare the hybrid DCCB without two SCMs and two separated CLRs, the DC fault current limiting and interrupting waveforms of the suggested hybrid DCCB were displayed in Figure 5 together. In the case of the larger DC fault current occurrence, as shown in Figure 5a, the complete opening operation at t₃ after the zero current in the MS through the series resonance of LC together with the twice DC fault current limiting operations of two SCMs was achieved. On the other hand, the DC fault current interrupting operation ($i_{MS}^{w/o}$, $i_{DCCB}^{w/o}$) in case the hybrid DCCB without two SCMs and two CLRs was not achieved.



Figure 4. Cont.



Figure 4. DC fault current limiting and interrupting operation waveforms of the hybrid DCCB using double quench in case of the lower DC fault current occurrence. (a) Current waveforms of DCCB, SCE₁ SCE₂, CLR₁, CLR₂ and SA (i_{DCCB} , i_{SCE1} , i_{SCE2} , i_{CLR1} , i_{CLR2} , i_{SA}). (b) Voltage waveforms of DCCB, MS, SCE₁, SCE₂, CLR₁ (v_{DCCB} , v_{MS} , v_{SCE1} , v_{SCE2} , v_{CLR1}). (c) DC current limiting and interrupting waveforms of DCCB, MS, LC, SCE₁ (i_{DCCB} , i_{MS} , i_{LC} , i_{SCE1}).



Figure 5. Comparative waveforms of DC fault current limiting and interrupting operation of the hybrid DCCB using double quench for the case without the hybrid DCCB. (a) In case of the larger DC fault current occurrence, (b) In case of the lower DC fault current occurrence.

Unlike the case of the larger DC fault current occurrence, the DC fault current interrupting operation ($i_{MS}^{w/o}$, $i_{DCCB}^{w/o}$) without two SCMs and two CLRs in case of the lower DC fault current occurrence was observed to succeed as shown in Figure 5b, which was made to zero current by the series LC resonance. However, it is compared to take a longer time compared to the case of the hybrid DCCB using the double quench although the quench in only SCE₁ comprising the hybrid DCCB using the double quench due to the lower DC fault current occurred.

4. Conclusions

In this paper, the hybrid DC circuit breaker using double quench was suggested and its DC fault current limiting and interrupting operation according to DC fault current amplitude was analyzed through the PSCAD/EMTDC modeling for its components. In the case of the larger DC fault current occurrence, the DC fault current interrupting operation through zero current generation in the MS using the series resonance together with the twice DC fault current limiting operations of two SCMs was successively achieved. On the other hand, the DC fault current interrupting operation in case with the hybrid DCCB without two SCMs and two CLRs was not achieved. In case of lower DC fault current occurrence, the DC fault current interrupting operation of the suggested hybrid DCCB was also made through once DC fault current limiting operation. However, the opening time was shorter than the case of the larger DC fault current.

In the future, the studies considering the application of the suggested hybrid DCCB into the multi-terminal MVDC system, which requires several DCCBs with different capacities, will be in progress.

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