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DC Solid-State Circuit Breakers with Two-Winding Coupled Inductor for DC Microgrid

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Abstract: Ensuring a protection scheme in a DC distribution system is more difficult to achieve against pole-to-ground faults than in AC distribution system because of the absence of zero crossing points and low line impedance. To complement the major obstacle of limiting the fault current, several compositions have been proposed related to mechanical switching and solid-state switching. Among them, solid-state circuit breakers (SSCBs) are considered to be a possible solution to limit fast fault current. However, they may cause problems in circuit complexity, reliability, and cost-related troubles because of the use of multiple power semiconductor devices and additional circuit configuration to commutate the current. This paper proposes a SSCB with a coupled inductor (SSCB-CI) that has a symmetrical configuration. The circuit is comprised of passive components like commutation capacitors, a CI, and damping resistors. Thus, the proposed SSCB-CI offers the advantages of a simple circuit configuration and fewer utilized power semiconductor devices than the other typical SSCBs in the DC microgrid. For the analysis, six operation states are described for the voltage across the main switches and fault current. The effectiveness of the SSCB-CI against the short-circuit fault is proved via simulation and experimental results in a lab-scale prototype.

Keywords: solid-state DC circuit breaker; coupled inductor; pole-to-ground fault protection; DC microgrid protection

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1. Introduction

In recent years, DC power systems have come to the fore in microgrid and distribution systems, configuring DC-based renewable energy such as PV and battery charging stations [1,2]. These features have prompted DC applications in shipboards, airplanes, telecommunication systems, and data centers [3–5]. However, fault detection and isolation to a fault area are still major technical barriers of DC-based systems. In a distribution network, fault protection against short circuits has difficulties. In AC distribution, the fault current is limited by high line impedance at a commercial frequency with zero crossing points. However, in DC distribution, the absence of zero crossing points and lower line impedances compared with AC distribution leads to a high fault current magnitude under pole-to-ground short-circuit faults [6]. Moreover, the fault current has become an important issue in energy storage systems, which has motivated steady research into this area [7,8].

So far, some challenges have arisen for limiting the fault current and reducing the clearing time on the fault area. In order to ensure protection against fault accidents, mechanical CB and solid-state CB are considered principally. Mechanical CB has the advantages of a lower conduction loss, but it has a breaking time of about several tens of milli seconds [9,10]. Thus, the solid-state circuit breakers (SSCBs) with a fast response time have become a solution for the quick isolation of a fault section.

SSCBs have been proposed in many studies to verify the validity of fault isolation effectively, and they have mainly dealt with the requirements of a fast fault clearing time or noticeable circuit configuration using several kinds of power semiconductor devices.

In order to achieve affordable circuit configuration and beneficial effects, the principally considered methods are circuit configuration based on power semiconductor devices or artificially commutating the fault current [11,12].

In the literature [11], SCR-based SSCBs have been proposed, with the main goal of reducing the number of inductors compared with the bi-directional SSCB in [12]. A three-winding transformer is adopted with a number of power semiconductor devices, two thyristors, and two diodes. However, in this circuit configuration, complex circuit configuration is caused by several components. Moreover, the proposed method needs an external circuit to commutate SCRs. Therefore, SCR-based SSCB still has a limitation in the aspect of a simple circuit configuration.

Another solution with SSCBs based on silicon carbide metal-oxide-semiconductor field-effect transistors (SiC MOSFETs) has been proposed [13]. Si power devices have some notable advantages compared with SCR in terms of their superior material properties, such as their thermal conductivity, energy gap, and conduction losses. However, SiC-based SSCB is not yet cost-effective. Therefore, a circuit configuration with SiC may increase the circuit cost.

As another way to insert a commutation path with passive components, LC resonance circuits have been considered [14,15]. LC resonance is a basic solution to create zero crossing points, and is one solution to limit or cut off the fault current. In these studies, a capacitor and an inductor are inserted in series to transform the fault current path into the LC circuit, so that the DC current wave can be changed into a sine wave passing by zero crossing points. However, one drawback is the need for an additional circuit to pre-charge the commutation capacitor, which increases the complexity of the circuit configuration of the SSCB. In addition, the increased number of inductors causes an increase in the volume of the overall topology. As a way to insert inductance into the circuit, a coupled inductor (CI) is considered. CI is a solution for the optimization of two or more inductors by one magnetic component [16,17]. Therefore, it has the advantage of a simple configuration with a bi-directional energy flow and fault interruption [18–20].

This paper presents a novel DC SSCB circuit without additional power semiconductor devices, except for a main switch that complements the aforementioned problems. With the traditional circuit configuration in SSCBs, the reported topologies rely on multiple power semiconductor devices that are employed to block an instantaneous short circuit current and a voltage spike. To come up with an effective method considering the drawbacks due to the complex circuit configuration and cost-related problems, several passive components, capacitors, resistors, and two-winding coupled-inductors are employed without semiconductor devices. The circuit configuration is combined based on the basic idea of a series of LC resonance and damping resistors. Capacitors are inserted to generate an alternate commutating current in the short circuit fault. A detailed explanation of the operation states and circuit configuration is presented in Section 2. Sections 3 and 4 illustrate the results about the simulated fault interruption in a lab-scale prototype. Finally, the conclusion and necessary improvements of SSCB-CI are discussed in Section 5.

2. Operation of the SSCB-CI

The circuit configuration of the SSCB-CI is illustrated in Figure 1, where the overall current flow and across voltages are denoted. The proposed circuit is functionally divided into several parts. Except for the main switches, SW_{main}, power semiconductor devices to block the fault current are not needed. The two-winding CI is given to commutate the sinusoidal current through zero crossing points from fault section to the secondary winding. In addition, CI is utilized to insert the commutation path into each of the windings. The inserted capacitors, C_{pri} and C_{sec}, generate the sinusoidal currents. The main function of the series resistances, R_{seri_p} and R_{seri_s}, is to damp the transient oscillation of the fault current and to limit the magnitude of the current to charge C_{pri} and C_{sec}. The parallel resistors, R_{para_p} and R_{para_s}, are linked so as to block an instantaneous voltage spike of the winding voltages, V_{pri} and V_{sec}.

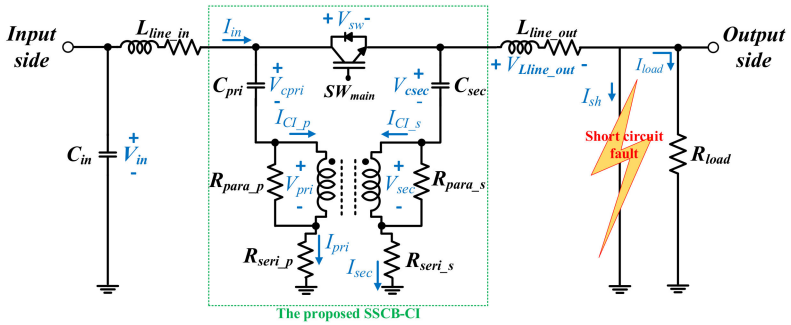

Figure 1. Circuit configuration of the proposed solid-state circuit breakers (SSCBs).

The proposed circuit configuration with a symmetrical structure has the advantage of responding to a short-circuit fault on both the input side and the load side [21]. Designing a CI is an important issue. A self-inductance can be designed by a turns-ratio, and the leakage inductance can be designed by a coupling coefficient, *k*. Previous studies on the use of a two-winding CI have confirmed that the higher the value of *k*, the better the dynamic response of the inductor current [22]. Thus, a *k* with a high value is also considered in the proposed circuit configuration. The overall operation states of the SSCB-CI are shown in Figure 2. In this figure, each state from States 1 to 3 represents the current flow when the circuit breaker is initially operated in the steady state of the DC microgrid. From States 4 to 6, these states represent the current flow under the pole-to-ground fault of the load side. The key waveforms in each of the parts for the overall operation states are shown in Figure 3. Detailed explanations depending on each state are as follows:

(i) State 1: Pre-charge of commutation capacitor in the primary side (t_0~t_1)

This state is occurred to charge C_{pri} under steady state of the DC microgrid. In Figure 2a, this state means the initial state of the SSCB-CI, and occurs when SW_{main} turns off at the normality of the input voltage V_{in}. During this state, C_{pri} is charged. The initial condition of I_{sh}, I_{pri}, and I_{in} can be expressed as Equation (1).

$$I_{sh} = 0\ ,\ I_{pri} = 0\ ,\ I_{sec} = 0\ and\ \frac{di_{in}}{dt} = 0 \tag{1}$$

The voltages across capacitors V_{Cpri} is similar to V_{in}. After charging, the primary winding current I_{CI_P} is removed, thereby eliminating any unexpected power losses by R_{para_p} and R_{seri_p} in the stationary state.

(ii) State 2: Pre-charge of commutation capacitor in the secondary side (t_1~t_2)

After State 1, if SW_{main} turns on, C_{sec} is charged, and it can be shown as in Figure 2b. The current flow in the secondary winding is similar as that in State 1, but C_{pri} is discharged temporarily because of the voltage fluctuation of the secondary winding voltage V_{pri}. After that, C_{pri} is charged again as V_{in}, where the input current and the input voltage can be expressed as Equations (2) and (3), respectively.

$$i_{in} = i_{pri} + i_{sec} + i_{out} = i_{pri} + i_{sec} + i_{sh} + i_{load} \tag{2}$$

$$v_{in} = \frac{1}{C_{pri}} \int i_{pri} \cdot dt + v_{Cpri}(t_1) - kv_{\sec} + \left(1 - k^2\right) L \frac{di_{CI\_p}}{dt} + R_{seri\_p} i_{pri} \tag{3}$$

where L is the self-inductance of each winding, L_p and L_s, where two self-inductances are considered herein to have equal inductance. That is, the CI is modeled as an ideal transformer, which has a turns ratio of 1:1, the same magnetizing inductor, and the same leakage inductor. In addition, the winding resistance is neglected for ease of understanding. Therefore,

$$L_p = L_s = L \tag{4}$$

(iii) State 3: Stationary (t_2~t_3)

This state means the interval between the capacitor charging state and time interval state, as shown in Figure 2c. SW_{main} is continuously turned on and the input current I_{in} flows to the load as I_{load}.

$$I_{in} \approx I_{load} \tag{5}$$

Until a line-to-ground short-circuit fault, the SSCB-CI stays. At this state, I_{CP_P} and I_{CP_S} are removed as zero. In addition, the voltages across C_{pri} and C_{sec} are regarded as equal to V_{in}.

(iv) State 4: Time interval (t_3~t_4)

Figure 2d indicates the voltage and current rise after the line-to-ground fault. In this state, the instantaneous fault current is generated because of the short-circuit fault at the load side. However, SW_{main} is not turned off immediately because of the short interval time from the trip delay and fault detection. Therefore, I_{in} and I_{sh} are increased simultaneously. During this state, I_{sh} can be expressed as Equation (6). In this equation, only inductance, L_{line_in} and L_{line_out}, as the line impedance are considered for an easy analysis.

$$i_{sh}(t_4) \approx \frac{1}{L_{line\_in} + L_{line\_out}} \int \{v_{in} - (R_{line\_in} + R_{line\_out}) i_{in}\} dt + i_{Load}(t_3) \; where, \; i_{Load}(t_3) \approx 0 \tag{6}$$

where R_{line_in} and R_{ine_out} are the mean resistor components of each line impedance.

(v) State 5: Block and commutating fault current (t_4~t_5)

Figure 2e shows the commutating fault current flow. When the detected level of I_{in} is exceeded, this state occurs, and consequently SW_{main} is turned off. The fault current in State 5 can be assumed using Equation (7).

$$i_{sh}(t_{state5}) = \frac{V_{in}}{L_{line\_out}\omega_d} e^{-\alpha t} \sin \omega_d t + i_{sh}(t_4) \; where, \; \omega_d = \frac{\sqrt{4L_{line\_out}C_{\sec} - \left\{(R_{para\_s} + R_{seri\_s})C_{\sec}\right\}^2}}{2L_{line\_out}C} \tag{7}$$

where α and ω_d mean the damping ratio and the resonant frequency by L_{line_out} and C_{sec}, respectively. Consequentially, the larger the resistance value, the larger the damping ratio.

After I_{sh} reaches the peak level, SW_{main} is stressed to more than V_{in}, namely a blocking voltage. Where, V_{sw} at State 5 can be expressed as follows:

$$V_{L\_line\_out}(t_{state5}) = \frac{V_{in}}{\omega_d} e^{-\alpha t}(-\alpha \sin \omega_d t + \omega_d \cos \omega_d t) \; Where, \; \alpha = \frac{R_{para\_s} + R_{seri\_s}}{2L_{line\_out}} \tag{8}$$

$$V_{sw}(t_{state5}) = V_{in} - V_{L\_line\_out}(t) = V_{in}\left\{1 - \frac{1}{\omega_d} e^{-\alpha t}(-\alpha \sin \omega_d t + \omega_d \cos \omega_d t)\right\} \tag{9}$$

After I_{sh} reaches the peak level, SW_{main} is stressed as V_{SW_max}, namely a blocking voltage, as Equations (10) and (11).

$$t_{\max} = \frac{1}{\omega_d} \arctan\left(\frac{2\alpha}{\frac{\alpha^2}{\omega_d} - \omega_d}\right) + \frac{\pi}{\omega_d} \tag{10}$$

$$V_{SW\_\max} = V_{SW}(t_{\max}) \tag{11}$$

After I_{sh} reaches the peak level, SW_{main} is stressed as V_{SW_max}, namely a blocking voltage. During this state, I_{sh} flows through the secondary winding by discharging the capacitor energy of C_{pri} and C_{sec}. As C_{sec} discharges, V_{Cpri} and V_{Csec} oscillate momentary for a few micro seconds, and then become stable. As a result, an induced energy to the primary winding decreases I_{sh}. As a result of the series resonance configuration, the current waveforms in the SSCB-CI circuit are produced as a sinusoidal current that has zero crossing points and is damped by R_{seri_p} and R_{seri_s}.

(vi) State 6: Protection (t_5~t_6)

The final state is the isolation of the load to V_{in} after a short-circuit fault. After blocking the fault current, C_{sec} is discharged. During this state, fault restoration should be adequately achieved. After fault restoration, the operation state is returned to State 1.

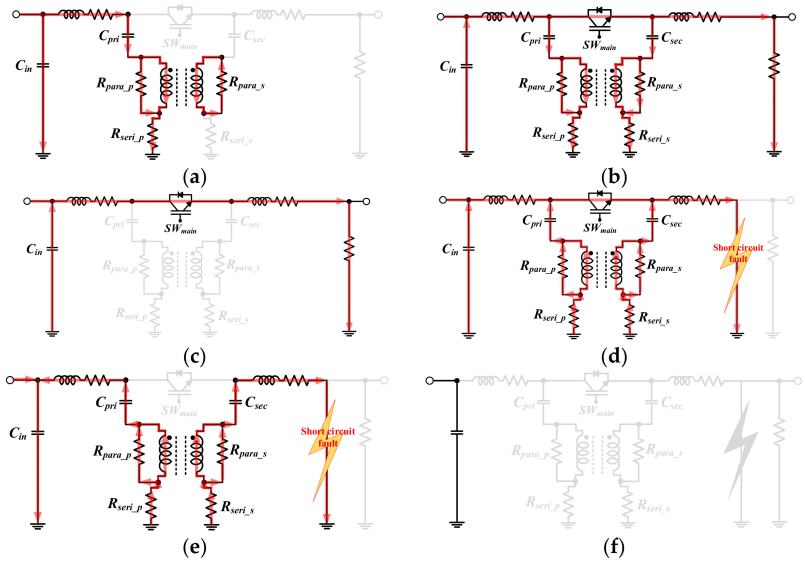

Figure 2. Operation states of SSCB-CI. (**a**) State 1: pre-charge of primary winding capacitor. (**b**) State 2: pre-charge of secondary winding capacitor. (**c**) State 3: stationary. (**d**) State 4: time interval. (**e**) State 5: block and commutation. (**f**) State 6: protection.

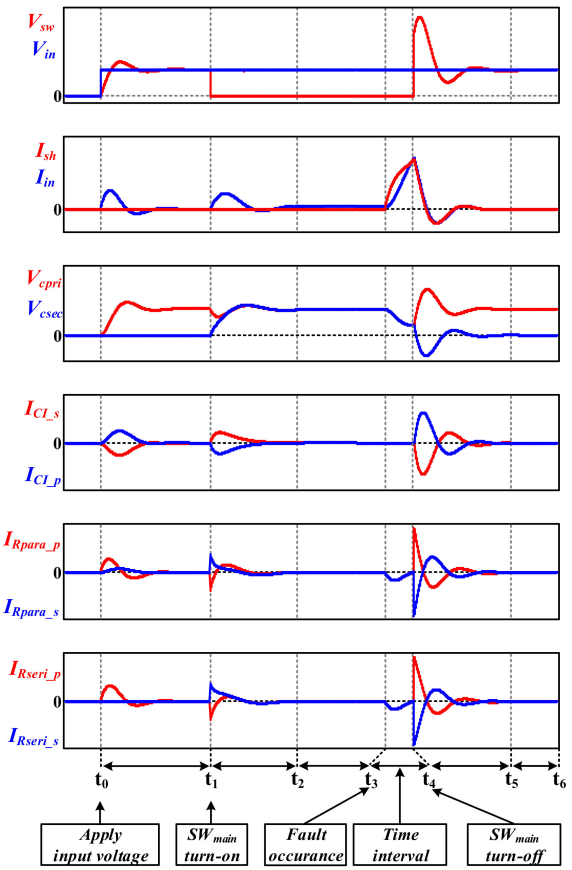

Figure 3. Key waveforms of the SSCB-CI under operation states.

3. Simulation Results

To verify the effectiveness under a pole-to-ground short-circuit fault, the SSCB-CI is simulated in PSIM. Detailed simulation parameters are listed in Table 1. As mentioned in Section 2, the parasitic components of the CI and the capacitors are neglected for ease of analysis. In addition, only the short-circuit fault on the load side is considered.

Table 1. Simulation parameters.

Symbol	Quantity	Value
V_{in}	Input voltage	100 V
R_{load}	Load resistor	32 Ω
C_{pri} and C_{sec}	Charging capacitor	10.5 μF
R_{para_p} *and* R_{para_s}	Parallel resistor	0.4 Ω
R_{seri_p} *and* R_{seri_s}	Series resistor	from 0.5 Ω to 3 Ω
L_{line_in} and L_{line_out}	Line impedance	66 μH
L	Self-inductance	580 μH
K	Coupling coefficient	0.96
L_{lk}	Leakage inductance	22 μH
t_2	The time at a short-circuit fault	at 2 ms
T_{delay}	Interval time	20 μs

Figure 4 shows representative waveforms under the operation states from stationary to protection, where R_{seri_p} and R_{seri_s} are considered as 1 Ω. After an interval time of 20 μs, V_{sw} is clamped to an adjustable voltage level of SW_{main}. At the same time, I_{in} is interrupted by the turn-off switch, and I_{sh} reaches the peak level. After starting to oscillate, I_{sh} is reduced gradually to zero.

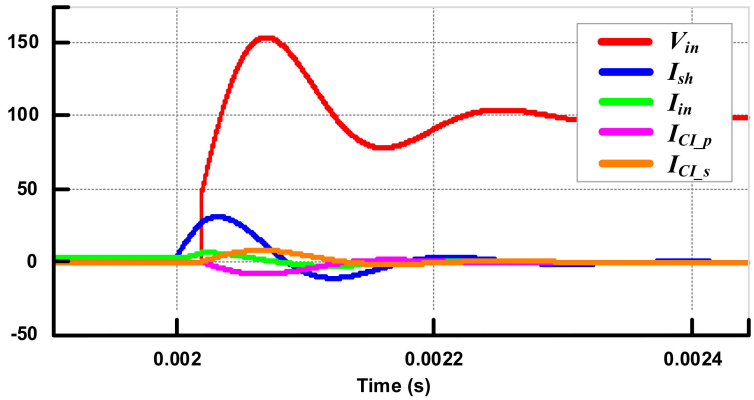

Figure 4. Key waveforms of simulation results.

Figure 5 shows the enlarged simulation waveforms of the commutation capacitors and each winding of CI. As shown in Figure 5a, V_{Cpri} does not become zero because of the continuous impressed input voltage. However, V_{Csec} becomes zero because of the turned-off SW_{main}. Figure 5b shows the current waveforms in the coupled inductor, which means the current reflected to each winding under a short circuit fault.

Figure 6 indicates the simulation waveforms under the different R_{seri_p} and R_{seri_s} values from 0.5 Ω to 3.0 Ω. Its waveforms show the better characteristic when R_{seri_p} and R_{seri_s} are selected as the high resistance ranges. However, this range selection causes more power burden of the resistors.

The peak of the voltage and current peak should be clamped within the allowable level of the main switch. In this paper, it is possible to explore an allowable level by selecting the value of R_{seri_p} and R_{seri_s}. In addition, the clearing time can be reduced correspondingly according to the resistance values. Figure 6 shows the output characteristic when R_{seri_p} and R_{seri_s} are set from 0.5 Ω to 3 Ω, respectively. Under the same simulation parameters

indicated in Table 1, the results reveal an increase in V_{sw} and I_{sh} as with the under-damping by the lower resistance value, and the clearing time is increased. On the contrary, V_{sw} and I_{sh} decrease as over-damping by a higher resistance value, and the clearing time is decreased. However, the over-damping condition has a disadvantage in that the power burden of R_{seri_s} to consume the fault current is increased, which increases the resistor size and rated power to circuit configuration. Therefore, the selection of an appropriate resistance value of R_{seri_p} and R_{seri_s} between under damping and critical damping should be explored. In another solution, the power burden of the resistor can be reduced by selecting a high k value.

Figure 7 shows the waveforms according to a k value over the range of 0.36 to 0.96 in accordance with the transient oscillation in a magnitude of I_{CI_P} and power burden of R_{para_s}. As the k value increases, the current magnitude increases, which decreases the power burden of R_{para_s}.

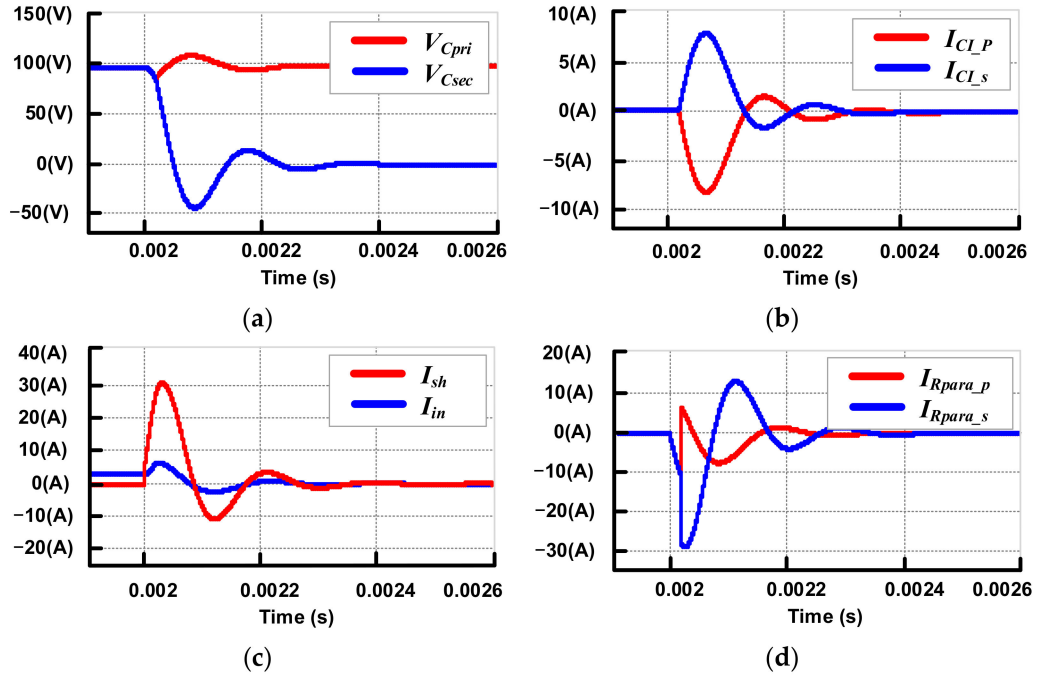

Figure 5. Simulation waveforms of commutation capacitors and the coupled inductor: (**a**) voltages across commutation capacitors, (**b**) coupled inductor currents, (**c**) currents of input and short-circuit fault, and (**d**) parallel resistor currents.

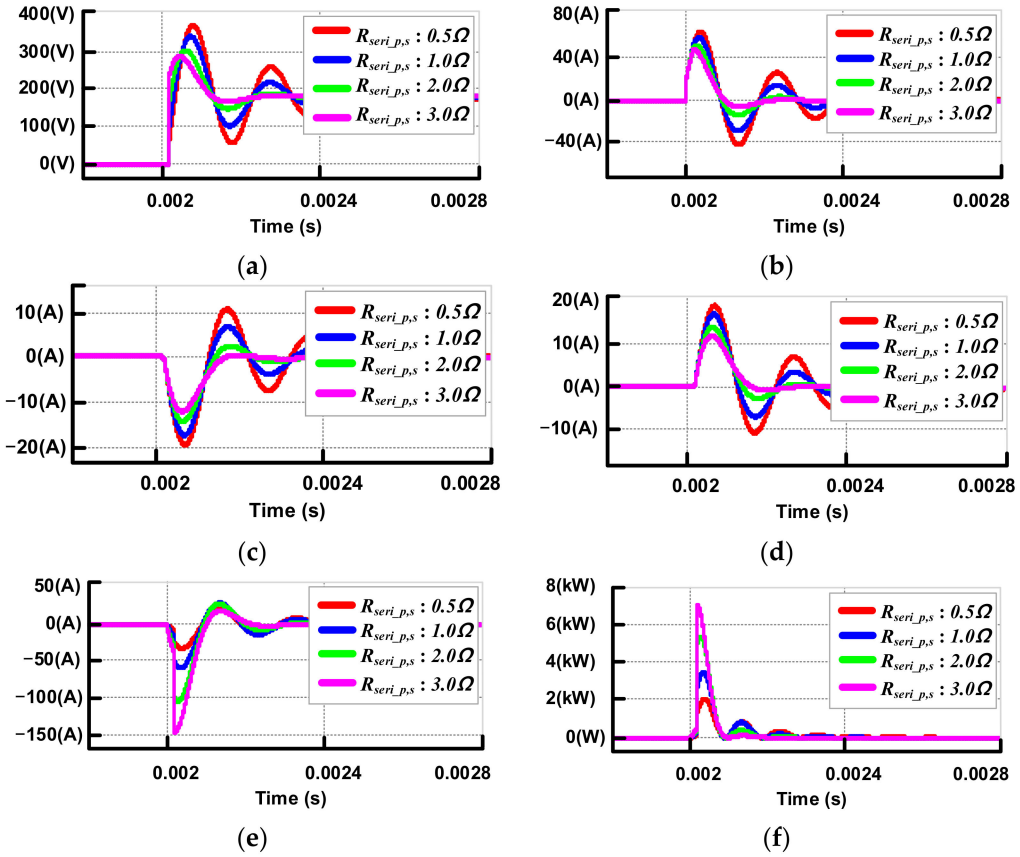

Figure 6. Simulation waveforms for different series resistor values: (**a**) voltage across main switch, (**b**) fault current, (**c**) current in primary winding, (**d**) current in secondary winding, (**e**) current of parallel resistor linked to secondary winding, and (**f**) power burden of series resistor linked to secondary winding.

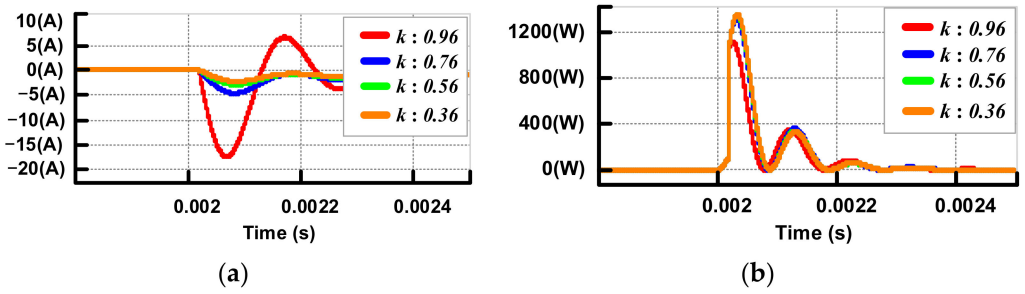

Figure 7. Simulation waveforms for different coupling coefficients: (**a**) current in secondary winding and (**b**) power burden of parallel resistor linked to secondary winding.

4. Experimental Results

Based on the simulation results, a lab-scale prototype was built in order to verify the performance of the proposed SSCB-CI. The test conditions and detailed parameters of the CI are considered in Tables 2 and 3, respectively, where the core shape was selected as the ferrite PQ core. In this paper, the fault detection condition was regarded as being when the MCU detects the input current above the limit current level. Specifications of the meas-urement sensors and instruments for experiment is indicated in Table 4. Where, the pro-totype SSCB-CI is composed of a FF150R12RT4 IGBT module, three PMC 700 V/5 μF ca-pacitors in parallel, and DSP TMS320F28335, where the ADC frequency is set as 40 kHz.

Table 2. Parameters of the experimental conditions.

Symbol	Quantity	Value
V_{in}	Input voltage	100 V
Z_{line_in} and Z_{line_out}	Line impedance	66 μH/0.2 Ω
C_{in}	Input capacitor	3200 μF
SW_{main}	Main switches	1200 V/150 A
C_{pri} and C_{sec}	Commutation capacitor	15 μF
R_{para_p} and R_{para_s}	Parallel resistors	0.4 Ω
R_{seri_p} and R_{seri_s}	Series resistors	1 Ω
T_{delay}	Time delay	about 190 μs
f_{ADC}	ADC frequency	40 kHz

Table 3. Parameters of the coupled inductor.

Symbol	Quantity	Value
k	Cou sharplypling coefficient	0.96
L	Self inductance	680 μH
L_m	Magnetizing inductance	652.8 μH
L_{lk}	Leakage inductance	27.2 μH

Table 4. Specifications of the measurement sensors and instruments.

Item	Model
Main switch	FF150R12RT4
Capacitor	PMC 700 V/μF
DC power supply	N8957APV
Voltage sensor	LV25P
Current sensor	LA100-P
DSP	TMS320F28335
Main switch	FF150R12RT4
Oscilloscope	Waverunner 44MXi

The overall testing configuration was built as shown in Figure 8a,b, and shows the prototype SSCB-CI configuration, which consists of an IGBT module, a gate driver, an MCU board, capacitors, and a CI.

The detailed short circuit test setup and overall configuration of the main components were designed as shown in Figure 9, where the sensing parts of the current and voltage value are indicated in red.

The sequence for the short circuit scheme is as follows: the input capacitor C_{in} is charged in advance by an AC/DC power supply under constant voltage constant current (CVCC) mode at 100 V via input from a side blocking diode, D, which has the role of blocking the inverse current to the power supply. After that, the SSCB-CI was operated in State 1. In order to force the pole-to-ground short-circuit fault, MCCB was turned on. Under this condition, there was a time delay of about 190 μs. The microcontroller unit measured the main switch voltage and the current in order to decide the pole-to-ground fault condition. If the fluctuation range of V_{sw} and I_{in} is over a certain value, it is judged as a short circuit fault.

Figure 10 shows the overall test results of the SSCB-CI from the initial condition to State 6, where R_{seri_p} and R_{seri_s} are set as 1 Ω. Figure 10a indicates the major experiment results and enlarged waveforms at a condition of intended fault accident. In addition, Figure 10b shows the voltage waveforms and current waveform at State 1. Once the power supply is turned on, V_{Cpri} is charged, and V_{in} is blocked because SW_{main} is turned off. Therefore, V_{Csec} is sustained by zero. At this time, each current of R_{para_p} and R_{para_s} flows momentarily, as shown in Figure 10c. After SW_{main} turns on, V_{Csec} is charged as V_{in}. At this state, I_{in} starts to flows to the load. Figure 10e,f shows the resulting waveforms from

State 3 to State 6. In these figures, the waveforms show across voltages and commutating currents into main components of SSCB-CI circuit after a short-circuit fault. At the initial time of State 5, V_{sw} increases rapidly up to 1.5 times that of V_{in}. However, V_{sw} reduces to the input voltage value after the clearing time, like with State 5.

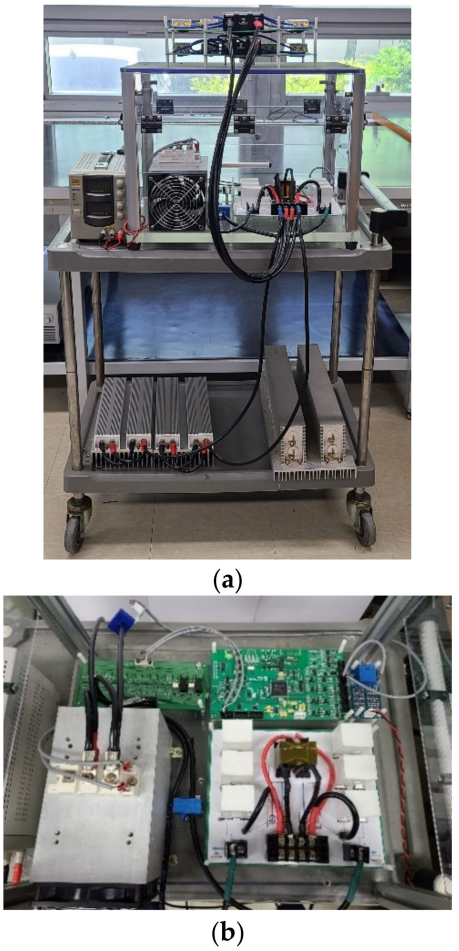

Figure 8. Experimental set-up of the SSCB-CI: (**a**) overall test circuit configuration and (**b**) inner structure.

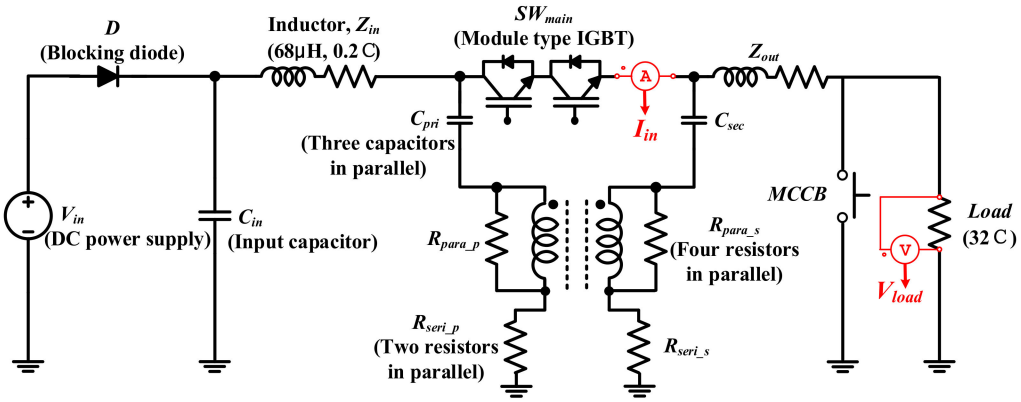

Figure 9. Test circuit schematic for the short-circuit scheme.

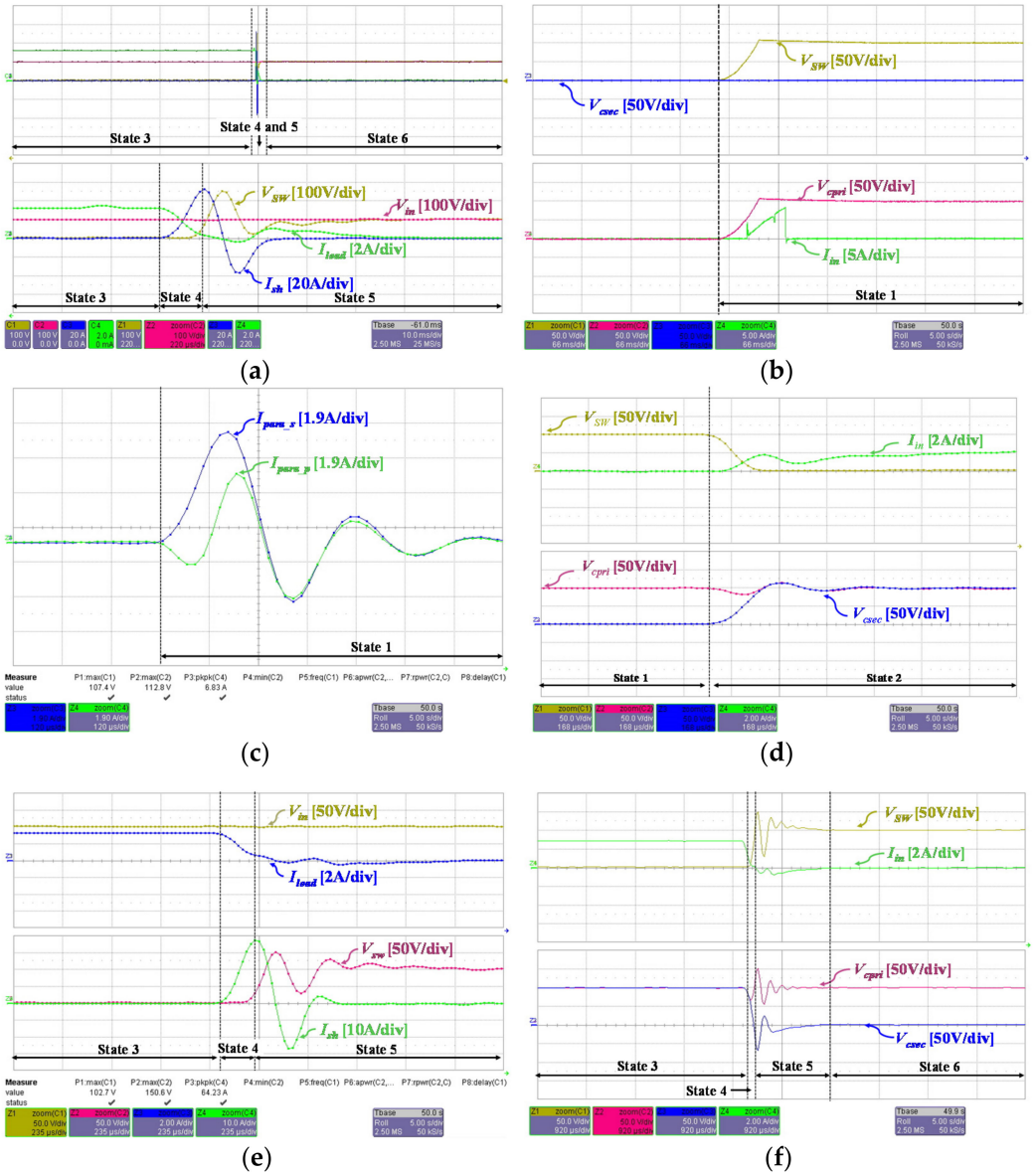

Figure 10. Experimental waveforms under overall operation states: (**a**) Key waveforms of experimental results; (**b**) switch, capacitor voltages, and input current under State 1; (**c**) parallel resistor current under State 1; (**d**) switch, capacitor voltage and input current under State 2; (**e**) input, switch voltage, load, and fault current under State 4; and (**f**) switch, capacitor voltage, and input current under States 4 and 5.

5. Conclusions

This paper explores the circuit configuration of a solid-state DC circuit breaker with CI and its applicability in short-circuit fault. In the circuit configuration, several passive components are considered for reducing the number of power semiconductor devices as a substitute for a complex circuit configuration in the early versions of the proposed SSCB. The operation states are analyzed in order to determine the overall voltage and current flow in the proposed circuit. The results indicate that the considered resistor value leads to a blocking voltage level of the main switches and clearing time of the fault current. The effectiveness of the SSCB-CI is verified through the simulation and experimental results. In the simulation results, it was found that the coupling coefficient affects the power burden of the parallel-linked resistors. In the experimental configuration, the circuit configuration of SSCB-CI as the small-scale prototype was implemented. The presented results demonstrate the functionality of blocking the fault current under the pole-to-ground

fault in the DC distribution. The rating power and blocking voltage of the devices used in the circuit are designed to be comparatively high. This intention caused problems regarding the bulky size and increased weight from the series or parallel configuration of the components. Considering the implemented prototype scale, future research needs to verify the effectiveness of the full-scale SSCB-CI for a practical DC microgrid and size optimization.

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