Article

Enhanced Boost Factor for Three-Level Quasi-Switched Boost T-Type Inverter

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Abstract: A new modulation strategy has been introduced in this paper in order to enhance the boost factor for the three-level quasi-switched boost T-type inverter (3L-qSBT^{2}I). Under this approach, the component rating of power devices is significantly decreased. Moreover, the use of a larger boost factor produces a smaller shoot-through current. This benefit leads to reducing the conduction loss significantly. Furthermore, the neutral voltage unbalance is also considered. The duty cycle of two active switches of a quasi-switched boost (qSB) network is redetermined based on actual capacitor voltages to recovery balance condition. Noted that the boost factor will not be affected by the proposed capacitor voltage balance strategy. The proposed method is taken into account to be compared with other previous studies. The operation principle and overall control strategy for this configuration are also detailed. The simulation and experiment are implemented with the help of PSIM software and laboratory prototype to demonstrate the accuracy of this strategy.

Keywords: third harmonic injection; single-stage inverter; shoot-through; three-level inverter; quasi-switched boost; T-type inverter

1. Introduction

Currently, a conventional three-level T-type inverter (3L-T^{2}I) is applied for low voltage applications due to its advantages of low conduction loss due to not using extra diodes compared to neutral point clamped inverter (NPCI) configuration or producing better output quality compared to two-level inverter [1,2]. This topology is recently adopted for many applications, especially photovoltaic (PV) systems and motor drives, etc. [3–5]. Nevertheless, the traditional 3L-T^{2}I produces a low value of AC output voltage in comparison to the input voltage of the inverter. Moreover, the conventional 3L-T^{2}I cannot accept the shoot-through (ST) state during operation because of leading to a short circuit at the DC input source.

Nowadays, impedance-source inverters have been considered as a solution to deal with the drawbacks of conventional inverters [6–8]. By using some passive components such as diodes, capacitors, and inductors in Z-source (ZS) circuit, the ZS inverter (ZSI) can behave as a buck-boost inverter with ST immunity. During operation, the ST state is utilized to belong to traditional vectors of the inverter to enhance the output voltage. The result is that the reliability is significantly improved. According to these advantages, several applications based on ZSI were discussed for the motor drive system, micro-grid connection, and PV applications [9,10]. Many traditional multilevel inverter topologies were considered to incorporate with the ZS network, such as NPCI and 3L-T^{2}I [11–14]. The works in [15,16] introduced a topology combining a single ZS network and 3L-T^{2}I. To ensure a three-level voltage operation, this combination uses a split DC input source. The neutral point of this source is utilized to belong to of ZS circuit to feed to the three-level inverter circuit. This configuration must use one extra diode to guarantee the symmetry of the impedance network. Instead of using full-ST (FST) state, this method used upper-ST (UST) and lower-ST(LST) states to conform to the buck-boost characteristic, which is added

within small vectors. In this strategy, the boost factor is equal to the traditional strategy in [8]. The work in [16] further proposed the neutral voltage balance strategy. However, this strategy required more dwell-time calculations and caused the boost factor effect.

To produce less component voltage rating and draw continuous input current, the quasi-Z-source (qZS) inverter (qZSI) has been presented in [17–22]. These topologies use the same components compared to ZSI, but these components were connected in another way. Like the ZS network, this type of impedance-source structure was considered to incorporate with the three-level inverter to provide multilevel characteristics [17–22]. In these approaches, two qZS circuits are connected to guarantee three-level operation at the output. However, the use of a large number of inductors and capacitors leads to increase volume and decrease power density of the inverter. Furthermore, buck-boost characteristics of the ZS/qZS inverters are only ensured by the ST duty ratio of the inverter branch, which decreases the flexibility of boost factor regulation. The literature [20] introduced the space-vector-modulation (SVM) method and the third harmonic injection scheme, which ensure the buck-boost operation by applying the UST and LST states. Similar to ZSI, these schemes required a split DC source to conduct UST and LST insertions. In [21,22], a novel SVM strategy was proposed to reduce the amplitude and the slew rate dv/dt of common-mode voltage (CMV). In this work, the neutral voltage unbalance problem was handled by adding one more extra small vector into the traditional switching sequence. However, the drew-time of additional small vectors is hardly determined. It produces the complexity of the calculation.

The quasi-switched boost (qSB) inverter (qSBI) was considered as an emerging topology that saves plenty of inductors and capacitors [23–30]. By installing one more active switch in the intermediate circuit, the boost factor of qSBI is so flexible to be controlled [16]. In this configuration, some advantages can be listed as high boost factor and voltage gain and good inductor current profile. These advantages lead to reducing voltage stresses on power devices and less capacitance requirement for passive components such as inductors and capacitors. The works of literature in [25–30] proposed the incorporation between qSB network and the multilevel inverter. In [25,26], the three-level NPCI was combined with two separated qSB networks. The 3L-T^{2}I was considered to combine with this type of impedance-source network in [27–30]. In [27–30], the qSB network utilized only one inductor and one DC input source, which saves one inductor and a split DC source compared to [25]. These works also proposed a new pulse-width modulation (PWM) strategy based on the phase shift carrier method to provide some benefits such as high voltage gain [21,27], common-mode voltage elimination [28], the capability of operating in normal and open-circuit faults [29], and small component rating. Similar to other types of single-stage buck-boost inverter, this configuration also utilizes the FST state to obtain buck-boost voltage capability, which is inserted within a zero vector to not affect the other voltage vectors. The closed-loop control is employed for capacitor voltage balance, which requires a larger time interval for neutral voltage recovery. The work in [30] adopted a corresponding small vector to balance the neutral voltage. However, this way introduced more CMV amplitude, which is generated by small vectors.

In this paper, a new PWM method is introduced, which improves the boost factor as well as voltage gain of this configuration. The neutral voltage balance is also considered in this paper. Unlike the methods in [16,22,30], where the neutral-voltage balance is ensured by corresponding small vectors of the inverter side, the active switches of the impedance-source network are utilized to balance neutral voltage. The duty cycle difference of these switches is determined based on actual capacitor voltages. This method brings benefits of reducing balancing recovery time and calculation complexity compared to [16,22,27]. The duty cycle of these switches and modulation index are considered to adjust the output voltage of the impedance-source circuit and AC output voltage. The operation modes, as well as the mathematical analysis, will be presented in this paper. Some simulation and experiment setups are used to confirm the accuracy of the proposed modulation method. The rest of this paper consists of four sections as follows. Section 2 introduces the operation

of the inverter and proposed PWM strategy. Section 3 presents a neutral voltage balancing scheme. In Section 4, a comparison study has been conducted to highlight the contribution of this scheme. In Section 5, the simulation and experimental results have been presented to confirm the accuracy of the introduced method. Section 6 presents a conclusion.

2. Proposed PWM Scheme for 3L-qSBT^{2}I

The 3L-qSBT^{2}I is established by an impedance-source network and a 3L-T^{2}I, as observed in Figure 1. The impedance-source network is constructed by two switches S_1 and S_2, four diodes D_1, D_2, D_3, and D_4, two capacitors C_1 and C_2, and one inductor L_B. The outputs of the intermediate circuit are "P", "O", and "N", which are used to ensure the three-level operation of the inverter. The three-phase resistive load is adopted to confirm the operation of the inverter with the proposed scheme, which is fed through a three-phase LC filter to guarantee the sinusoidal waveform of output load voltage with a low THD value, as depicted in Figure 1. The control scheme of this configuration is detailed in the rest of this section. The operating modes, steady-state analysis, and parameter selection are also presented.
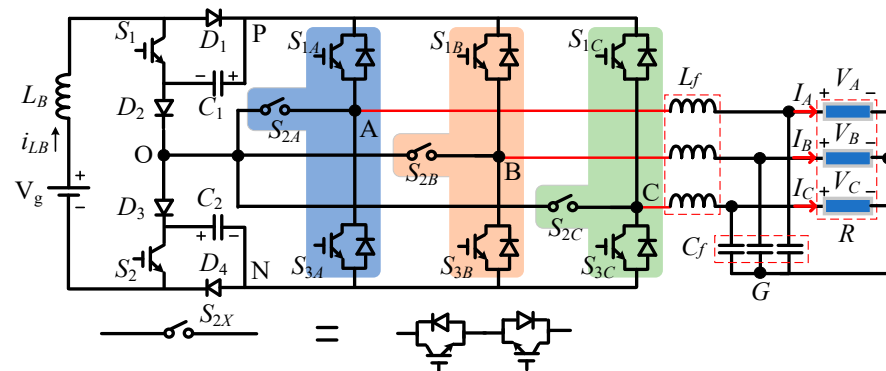

Figure 1. 3L-qSBT^{2}I topology [27].

2.1. PWM Signal Generation

The control method for the 3L-qSBT^{2}I is based on a phase-shift sinusoidal PWM scheme. The PWM control signal generation is divided into two cases: (1) inverter side PWM generation and (2) impedance-source switch PWM generation. For the inverter side, the six reference sinusoidal signals ($\pm v_a$, $\pm v_b$, and $\pm v_c$) are compared with a high-frequency triangle signal (V_{tri1}) to generate control signals for the inverter switches. Figure 2 shows the control signal generation for switches of phase A. In detail, switch S_{1A} is turned on when $-v_a < V_{tri1} < +v_a$, switch S$_{3A}$ is triggered on when $+v_a < V_{tri1} < -v_a$, and switch S$_{2A}$ is turned on when switches S_{1A} and S_{3A} are off. Signals V_{ST} and $-V_{ST}$ are used to create the ST signal denoted by yellow highlight in Figure 2. This ST state is generated by turned on all switches on the inverter side. In order not to affect the output voltage, the V_{ST} must not be smaller than the peak value of reference signals.

For the impedance source side, the triangle signal (V_{tri2}) is used, which is shifted 90 degrees compared to V_{tri1} to create the control signals for the active switches of the impedance-source network [27]. Signals V_{ST} and $-V_{ST}$ are also used with V_{tri2} to generate the ST signal of the intermediate network, which is denoted by green highlight, as shown in Figure 2. Furthermore, two control signals, V_{con1} and V_{con2}, are further used to enhance the duty ratio of S_1 and S_2, as illustrated in Figure 2.

2.2. Operating Modes

Based on the PWM strategy presented in Figure 2, the inverter can be operated under two modes which are ST and non-ST (NST) modes. These modes are divided into five modes, which are ST mode, NST mode 1, NST mode 2, NST mode 3, and NST mode 4,

as observed in Figure 3. To simplify, in non-ST modes, the inverter side is considered a current source, i_O. The on switches and forwarded diodes are shown in Table 1.
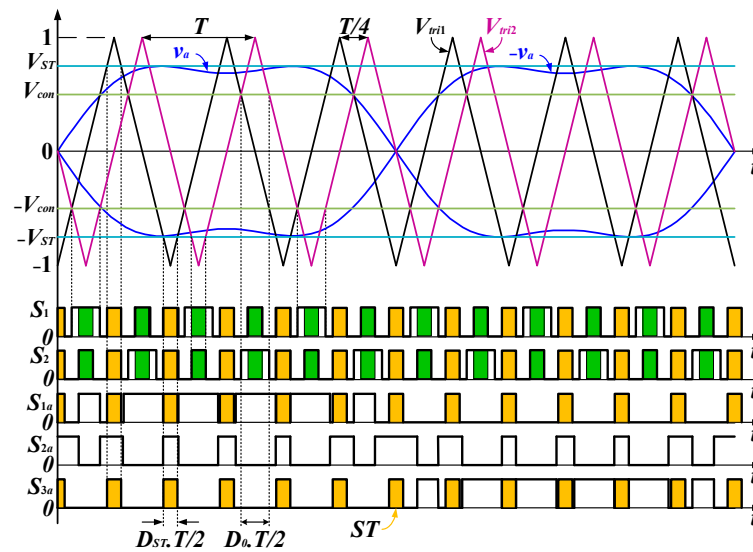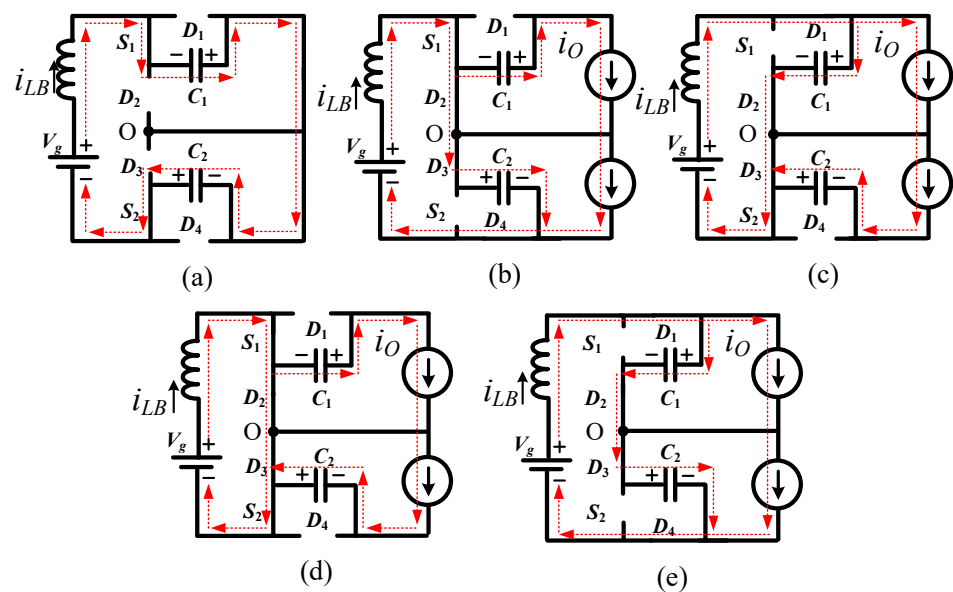

Figure 2. The proposed PWM scheme.

Figure 3. The modes of 3L-qSBT^{2}I: (**a**) ST mode, (**b**) NST mode 1, (**c**) NST mode 2, (**d**) NST mode 3, and (**e**) NST mode 4.

Table 1. On/Off states of 3L-qSBT^{2}I switches and diodes ($X = A, B, C$).

Mode	ON Switches	ON Diodes	V_{XO}
NST mode 1	S_1	D_2, D_3, D_4	$+V_{PN}/2, 0$ or $-V_{PN}/2$
NST mode 2	S_2	D_1, D_2, D_3	$+V_{PN}/2, 0$ or $-V_{PN}/2$
NST mode 3	S_1, S_2	D_2, D_3	$+V_{PN}/2, 0$ or $-V_{PN}/2$
NST mode 4	S_{1X} S_{2X} S_{3X}	D_1, D_2, D_3, D_4	$+V_{PN}/2$ 0 $-V_{PN}/2$
ST mode	$S_1, S_2, S_{1X}, S_{2X}, S_{3X}$		0

In ST mode, both switches S_1 and S_2 of the qSB circuit and all switches of inverter side are turned on at the same time. The result is that input inductor L_B is stored energy from the input source and C_1 and C_2 capacitors, as shown in Figure 3a. Conversely, methods in [27,30] only turned on all switches of inverter side, which decrease energy stored in the inductor and boost factor. The voltage across inductor L_B and current across two capacitors are expressed as

$$\begin{cases} L_B \frac{di_{LB}}{dt} = V_g + V_{C1} + V_{C2} \\ C_1 \frac{dv_{C1}}{dt} = C_2 \frac{dv_{C2}}{dt} = -i_{LB} \end{cases} \tag{1}$$

In NST mode 1 and NST mode 2, as shown in Figure 3b,c, capacitors C_1 and C_2 are respectively charged from the DC input source and the energy of inductor L_B. The following equations are obtained as

$$\begin{cases} L_B \frac{di_{LB}}{dt} = V_g - V_{C2} \\ C_1 \frac{dv_{C1}}{dt} = -i_O, \ C_2 \frac{dv_{C2}}{dt} = i_{LB} - i_O \end{cases} \tag{2}$$

$$\begin{cases} L_B \frac{di_{LB}}{dt} = V_g - V_{C1} \\ C_1 \frac{dv_{C1}}{dt} = i_{LB} - i_O, \ C_2 \frac{dv_{C2}}{dt} = -i_O \end{cases} \tag{3}$$

where i_O is the equivalent output current.

In NST mode 3, as illustrated in Figure 3d, the inductor L_B is stored energy from the DC input power supply, whereas two capacitors, C_1 and C_2, transfer energy to the load. The inductor voltage and capacitor currents are expressed as

$$\begin{cases} L_B \frac{di_{LB}}{dt} = V_g \\ C_1 \frac{dv_{C1}}{dt} = C_2 \frac{dv_{C2}}{dt} = -i_O \end{cases} \tag{4}$$

NST mode 4 is shown in Figure 3e, the lower capacitor and upper capacitor are further stored energy in NST modes 1 and 2. In these modes, the voltage across the input inductor and capacitor currents are calculated as

$$\begin{cases} L_B \frac{di_{LB}}{dt} = V_g - V_{C1} - V_{C2} \\ C_1 \frac{dv_{C1}}{dt} = C_2 \frac{dv_{C2}}{dt} = i_{LB} - i_O \end{cases} \tag{5}$$

2.3. Steady-State Analysis

The key waveform of inductor current i_{LB} and capacitor voltages V_{C1} and V_{C2} are depicted in Figure 4. Considering one switching period, the time intervals of ST state is $D_{ST}.T$. The time interval of NST mode 3 is also $D_{ST}.T$. The total time interval of NST mode 1 and NST mode 2 is $(D_0 - D_{ST})T$. The rest time of switching period is $(1 - D_0 - D_{ST})T$, which is the time interval of NST mode 4. The average values of inductor voltage $(\overline{V}_{LB})$ and capacitor currents $(\overline{I}_{C1}, \overline{I}_{C2})$ are calculated as in Equation (6). Noted that the following equations are achieved by considering $V_{C1} = V_{C2}$.

$$\begin{cases} \overline{V}_L = [(V_g + 2V_{C1})D_{ST}T + (V_g - V_{C1})(D_0 - D_{ST})T \\ +V_g D_{ST}T + (V_g - 2V_{C1})(1 - D_0 - D_{ST})T]/T \\ \overline{I}_{C1} = \overline{I}_{C2} = [-i_{LB}D_{ST}T - i_O(D_0 - D_{ST})T/2 + (i_{LB} - i_O)(D_0 - D_{ST})T/2 \\ -i_O D_{ST}T + (i_{LB} - i_O)(1 - D_0 - D_{ST})T]/T \end{cases} \tag{6}$$
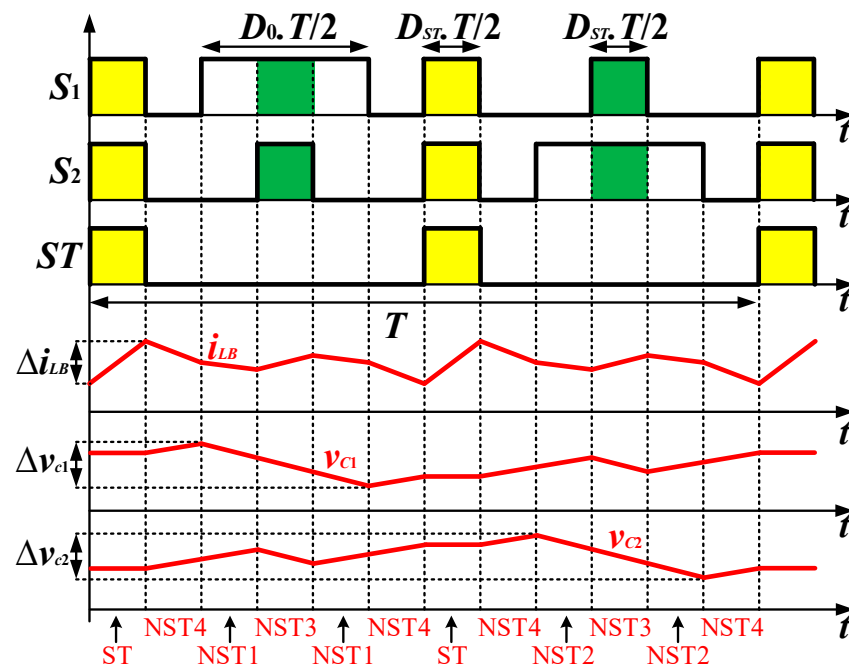
Figure 4. The key waveform in switching period.

In steady-state, these average values are equal to zero, thus the capacitor voltages and average value of inductor current can be expressed as:

$$\begin{cases} V_{C1} = V_{C2} = \dfrac{V_g}{2-5D_{ST}-D_0} \\ I_{LB} = 2i_O \dfrac{1-D_{ST}}{2-5D_{ST}-D_0} \end{cases} \tag{7}$$

The max value of V_{PN} voltage is identified by summing of two capacitor voltages and expressed as

$$V_{PN} = V_{C1} + V_{C2} = \frac{2V_g}{2-5D_{ST}-D_0} \tag{8}$$

The boost factor is defined as

$$B = \frac{V_{PN}}{V_g} = \frac{2}{2-5D_{ST}-D_0} \tag{9}$$

The first-order of output load voltage is identified as

$$V_{x,peak} = 1.15MV_{PN}/2 = \frac{1.15MV_g}{2-5D_{ST}-D_0} \tag{10}$$

The voltage gain, G, is calculated as

$$G = \frac{V_{x,peak}}{V_g/2} = \frac{2 \cdot 1.15M}{2-5D_{ST}-D_0} \tag{11}$$

The relationship between two coefficients, D_{ST} and D_0, is defined as

$$D_{ST} \le D_0 \le 1 - D_{ST} \tag{12}$$

From Equation (12), by adopting D_{ST} and $1 - D_{ST}$ for the coefficient D_0, the minimum and maximum voltage gain is identified by the following equation, noting that the value $(1 - M)$ is employed for D_{ST}

$$\begin{cases} G_{\min} = 1.15M/(3M - 2) \\ G_{\max} = 2 \cdot 1.15M/(6M - 5) \end{cases} \tag{13}$$

2.4. Parameter Selection

The inductor current ripple (Δi_{LB}), illustrated in Figure 4, is calculated with the help of Equation (1) as

$$\Delta i_{LB} = \frac{1}{2L_B f_s} V_g D_{ST} \left(1 + \frac{2}{2 - 5D_{ST} - D_0}\right) \tag{14}$$

where f_s is the switching frequency.

Inductance, L_B, is selected in term of $\Delta i_{LB}/i_{LB} \leq \%x$ as

$$L_B \geq \frac{\mu}{2P_O \%x f_s} V_g^2 D_{ST} \left(1 + \frac{2}{2 - 5D_{ST} - D_0}\right) \tag{15}$$

where $\%x$, μ, and P_O are the maximum percentage of inductor current ripple, the inverter efficiency, and the output power.

The peak-to-peak value of capacitor voltages, V_{C1} and V_{C2}, illustrated in Figure 4, is calculated as

$$\Delta v_{C1} = \Delta v_{C2} = \frac{1}{2C f_s} D_0 i_O \tag{16}$$

The selection of capacitors, C_1 and C_2, is conducted in terms of $\Delta v_C/V_C \leq \%y$ as follows

$$C_1 = C_2 \geq \frac{1}{4\%y f_s} D_0 \frac{P_O (2 - 5D_{ST} - D_0)^2}{\mu V_g^2 (1 - D_{ST})} \tag{17}$$

where $\%y$ is the maximum percentage of capacitor voltage ripple.

The voltage stresses of impedance switches and diodes are the same as capacitor voltage. The max currents of switches and diodes of the qSB circuit are equal to the max value of the current across the inductor ($i_{LB,peak}$), which is calculated as

$$i_{LB,peak} = \frac{\mu P_O}{V_g} + \frac{1}{4L_B f_s} V_g D_{ST} \left(1 + \frac{2}{2 - 5D_{ST} - D_0}\right) \tag{18}$$

The current stresses of 3L-T^{2}I switches are selected as

$$\begin{cases} I_{Sxy} = i_O, & \text{when } 13D_{ST} + 3D_0 \leq 4 \\ I_{Sxy} = i_{LB}/3, & \text{when } 13D_{ST} + 3D_0 > 4 \end{cases} \tag{19}$$

where S_{xy} ($x = 1, 2, 3$; $y = A, B, C$) is the inverter side switch. The voltage across S_{1X} and S_{3X} is the same as the DC-link voltage, whereas it is half of the capacitor voltage for bidirectional switches.

3. Proposed Capacitor Voltage Balance Scheme and DC-Link Voltage Control

As illustrated in Figure 3b, in NST mode 1, the capacitor C_1 is discharged, whereas the capacitor C_2 is stored energy from the input DC source and the input inductor L_B. Therefore, in this mode, the voltage across C_1 is reduced, while C_2 voltage is raised. As opposed to NST mode 1, the C_1 voltage is raised, while the C_2 voltage is reduced, in NST mode 2, as illustrated in Figure 3c. Noted that these modes generate the same inductor voltage, $V_{LB} = V_g - V_C$, in terms of achieving a small difference between two capacitor voltages. Therefore, the boost factor is not much affected when replacing the NST mode 1 to NST mode 2, and vice versa.

To achieve a balancing condition, the proposed method replaces the NST mode 2 with NST mode 1 when $V_{C1} > V_{C2}$. Conversely, NST mode 2 is utilized instead of NST mode 1 when $V_{C2} > V_{C1}$, as presented in Figure 5. The S_1 and S_2 pulses are responsible for doing this work, which is detailed as follows. First, the traditional pulses of S_1 and S_2 are generated by using the V_{tri2}, $\pm V_{ST}$, and $\pm V_{con}$, as shown in Figure 5. Then, V_{C1} and V_{C2} are considered to generate the final pulses of S_1 and S_2. Accordingly, the duty ratio of S_2 is enhanced when $V_{C1} > V_{C2}$. In contrast, the pulse of switch S_1 is enhanced when $V_{C2} > V_{C1}$.
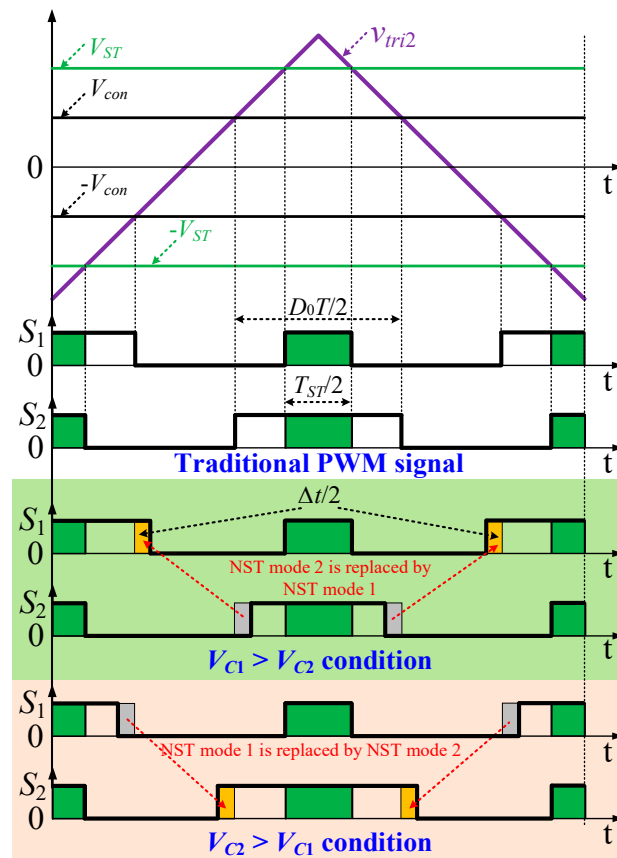

Figure 5. PWM generation for capacitor voltage balance.

In order to detail this strategy, the difference between the two capacitor voltages is defined as

$$v_{dif} = V_{C1} - V_{C2} \tag{20}$$

where:
v_{dif}—the difference voltage between V_{C1} and V_{C2}.

The total time offset, which is used to replace the NST mode 1 with NST mode 2 and vice versa, is identified as

$$\Delta t = \alpha t_{NST1} = \alpha t_{NST2} = \alpha(D_0 - D_{ST})T/2 \tag{21}$$

where:
Δt—the time offset between NST mode 1 and NST mode 2 in one switching period;
t_{NST1} and t_{NST2}—the traditional time intervals of the NST mode 1 and NST mode 2, respectively:
α—is the offset duty ratio ($0 < \alpha \leq 1$).

The capacitor voltage balance strategy is analyzed in two cases that depend on the sign of v_{dif}.

In case 1, the sign of v_{dif} is positive. To achieve capacitor voltage balance, in each switching period, the total time of the *NST*1 and *NST*2 can be redefined as

$$\begin{cases} t'_{NST1} = t_{NST1} + \Delta t = (1 + \alpha)(D_0 - D_{ST})T/2 \\ t'_{NST2} = t_{NST2} - \Delta t = (1 - \alpha)(D_0 - D_{ST})T/2 \end{cases} \tag{22}$$

where t'_{NST1} and t'_{NST2} are the redefined time interval of NST mode 1 and NST mode 2 in one switching period.

In case 2, the sign of v_{dif} is negative. To obtain capacitor voltage balance, in each switching period, the total time of NST mode 1 and NST mode 2 can be redefined as

$$\begin{cases} t'_{NST1} = t_{NST1} - \Delta t = (1 - \alpha)(D_0 - D_{ST})T/2 \\ t'_{NST2} = t_{NST2} + \Delta t = (1 + \alpha)(D_0 - D_{ST})T/2 \end{cases} \tag{23}$$

Noted that the larger value of α leads to the faster neutral voltage balance speed. Moreover, having a fixed difference time Δt between on-times of switches S_1 and S_2 makes this scheme easier to be employed than the method in [27]. As mentioned above, in this method, the operation of the inverter side is maintained, and the replacement of NST modes 1 and 2 produces the same voltage across the boost inductor. Therefore, this work does not affect the boost factor and voltage gain.

The control block diagram for the inverter is presented in Figure 6. In this figure, the controller consists of two separated parts, the DC-link voltage and AC output voltage regulations. From Equation (8), V_{PN} can be regulated through two coefficients, D_{ST} and D_0. Like [27], this scheme also fixes the value D_{ST} based on the DC source range. The result is that V_{PN} is controlled through coefficient D_0. Based on Equation (10), the AC output voltage control is achieved by adjusting capacitor voltage and modulation index M. However, when V_{PN} regulation is obtained, the capacitor voltage is fixed at half of DC-link voltage $V_{PN}/2$. Therefore, the AC voltage regulation is obtained by selecting the corresponding value of M.
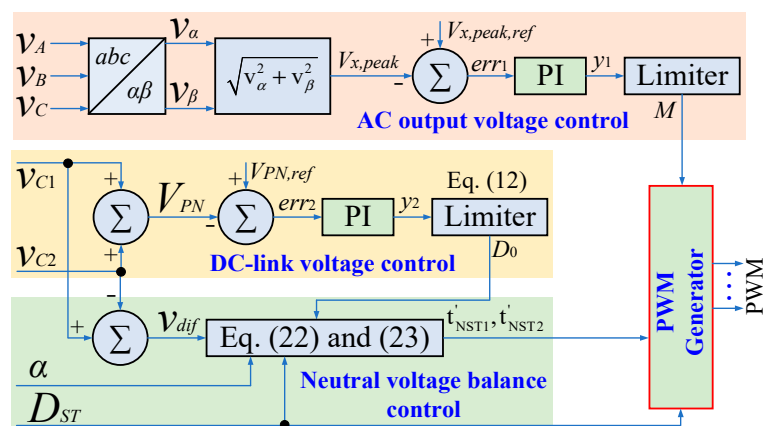

Figure 6. Coordinate control between capacitor voltage balance and DC-link voltage regulation.

For the DC-link voltage regulation, the actual value of V_{PN} is obtained by totaling V_{C1} and V_{C2}. The difference between V_{PN} and the desired DC-link voltage, $V_{PN,ref}$, is minimized by applying the PI controller. The coefficient D_0 is reached by limiting the output of the PI controller by (12).

For the AC output voltage regulation, the actual output voltages (v_A, v_B, v_C) are utilized to calculate the actual $V_{x,peak}$. The abc/$\alpha\beta$ transformation is used to obtain this work, as shown in Figure 6. In this scenario, the PI controller is also considered to generate the modulation index M, noted that modulation index M is limited as $(1 - D_{ST})$.

After calculating three coefficients M, D_{ST}, and D_0, the proposed scheme can generate the control signals of inverter switches similar to the conventional scheme. Noted that the

time intervals of NST mode 1 and NST mode 2 have been adjusted, as mentioned above, to obtain neutral voltage balance.

4. Comparative Study

In Section 4, the superior of the proposed method is demonstrated by comparing it to other single-stage inverters and schemes. The PWM strategies of 3L-qSBI in [27,30] are considered to make the comparison with the proposed method. The overview of boost factor, voltage gain, etc., comparison can be observed in Table 2 and Figure 7. In literature [27,30], the comparison between the qSBI, ZSI, and qZSI has been already conducted. It proved that the PWM method in [27,30] provides the highest boost factor and lowest component rating over other single-stage inverters. To simplify, only the PWM method in [27,30] is considered in comparison to the proposed method. It should be noted that the method in [27] is implemented with a third harmonic injection scheme instead of the sinusoidal scheme. This change increases the voltage gain of the method [27] to 1.15 times and does not affect the operation of the inverter. To achieve the highest performance, the D_{ST} is set to $(1 - M)$ for the proposed method and the method in [27]. For the method in [30], the D_{ST} is set to $2(1 - M)$. In these methods, both the maximum boost and minimum boost schemes are investigated. The max boost control is achieved by setting D_0 to $(1 - D_{ST})$, and the min boost control is obtained by applying D_{ST} to D_0.

Table 2. Overall comparison study of the proposed method and strategies in [27,30] for 3L-qSBT^{2}I.

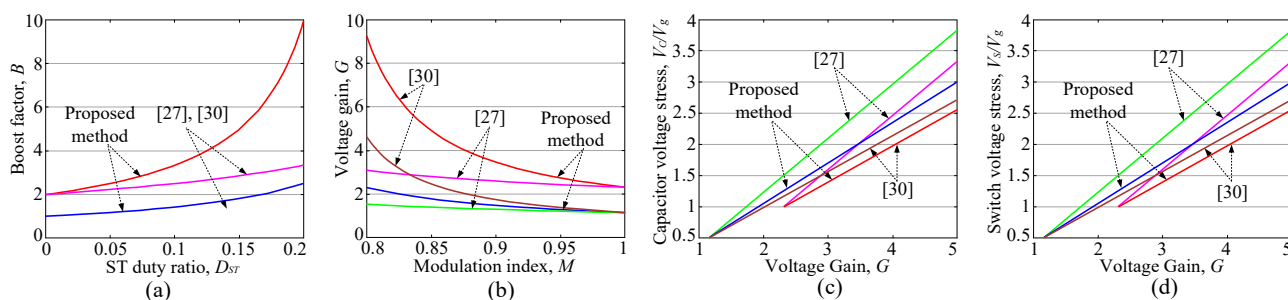|	Strategy in [27]	Strategy in [30]	Proposed Method
Max ST duty ratio, D_{ST}	$1 - M$	$2(1 - M)$	$1 - M$
Boost factor, B	$2/(3 - 2D_{ST} - D_0)$	$2/(3 - 2D_{ST} - D_0)$	$2/(3 - 5D_{ST} - D_0)$
Voltage gain, G	$1.15 \cdot MB$	$1.15 \cdot MB$	$1.15 \cdot MB$
Capacitor voltage rating, V_c/V_{dc}	$1/(3 - 2D_{ST} - D_0)$	$1/(3 - 2D_{ST} - D_0)$	$1/(3 - 5D_{ST} - D_0)$
Diode voltage rating, V_D/V_{dc}	$1/(3 - 2D_{ST} - D_0)$	$1/(3 - 2D_{ST} - D_0)$	$1/(3 - 5D_{ST} - D_0)$
Switch voltage rating, V_S/V_{dc}	$1/(3 - 2D_{ST} - D_0)$	$1/(3 - 2D_{ST} - D_0)$	$1/(3 - 5D_{ST} - D_0)$

Figure 7. (**a**) The ST duty ratio vs boost factor, (**b**) modulation index vs voltage gain, (**c**) voltage gain vs capacitor voltage rating, and (**d**) voltage gain vs switch voltage rating.

As shown in Figure 7a, when applying the same ST duty ratio, the boost factors, *B*, of the methods in [27,30] are the same, whereas the proposed method provides the largest boost factor. In voltage gain comparison, the proposed method and the method in [30] are the same, which is larger than that of the method in [27], for the same modulation index, *M*, as observed in Figure 7b. Due to having a larger boost factor, the proposed method needs a smaller D_{ST} than that of the methods in [27,30] for the same voltage gain. For example, when applying max boost control, if the proposed method needs the value *k* for D_{ST} to produce voltage *G*, the value of D_{ST} for the methods in [27,30] must be $(1 + 2k)/(3k)$ and $2k$, respectively. Noted that the most conduction loss of the single-stage inverter is mostly produced in ST mode, thus having smaller D_{ST} makes the proposed method produce less conduction loss than [27,30].

The capacitor voltage rating comparison is illustrated in Figure 7c. It proves that the proposed scheme has smaller voltage stress on the capacitor compared to the method

in [27]. As mentioned in Section 4, the voltage stress on impedance-source switches and diodes are the same as capacitor voltage, while voltage stresses of upper and lower switches of inverter side S_{1X}, S_{3X} ($X = A, B, C$) are twice the capacitor voltage and that is half of the capacitor voltage for bidirectional switches. Therefore, the reduction of capacitor voltage stress causes a reduction of component rating of switches, as presented in Figure 7d.

In summary, the proposed method has produced the largest boost factor and voltage gain over other single-stage three-level buck-boost inverters such as ZSI and qSBIs. These advantages can cause capacitor voltage rating and semiconductor voltage rating reduction. Moreover, the largest boost factor can lead to reducing the conduction loss, which increases the overall efficiency of the inverter.

5. Simulation and Experimental Verifications

5.1. Simulation Results

With the help of PSIM simulation software, the simulation is conducted to validate the operation of the inverter under the proposed method. The simulation parameters are listed in Table 3. Both maximum and minimum boost factor control methods are validated with DC input range from 70 V to 200 V. In both cases, M and D_{ST} are set as 0.76 and 0.15, respectively. The extra duty ratio, D_0, of switches S_1 and S_2 is set to 0.15 and 0.85 to achieve the min and max boost factors, respectively. With these control parameters, the AC output load voltage is maintained at 110 V_{RMS}. The simulation results for both cases are shown in Figures 8 and 9.

Table 3. Simulation and experiment parameters.

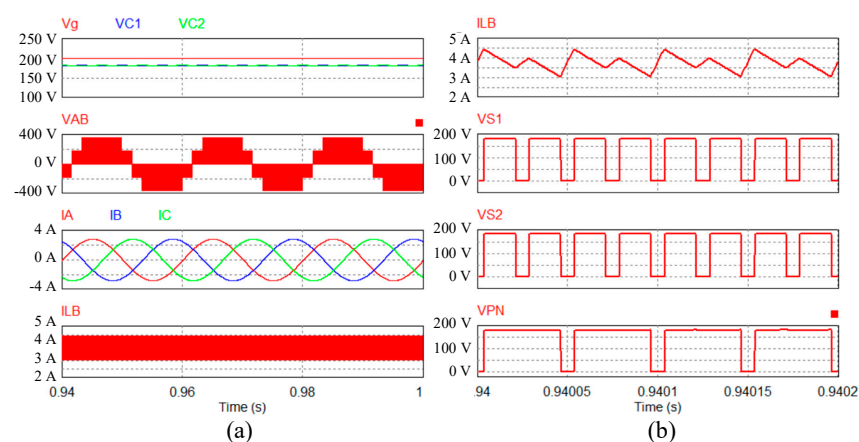| Parameter/Components		Values
Input voltage	V_g	70 V ÷ 200 V
Output load voltage	$V_{x,RMS}$	110 V_{RMS}
Output frequency	f_o	50 Hz
Switching frequency	f_s	10 kHz
Extra duty ratio	D_0	0.15 ÷ 0.85
ST duty ratio	D_{ST}	0.15
Modulation index	M	0.76
Boost inductors	L_B	3 mH/20 A
Capacitors	$C_1 = C_2$	2200 μF/400 V
LC filter	L_f and C_f	3 mH and 10 μF
Resistor load	R	56 Ω

(a) (b)

Figure 8. The simulation results of the proposed method when V_g = 200 V. From top to bottom: (**a**) input voltage (V_g), capacitor voltage (V_{C1}, V_{C2}), line-to-line voltage (V_{AB}), load current (I_A, I_B, I_C), inductor current (I_{LB}), (**b**) zoom in of inductor current (I_{LB}), impedance switch voltages (V_{S1}, V_{S2}), DC-link voltage (V_{PN}).
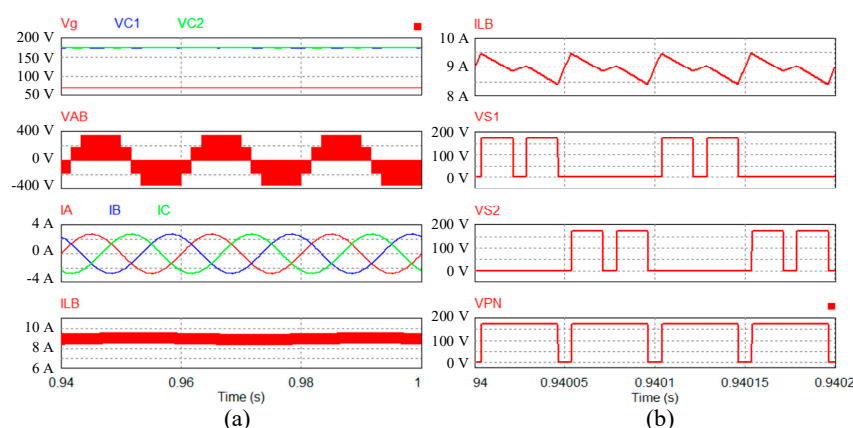
Figure 9. The simulation results of the proposed method when V_g = 70 V. From top to bottom: (**a**) input voltage (V_g), capacitor voltage (V_{C1}, V_{C2}), line-to-line voltage (V_{AB}), load current (I_A, I_B, I_C), inductor current (I_{LB}), (**b**) zoom in of inductor current (I_{LB}), impedance switch voltages (V_{S1}, V_{S2}), DC-link voltage (V_{PN}).

In both cases, the voltages on capacitors C_1 and C_2 are boosted to 180 V, as illustrated in Figures 8a and 9a. These capacitor voltages are also the voltage stresses of switches S_1 and S_2, as shown in Figures 8b and 9b. The peak value of V_{PN} is 360 V, as illustrated in Figures 8b and 9b. The maximum value inductor current ripple is approximately 1.5 A and 1 A for the cases of 200 V input voltage and 70 V input voltage, respectively. These values are obtained in ST mode, which is represented by the zero value of DC-link voltage, as presented in Figures 8b and 9b. The inductor current, I_{LB}, is also increased in NST 3, where S_1 and S_2 are turned on simultaneously. However, it is not increased faster than that of ST mode. The average inductor current is 3.4 A and 9 A for min boost and max boost control schemes, respectively. The waveform of V_{AB} is varied from -360 V and 360 V, as shown in Figures 8a and 9a. The THD value of V_{AB} is 66%. The output load current is measured as 1.95 A$_{RMS}$, and its THD value is 0.56% for both cases.

The comparison of CMV, V_{GO}, between the proposed scheme and strategies in [27] and [30] is shown in Figure 10. The max boost control of methods in [27,30] is applied in the simulation. The method in [30] has the largest peak-to-peak CMV value of 200 V. It can be explained by using small vectors that generate a large value of CMV in [30]. The peak-to-peak CMV values of the scheme in [27] and the proposed PWM strategy are 130 V and 120 V, respectively. The RMS CMV values of the proposed method and methods in [27,30] are 34.8 V$_{RMS}$, 36.5 V$_{RMS}$, and 56.9 V$_{RMS}$, respectively. It is proved that the proposed PWM strategy produces the smallest CMV.

5.2. Experimental Results

The effectiveness of the proposed PWM strategy is also validated by experiments that are obtained through a laboratory prototype, as observed in Figure 11. The parameters used for experimental verification are also the same as simulation. The IGBTs FGL40N150 are used for the S_{1X} and S_{3X} of the inverter leg as well as the active switches of the intermediate network (S_1 and S_2). The isolated voltage sensors based on LEM LV20-P sensor are used to detect the capacitor and output load voltages. The experimental results are presented in Figures 12 and 13.

For the case of a 200 V DC input source, as shown in Figure 12, the V_{C1} and V_{C2} are measured as 163 V and 170 V, respectively, as illustrated in Figure 12a. These capacitor voltages are also the voltage stresses of switches S_1 and S_2, which are 163 V and 170 V, respectively, as presented in Figure 12b. Furthermore, the max value of V_{PN} is determined as 333 V, as shown in Figure 12b. The NST mode 3 can be determined by observing the value zero of both switch S_1 and S_2 voltages, while the ST mode can be identified by observing the value zero of DC-link voltage. The inductor current is increased in both NST mode 3 and ST mode, as shown in Figure 12b. However, in ST mode, the inductor

current increment is faster than that of NST mode 3 because the voltage across the inductor is larger than that in NST mode 3, as demonstrated in Equations (1) and (4). Inductor current ripple is measured around 1.5 A. The average value of i_{LB} is measured as 3.5 A, as presented in Figure 12a. The variation of V_{AB} is from $-V_{PN}$ to $+V_{PN}$, as illustrated in Figure 12c. The output load current is measured as 1.85 A_{RMS}, and its waveform is sinusoidal. The FFT analysis for V_{AB} can be seen in Figure 12c. The first-order harmonic is also the maximum value, which is 190 V. The THD values of V_{AB} and output load current I_A are 80.5% and 2.51%.

When applying 70 V DC input source, the capacitor C_1 and C_2 voltages are 153 V and 159 V, when the coefficient D_0 is 0.85. These voltages generate 312 V of DC-link voltage, as illustrated in Figure 13b. The inductor current ripple is approximately 1.1 A, as shown in Figure 13b, and its average value is 10.4 A, as shown in Figure 13a. The output load current is 1.71 A_{RMS}. Figure 13c presents the FFT spectrum of V_{AB}, where the peak-to-peak value is 180 V at the first-order harmonic. The THD values of V_{AB} and I_A are 82.6% and 2.55%, respectively.
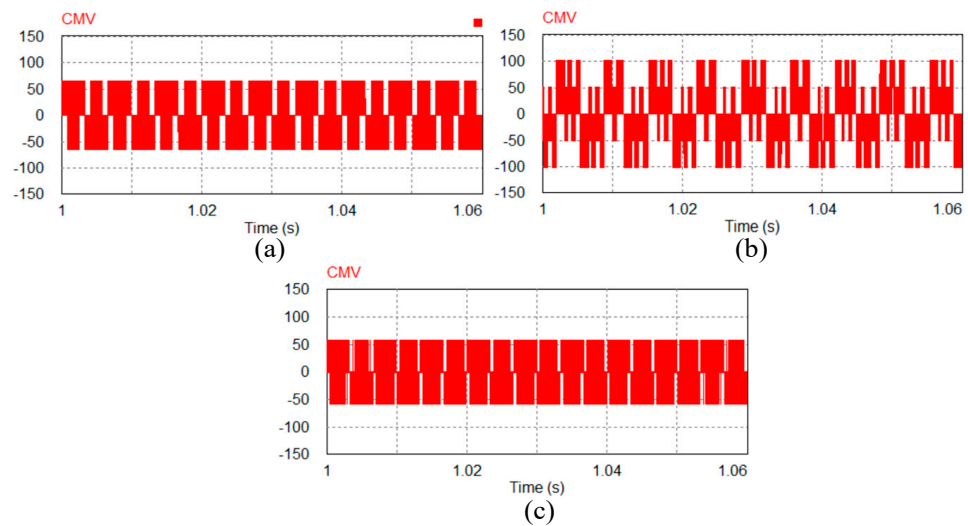

Figure 10. CMV comparison between (**a**) the method in [27], (**b**) the method in [30], and (**c**) the proposed method.
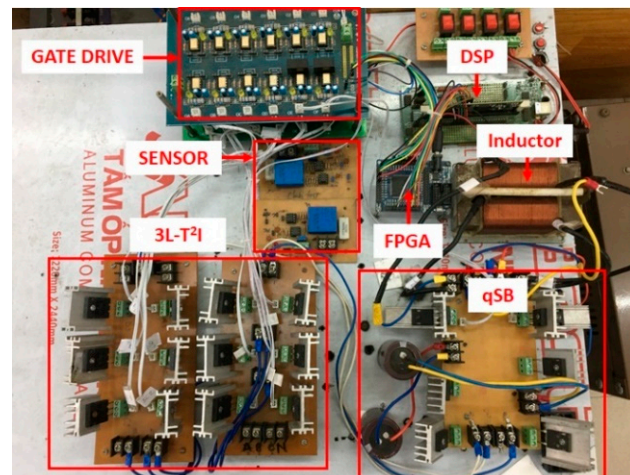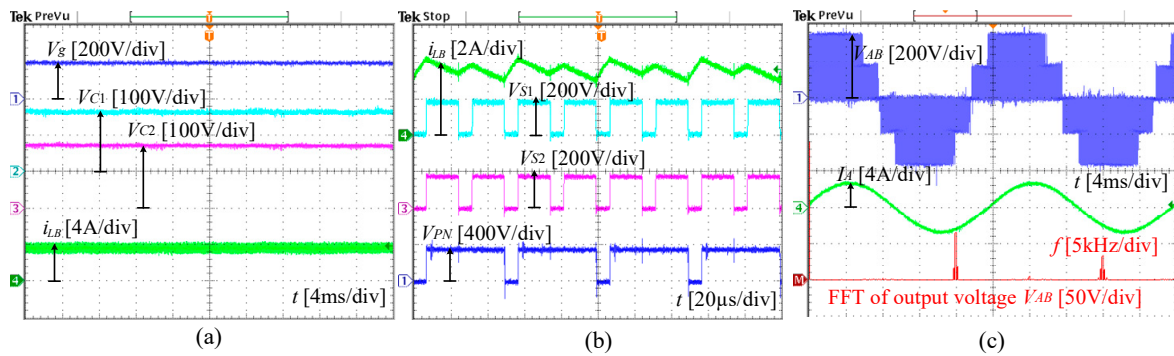

Figure 11. Experimental prototype.

Figure 12. Experimental results of the inverter under the proposed method when $V_g = 200$ V. From the top to bottom: (**a**) V_g, V_{C1}, V_{C2}, and i_{LB}; (**b**) i_{LB}, V_{S1}, V_{S2}, and V_{PN}; (**c**) V_{AB}, I_A, and FFT spectrum of the output voltage V_{AB}.
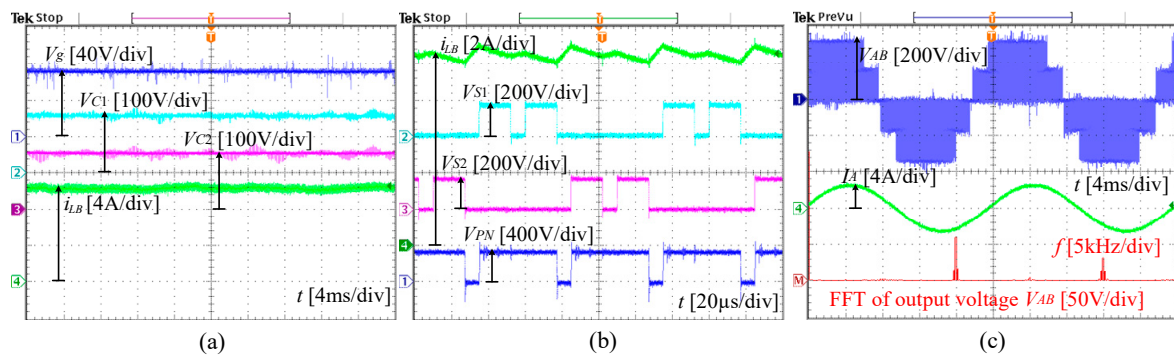

Figure 13. Experimental results of the inverter under the proposed method when $V_g = 70$ V. From the top to bottom: (**a**) V_g, V_{C1}, V_{C2}, and i_{LB}; (**b**) i_{LB}, V_{S1}, V_{S2}, and V_{PN}; (**c**) V_{AB}, I_A, and FFT spectrum of the output voltage V_{AB}.

The capacitor voltage balance scheme and the closed-loop control implementation for the proposed method have been conducted. The results are shown in Figures 14 and 15. The neutral voltage control is implemented in two cases: (1) the difference voltage between these capacitors v_{dif} is positive, and (2) the difference voltage between these capacitors v_{dif} is negative. In both cases, the neutral voltage balance condition is recovered after approximately 20 ms, as shown in Figure 14a,b. These results are conducted with the coefficient α of 0.3.
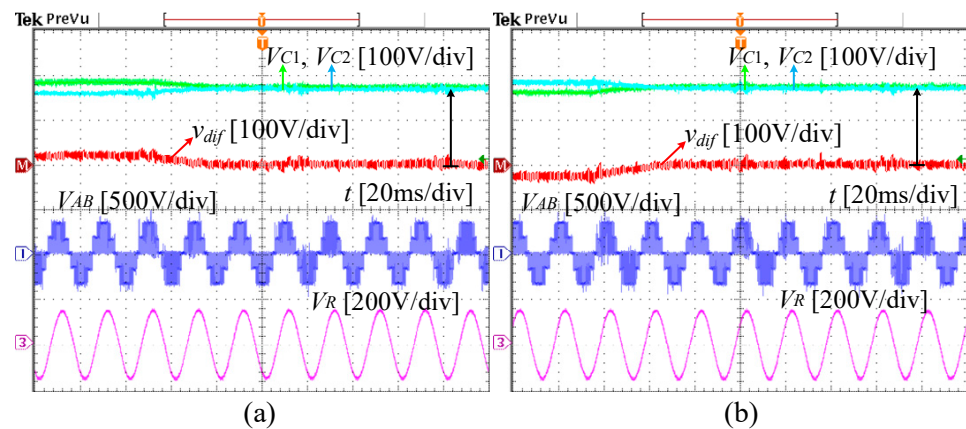

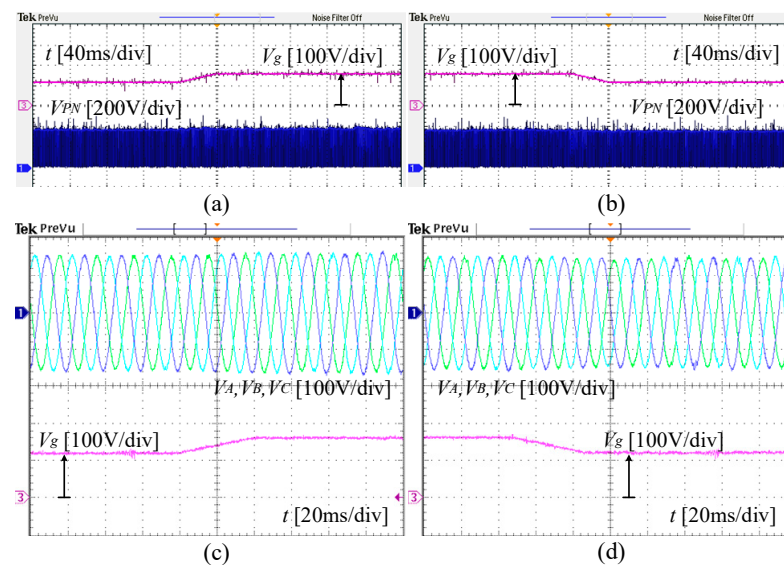**Figure 14.** The experimental results for capacitor voltage balance. (**a**) $v_{dif} > 0$, (**b**) $v_{dif} < 0$.

Figure 15. The experimental verification for DC-link voltage control and output load voltage control. (**a**,**c**) Input voltage increment, (**b**,**d**) input voltage decrement.

The input voltage is regulated to increase from 120 V to 160 V and decrease from 160 V to 120 V to validate the closed-loop control. In both cases, the V_{PN} is maintained at 360 V, which can be seen from Figure 15a,b. The output load voltage is kept at 110 V_{RMS} without DC input voltage variation, as presented in Figure 15c,d. In this work, the ST duty ratio D_{ST} is kept at 0.15. The modulation index is used to regulate the output load voltage and is limited to 0.85. The coefficient D_0 is utilized to control DC-link voltage, and its range is from 0.15 to 0.85.

6. Conclusions

This paper has introduced a PWM method for the 3L-qSBT^{2}I based on a third harmonic injection scheme. By applying this method, many benefits have been obtained, such as high boost factor, high voltage gain, and less voltage rating on impedance-source network devices. These advantages have been validated through some investigations, which were conducted belonging to previous publications. The details of relevant equations and designed parameter selection have been presented. Furthermore, this paper also considered the capacitor voltage unbalance problem. The time interval of NST mode, which is generated by triggering only one switch of the qSB network, has been recalculated based on the actual capacitor voltages to provide neutral voltage balance characteristics. The output voltage and DC-link voltage have been controlled by using PI controllers. The extra duty cycle of two active switches of the qSB network was adopted to regulate DC-link voltage, whereas the modulation index has been utilized to regulate the AC output voltage. The accuracy of this scheme has been validated by simulation and experimental results. With some benefits listed, such as buck-boost operation, reduced conduction loss, the low voltage stress on devices, and an easy capacitor voltage balance scheme, the 3L-qSBT^{2}I under the proposed method is suitable for PV applications where a low DC input voltage needs to be converted to a high AC output voltage with high efficiency and output quality.

Author Contributions: This article has received the same contributions from the authors. which include writing the paper and experiment implementation. This manuscript has been received agreement from all authors. This paper was a collaborative effort among all authors. D.-T.D., V.-T.T. and M.-K.N. conceived the methodology, conducted the performance tests and wrote the paper. All authors have read and agreed to the published version of the manuscript.

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