Article

Investigating the Shielding Effect of Pulse Transformer Operation in Isolated Gate Drivers for SiC MOSFETs

Loreine Makki [1], Marc Anthony Mannah [2], Christophe Batard [1,*], Nicolas Ginot [1] and Julien Weckbrodt [1]

1   Department of Electrical Engineering, Université de Nantes, IETR, Site de la Chantrerie, 44306 Nantes, France; loreine.makki@etu.univ-nantes.fr (L.M.); nicolas.ginot@univ-nantes.fr (N.G.); julien.weckbrodt@univ-nantes.fr (J.W.)
2   Department of Electrical Engineering, School of Engineering, The International University of Beirut BIU, Beirut, Lebanon/Lebanese International University LIU, Bekaa, Lebanon; marc.mannah@b-iu.edu.lb
*   Correspondence: christophe.batard@univ-nantes.fr

Abstract: Wide-bandgap technology evolution compels the advancement of efficient pulse-width gate-driver devices. Integrated enhanced gate-driver planar transformers are a source of electromagnetic disturbances due to inter-winding capacitances, which serve as a route to common-mode (CM) currents. This paper will simulate, via ANSYS Q3D Extractor, the unforeseen parasitic effects of a pulse planar transformer integrated in a SiC MOSFET gate-driver card. Moreover, the pulse transformer will be ameliorated by adding distinctive shielding layers aiming to suppress CM noise effects and endure high dv/dt occurrences intending to validate experimental tests. The correlation between stray capacitance and dv/dt immunity results after shielding insertion will be reported.

Keywords: wide-bandgap; gate-driver; planar transformer; CM noise; ANSYS Q3D Extractor; SiC MOSFET; shielding

1. Introduction

The evolution of electronic devices over the past few years has resulted in compelling impacts on the community and industry. Gradual technological leaps in the field of semiconductors and power devices are forecasted to structure the mechanized sector of the revolutionized globe [1,2]. Robust power electronic systems are demanded in automotive, energy management, telecommunication, medical, and aeronautic applications [3]. Since 1970, the power density of power electronic converters in diverse operations has nearly doubled every ten years [4]. The primary agent of this trend was the proficiency to increase the switching frequency by a multiple of ten every decade, which was realized by the incessant improvement of power semiconductor device technologies [5]. This continual advancement of power density converters is portrayed by the demanded requirements for higher efficiency and reliability, volume reduction, lightweight materials, and cost-effectiveness [6,7]. Substantial research and examinations have been applied to different aspects of the aforementioned power converter system constituents to attain significant efficiency and power density objectives.

The breakthrough of wide-bandgap (WBG) device technology is a pivotal promoter for power electronic system curtailing and miniaturizing [8]. Various studies revealed the leading incentives and expansion of this technology which can induce momentous impacts on system modeling and assemblage, prompting paragon transitions within the entire power electronics industry [9,10]. The two predominantly engaged semiconductor materials are silicon carbide (SiC) and gallium nitride (GaN), which surpass their silicon (Si) counterpart by acquiring substantial intrinsic properties, making it feasible to intensify the switching frequency of converters from a few hundred kHz to the MHz frequency region [11,12]. However, optimization always comes with a cost; with every advance-

ment, researchers and analysts are confronted with challenges and impediments to realize upgraded power converter designs.

Favorable high switching frequency attainment becomes conflicting and challenging when resulting in high switching transitions dv/dt, amounting to 100 kV/μs, provoking electromagnetic disturbances in gate driver circuits due to parasitic capacitances and inductances [13]. Hence, to profit from the encouraging advancements while inspecting the demerits, printed circuit board (PCB)-integrated gate driver technology for WBG device technology has been explored [14]. Electromagnetic compatibility (EMC) conformity is crucial when designing gate driver circuits amid preserving high power density and minimum isolation capacitance. This is attained by the utilization of planar transformers, which harmonize with the growing demand of slim-profile power supplies, and comprising low leakage inductance, repeatability, and low thermal resistance [15]. Yet, as previously mentioned, a downgrade for every upgrade creates a limitless road for renovation.

Traditional planar transformers present high levels of common-mode (CM) noise due to the presence of stray capacitances between primary and secondary windings providing a route for CM currents generated due to large dv/dt occurrences from fast switching devices. These circulating pulsating currents are the main originators of electromagnetic interference (EMI) issues [16]. Various studies have been conducted to mitigate the CM noise occurrence in planar transformers, such as adding anti-phase windings [17], including a Y capacitor [18], or the insertion of faraday shielding layers [19–22]. Referring to Cochrane et al. [23], the employment of a compensation capacitor with an antiphase winding to cancel noise current from flowing through MOSFET parasitic capacitor cannot considerably stop the noise current from flowing to the secondary side and return via a ground path. Moreover, including bypass capacitors [18] is always limited by safety standards and is challenging when it comes to the repeatability of prototype designs.

The objective of this paper is to investigate a pulse planar transformer integrated in a gate driver card. Planar transformers are renowned for ultimate repeatability attributes. The effect of integrating several modeled and designed electrostatic screens to shunt noise current were studied to validate experimental analysis which was conducted based on trial and error. To conserve time and expenses, the latter were designed and analyzed using finite element analysis (FEA) tools such as ANSYS Q3D Extractor dynamically linked with ANSYS Circuit design to analyze the transformer's susceptibility to high dv/dt application. The simulation of the steep dv/dt occurrence was conducted on an equivalent transformer P-Spice model generated by ANSYS which revealed the resourcefulness of this investigation to ensure safe operation and behavior prediction of upcoming research examinations.

The rest of this paper is structured as follows. Section 2 focuses on gate driver illustration, constituents, and requirements. Section 3 focuses on planar transformers integrated in gate drivers with the simulation of innovative ameliorated modeled designs and the presentation of the simulated results. Section 4 reveals experimental validation of results, highlighting outcome dependencies. Section 5 concludes this paper.

2. Gate Driver Convention for Power Semiconductors

2.1. Inverter Principles

The fundamental objective of power electronic technology is to transform and regulate the flow of electrical energy aiming to supply optimum voltages and currents that fulfill user-defined requirements. As its name signifies, a power converter is the process of converting electrical energy from one form to another. The conversion method assigns the category type of the power converter which can be classified as AC/AC, AC/DC, DC/AC, or DC/DC.

Modernized power electronic converters participate in a broad scope of applications such as switched mode power supplies (SMPS), renewable energy conversion systems, active power filters, and vehicle technology. Typically, DC/AC converters are called inverters, and are used to generate alternating voltages/currents from a fixed direct voltage source such as a battery. Figure 1 reveals an example of a single-phase full bridge inverter where

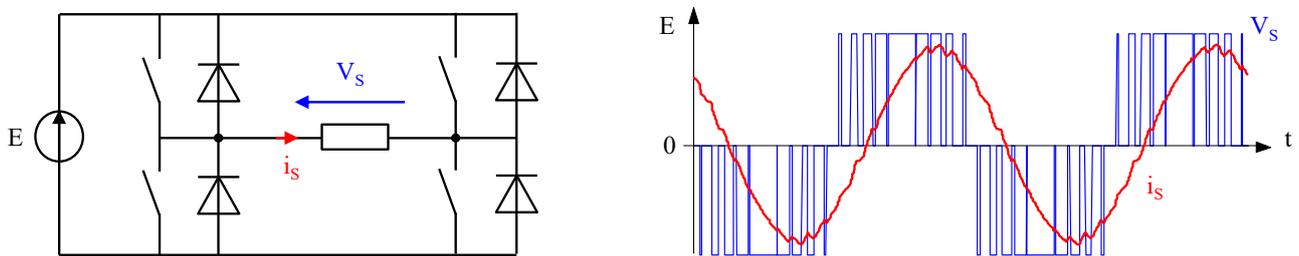four switches are utilized, resulting in a load current that corresponds to an alternating current source.

Figure 1. Single-phase full bridge inverter and its associated waveform.

A half-bridge switching cell, known as the vertical arm of a full bridge inverter, comprises controlled switches that are unidirectional in voltage and bidirectional in current and are ordered to be either excited or blocked, and protected against arm short circuits [24]. There are diverse contemporary and controllable power electronic switches that can be utilized such as relays, thyristors, IGBTs (insulated gate bipolar transistors) and MOSFETs (metal oxide semiconductor field effect transistor) [25].

An example of the composition of controlled insulated-gate field-effect transistors, commonly known as MOSFETs is shown in Figure 2. The aforementioned depiction highlights that the practical switching times of the MOSFETs are relatively prolonged with respect to the theoretical switching times, in addition to the inevitability of a galvanic isolation safeguarding independent transistor control [26].
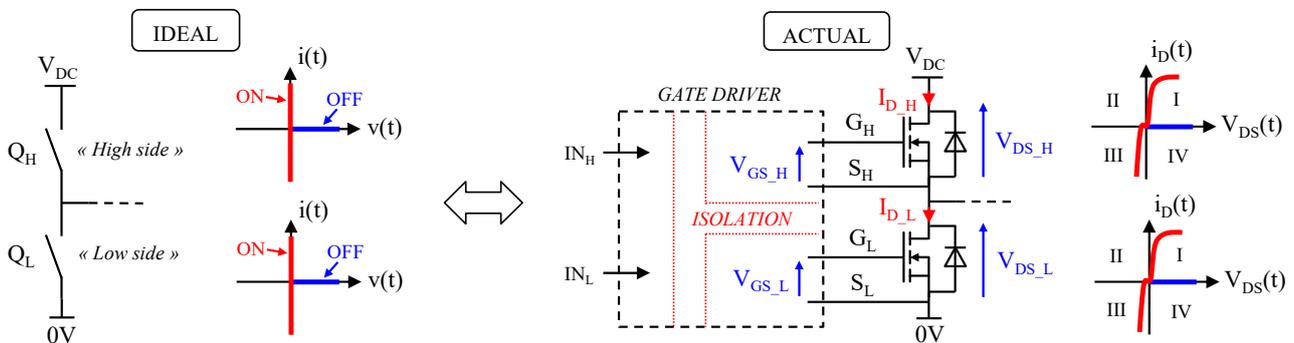

Figure 2. A fundamental example of a switching N-MOSFET cell.

Wide-Bandgap Technology

Although silicon (Si)-based IGBTs have been on the market for more than 30 years, they have reached their physical limits when confronted with the demand of high-power density converters (HPDC) and therefore higher switching frequencies [27]. The emergence of commercial WBG semiconductor devices based on SiC and GaN promoted ample reduction in conduction losses due to their lower ON-resistance. Moreover, they are featured with notable inferior gate capacitance, permitting them to operate at exceptional exceeding frequencies [28]. The prominent substitutes of Si-IGBTs in power utility applications are SiC MOSFETs due to their lower losses, higher speed operations, and higher thermal capabilities as shown in Figure 3 [12,27,29].
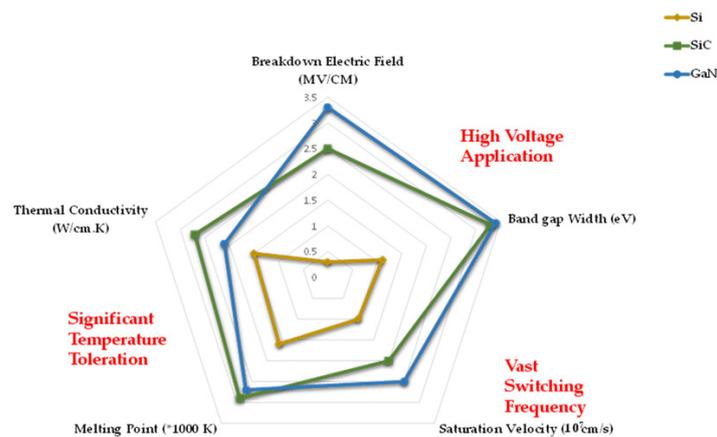
Figure 3. Intrinsic properties of particular semiconductor materials: Si, SiC, GaN.

2.2. Gate Driver Illustration

Due to the sublime convenience of WBG devices, the market witnessed immense employment of this technology [30]. Nonetheless, to benefit from the technologies' distinguished performance, it is vital to upgrade its operation and system environment [31].

One of the imperative constituents of power electronic systems is gate drivers, which serve as an interface between microcontrollers that manage the switching operations (low voltage side) and the power module (high voltage side) as presented in Figure 4 [32]. This is generally referred to as the amplification stage to drive semiconductor devices. The terminology 'gate driver' implies supplying a high-current drive input for a gate of a high-power transistor such as a MOSFET.
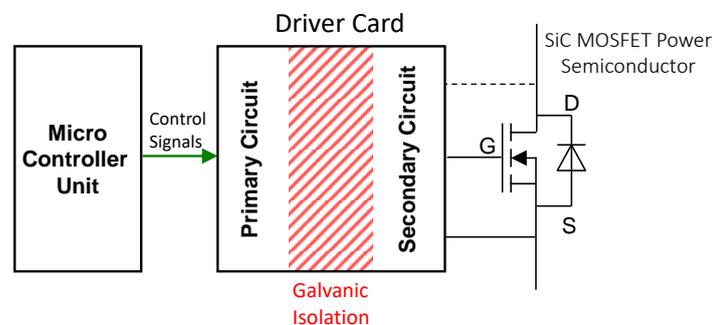

**Figure 4.** Generic demonstration of gate driver card assemblage.

Prevalent and common attributes of gate drivers are as follows [33,34]:

- Converts and amplifies power signals to drive semiconductor devices;
- Provides protection schemes and delivers feedback for operation monitoring of power converters; and
- Grants galvanic isolation crucial to certify competent system functioning and user's safety.

Galvanic Isolation Requirement

Galvanic isolation, a prevailing gate driver characteristic, is an isolation barrier that electrically isolates primary to secondary circuitry, by founding segregated ground references. It concerns the isolation of the control signal transmission and the power supply circuit of the driver card. The power supply circuit is usually achieved by a transformer, yet, the transmission of control signals or switching commands through the galvanic isolation of gate drivers can be realized by the following technologies, appointed based on the voltage and power range of specific applications [30]: optocoupler, transformer (with core/coreless), optical fiber, capacitive link, piezoelectric coupling.

Despite the extensive adoption of advantageous optocouplers in low to medium power applications, they comprise significant parasitic capacitances which induce common mode current circulations between the primary and secondary circuit, instigating electromagnetic disturbances [17]. Amongst the above-mentioned classifications, pulse transformers are commonly used for medium to high power applications. Moreover, the effective development of PCB technology supported the fabrication of practical planar transformers (Figure 5) that are distinguished with miniaturization, good thermal characteristics, transcendent repeatability, low cost, smooth fabrication, and predictable parasitic parameters [35].
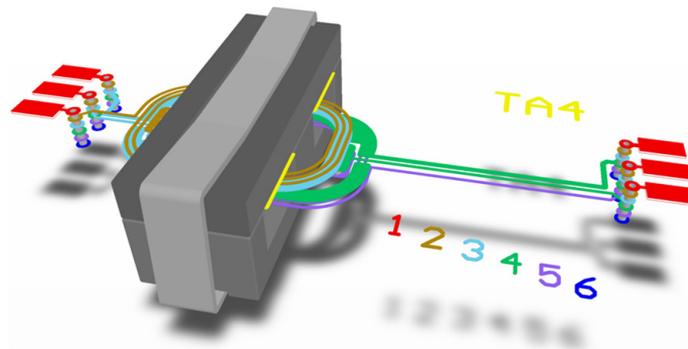
Figure 5. An example of a planar transformer with an EI core.

The illustration in Figure 6 reveals the examined gate driver at IETR lab which drives two power semiconductors, namely SiC MOSFETs. As depicted, the gate driver card comprises four planar transformers, of which two are dedicated to supplying the electronic circuit, and two are committed to authorizing the switching of the power semiconductors by the transmission of triggering positive and negative pulses.
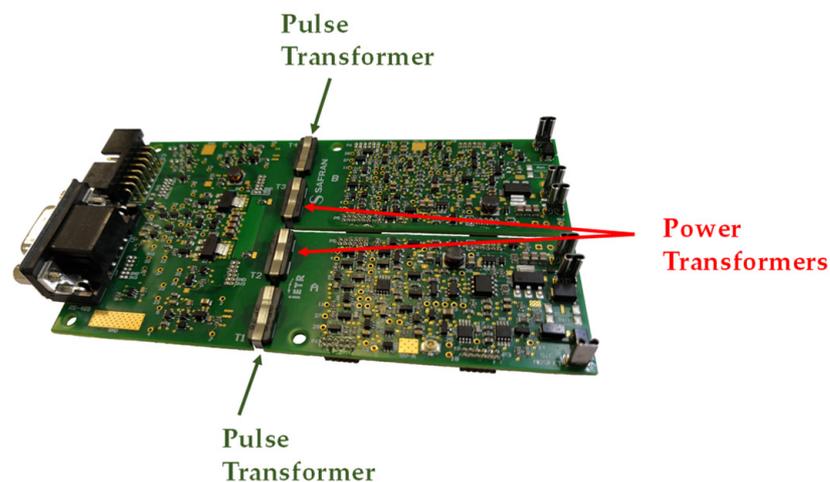
Figure 6. Gate driver card for two semiconductors with four designated planar transformers.

Accompanying the high-caliber superiority of medium-voltage (MV) SiC MOSFETs, rigorous consideration and attention must be regarded when managing a fast-switching component whilst safeguarding reliable circuit operation and performance.

2.3. Electromagnetic Compatibility (EMC) Compliance

MV SiC MOSFETs feature extensively rapid switching speeds with high dv/dt amounting to 100 kV/µs [36]. The electronics of the secondary driver circuit are referenced with respect to the source of the controlled semiconductor, hence, the occurrence of a potential

variation across the primary and secondary depends on the state of the adjacent transistor [37]. The existence of substantial potential variation due to switching induces the passage of CM currents [17] through parasitic capacitances of planar transformers, known as interwinding capacitances, prompting EMI dilemmas [18,38]. Thus, it is crucial to analyze the EMI generated by the converters and adhere to EMC standards [39].

Since power transformers, presented in Figure 6, are utilized to supply the electronic circuitry, the passage of CM current through the latter does not impose unfavorable consequences on the reliability of semiconductor performance. However, significant attention and awareness is demanded when designing pulse transformers, as they are responsible for executing the switching orders for booting or blocking power semiconductor transistors. Hence, a steep dv/dt occurrence might provoke faulty or invalid switching orders due to the passage of CM currents across pulse transformers as seen in Figure 7, leading to adverse, unfavorable results such as the occurrence of a short circuit branch.
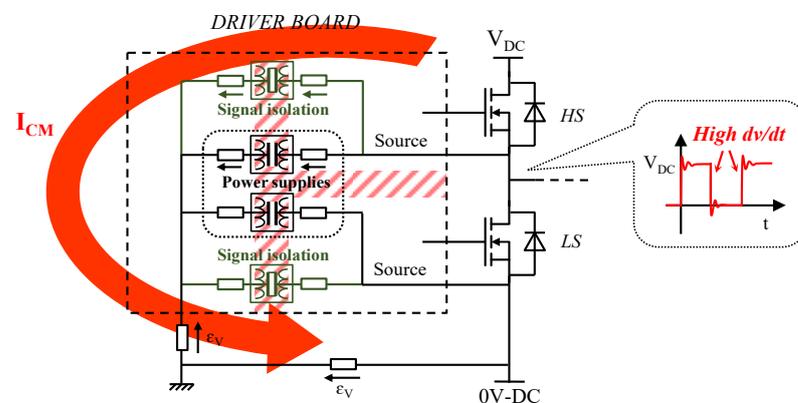
Figure 7. Common-mode current routing through isolated signal transformers on gate driver board.

2.4. Conclusion

The presented and previously conferred matter highlights the necessity of ensuring reliable gate driver operation by implementing adequate pulse transformer isolation providing dv/dt robustness.

Since 1970, various studies have been conducted to optimize pulse transformer design circuits, whilst studying the effects of parasitic elements [40]. Presently, with the aid of rapid computer analysis and renovated software, magnetic circuit behavior can be simulated, analyzed, and optimized to enhance design and mitigate the effect of parasitic elements which will be demonstrated in the upcoming section.

3. Pulse Transformer Simulated Model Analysis

3.1. Planar Transformers in Gate Drivers

To realize exceptional and challenging performance levels, researchers and designers encounter diversified confrontations when ensuing optimum upgraded design objectives: reinforced, economical, and efficient converter designs.

WBG technology successfully grants higher switching frequency and voltage blocking applications; nonetheless, EMI disturbances originate with power devices' switching transitions [41]. Hence, as mentioned earlier, a PCB layout design was explored and implemented for CM EMI reduction [42,43] where planar transformer integration is renowned for the following incentives:

- Low profile, light weight;
- Consistent manufacturing;
- High power density;
- Distinguished repeatability; and
- Greater operating frequency in comparison to wire wound transformers.

Table 1 below demonstrates various driver types with their corresponding features, aiming to highlight the use of PCB arrangement:

Table 1. Comparison example of gate driver types and their relevant features.

Gate Driver	Name	Features
	Plug and play	Nearest card Specific module Applications > 100 kW
	Core driver and passive card	Generic driver module Low cost Applications > 100 kW
	Integrated circuit drivers	Compact External power supply Deficit performance

This paper will present an alleviated planar pulse transformer design study that will be experimentally tested for safe and reliable operation.

3.2. Pulse Transformer Scheme

A positive impulse on the primary winding of the pulse transformer invoked an activation of the power semiconductor, a 1200 V SiC MOSFET, whereas a negative impulse transmitted a turn off signal to block the device. The pulses transferred were shortened to a duration of 25 ns, allowing them to cross the galvanic isolation barrier but not impact other transmitted control command signals as revealed in Figure 8.
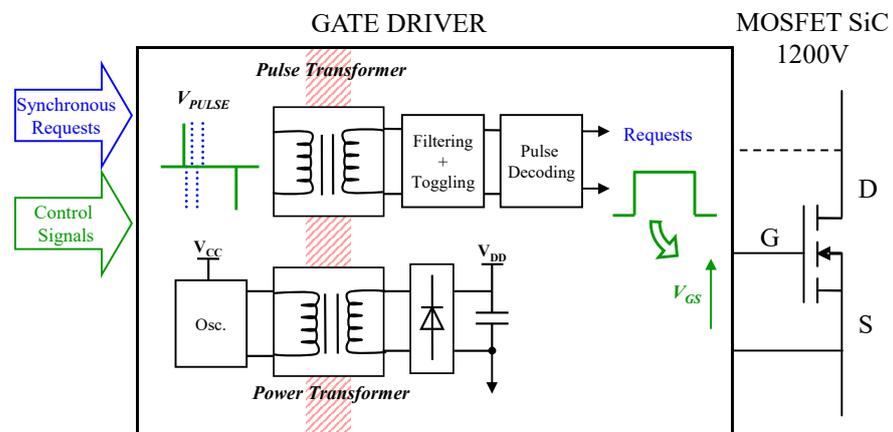
Figure 8. Principle of data signal transmission through a gate driver.

For a switching frequency of 100 kHz, the use of short pulses (25 ns) is necessary but requires considerable noise control, especially ones arousing from electromagnetic disturbances.

It is imperative to mention that the integration of the planar transformers in the gate driver card was achieved in compliance to electrical insulation standards. Clearance (short-

est distance through air between two conductive parts) and creepage (shortest distance over surface between two conductive parts) measurements were implemented and considered [44]. Moreover, the insulation between layer stacks of the PCB was respected, noting that this is not very restraining due to the utilization of rigid FR4 epoxy dielectric material which can tolerate 20 kV/mm before breakdown. Furthermore, the design and spacing requirements on the driver card were in accordance with the IPC-2221 standard, the generic standard of PCB design.

The gate driver card was comprised of six stacked layers insulated by FR4 epoxy; hence, the design of the pulse transformer respected the layering protocol of the driver.

3.3. Pulse Transformer Model Simulation Analysis

To further augment the enhancement and improvement of the global gate driver design, the pulse transformer was explicitly elected for CM noise reduction technique application. Several methods that serve this objective have been discussed in literature, aiming to decrease the interwinding or coupling capacitance between the windings or define a displacement path for CM current. Symmetry, balancing, and shielding techniques are well-known tested methods [38,45,46]. Symmetry and balancing applications are not effective in mass production and cannot achieve promising results at high frequencies. Nevertheless, inserting electrostatic screens or Faraday shielding between winding layers of transformers presents a defined grounded route for CM current flow [47], refer to Figure 9.

Figure 9. Correlation of CM current displacement across a transformer: (**a**) Standard unshielded transformer; (**b**) transformer with grounded electrostatic screens.

The exploited simulation methodology associated several design programs: the pulse transformer was primarily designed in Altium Designer with different shielding models, thereafter it was imported into ANSYS SIWAVE to verify the layer stack up, thickness, and material assignment before being exported into ANSYS Q3D Extractor and ANSYS Circuit Design for further analysis as depicted in Figure 10.

Simulation Methodology
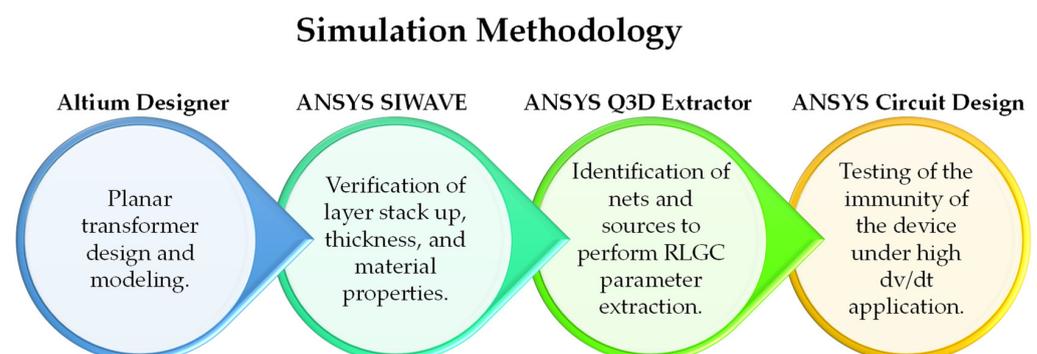
Figure 10. Simulation methodology process followed to analyze pulse transformers.

3.3.1. ANSYS Q3D Extractor and Dynamic Links

To reduce design time and prototype expenses, ANSYS Q3D Extractor, the leading parasitic extraction tool, was exploited to model and simulate the planar pulse transformer proposed models presented in Section 3.3.3. This software performs electromagnetic field simulations essential for the extraction of resistance, conductance, partial inductance, and capacitance, known as RLGC parameters. The objective was to simulate realized pulse planar transformers to ensure conformity of simulation and experimental results which will be the groundwork for forthcoming design modeling and experimentations. Q3d Extractor utilizes the finite element method (FEM) and method of moments to generate an electromagnetic field solution. This is achieved by either dividing the full problem space or surface of conductors into tetrahedral elements. It is based on the simplification of Maxwell's equations named quasistatic approximation by assuming that the size of the analyzed design is small compared to the wavelength of maximum desired frequency where the coupling between magnetic and electric fields can be neglected.

The design created in Altium designer was imported into ANSYS Q3D after verifying layer stack up in ANSYS SIWAVE, with the respective material properties of the modeled design displayed in Figure 11. The analysis allows one to observe and determine the RLGC parameters of the model [48]. The source and sink identifications in the Figure signify where the current enters and exits the windings, respectively, this is essential for AC/DC RL analysis. However, to compute the GC matrices, it is vital to identify all copper layers as nets.
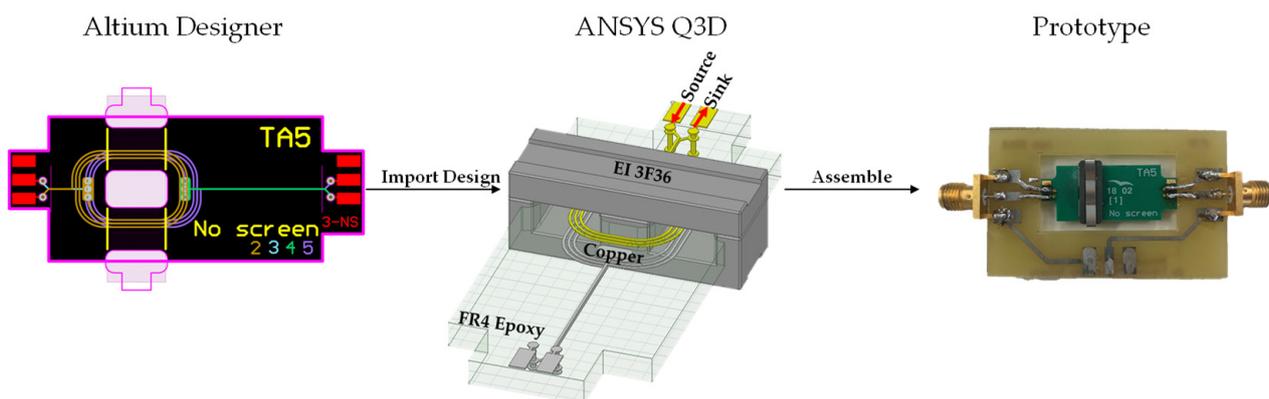
Figure 11. Pulse transformer design analysis in Altium Designer and ANSYS Q3D.

Surplus, dynamic linking with ANSYS Circuit Design from a created Q3D project allows the simulation of the sub-circuit with the project original simulator to be aligned with the circuit simulator [49]. Consequently, this further expands the analysis by granting co-simulation features and allowing the addition of electrical components and sources to actualize an intended experimental analysis.

3.3.2. Pulse Transformer Electronic Circuitry

Power transistor switching orders and data transfer were achieved as per the electronic circuit presented in Figure 12 below. The circuit operation was based on a sequential logic circuit, Set/Reset latch principle, where a positive pulse delivered a high logic, and a negative pulse rendered a low output signal. As the sequence in the Figure conveys, firstly, the short pulses were generated with a 15 V amplitude which increased signal/noise ratio, then pulse selection was needed to disparate between positive and negative pulses. Progressing, a filter stage was carried out to reduce the signal noise suitable for a 0–3.3 V logic at output. Lastly, an RS flip-flop with an integrated Schmitt trigger allowed the original signal to be reconstructed from the sequence of pulses and guaranteed the integrity of the signals in the presence of noise. The disturbance caused by a steep dv/dt was

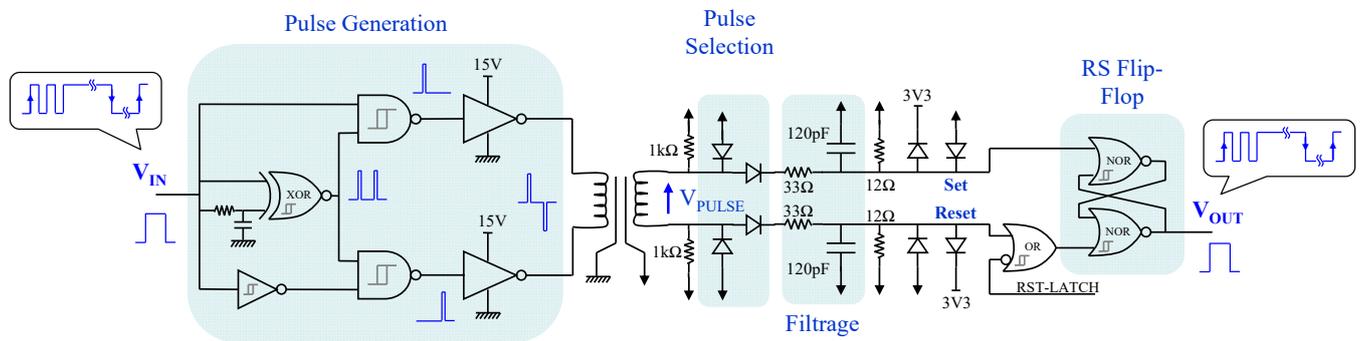prohibited from corrupting the control signal, justifying the selection of low impedances on the secondary circuit.

Figure 12. Pulse generation and transmission electronic circuit.

3.3.3. Planar Pulse Transformer Analyzed Models

The investigated pulse transformer was of planar type integrated in a six-layer PCB stack. Four layers were designated for the conductors, primary and secondary windings, and two shielding layers. The number of turns of the primary and secondary windings was three, characterized by a turn's ratio of 1, separated by FR4 epoxy dielectric material and secured with a 3F36 EI ferrite core. Distinct electrostatic screen arrangements were designed and simulated, as shown in Table 2, implemented based on the transformer section view in Figure 13, showing the mid-layers along with the separating distances. The objective of the shielding layers was to demonstrate their relevance in minimizing the parasitic capacitance between the primary and secondary windings.

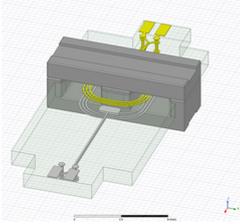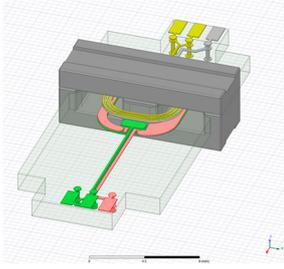**Table 2.** Examined pulse transformer designs to study the effect of Faraday shield insertion.

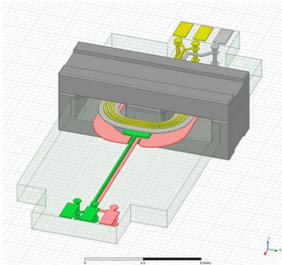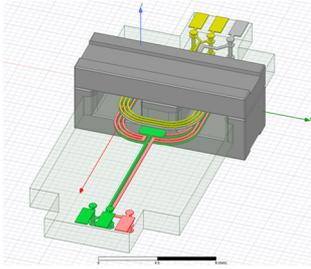| Pulse Transformer	Type	Description
	Unshielded	Primary and secondary windings separated by FR4 epoxy without insertion of shielding layers.
	Typical shield	Filled typical shielded layers that cover the exact winding periphery.

Table 2. *Cont.*

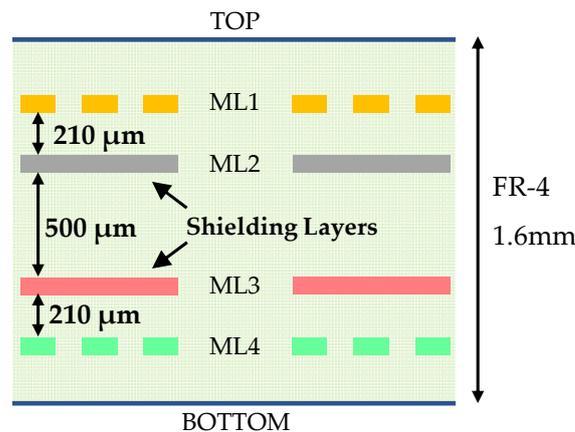| Pulse Transformer	Type	Description
	Large shield	Filled large shielded layers that cover an area larger than the winding periphery.
	Mirror winding shield	Duplicated primary and secondary windings that screen the exact winding shape.

Figure 13. Pulse transformer section view.

3.4. Dv/Dt Immunity Test

With a motive of simulating before fabricating, the reliability of operation of the modeled transformers and their endurance to steep dv/dt of 125 kV/μs, which simulates severe switching conditions of power semiconductors, the designs were co-simulated in ANSYS Circuit design software. The objective was to evaluate the merit of grounded electrostatic screens and test the transformers' immunity to sharp dv/dt occurrence when driving a 1200 V SiC MOSFET using a 100 kHz frequency PWM signal. The imported Q3D subcircuit revealed the ports correlated to nets assigned in the latter tool and are shown as an N-port device.

At IETR lab, a Haefely generator was used to simulate a dv/dt incident; the signal outcome of a 125 kV/μs potential variation was exported from the generator and imported to a piecewise linear source simulated in ANSYS Circuit, aiming to originate a legitimate simulated framework as reproduced in Figure 14.
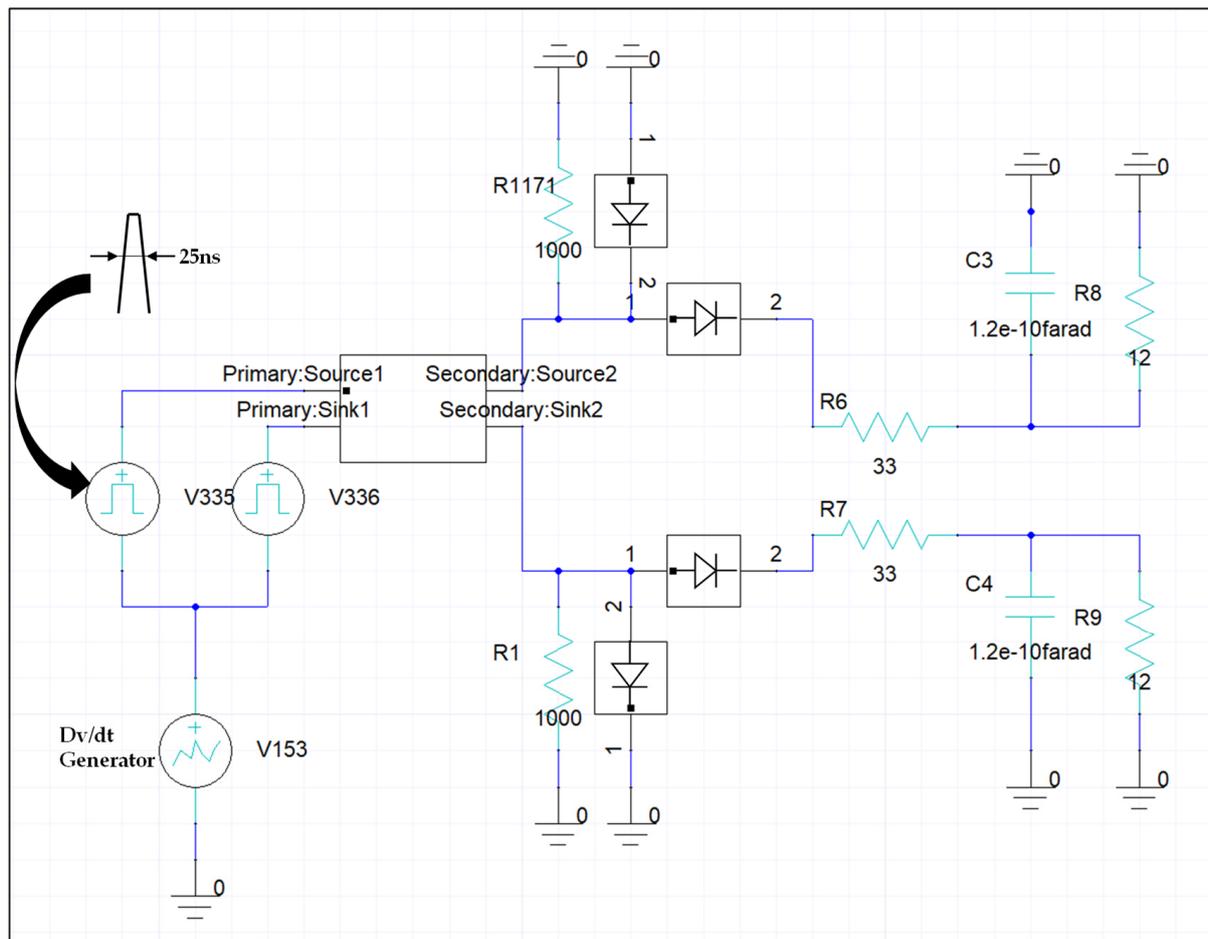
Figure 14. Sustainability of planar transformer to 125 kV/μs dv/dt simulated in ANSYS Circuit Design.

The generated noise results of all the modeled transformers after dv/dt test application are summarized in Table 3 below.

Table 3. Abrupt dv/dt immunity test results for modelled transformers.

Transformer Type	Noise (V)	Assembly Selection
Unshielded	0.8031	X
Typical shield	0.5778	ding52
Large shield	0.6527	X
Mirror winding shield	0.6452	X

With phenomenal results for the typically shielded transformer, with interwinding capacitance of 1.6 pF compared to 2.2 pF for the unshielded planar transformer, it was appointed to be analytically examined and experimented on to validate its dv/dt immunity. It is worth mentioning that after ten adaptive passes, the total number of triangles for a converged CG matrix with a high solution order and a default percent refinement per pass amounted to 108,506 triangles. As for the mesh statistics, the total number of elements created for a CG solution was 184,876.

4. Experimental Authentication

The typical shielded transformer was manufactured to be tested at the IETR lab under the previously mentioned conditions, intending to inspect dv/dt immunity, as shown in Figure 15, and monitor safe operation when integrated in the gate driver card.
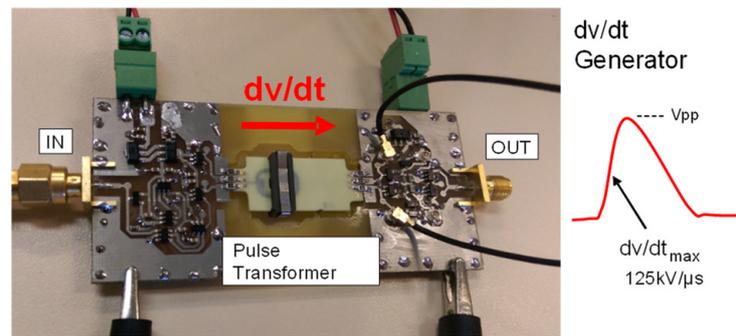
Figure 15. Experimental evaluation of typical shielded pulse transformer toleration to high dv/dt.

Figures 16 and 17 below correlate the experimental and simulated results after a high dv/dt application between the primary and secondary grounds whilst transmitting a set pulse. Figure 17 reveals convenient experimental and simulation results of 0.62 V and 0.5778 V, respectively. The values were much less than the threshold voltage (VT+) of the Schmitt-trigger or logic gates [50].

Figure 16. Experimental vs. simulated high dv/dt application.

Figure 17. Experimental vs. simulated dv/dt immunity of a typically shielded transformer.

5. Conclusions and Future Scope
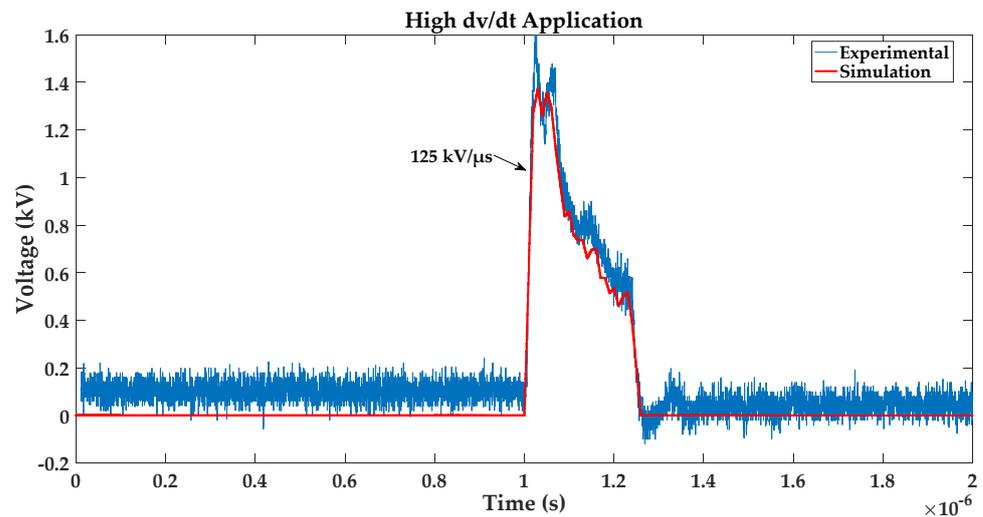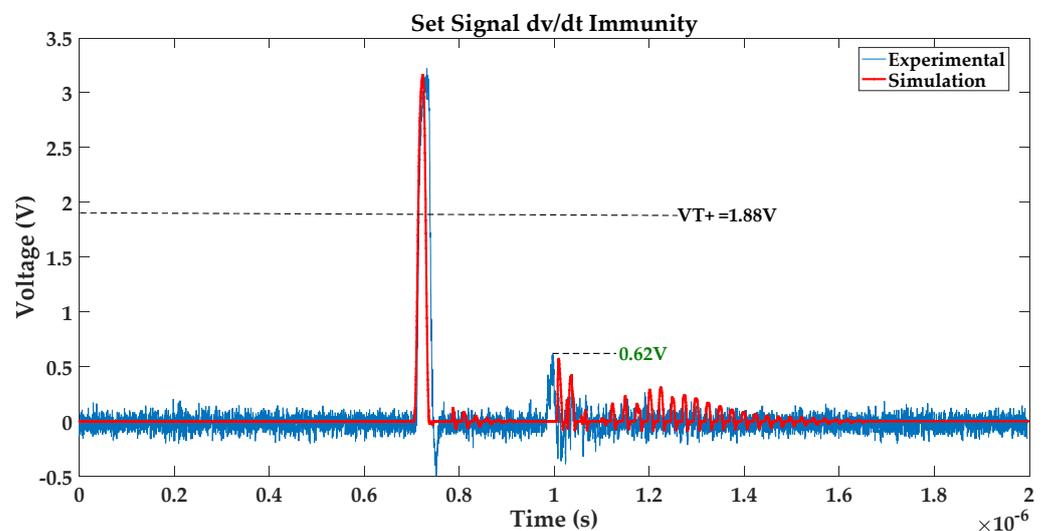
The root cause of CM noise in planar transformers is the existence of stray capacitances between the primary and secondary windings. This uncertain performance can become evident by the exploitation of adequate software tools such as ANSYS Q3D Extractor to derive the parasitic RLGC parameters and further analyze the transformer. The utilization of the aforementioned design software allows the prediction of the behavior of planar transformers for forthcoming design experimentations.

This paper demonstrated the importance of adding grounded typical shielding layers to a pulse transformer to drain the pulsating currents to ground, thus guarding EMC standards and ensuring gate driver card reliability. This was validated by the decrease in the stray capacitance from 2.2 pF for the unshielded transformer to 1.6 pF for the typically shielded one, which led to improved dv/dt susceptibility decreasing from 0.8 V to 0.6 V.

Continuing studies will demonstrate an equivalent electronic circuit model of the analyzed planar transformer based on S Parameter analysis and extracted RLGC values. The transformer, in addition to the Haefely generator exploited, will be presented as an equivalent circuit model to further validate the simulation attained by ANSYS Circuit design. The modeling of the transformer in ANSYS Circuit will be based on the reduce matrix option in ANSYS Q3D Extractor to extract the essential parameters.

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