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Variable-Frequency Pulse Width Modulation Circuits for Resonant Wireless Power Transfer

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Abstract: In this paper, we develop a variable-frequency pulse width modulation (VFPWM) circuit for input control of 6.78-MHz resonant wireless power transfer (WPT) systems. The zero-voltage switching control relies on the adjustments of both duty cycle and switching frequency for the class-E amplifier used in the WPT as the power transmission unit. High-frequency pulse wave modulation integrated circuits exist, but some have insufficiently high frequency or unfavorable resolution for duty cycle tuning. The novelty of this work is the VFPWM circuit design that we put together. A voltage-controlled oscillator (VCO) of radio frequency and capacitor-coupled difference amplifiers are used to simultaneously perform the frequency and duty cycle tuning required in resonant WPT applications. Different circuit topologies of VFPWM are compared analytically and numerically. The most favorable circuit topology, enabling independent control of the frequency and duty cycle, is employed in experiments. The experimental results demonstrate the validity of the novel VFPWM, which is capable of operating at 6.78-MHz and has a duty ratio adjustable from 20% to 45% of the range applicable in the resonant WPT applications.

Keywords: wireless power transfer (WPT); class-E amplifier; voltage-controlled oscillator (VCO); variable-frequency pulse width modulation (VFPWM); difference amplifier

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1. Introduction

Wireless power transfer (WPT) [1] offers a novel means of delivering energy from a power source to a target load through the air instead of the wire that is conventionally used for electricity-powered devices. The WPT method has excellent flexibility and non-contact characteristics. In the near future, it will be an ideal technical solution for powering electrical equipment in various applications within certain fields; for example, it will be ideal for portable electronic devices, implantable medical devices, integrated circuits (ICs), solar-powered satellites, electric vehicles, and unmanned aerial vehicles. Inductive power transfer (IPT) is based on the changing magnetic field generated by alternating currents in the primary coil when the voltage and current induced through the air gap in the secondary coil. IPT is the most widely used WPT technology.

The class-E power amplifier [2,3] is simple and highly efficient in WPT applications, providing an additional degree of design freedom that enables optimal WPT operation over a wide range of operating conditions [4]. However, class-E power amplifiers still suffer from sensitivity to the changes in load impedance values due to changing distance from the receiver to the transmitter or changes in the orientation of the receiver. Compensation methods include replacing the capacitor on the receiver side and adjusting the switching frequency, as proposed in [3], controlling the duty cycle and the DC feed inductance, as proposed in [5,6], and implementing a voltage-controlled capacitor and a NIC (Negative

Impedance Converter), as proposed in [7]. High efficiency can be achieved by applying zero-voltage switching (ZVS) and zero-current switching (ZCS) by monitoring and tuning the inductive link dynamically. The ZVS produces soft switching at a switching frequency in the megahertz range. Furthermore, the impedance matching approach [8], charging/discharging the ultra-capacitor bank [9], and regulating the self/mutual inductance [10] are useful for tracking the maximum efficiency and improving system stability. Class-E power amplifiers belong to the class of high-frequency, high-efficiency electronic power circuits [11,12] that simultaneously consider the effects of the transistor's parasitic elements [13,14].

Class-E power amplifiers use transformers with loosely coupled windings, where the coupling coefficient k can range from 0 to 0.9. Changes in the coupling coefficient over a wide range may cause the inverter to operate under non-ZVS conditions, thereby decreasing the efficiency. The challenging task is to ensure ZVS operation over a wide range of coupling coefficients. Because operation occurs in a relatively high-frequency range, the power efficiency is limited by the switching device and the associated control scheme. Compared with silicon-based devices, GaN high-electron-mobility transistors (HEMTs) have a much lower gate charge and lower output capacitance. GaN HEMTs have excellent performance for input signals with different duty cycles, making it possible to realize high-efficiency operations and considerably improve efficiency [15,16]. The currents flowing through the magnetizing inductance and load are distributed such that the transistor operates at ZVS over a wide range of loads and coupling coefficients. The adjustable duty cycle control scheme achieves maximum power transfer in the resonant wireless power transfer system.

The pulse width modulation (PWM) duty control method is a widely used approach in IC design because digital signal processors can easily provide the required signal. However, most platforms for generating PWM signals only support applications in the tens of kilohertz range. These solutions are not suitable for applications where GaN operates in the megahertz frequency range. One means of overcoming this limitation is using a field-programmable gate array (FPGA) device, which can generate high-precision PWM signals with key parameters such as duty cycle and frequency even if the operating frequency increases to tens of megahertz [17]. The main advantages of FPGA-based controllers are rapid response, precise switching, and flexible adjustment of the dead time and switching frequency. These advantages are suitable for driving numerous semiconductor-switching devices in practical applications. Tavares et al. [18] presented a static power converter developed using an FPGA platform; this converter was able to generate a PWM gating signal with a frequency reaching 2 MHz for driving GaN power field-effect transistors (FETs).

PWM is usually implemented using a voltage comparator that compares a reference voltage with a generated sawtooth signal. However, when the operating frequency increases, the comparator should complete the comparison within a few tens of nanoseconds. This causes PWM controllers based on the ramp comparator to malfunction, meaning that additional effort must be spent to adapt to megahertz operation. Digital PWM (DPWM) is implemented using a counter and comparison structure and resembles analog PWM based on sawtooth signals. The functionality is as follows: if the duty cycle command exceeds the counter value, which is equivalent to a sawtooth signal, the output is ON; when the counter reaches the duty cycle, the output turns OFF. Compared with the sequential encoding method, one-hot encoding and Gray encoding methods with fewer states are used to create varying pulses [19]. However, high resolution cannot be obtained, because the minimum time step is equal to the clock period of the counter. In addition, the power consumption is directly proportional to the clock frequency [20]. To address this issue, a delay-line-based voltage-to-duty-cycle (V2D) technique was presented that did not use any comparators. Cheng et al. [21] presented a delay-line DPWM architecture based on a phase-locked loop (PLL) and carry chain flag. This architecture had three parts: the first coarse delay module based on a counter, the second coarse delay module based on a PLL,

and the fine delay module based on a carry chain. The main purpose is to compensate for the propagation delay through the tool command language, because propagation delays in the internal logics and interconnects may increase the duty cycle, thereby affecting the regulation performance of the converter, especially when the delay is of the same magnitude as the switching period. The duty-cycle increment phenomenon caused by superposition of critical path delays affects the regulation performance of converters with a switching frequency of tens of megahertz or higher. Huang et al. [22,23] used two voltage-to-delay cells to convert the voltage difference into a delay-time difference. A charge pump was used to charge or discharge the loop filter depending on whether the feedback voltage was larger or smaller than the reference voltage. A V2D controller based on delay-line control techniques was implemented to replace the classical ramp-comparator-based V2D controller and achieve a wide duty cycle, which was employed in a digitally controlled voltage-mode buck converter. The main advantages of delay-line DPWM are high resolution and low power consumption. However, this method exhibits low linearity and non-monotonic behavior in some cases. For a class-E dc–dc converter, the accuracy of the frequency, phase, and pulse width of the signal is critical in circuit applications.

Within the similar context of delay-line DPWM, this paper proposes a PWM method enabling a switching frequency of up to 7 MHz for driving a GaN power FET. In the first stage, a voltage-controlled oscillator (VCO) is used to generate periodic square signals of variable frequency. The frequency of the output voltage can be varied using the input dc voltage. The duty cycle generator of the second stage is designed to have two functions: to generate a duty cycle of less than 50% and achieve wide range correction. This paper is organized as follows. Section 2 briefly introduces the class-E amplifier circuit and the specifications and characteristics of the GaN FET. Section 3 describes the proposed circuit and provides derivations. Then, we illustrate and simulate different capacitor-coupled difference amplifiers (CCDAs) in Section 4. The experimental results obtained to validate the duty generation circuit are provided in Section 5. Finally, the conclusions and some high-frequency GaN-based potential power applications that could take advantage of the present work are presented in Section 6.

2. Class-E Amplifier Circuit and the Gate Drive

The high-level block diagram for the resonant wireless power transfer system shown in Figure 1a consists of four modules, including the tuning strategy for the WPT, the xCCDA design, the VFPWM feedback control, and the class-E amplifier for wireless power transfer. The class-E amplifier as shown in Figure 1b, which consists of a VFPWM circuit that generates the switching signal to the gate drive, is used in resonant WPT applications. The nominal values of the circuit parameters on the switching power supply side (or the transmitter side) and the equivalent values on the impedance load side (or the receiver side together with the transmitter antenna) are shown in Table 1. The load impedance is simplified into a resistor R_L with a capacitor C_2. The capacitor C_{DS} is the parasitic capacitor of the D-mode GaN HEMT. A charge pump gate drive with output voltage v_{GS} from 0 to a negative voltage (e.g., -7 V) is used to turn the GaN HEMT on and off according to the signal v_s from 5 to 0 V. The GaN HEMT, which has no body diode, is periodically switched to form a sinusoidal resonant current i_2. In the equivalent circuit, as shown Figure 1, the power transfer efficiency (PTE) is defined as the output power on the receiver $P_{out} = i_2 v_L$ divided by the input power on the transmitter $P_{in} = i_1 V_{DD}$. The switching of the GaN HEMT transistor M_1, including the switching frequency and turn-on time duty, directly determines the distance and efficiency of the WPT application. The experimental layout is shown in Figure 2. In our previous paper [24], the governing equations of the ZVS control for a class-E WPT unit was derived. The ZVS and its derivative, the zero-current switching (ZCS), conditions are achieved by adjusting the duty cycle and resonant frequency simultaneously. In the previously published paper [25], a minimum power input control strategy was proposed, which results in the switching frequency f_o and the duty

cycle δ the WPT being based on empirical data or equations that can yield the optimal power transfer efficiency.

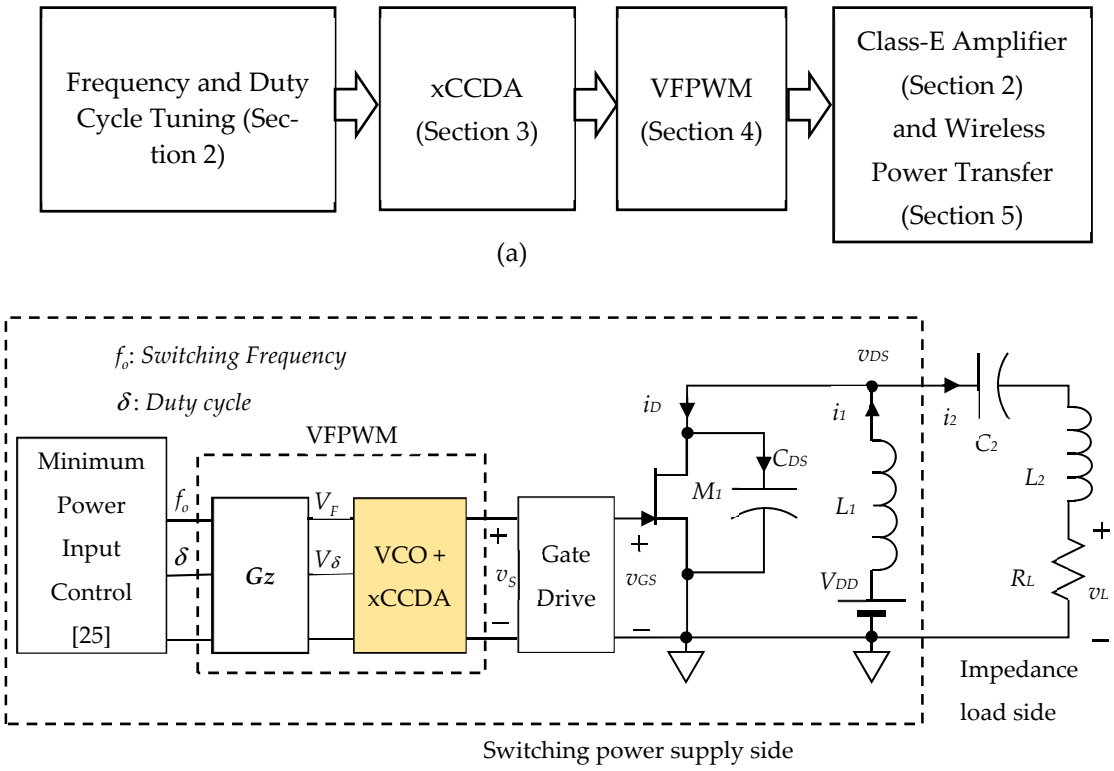


Figure 1. Implementation of the WPT system: (**a**) high-level block diagram and (**b**) class-E amplifier as the power transmission unit.

Table 1. Parameters used in the class-E amplifier model and charge pump gate drive.

Symbol	Parameter	Value	Unit
R_L	Equivalent Loading	5	kΩ
C_2	Equivalent Coupling Capacitance on PRU	75	pF
L_2	Equivalent Inductance of the PRU	8	μH
L_1	Inductance of the PTU	47	μH
C_{DS}	Parasitic Capacitance of GaN HEMT	75	pF
$R_{G,p}$	Turn-on Gate Resistance	12	Ω
$R_{G,n}$	Turn-off Gate Resistance	30	Ω
C_C	Charge Pump Capacitance	5	nF
C_{GS}	Parasitic Capacitance of GaN HEMT	140	pF
I_R	Diode Reverse Saturation Current	50	μA

The switching frequency f_o and the duty cycle δ are subsequently converted into the input voltages of the PWM generator, which consists of the VCO and capacitor-coupled difference amplifier to form a variable-frequency PWM module. The VFPWM module generates a switching signal v_S to the gate driver. In Figure 1, G_z is the zero-order hold transfer function matrix that converts the switching frequency f_o and the duty cycle δ into the corresponding voltages V_F and V_δ, which is described in detail in the following sections with respect to different VFPWM topologies.

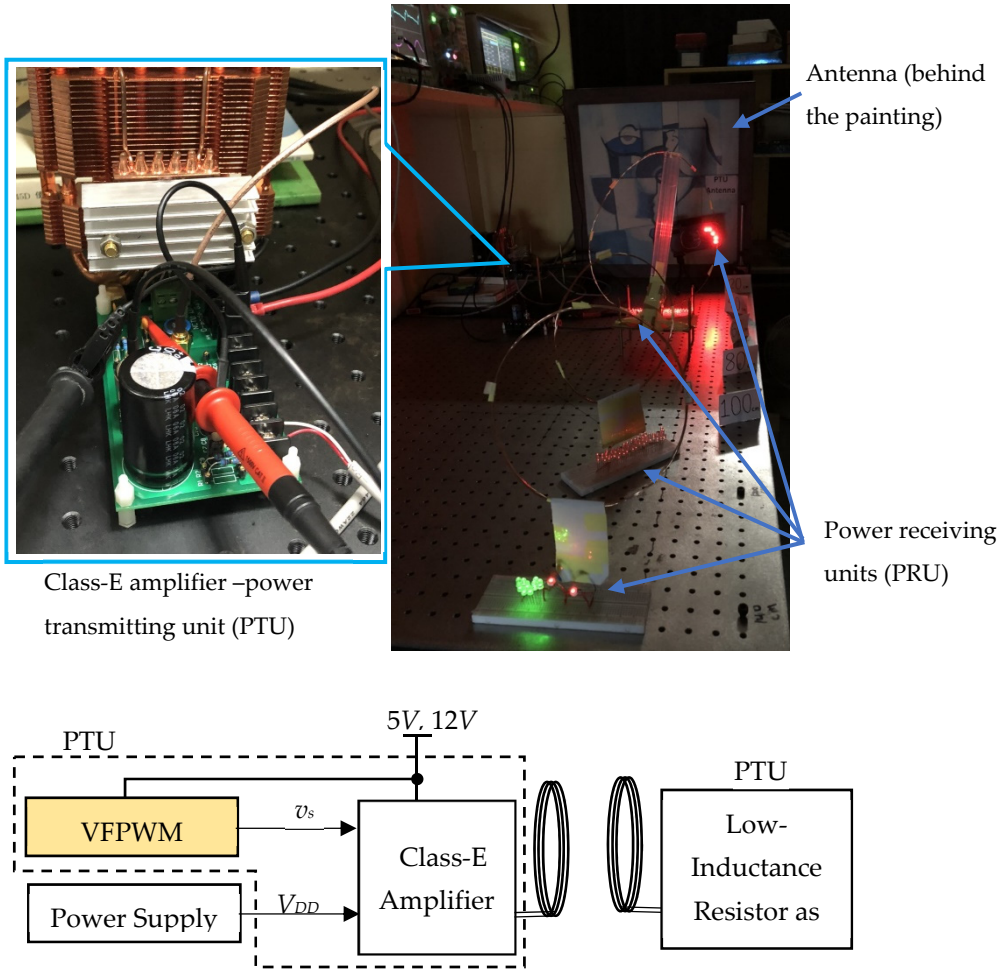


Figure 2. Experimental layout.

2.1. Charge Pump Gate Drive

The charge pump gate drive presented by Okamoto [26] is useful in class-E amplifiers. The previous disadvantage of charge pump circuits—the leakage of current through the diode reverse saturation current—is not a problem because of the high-frequency switching. However, the class-E amplifier still suffers the effect of C_{GD} linking to the high voltage switching of v_{DS}. As illustrated in Figure 3, we first assume that v_{DS} floating. The corresponding gate drive design parameters are presented in Table 1.

As shown in Figure 3, the gate drive receives the PWM signal from a PWM circuit. This PWM circuit is capable of operating at an adjustable frequency around 6.78 MHz, and the duty cycle is adjustable from 20% to 50%, meaning that the gate drive can be successfully switched to perform the WPT task. High-frequency PWM ICs such as the TI SLUS489 with the maximum frequency of 2 MHz cannot meet the required frequency of 6.78 MHz. The other commercially PWM IC, the AD9560, is a high-speed, digitally programmable pulse width modulator with an output pulse width proportional to an 8-bit data input value. The pulse width can be changed every clock cycle by up to 50 MHz. The drawbacks of this IC include the requirement of a high-speed digital processor such as the ESP8266 Wi-Fi module to fulfill the 6.78-MHz control, which means that it cannot be used in low-cost applications, and that the 8-bit resolution for the output pulse width is insufficient for resonant tuning in 6.78-MHz resonant WPT applications in practice. The purpose of this paper is to construct a low-cost, PWM, high-frequency-resolution circuit feasible for 6.78-MHz resonant WPT applications. A VCO or voltage-to-frequency converter may be useful for the frequency control needed for resonant WPT; however, the ICs are usually designed for a 50% duty cycle. To achieve WPT with a transmission of 100 cm and greater,

such as that shown in Figure 2, adjustments to both the frequency and duty cycle are required. We require a circuit that converts the VCO signal into the variable-frequency pulse width modulation (VFPWM) wave form. In the following sections, we first introduce the difference amplifier coupled with capacitors that can convert a 50% duty cycle square wave into a PWM signal.

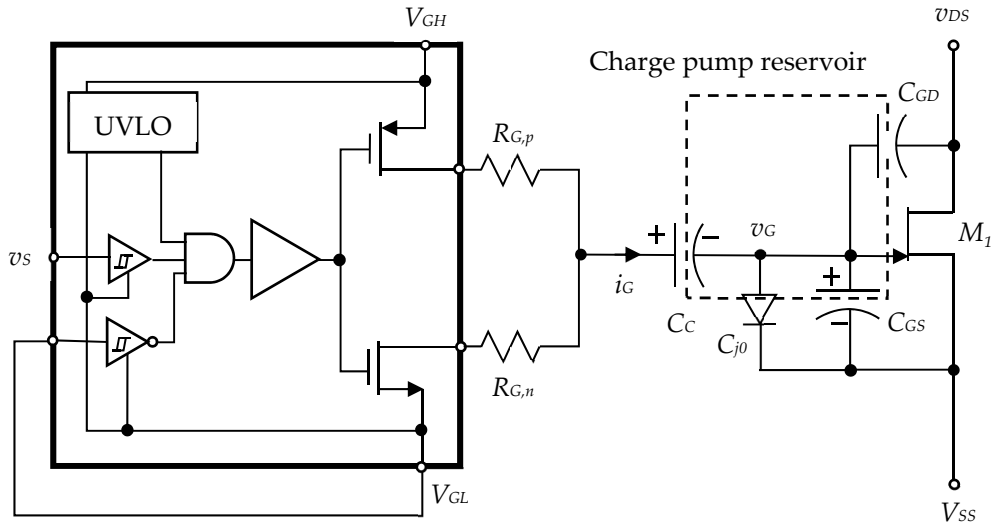


Figure 3. Gate drive design.

2.2. The Minimum Power Input Control Strategy

By controlling the duty ratio δ and the switching frequency simultaneously, minimum power input control [25], which trades off the PDL (Power Delivered to Load) for the switching loss of the GaN HEMT, can be used to obtain the optimal PTE (Power Transfer Efficiency). The minimum power input control strategy, which concerns the feedback from PRU (Power Receiving Unit), consists of the following steps.

Step 1. According to the PRU feedback regarding the distance between the PTU (Power Transmitting Unit) and PRU and the power transfer requirement from the PRU, we determine the input voltage V_{DD}. The input voltage, according to the experimental data [24], as shown in Figure 4, should be tuned to a low voltage for short-range WPT and a high voltage for long-range WPT.

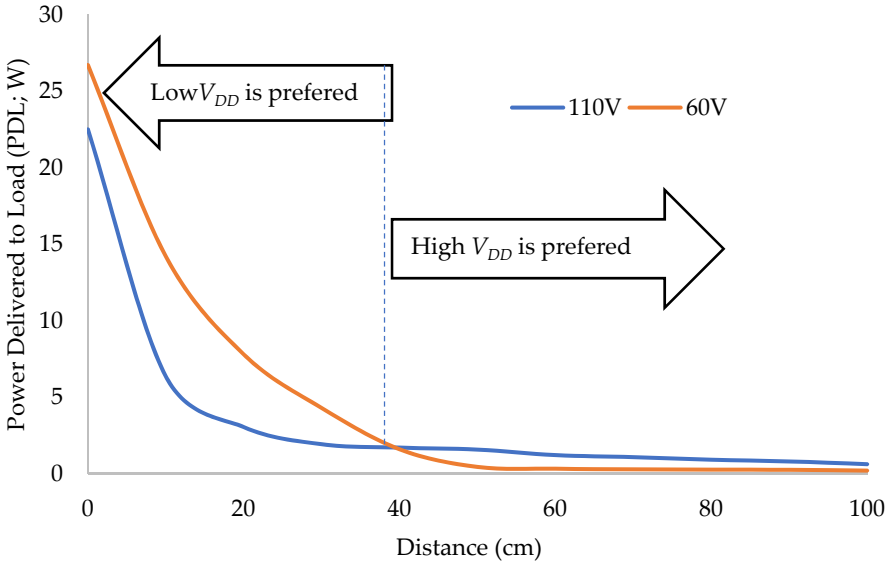


Figure 4. PDL vs. distance and input voltage V_{DD}.

Step 2. The input power of the PTU is determined from the feedback power requirement from all PRUs. Consequently, the duty cycle δ (or duty ratio %) is determined from the input power and the given input voltage V_{DD} from Step 1. As shown in Figure 5, which is interpolated in [25], it is observed that the duty ratio δ% increases monotonically, in general, with increasing PTU input power.

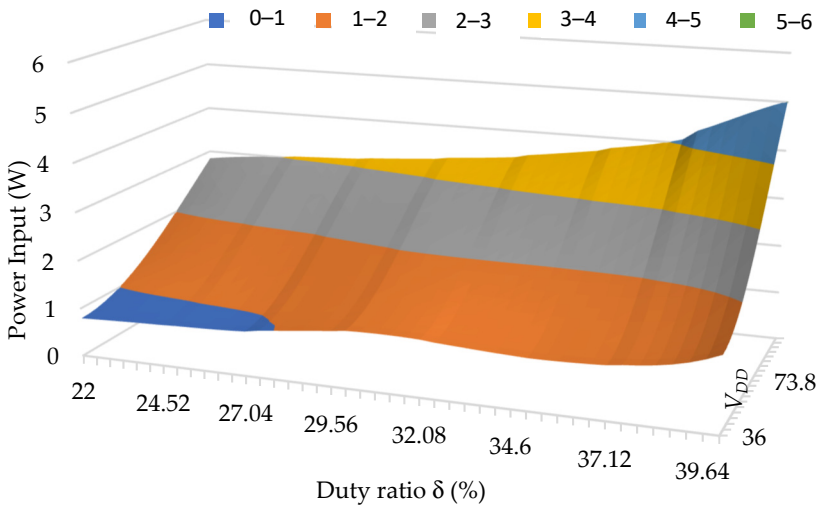


Figure 5. Power input vs. duty ratio % and Input voltage V_{DD}.

Step 3. From the given input voltage V_{DD} and the duty ratio δ% calculated in step 2, we determine the switching frequency f_o according to the empirical function shown in Figure 6, which is interpolated in [25].

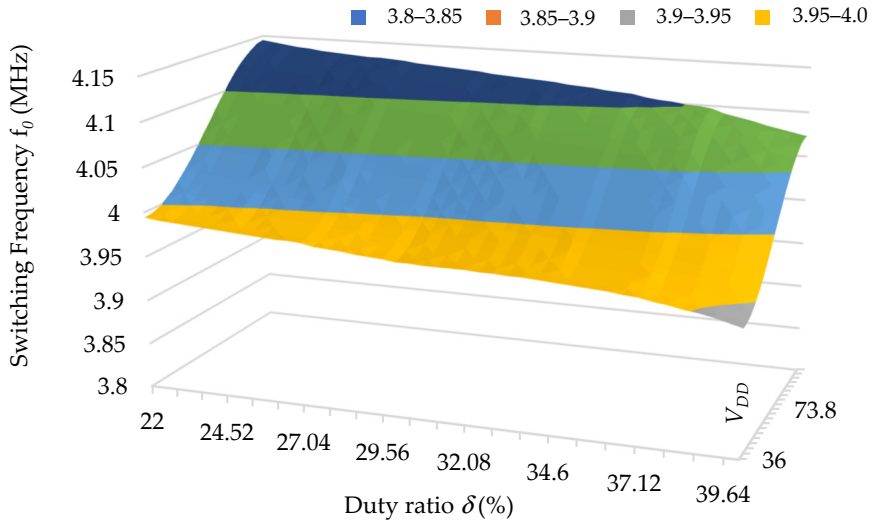


Figure 6. Desired switching frequency vs. duty ratio δ% and input voltage V_{DD}.

The goal of the minimum power input control strategy is to optimize the power efficiency of the WPT system when multiple PTUs and multiple PRUs are interacting. The control strategy will calculate the best switching frequency f_o and duty ratio δ% for each individual PTU.

2.3. Parameters of the Class-E Amplifier and WPT System

Two arrangements of PTU/PRU inductor settings are used in the experiments. The data were reported in [24] and are reproduced in Table 2. The distance between the PTU and the PRU, as well as the orientation of the PRU toward the PTU, affects the coupling

coefficient in the wireless power transfer. The tuning of both switching frequency f_o and the duty ratio δ must respond to the coupling coefficient change dynamically in order to achieve the impedance matching condition. The nominal input/output parameters of the class-E amplifier and WPT system in this research are shown in Table 3. The nominal values are only reference values for typical 10 W and 40 cm distance resonant WPT applications.

Table 2. Coil specifications used in the WPT experiments in this paper [24].

Inductor ID	Inductance (uH)	Capacitance (pF)	Resistor (Ohm)	Q Factor	SRF (MHz)
Tx1	8.87	28.54	0.128	4.364	10.00
Tx2	8.88	28.53	0.128	4.342	9.99
Rx1	9.03	27.7	0.081	7.06	10.06
Rx2	9.05	27.9	0.074	7.66	10.02

Table 3. The nominal input/output parameters of the class-E amplifier and WPT system.

Symbol	Unit	Nominal Value	Min. Value	Max. Value
V_{DD}	Volt	108	36	300
f_o	MHz	4.1	3.8	4.4
δ (%)		30	20	40
PDL *	Watt	5	0.1	20
v_{DS}	volt	400	100	800
i_D	Ampere	0.05	0.01	0.2

PDL (Power Delivered to Load) *: based on a single PTU to multiple PRUs and calculated from summation on all the individual power received by the PRUs.

3. CCDAs

Two types of CCDA, common mode and difference mode, are discussed in detail in this section.

3.1. Difference-Mode CCDA

The difference-mode CCDA (dCCDA), illustrated in Figure 7, consists of the standard arrangement of a difference amplifier and a capacitor inserted between the noninverting and inverting terminals. The capacitor is referred to as a differential-mode capacitor.

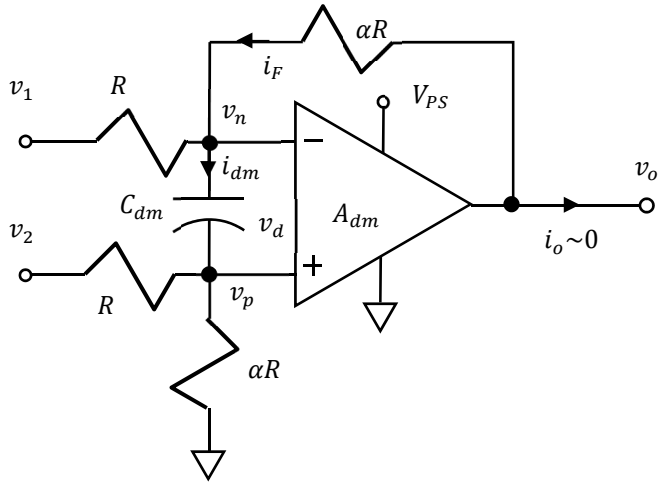


Figure 7. The dCCDA circuit.

Assuming an operational amplifier of zero offset voltage, an output resistance that is negligibly small, and an input resistance that is much larger than R, we obtain

$$i_{dm} = \frac{(1+\alpha)v_p(s) - \alpha v_2(s)}{\alpha R} \tag{1}$$

The difference voltage is

$$v_d(s) = -\frac{i_{dm}}{sC_{dm}} = \frac{\alpha v_2(s) - (1+\alpha)v_p(s)}{\alpha R C_{dm} s} \tag{2}$$

or

$$v_p(s) = \frac{\alpha v_2(s) - \alpha R C_{dm} s v_d(s)}{1+\alpha} \tag{3}$$

The output voltage is

$$v_o(t) = \begin{bmatrix} \min(V_{PS},\ A_{dm}v_d(t)) & \text{if } v_d(t) > 0 \\ 0 & \text{if } v_d(t) \le 0 \end{bmatrix}$$

The voltage on the inverting terminal of the operational amplifier is then derived as

$$v_n(s) = v_p(s) - v_d(s)$$

Additionally, when $v_d(t) > 0$, we have

$$i_{dm} = \frac{\alpha v_1(s) + v_o(s) - (1+\alpha)v_n(s)}{\alpha R} \tag{4}$$

If $v_d(t) \le 0$, we have

$$i_{dm} = \frac{\alpha V_1(s) - (1+\alpha)V_n(s)}{\alpha R}$$

Substituting Equation (1) into (4)—that is, when $v_d(t) > 0$ and $v_o(t) = A_{dm}v_d(t)$ are assumed—we have

$$2(1+\alpha)v_p(s) - \alpha v_1(s) - \alpha v_2(s) = (A_{dm} + 1 + \alpha)v_d(s) \tag{5}$$

Let $T_{dm} = \alpha R C_{dm}$; Equation (5) can then be expressed as

$$(2(1+\alpha)T_{dm}s + (A_{dm}+1+\alpha)(1+\alpha))v_p(s) = \alpha T_{dm} s v_1(s) + ((A_{dm}+1+\alpha)\alpha + \alpha T_{dm}s)v_2(s)$$

Assuming that $A_{dm} \gg (1+\alpha)$, and letting $T'_{dm} = T_{dm}/A_{dm}$, the above equation is simplified to

$$v_p(s) = \frac{\alpha}{1+\alpha}\left(\left(\frac{T'_{dm}s}{1+2T'_{dm}s}\right)v_1(s) + \left(\frac{1+T'_{dm}s}{1+2T'_{dm}s}\right)v_2(s)\right)$$

Equation (2) yields

$$v_d(s) = \alpha\frac{v_2(s) - v_1(s)}{A_{dm}(1+2T'_{dm}s)} \tag{6}$$

Substituting Equation (1) into (5) and then Equation (3) for $v_d(t) \le 0$, we have

$$v_d(s) = \alpha\frac{v_2(s) - v_1(s)}{(1+\alpha) + 2T_{dm}s} \tag{7}$$

Let $v_2(s) = V_Z/s$ be a square-wave pulse train, V_Z range from 0 to V_{PS}, and $v_1(s) = V_{ref}/s$, where $0 < V_{ref} < V_{PS}$; the difference voltage response for $v_d(t) > 0$ is then obtained as

$$v_d(t) = \begin{bmatrix} \frac{\alpha}{A_{dm}}\left(1 - e^{\frac{-t}{2T_{dm}'}}\right)\left(V_Z - V_{ref}\right) + v_d(0) & \text{if } v_d(t) > 0 \\ \alpha\left(1 - e^{\frac{-(1+\alpha)t}{2T_{dm}}}\right)\left(V_Z - V_{ref}\right) + v_d(0) & \text{else} \end{bmatrix} \quad (8)$$

The corresponding output of the operational amplifier is

$$v_o(t) = \begin{bmatrix} \min\left(V_{PS},\ \alpha\left(1 - e^{\frac{-t}{2T_{dm}'}}\right)\left(V_Z - V_{ref}\right) + v_o(0)\right) & \text{if } v_d(t) > 0 \\ 0 & \text{else} \end{bmatrix} \quad (9)$$

Figure 8 illustrates the response of v_o and v_d when the resistance R is large. In other applications with a low R, the difference amplifier is governed by the amplifier equation as follows:

$$v_o(t) = \min\left(V_{PS},\ \alpha\left(V_Z - V_{ref}\right)\right) \quad (10)$$

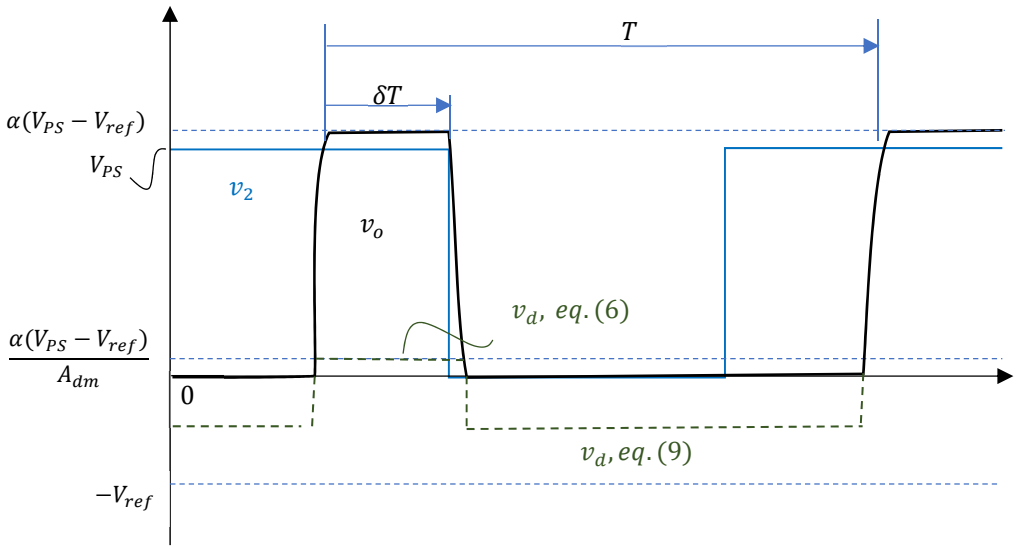


Figure 8. Response of a dCCDA with large resistance.

The amplification is A_{dm} if $v_d(t) > 0$; the amplification is unity if $v_d(t) \leq 0$. The time constant in the case of $v_d(t) \leq 0$ is $A_{dm}/(1 + \alpha)$ times larger than that when $v_d(t) > 0$. The analytical results are depicted in Figure 8.

3.2. Common-Mode CCDA

The common-mode CCDA (cCCDA), illustrated in Figure 9, consists of a standard arrangement of a difference amplifier and two capacitors added to the terminals. The capacitors are referred to as common-mode capacitors. Assuming the operational amplifier has zero offset voltage, the output resistance is negligibly small, and the input resistance is much larger than R, we obtain

$$i_{cm,p} = \frac{T_{cm}s}{(1 + \alpha + T_{cm}s)}\frac{v_2(s)}{R} \quad (11)$$

where:

$$T_{cm} = \alpha R C_{cm}$$

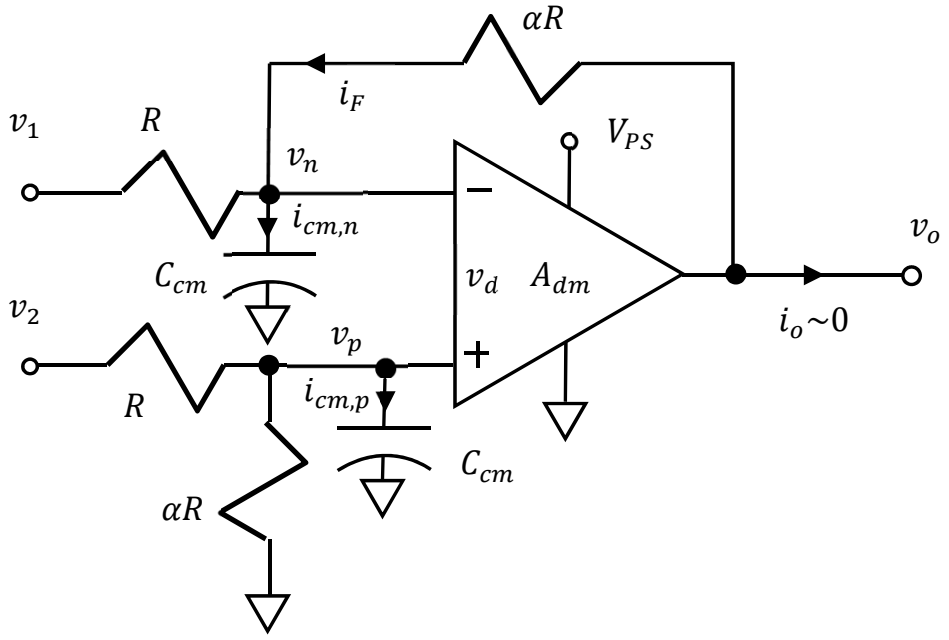


Figure 9. The cCCDA circuit.

From the inverting terminal, the following is obtained:

$$i_{cm,n} = \frac{T_{cm}s}{(1+\alpha+T_{cm}s)}\frac{v_1(s)}{R} + \frac{T_{cm}s}{(1+\alpha+T_{cm}s)}\frac{v_o(s)}{\alpha R} \tag{12}$$

The difference voltage is

$$v_d = \frac{\alpha v_2(s)}{(1+\alpha+T_{cm}s)} - \frac{v_o(s)}{(1+\alpha+T_{cm}s)}$$

or

$$v_d(s) = \begin{bmatrix} \frac{\alpha(v_2(s)-v_1(s))}{(1+\alpha+A_{dm}+T_{cm}s)} & \text{if } v_d(t) > 0 \\ \frac{\alpha(v_2(s)-v_1(s))}{(1+\alpha+T_{cm}s)} & \text{else} \end{bmatrix} \tag{13}$$

After the substitution of $v_2(t) = V_Z$ and $v_1(t) = V_{ref}$ for $v_d(t) \leq 0$, the common-mode capacitor starts to charge to a positive voltage from time $t = 0$ in a steady state, such that

$$v_d(t) = \left(1 - e^{\frac{-(1+\alpha)t}{T_{cm}}}\right)\left(V_Z - V_{ref}\right) + v_d(0) \tag{14}$$

When $v_d(t) > 0$, that is, after time $t \geq \beta T$, the voltage of the common-mode capacitor rises for $A_{dm} \gg 1+\alpha$ such that

$$v_d(t) = \frac{\alpha}{A_{dm}}\left(1 - e^{\frac{-(1+\alpha)(t-\beta T)}{T_{cm}}}\right)\left(V_Z - V_{ref}\right) \tag{15}$$

Because $\delta + \beta = 0.5$, after the time $t \geq T/2$, we have $v_2(t) = 0$, and the voltage of the common-mode capacitor decreases.

$$v_d(t) = \left(1 - e^{\frac{-(1+\alpha)(t-T/2)}{T_{cm}}}\right)\left(0 - V_{ref}\right) + v_d(T/2) \tag{16}$$

Consequently, the minimum voltage on the common-mode capacitor is

$$v_d(0) = v_d(T) < 0 \tag{17}$$

Assuming that v_d is negligibly small during the time $T/2 \geq t \geq \beta T$, Equations (14)–(17) yield

$$-e^{\frac{-(1+\alpha)\beta T}{T_{cm}}} V_Z + \left(e^{\frac{-(1+\alpha)\beta T}{T_{cm}}} + e^{\frac{-(1+\alpha)T/2}{T_{cm}}} \right) V_{ref} + V_Z - 2V_{ref} = 0$$

Assuming that $e^{\frac{-(1+\alpha)T/2}{T_{cm}}} \ll e^{\frac{-(1+\alpha)\beta T}{T_{cm}}}$, we obtain

$$\beta = -\frac{T_{cm}}{(1+\alpha)T} \ln\left(\frac{V_Z - 2V_{ref}}{V_Z - V_{ref}} \right) \tag{18}$$

and

$$\delta = \frac{1}{2} - \beta = \frac{1}{2} + \frac{T_{cm}}{(1+\alpha)T} \ln\left(\frac{V_Z - 2V_{ref}}{V_Z - V_{ref}} \right) \tag{19}$$

From Equations (16) and (19), the constraint for V_{ref} is $0 < V_{ref} < V_Z/2$. The smaller the V_{ref}, the higher the duty cycle δ. From Equation (19), it is confirmed that $\delta_{max} = 0.5$, which is identical to the VCO output when V_{ref} = 0 V. The sensitivity of δ with respect to V_{ref} is derived as follows:

$$\frac{\partial \delta}{\partial V_{ref}} = \frac{-6T_{cm}V_Z}{(1+\alpha)\left(V_Z - 2V_{ref}\right)\left(V_Z - V_{ref}\right)T} \tag{20}$$

Equation (20) shows that we must reduce either R or C_{cm} and let α = 1 to ensure small sensitivity of V_{ref} to the duty cycle δ. When $\delta = 0$ and α = 1, the higher bound for V_{ref} is obtained as follows:

$$V_{ref}|_{\delta=0} = \frac{1 - e^{-T/T_{cm}}}{2 - e^{-T/T_{cm}}} V_Z$$

For example, if $T = 1/(4{\cdot}\text{MHz})$, $T_{cm} = 10\ \text{k}\Omega{\cdot}15\ \text{pF}$, and $V_Z = 5$ V, the higher bound is calculated to be 2.24 V.

Let $V_2(s) = V_Z/s$ be a square-wave pulse train, V_Z range from 0 to V_{PS}, and $0 < V_{ref} < V_{PS}$; consequently, the corresponding output is

$$v_o(t) = \begin{cases} \min\left(V_{PS},\ \alpha\left(1 - e^{\frac{-(1+\alpha)t}{T_{cm}'}}\right)\left(V_Z - V_{ref}\right) + v_o(0) \right) & \text{if } v_d(t) > 0 \\ 0 & \text{else} \end{cases}$$

The analytical results are depicted in Figure 10. It is difficult to compare Figures 8 and 10, because they have two similar characteristics: fast charging of the coupled capacitor when the operational amplifier is functioning as a voltage amplifier, and slow charging of the capacitor when the operational amplifier is outputting zero voltage. However, they are different with respect to their time constant during slow charging.

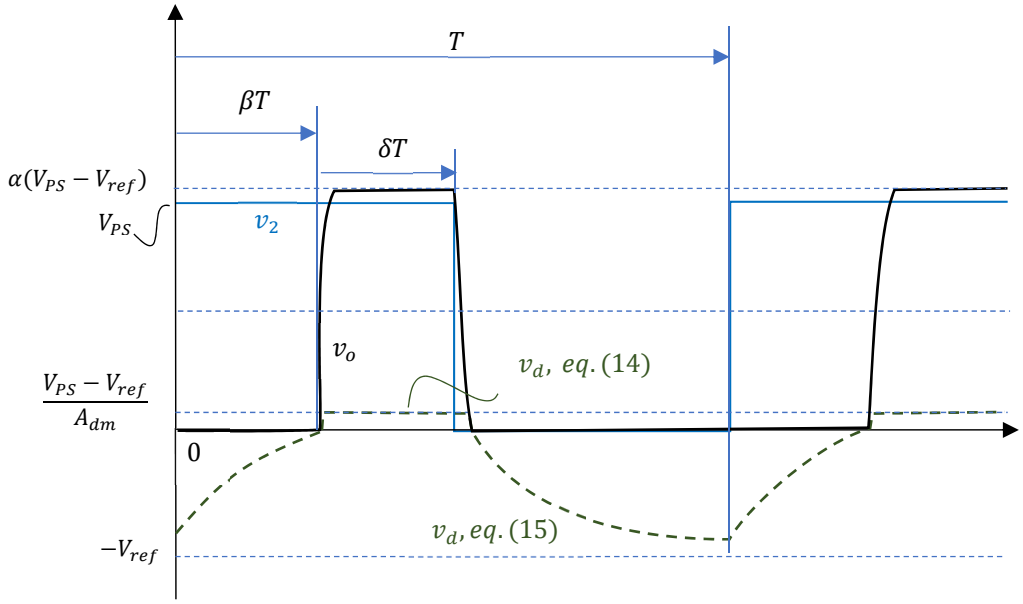


Figure 10. Response of a cCCDA with large resistance.

4. CCDA Application

To validate the applicability of the CCDAs, in this section, two designs are illustrated, analyzed, and applied using the cCCDA and dCCDA.

4.1. VCO to VFPWM Using Low-Resistance dCCDA Feedback

The block diagram of the dCCDA is shown in Figure 11. The transfer function of a low-resistance dCCDA typically yields a difference amplifier unity gain when $\alpha = 1$.

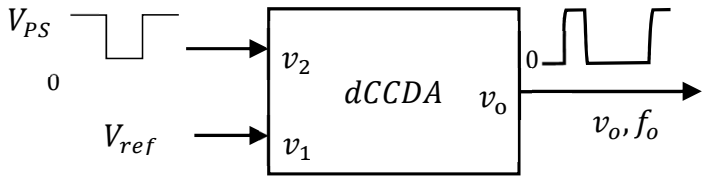


Figure 11. Block diagram of the dCCDA.

The function of a practical VCO, such as the IC-SN54LS628, as shown in Figure 12 as an example, can be simplified into the following expression:

$$f_o = G_{Z0}\left(V_{I(freq)} - g\left(V_{I(rng)}\right)\right) \tag{21}$$

The nonlinear function $g\left(V_{I(rng)}\right)$ increases monotonically with increasing $V_{I(rng)}$, i.e., the voltage input to control the frequency range of the SN54LS628 VCO. When the voltage $V_{I(rng)}$ increases, the feedback signal $g\left(V_{I(rng)}\right)$ increases and the frequency f_o decreases simultaneously. To be consistent with our WPT application shown in Figure 1, we defined $V_F \equiv V_{I(freq)} - g\left(V_{I(rng)}\right)$ and G_{Z0} as the gain of the switching frequency to voltage transfer function.

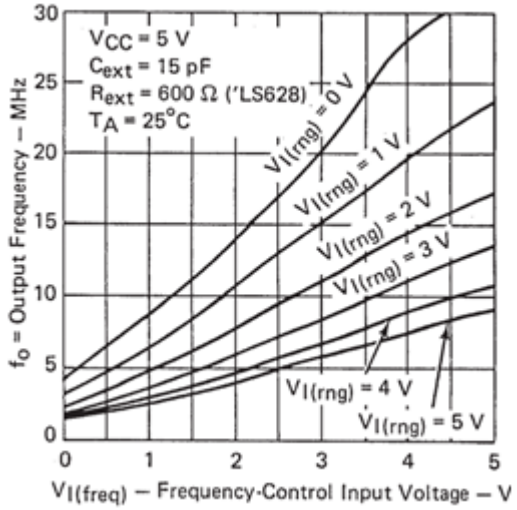


Figure 12. Output frequency versus frequency-control input voltage of the SN54LS628 (courtesy of Texas Instruments Inc., Dallas, Texas).

The output v_o of the dCCDA with low resistance and $\alpha = 1$ is presented as a simple difference amplifier as follows:

$$V_{I(rng)} = v_o = \begin{bmatrix} V_{PS} - V_{ref} & \text{if } V_{PS} > V_{ref} \\ 0 & \text{else} \end{bmatrix}$$

The dCCDA can be derived from the intrinsic parasitic capacitance of the operational amplifier. As shown in Figure 13, when $V_{I(rng)} = 0$, the output of the VCO has a frequency of $G_{Z0}V_F$. When $V_{I(rng)} = V_{PS} - V_{ref}$, the output of the VCO is in the frequency range $G_{Z0}\left(V_{I(freq)} - g\left(V_{PS} - V_{ref}\right)\right)$. The sampling time for v_2 of the dCCDA is then written as follows:

$$T = G_{Z0}\frac{2 + g\left(V_{PS} - V_{ref}\right)/V_{I(freq)}}{V_{I(freq)} - g\left(V_{PS} - V_{ref}\right)} \tag{22}$$

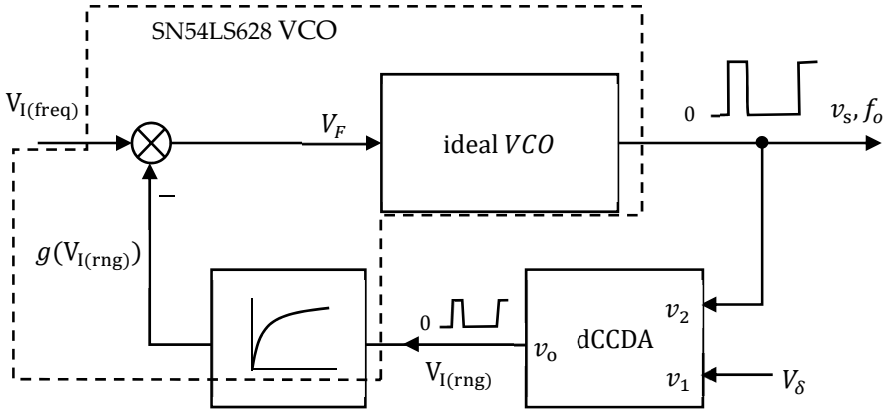


Figure 13. VFPWM with a low-resistance dCCDA feedback to a VCO.

The duty cycle of v_2 of the dCCDA can expressed as

$$\delta = \frac{g\left(V_{PS} - V_{ref}\right)}{2V_{I(freq)} + g\left(V_{PS} - V_{ref}\right)} \tag{23}$$

The switching frequency f_o is

$$f_o = \frac{1}{G_{Z0}} \frac{V_{I(freq)} - g\left(V_{PS} - V_{ref}\right)}{2 + g\left(V_{PS} - V_{ref}\right)/V_{I(freq)}} \tag{24}$$

The VFPWM has a slew rate limit on the voltage output of the dCCDA; however, the slew rate limit due to the need to charge the difference-mode capacitor does not harm the VCO's digital output. By contrast, the slew rate limit can prevent high-frequency noise in the feedback loop to the VCO. In practice, adding some more difference-mode capacitance C_{dm} to the dCCDA is preferable in order to improve the stability of the VFPWM. The corresponding SPICE analysis is shown in Figure 14. In the SPICE circuit model, a VCO with a center frequency of 5.5 MHz, a frequency range of 2.5 MHz, and a sensitivity of 1.0 MHz/V is used. Because the output of the VCO is 1 V, we amplify the output to 5 V before feeding it to the dCCDA. The result shows that the duty ratio is no more than 50%.

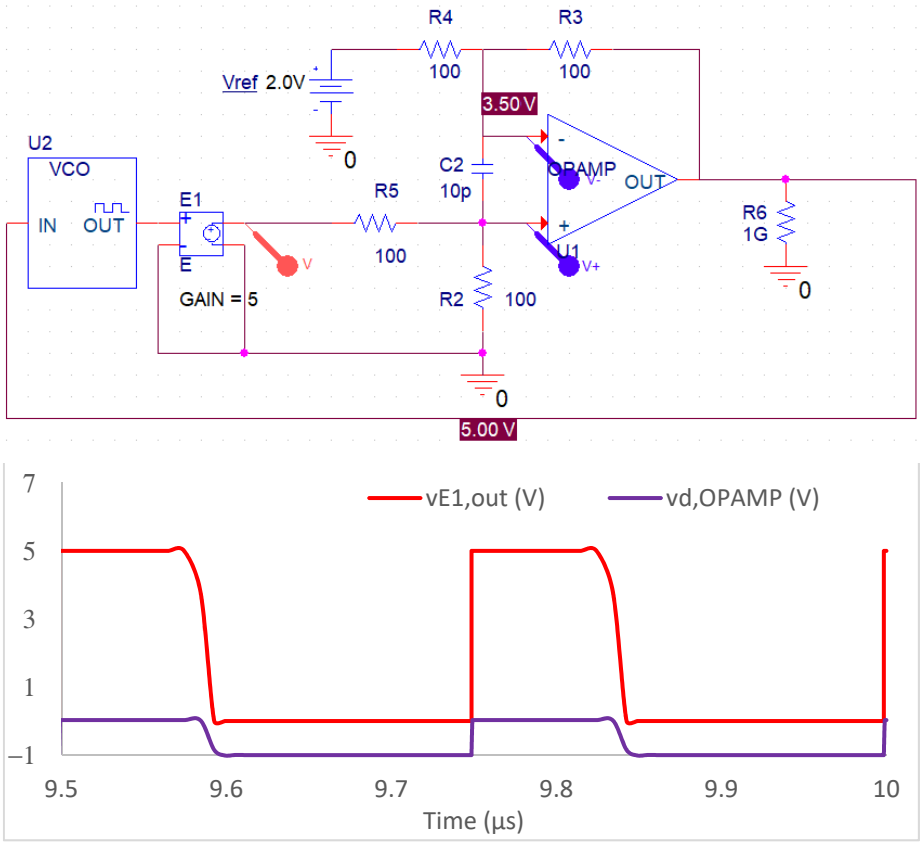


Figure 14. SPICE analysis of VFPWM using dCCDA feedback.

4.2. VCO to VFPWM by Using High-Resistance cCCDA

By having a VCO in series with a cCCDA that converts the 50% duty cycle square wave into PWM, the circuit achieves frequency control by simply adjusting V_F, and the duty ratio is controlled by $V_{ref} = V_\delta$. Compared with Equations (22) and (23), the frequency and duty cycle of the VFPWM using the low-resistance dCCDA are coupled, which increases the complexity of the WPT control, whereas VFPWM using the high-resistance cCCDA can control the frequency and duty cycle separately, resulting in less complex circuit calibration. The block diagram of a VCO to VFPWM using the high-resistance cCCDA is depicted in Figure 15. SPICE analysis demonstrates the VFPWM result, and the findings are shown in Figure 16. In the SPICE circuit model, a VCO is used with the same settings as for Figure 14.

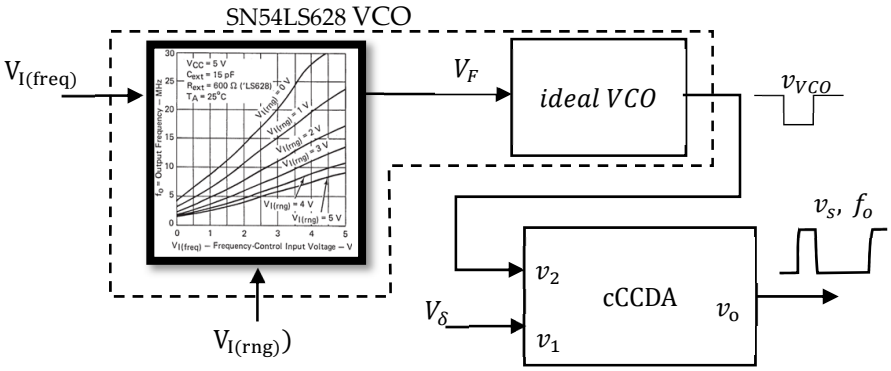


Figure 15. High-resistance cCCDA in series with a VCO.

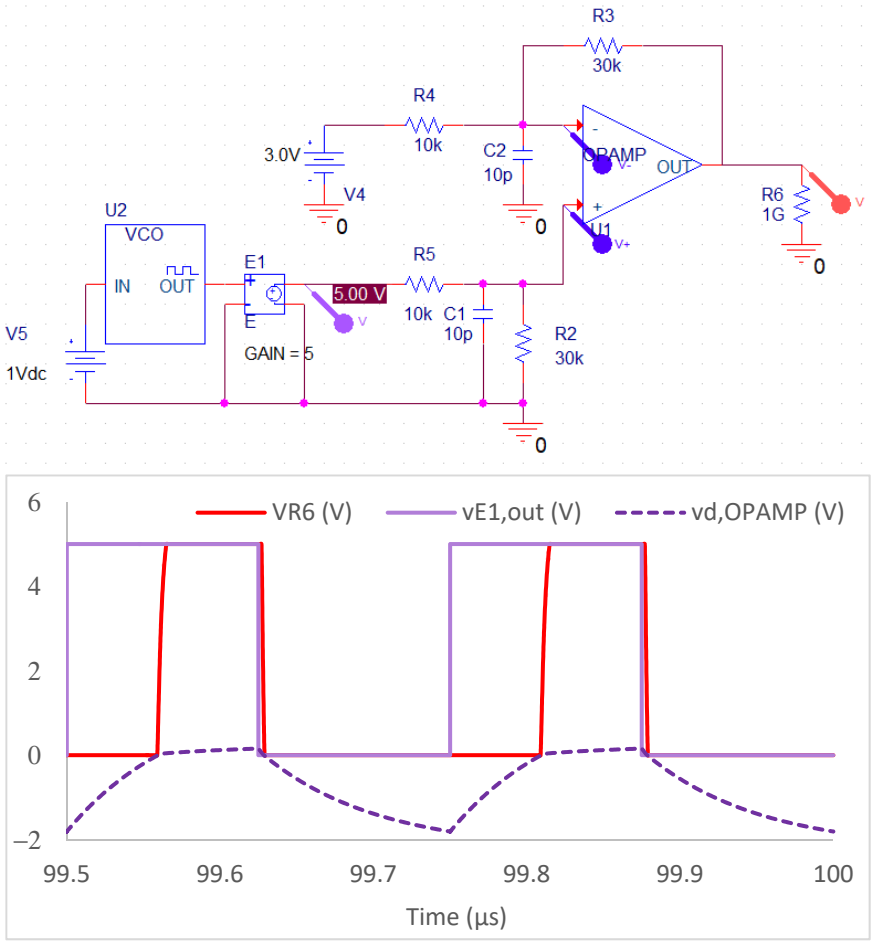
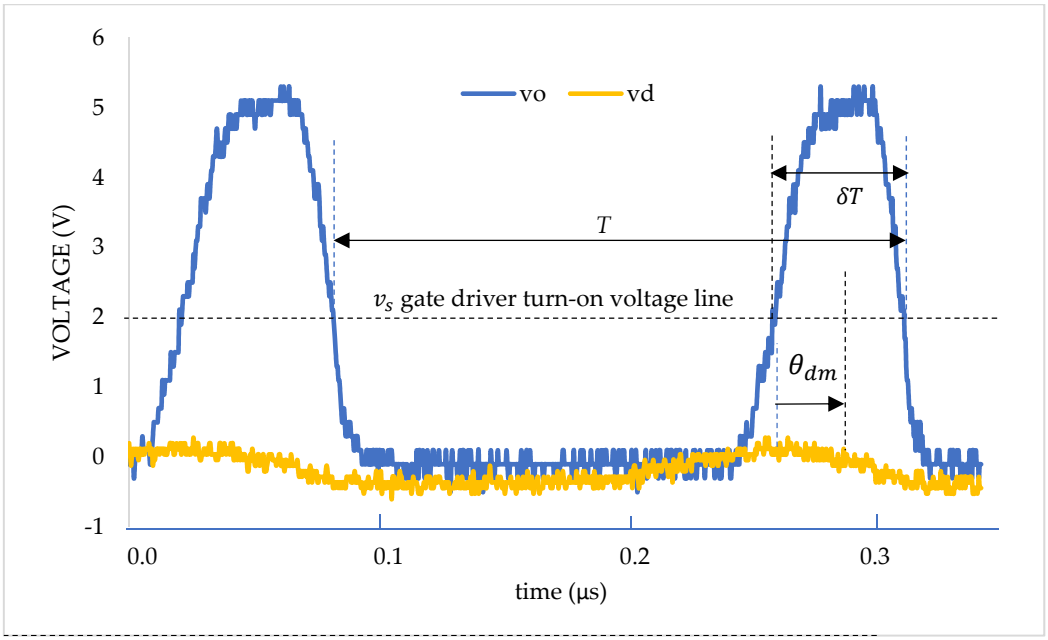


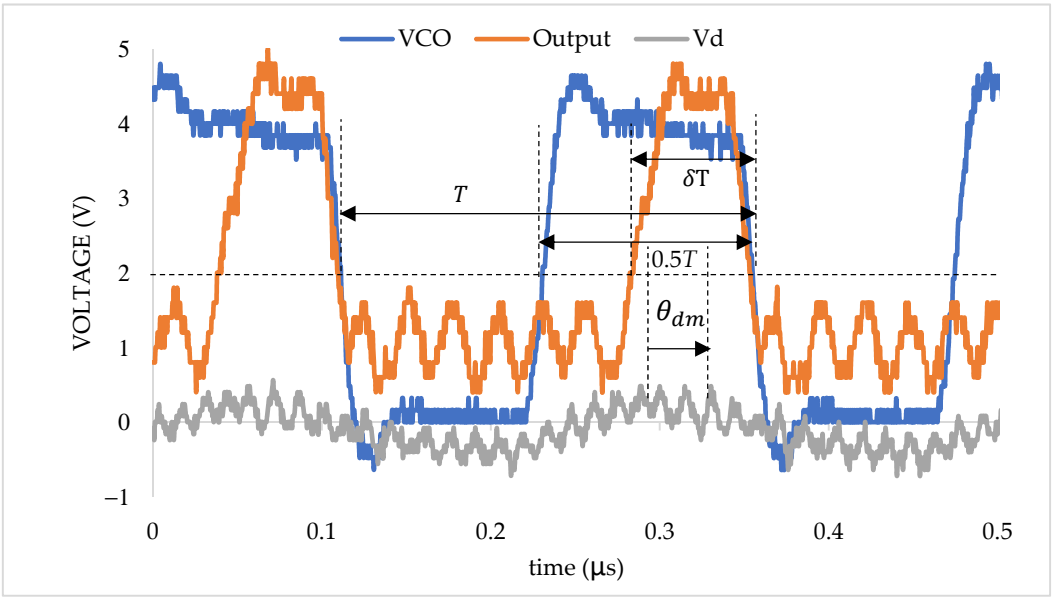
Figure 16. SPICE analysis of VFPWM using a high-resistance cCCDA in series with a VCO.

5. Experimental Results

A high gain bandwidth product operational amplifier is used, namely the MAX4265 400-MHz operational amplifier, which yields gain of nearly 100, that is $A_{dm} = 100$ with a nearly 60° phase lag, i.e., $\theta_{dm} = 50^{\circ}$, at the operation frequency around 4 MHz. Examples of the VFPWM output from a VCO versus v_d and the output in a dCCDA experiment are shown in Figure 17a. The circuit topology is presented in Figure 7. The circuit parameters are similar to those listed in Table 4. The operation voltage, V_{ref}, in this dCCDA configuration is 1.0 V, and the duty ratio, δ, is 22%. The phase lag of v_d versus the output from the VCO is approximately 50°, which matches the phase lag of the opamp.



(**a**)



(**b**)

Figure 17. (**a**) VFPWM output and v_d from a low-resistance dCCDA. (**b**) VFPWM output (=v_s) versus the VCO output (=v_{VCO}) and v_d of the VCO in series with the high-resistance cCCDA.

The experimental results of the VFPWM using a high-resistance cCCDA in series with a VCO, with circuit parameters as shown in Table 4, are illustrated in Figure 17b. The VCO generates nearly 50% duty ratio output when the output of the low-resistance cCCDA is of the duty ratio $\delta = 30\%$. The phase lag of v_d versus the output from the VCO is also approximately 50°.

Table 4. Parameters for the cCCDA and dCCDA designs.

Parameter	Unit	cCCDA	dCCDA
T	ns	250	250
R	Ω	10k	100
C_{cm}	pF	15	
C_{dm}	pF		15
T_{dm}	ns	100	100
A_{dm}		100	100
θ_{dm}@4MHz	degree	50	50
T'_{dm}	ns	1.0	1.0
α		3	1

To understand the influence of capacitance in this cCCDA configuration, we measure the duty ratio δ and tuning results versus operation voltage V_{ref} and compare them with the theoretical result obtained using Equation (19). The parameters R and α in Table 4 are set to 20 kΩ and 1, respectively. The parameter C_{cm} in Table 4 is set to two capacitances, C_{cm}^{+} and C_{cm}^{-}, respectively, according to the two $\pm$ terminals of the amplifier in Figure 9. The selection of C_{cm}^{+} and C_{cm}^{-} could be many combinations. Figure 18 shows the results for $C_{cm}^{-} = 15$pF, and C_{cm}^{+} varies from 9 to 23 pF when R = 20 kΩ and $\alpha = 1$.

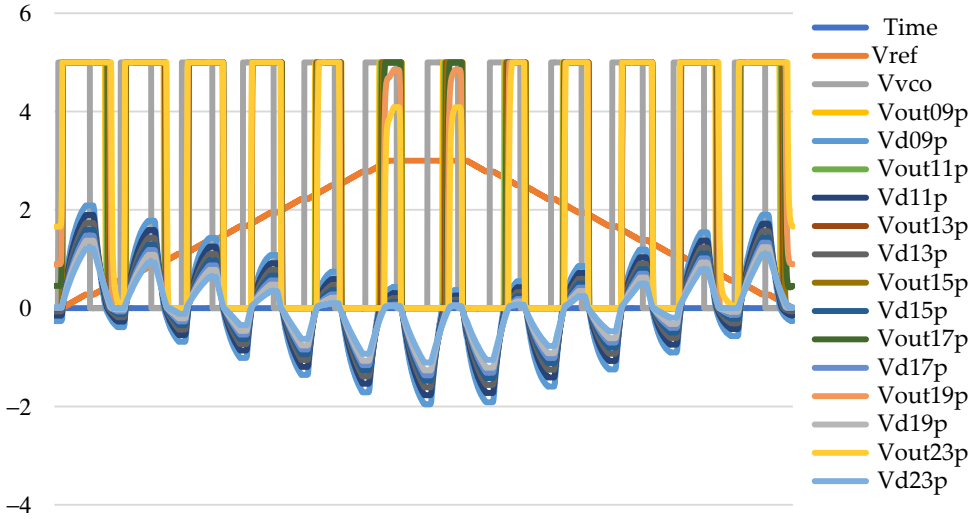


Figure 18. Influence of the capacitance C_{cm} on the VFPWM output.

Then, only three combinations of (C_{cm}^{+}, C_{cm}^{-}), that is, (15 pF, 15 pF), (15 pF, 10 pF), and (10 pF, 15 pF), are implemented in the experiments, and a comparison of the measurements with the experimental results of Equation (19) is presented in Figure 19. The duty ratio responses of the three capacitance combinations match the theoretical response; however, the combination with identical capacitances, namely (C_{cm}^{+}, C_{cm}^{-}) = (15pF, 15pF), is closest to the theoretical response. Thus, the VFPWM design of the cCCDA configuration is well balanced in practice.

Figure 20 illustrates the influence of resistance on the relationship between the duty ratio and operation voltage V_{ref} in the cCCDA configuration. The δ_{max} values are all close to 50% when $V_{ref} = 0$, but they decrease slightly when the resistance in Table 4 increases from 8.2 to 20 kΩ. The limitation values of V_{ref}, when the duty ratios are diminished, move away from the cutoff operation voltage at $V_{ref} = 2.5$ V when the resistances are increased from 8.2 to 20 kΩ. The intersection of the duty ratio curves in Figure 20 is located at approximately $V_{ref} = 1.2$ V, probably because we set a threshold of $V = 1.2$ V when analyzing the experimental results.

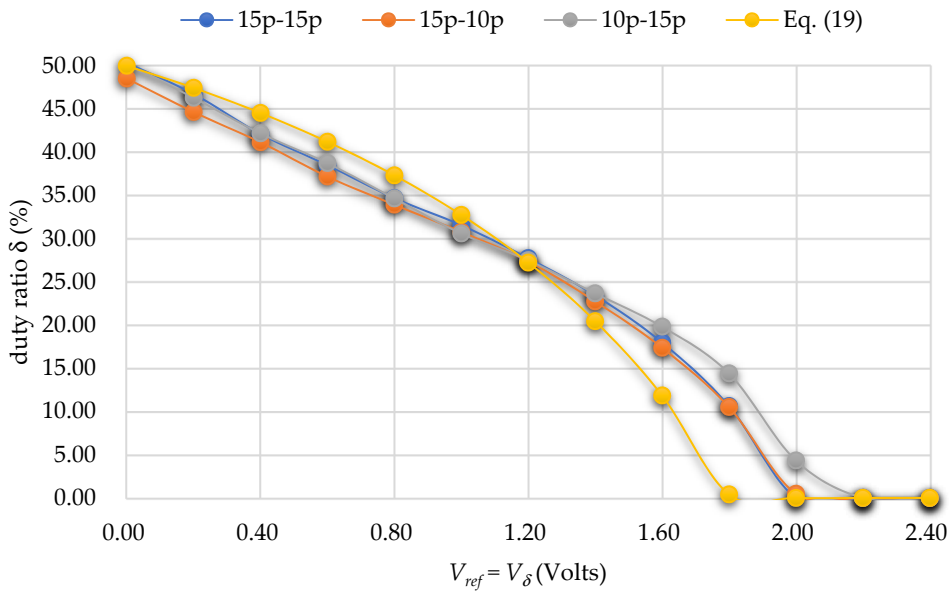


Figure 19. Influence of the capacitance C_{cm} on the duty ratio vs. control voltage (V_δ) in cCCDA letting $\alpha = 1$ and $R = 20$ kΩ in Table 2.

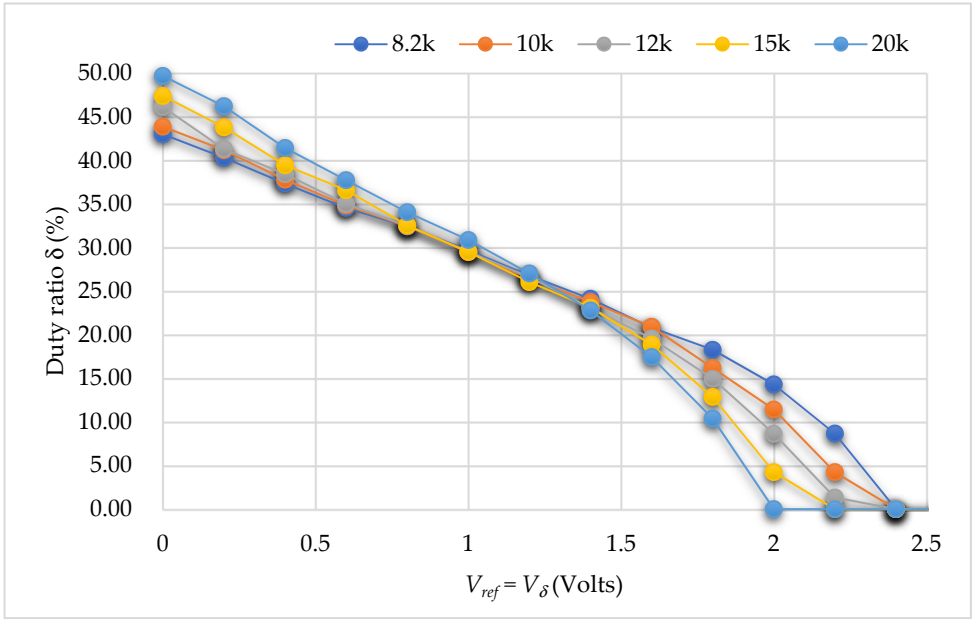


Figure 20. Influence of the resistance on the duty ratio vs. control voltage (V_δ) in cCCDA letting (C_{cm}^+, C_{cm}^-) be (15 pF,15 pF).

The results in Figures 19 and 20 provide the transfer function between duty ratio δ (%) and the control voltage of V_δ for the VFPWM circuit associated with the high-resistance cCCDA. The switching control depicted in Figure 1 consisting of the transfer matrix could be formulated into the following equation.

$$G_z = \begin{bmatrix} G_{zo} & 0 \\ 0 & G_{z1} \end{bmatrix} \tag{25}$$

The gain G_{z1} from δ to V_δ are piecewise linear functions interpolated from Figures 19 and 20 according to the selection of (C_{cm}^+, C_{cm}^-) and R.

The VFPWM driving circuit PCB was fabricated according to Figure 15, as shown in Figure 21. The VFPWM was integrated into a WPT device, as shown in Figure 22. It

illustrates the validity of the cCCDA of the VFPWM in the WPT system application; the distance of the wireless transfer was more than 100 cm. In the photo in Figure 23, it can be seen that all output connectors of the function generator are disconnected. The cCCDA is used instead of the function generator to provide the switching signal to the gate driver of the PTU. In addition, there are multiple PTUs powering multiple PRUs.

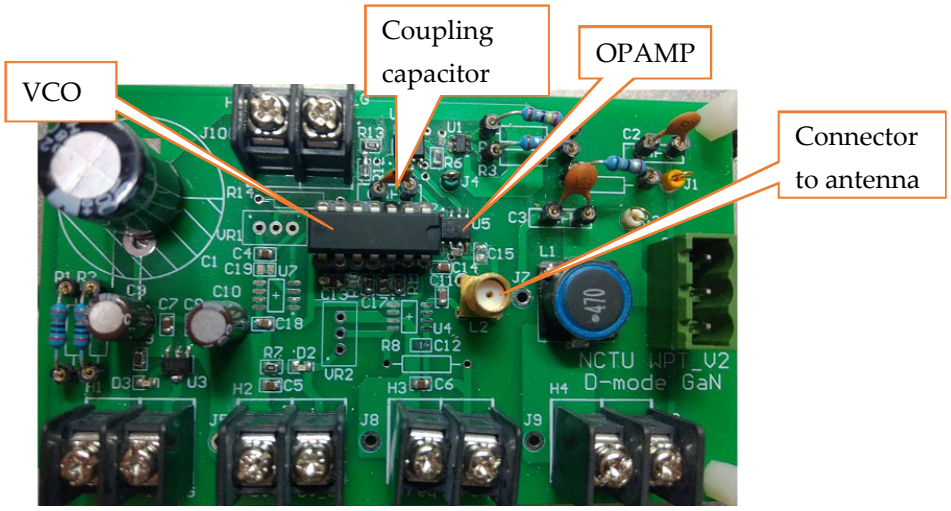


Figure 21. A cCCDA driving circuit board 6.5 cm wide and 11 cm long.

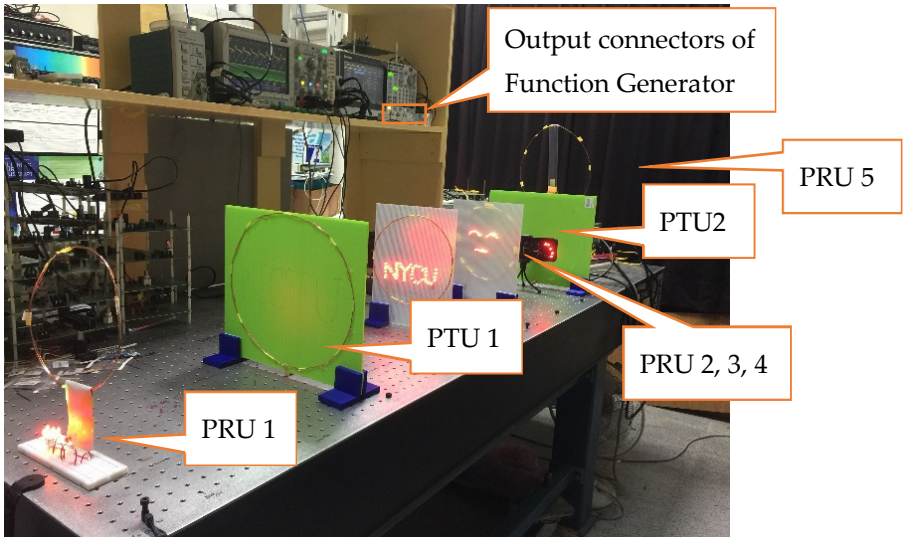


Figure 22. Integration of the VFPWM of the cCCDA scheme applied to WPT.

The power transfer efficiency was reported in [24]. The maximum distance for 1 W power delivery can be as far as 140 cm when v_{DS} is $\geq$ 700 V and the corresponding input voltage V_{DD} is around 300 V. We achieved the same result as before. In addition, we surpassed the previous achievement by enabling MIMO (multiple input and multiple output) applications, because the function generator can only control a maximum of two PTUs at a time. Nevertheless, the VFPWM is much less inexpensive than the function generator, and it is very handy and small. In [25], we derived a theory called the minimum power input control, which trades off PDL (Power Delivered to Load) for the switching loss of the GaN HEMT in order to yield the optimal PTE (Power Transfer Efficiency). However, the MIMO control was not shown in [25], because the function generator Tektronix AFG 31054, which is a dual channel output equipment, does not allow easy management of the phase difference required for the operation of different PTUs in different arrangements. On the other hand, we were able to easily adjust the individual VFPWM boards in this paper

to obtain the required phase difference among the PTUs and achieve the best power output for multiple PRUs.

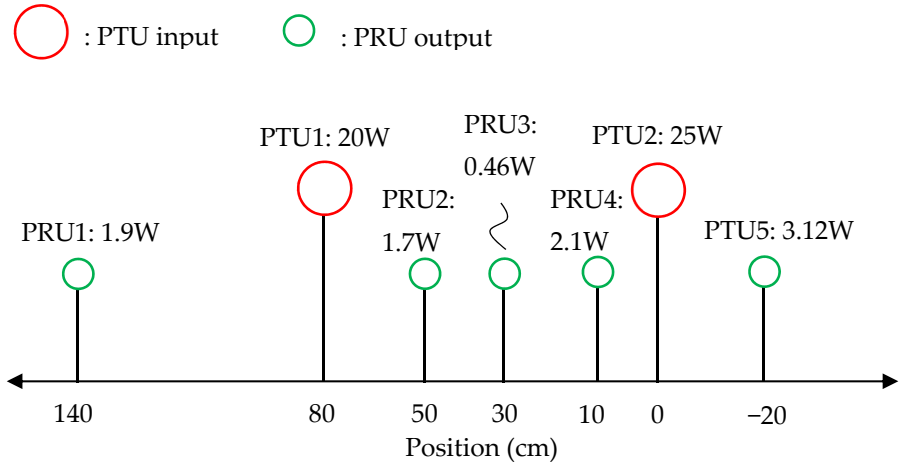


Figure 23. PDL of MIMO applications.

The experiment of a MIMO WPT demo is depicted in Figure 23, which uses the VFPWM shown in Figure 21 to control class-E amplifier switching. In this experiment, we set $C_{cm}^{+} = C_{cm}^{-} = 15$pF, $R = 20$ kΩ and $\alpha = 1$ for the cCCDA. One of the VCO inputs $V_{I(rng)}$ is set to 5 V. The measured results show a total power output from five PRUs of 9.26 W when the total power input from two PTUs is 45 W. The input signals to the charge pump gate drive and the drain-source voltage of the class-E amplifier are shown in Figure 24. The control voltages of the VFPWM are shown in Table 5. Compared to the theoretical results, the estimated value of the switching frequency closely matches the data read from Figure 12. There is some difference, within 20%, between the estimated duty ratio δ% from the measurement and the theoretical duty ratio δ% interpolated from Figure 20. The differences are a result of the input impedance of the charge pump gate drive and the input impedance of the GaN HEMT transistor, which can be eliminated by the closed loop control in the WPT system using the minimum power input control [25].

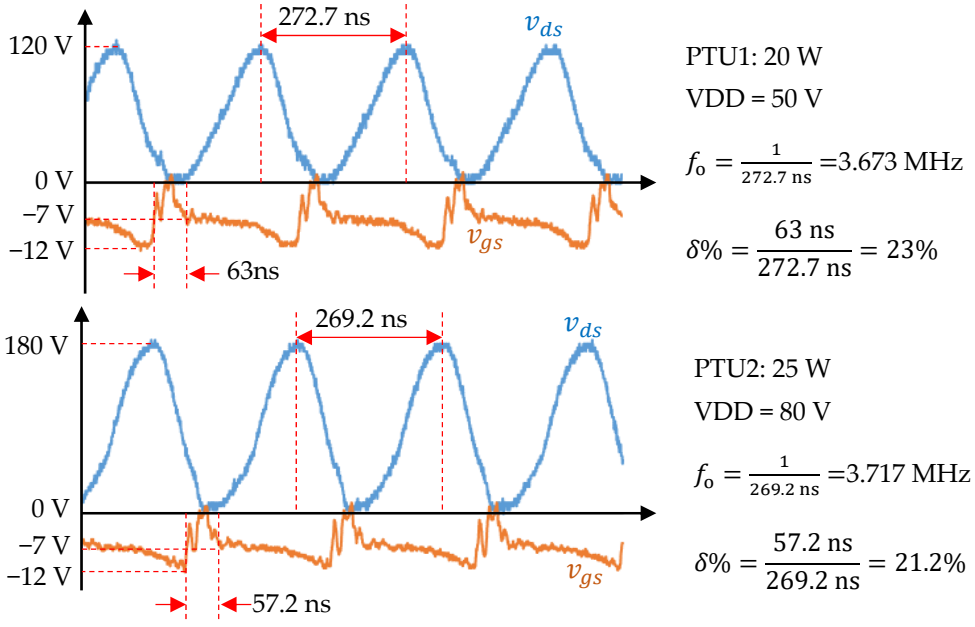


Figure 24. The wave form of the input signal v_{GS} and output signal v_{DS} of class-E Amplifier.

Table 5. Control voltage inputs of the individual PTUs in Figure 23.

	Corresponding Control Voltage	Unit	Value	Symbol	Unit	Estimated Value	Theoretical Value
PTU1	$V_{I(freq)}$	V	1.92	f_o	MHz	3.673	3.65 *
	V_δ	V	1.76	δ (%)		23	19 **
PTU2	$V_{I(freq)}$	V	2.02	f_o	MHz	3.717	3.77 *
	V_δ	V	1.86	δ (%)		21.2	17 **

* corresponds to Figure 12 and ** corresponds to Figure 20.

6. Discussion

The existing, and widely popular, inductive power transfer (IPT) cannot achieve long-distance power delivery, in theory. Resonant wireless power transfer allows electrical power to be delivered over long distances with acceptable efficiency, which is usually higher than 80%. Inductive power transfer through a metal object is also a major obstacle due to the generation of eddy currents, leading to substantial device heating. The resonant WPT system with a frequency of 6.78 MHz is capable of transferring power into metal-encapsulated mobile devices without considering the eddy current effect. However, many technologies and tests for resonant WPT systems are still under investigation. Namely, the class-E amplifier, the control of which still needs to be validated with respect to installation costs and radio regulations. The power efficiency for the WPT is also one of the major concerns in real-life scenarios; WPT will never be as efficient as wired power transfer, but how close could the efficiency be? In addition to low cost, low environmental contamination, and high efficiency, the maximum power that can be transferred in a desired distance between the power transfer unit (PTU) and the power receiving unit (PRU) is also a factor that affects the decision to use resonant WPT systems. In this paper, we focused on the critical aspect of the gate driving the physical control of the class-E amplifier. The control of class-E amplifiers takes the optimal tuning of switching frequency and duty cycle as the inputs and generates the corresponding pulse train to switch the transistor on or off. Considering the multiple-input–multiple-output (MIMO) applications of WPT, the control hardware should be small in size, such that the PTU can be placed easily. It is recommended that the size of the PTUs be made so small that they can be placed directly into the socket on the wall or into a power extension cord, just like chargers for mobile devices. In this paper, the VFPWM consists of only a VCO and an OP-amp, and can be miniaturized into a system in packaging (SiP), while the class-E amplifier can also be reduced to the size of a cigarette box. The antenna of the PTU can also be made into the stickers that go on different faces of the PTU box. The minimum power input control [25] can also be implemented in the microprocessor or FPGA. The VFPWM proposed in this paper is a low-cost and high-reliability solution for the control of class-E amplifiers. Nevertheless, the duty cycle control, which is independent from the frequency control, can be adjusted via the analog voltage input, as shown in Figures 19 and 20, with the circuit topology as shown in Figures 15 and 16. The live demo photo shown in Figure 22 displays the possibility of multiple PRUs being charged simultaneously since PRUs can be distanced from one another.

7. Conclusions

Two VFPWM circuitries derived from a VCO and CCDAs, classified as the dCCDA and cCCDA, are proposed in this paper. The dCCDA with low resistance reduces the noise in the feedback loop to the VCO. The cCCDA with high resistance can be used in series with the VCO to meet the VFPWM requirements. Compared with dCCDA, the cCCDA circuit enables independent control of the frequency, and the duty cycle is deemed to be better in 6.78-MHz resonant WPT applications. The circuit was fabricated and used in a field test, yielding power transfer to 100 cm away for multiple power receiving units. The output power of the corresponding single power transmission unit was more than 10 W.

The corresponding control can be either digital or analog for different WPT applications and market segments. With the VFPWM design introduced in this paper, the challenge of electromagnetic interference (EMI) from the antenna to the power supplies remains to be addressed in future studies. Currently, we can integrate multiple power transmission units to form a multiple-input–multiple-output system for WPT applications. In the future, we will devote more attention to high-power delivery, providing that the environmental safety issues are simultaneously addressed. High power delivery to load (PDL) can be achieved by using either multiple PTUs to the load or multiple PRU antennas on the load, depending on the load characteristics. The use of this resonant WPT technology will be seen in the future in electrical vehicle (EV) charging applications.

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Nomenclature

f_o (Hz)	switching frequency in wireless power transfer
δ	duty cycle of the switching control
L_1	inductance on the switching power supply side of the PTU
C_1	resonant capacitance on the switching power supply side of the PTU
L_2	equivalent inductance including the load inductance on the PTU side
C_2	equivalent capacitance including the load capacitance on the PTU side
R_L	equivalent resistance of PRU on the PTU side
v_s	switching control signal of PTU
V_F	control voltage corresponding to the frequency f_o to the VFPWM;
V_δ	control voltage corresponding to the duty ratio δ to the VFPWM
V_{DD}	input voltage of the PTU
Gz	zero-order hold transfer function matrix
G_{Z0}	gain of the switching frequency to voltage transfer function
G_{Z1}	gain of the duty ratio to voltage transfer function
A_{dm}	differential mode gain of the OPAMP
θ_{dm}	differential mode phase lag of the OPAMP @ 4MHz
v_d	Difference voltage of the OPAMP
V_{PS}	power supply voltage of the OPAMP
C_{dm}	differential mode capacitance added to the difference amplifier
C_{cm}	common mode capacitance added to the difference amplifier

α	feedback gain of the difference amplifier
R	Base resistance of the resistors of the difference amplifier
T_{dm}	time constant for charging the difference mode capacitor
T_{cm}	time constant for charging the common mode capacitor
$V_{I(freq)}$	voltage input to control the center frequency of the SN54LS628 VCO
$V_{I(rng)}$	voltage input to control the frequency range of the SN54LS628 VCO

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