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# A New GaN-Based Device, P-Cascode GaN HEMT, and Its Synchronous Buck Converter Circuit Realization

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**Abstract:** This paper attempts to disclose a new GaN-based device, called the P-Cascode GaN HEMT, which uses only a single gate driver to control both the D-mode GaN and PMOS transistors. The merit of this synchronous buck converter is that it can reduce the circuit complexity of the synchronous buck converter, which is widely used to provide non-isolated power for low-voltage and high-current supply to system chips; therefore, the power conversion efficiency of the converter can be improved. In addition, the high side switch using a single D-mode GaN HEMT, which has no body diode, can prevent the bi-directional flow and thus reduce the power loss and cost compared to a design based on a series of two opposite MOSFETs. The experiment shows that the proposed P-Cascode GaN HEMT efficiency is above 98% when it operates at 500 kHz with 6 W output. With the input voltage at 12 V, the synchronous buck converter provides an adjustable regulated output voltage from 1.2 V to 10 V while delivering a maximum output current of 2 A.

**Keywords:** synchronous buck converter; single gate driver; D-mode GaN HEMT; P-Cascode GaN HEMT



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## 1. Introduction

Synchronous buck converters are widely used in industries, consumer, and automotive applications. As the size becomes more compact, designers have turned to faster switching speeds in order to reduce the size of the converter [1,2]. However, the switching speed is limited by the switching loss and the reverse recovery characteristic of the transistors. Therefore, wide-bandgap devices, such as GaN and SiC, have the potential benefits of achieving high switching and high efficiency capability because of their superior material properties, including a small gate charge and low $C_{oss}$ loss [3,4]. The disadvantage of the GaN HEMTs is the normally-on characteristic with negative $V_{th}$. From the fail-safe and simple gate drive point of view, cascode configuration is one of the suitable ways to turn the normally-on into normally-off devices [5].

Few studies have presented the benefits of the cascode configuration to achieve the advantages of a high switching operation, high efficiency performance, and simple gate drive circuit requirement [6,7]. A cascode SJ-FET/LV-FET configuration, which avoids the activation of the body diode by keeping the SJ-FET in the on-state, provides better performance in the third quadrant operation [6]. In [7,8], demonstration of the cascode GaN/SiC power device, combining the benefits of a GaN device's fast switching ability and a SiC device's high-voltage blocking capability, was shown to reach lower $C_{oss}$ loss and higher device ratings. Nevertheless, the aforementioned literature results show great performance

in cascode configuration with respect to in the standalone configuration, the issues being the match in intrinsic capacitances [9], an avalanche in the low side switch [10], and stray inductance analysis between the two cascode devices' interconnection [11,12]. Decayed Negative Voltage [13] and dv/dt control [14] were proposed to solve the switching controllability, suppress the oscillation, and prevent the false turn-on phenomenon. Cascode configuration provides a positive $V_{th}$ to control the GaN HEMT, but it is still limited by the package parasitic capacitance [15]. There is big appreciation of the development teams of previous work on NCTU GaN HEMT devices, covering every aspect of materials, process development, devices [16–18], thermal performance [19,20], and the spice model [21,22], leading to the lab-made cascode GaN HEMT, equipped to potentially be capable of being realized in circuit applications. However, the cascode topology faces two problems which includes the switching frequency limited by the NMOS switch, and the returning current flow from the load to the power source due to the body diode of the high-side E-mode transistor, which makes it unsuitable for synchronous rectifier applications. Therefore, a P-Cascode GaN HEMT Module topology is proposed. The GaN HEMT in this paper is used as the high side switch that can go to several MHz, switching with a very small switching loss due to its output capacitance. $C_{oss}$ varies much less than the MOSFET and the energy loss in the reverse recovery charge process is insignificant with respect to the MOSFET.

The novel P-Cascode GaN device is implemented by using discrete TO-220 package D-mode MIS-HEMT GaN and TO-220 package P-MOSFET. Comparing to the previous achievements in NCTU [16–22], which needed two E-mode cascode GaN HEMT devices to achieve the synchronous bulk operations, we need only one P-Cascode GaN device to implement the same operations. The aim of this paper is to reduce the shooting through problems inherent in the synchronous buck converter. Previous achievements will need two individual gate drivers, which follow the well-known dead-time control to prevent the shooting through. The novelty of this work is to use a single P-Cascode GaN power module that embodies only one gate drive to yield the equivalent dead-time control for preventing the shooting-through problem. The efficiency can be improved due to the number of devices used being cut in half.

This paper introduces the P-Cascode GaN power module in the following order. This paper is organized as follows. The novel P-GaN cascode device is presented by using a discrete TO-220 package D-mode MIS-HEMT GaN and TO-220 package P-MOSFET. To fulfill the transistor-matching issues, the characteristics of the D-mode MIS-HEMT GaN is studied, including the epitaxial structure and the field plate, in Section 2.1, to provide the designed information for circuit configuration. Section 2.2 reviews the previous lab-made GaN HEMTs cascode topology from NCTU [16–22]. Due to this cascode topology, which did not perform well in synchronous rectifier applications for solving the switching frequency limited by the NMOS switch and the returning current flow from the load problems, a single gate controlled P-Cascode GaN HEMT module configuration is proposed in Section 2.3. To provide the compatible gate drive for the proposed single gate P-Cascode GaN HEMT, the biased charge pump gate drive is presented in Section 2.4. Then, the synchronous buck converter based on the created P-Cascode GaN HEMT module with the biased charge pump gate drive is analyzed and used to verify the performance in Section 2.5. The experimental results and conclusion are shown in Sections 3 and 4.

## 2. Materials and Methods

### *2.1. D-Mode GaN MIS-HEMT Characteristics*

From the top to the bottom, the epitaxial structure of our GaN device consists of a 2 nm SiNx and 1 nm GaN cap, a 25 nm AlGaN barrier layer, a 1 um GaN layer, a 4 um-thick AlGaN/AlN supper-lattice buffer layer, an AlN seed layer, and the Si substrate; the schematic cross section of the epitaxy structure is shown in Figure 1a. The 120 mm GaN MIS-HEMT process can be divided into four parts (Process flow and 120 mm GaN MIS-HEMT design and pictures shown in Figure 1b), including the ohmic contact, mesa isolation, gate formation, and field-plate formation. The fabrication process of the ohmic contact

and mesa isolation is presented in [23]. A 40 nm SiNx passivation layer was deposited by plasma-enhanced chemical vapor deposition (PECVD). For device gate formation, a two-step gate was defined by the mask aligner using the photoresist T-gate structure, a field plate defined by the mask aligner, and metal deposition of the Ti/Au by e-gun. Finally, a 100 nm SiNx layer was deposited with nitride via the fabricated device pad region. After device fabrication, the Si substrate back side grinding, polishing, and back side metal deposition were formatted, and after chip dicing, all the GaN devices were packaged in a TO220 case package.

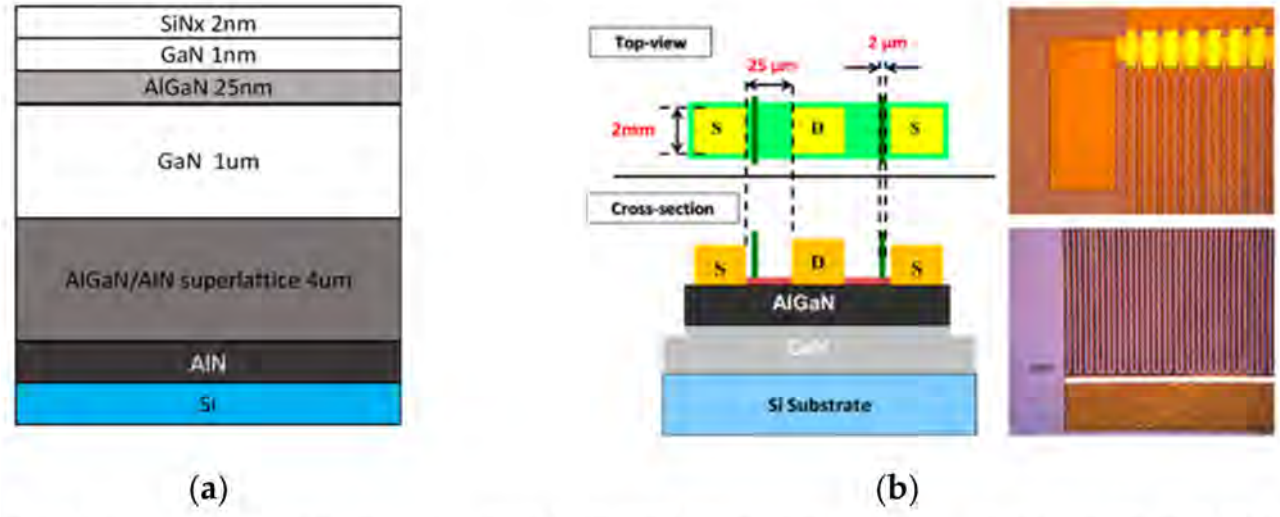



**Figure 1.** (**a**) Cross-section of the D-mode GaN MIS-HEMT; (**b**) 120 mm D-mode GaN MIS-HEMT devices.

The parasitic capacitance $C_{ISS} = C_{GD} + C_{GS}$ is only 6% [24] smaller when the transistor is turning on than when turning off. Hence, the turn-on delay time will be similar to the turn-off delay time. The electrode of the field plate, as shown in Figure 2, represents a metallization above the passivation layer, making the GaN HEMT possible to reach exceptional power densities. That allows modifying some electric properties of the HEMT, such as the distribution of the electric field at the edge of the gate near the drain and the breakdown voltage. One dominant effect of the field plate is that the distribution of the electric field at the edge of the drain and gate side reduces the peak of the electric field. However, it also equalizes the roles of the source and the drain and made them undistinguishable.

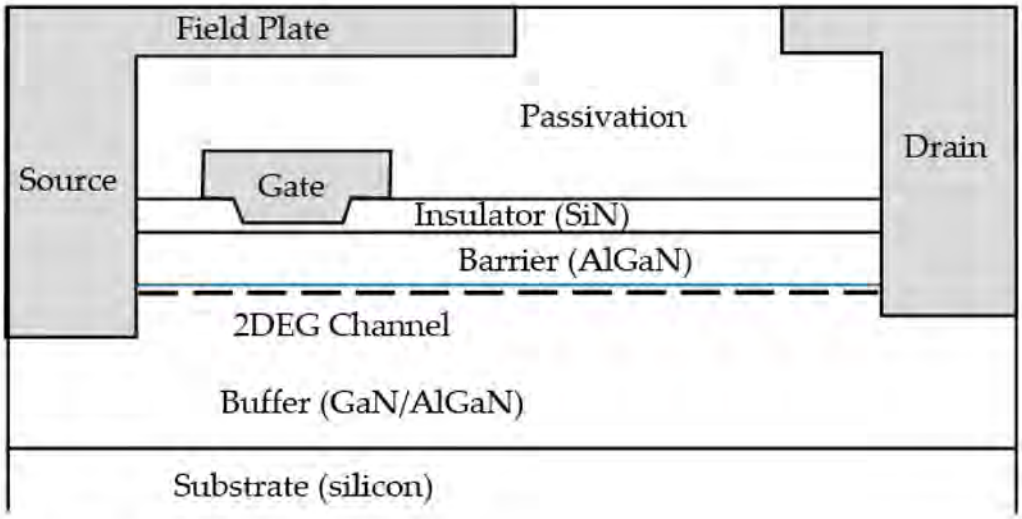



**Figure 2.** The field plate of the D-mode GaN MIS-HEMT.

In order to evaluate the effect of field plate, the switching test as shown in Figure 3 is proposed. In the switching test, each terminal of the drain and source is connected to a 10 Ω resistor. The $V_{DD}$ = 12 V is used to float the source to 6 V while the gate voltage is applied with a low frequency, 10 Hz, triangular wave input. The D-mode GaN MIS-HEMT is gradually turned on from $V_G = -10$ V to 10 V. For the switching test (I), when the gate is turning on, there is an increasing feedback voltage on the source terminal to reduce the gate-source voltage, which is equivalent to the Miller plateau effect that the current $i_D$ can only increase slowly. As shown in Figure 4, the function of $v_{GD}$ in terms of $v_{GS}$ is proposed to observe the voltage feedback effect from the resistors. The switching test is used to justify the degree of drain-source symmetry of the transistor as follows.

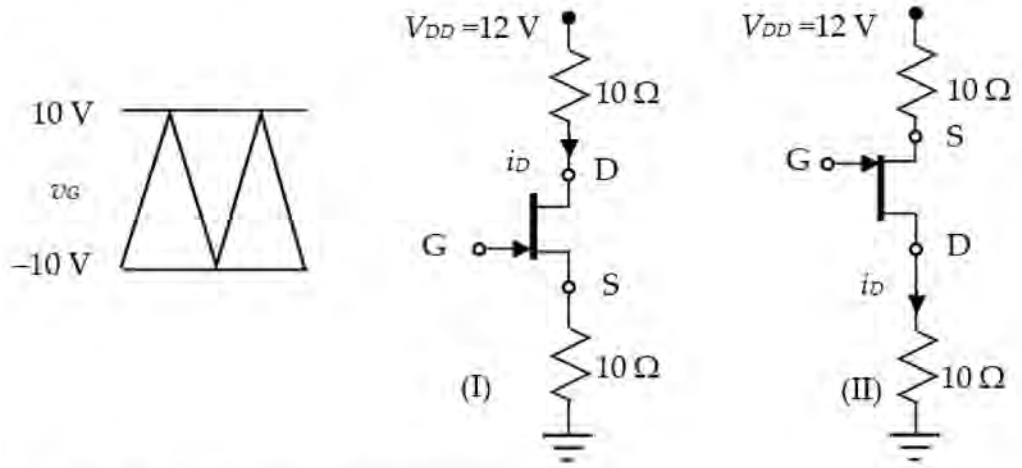



**Figure 3.** The triangular wave on–off experiment setups.

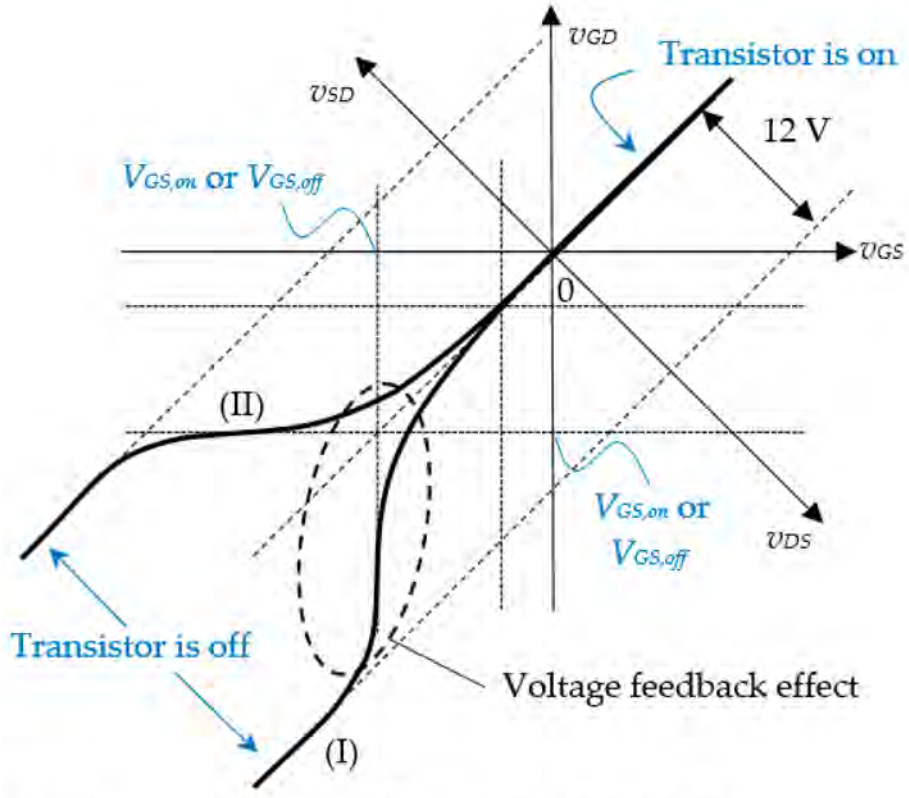



**Figure 4.** The triangular wave on–off traces of a D-mode GaN HEMT.

In Switching Test (I), we have

$$v_{GS} = v_G - 10i_D \tag{1}$$

$$v_{GD} = v_G + 10i_D - V_{DD} \tag{2}$$

that yields

$$v_{GD} - v_{GS} = 20i_D - V_{DD} \tag{3}$$

In Switching Test (II), we have

$$v_{GS} - v_{GD} = 20i_D - V_{DD} \tag{4}$$

Since the gate voltage $v_G$, a triangular wave input, is implicit in both Equations (3) and (4), the voltage feedback $20i_D$ from the resistors can help to show the turn-on and turn-off transitions as well as to indicate the threshold voltages, as shown in Figure 4. In the turn-on states, both switching tests yield $v_{GD} \approx v_{GS}$ due to the drain-source voltage $v_{DS}$ being small. In the turn-off states, the Switching Tests (I) is $v_{GD} - v_{GS} = V_{DD}$ and (II) is $v_{GD} - v_{GS} = -V_{DD}$ due to $i_D$ being zero.

On the other hand, when the gate is turning off, the decreasing feedback voltage will increase the gate-source voltage, which causes the current $i_D$ to decrease slowly. In case that the drain and source terminals are perfectly symmetric to the gate on the D-mode GaN MIS-HEMT, Switching Test (II) will be symmetric to Switching Test (I) with respect to the $v_{GD} = v_{GS}$ axis.

The experimental result is shown in Figure 5. According to the experiment's result, the gate-source voltage determines that turn-on and turn-off is a function of switching frequency. In the frequency lower than 1 kHz, the turn-on and turn-off voltage of the D-mode GaN is identical, which are both −4 V. In a high frequency higher than 100 kHz, the turn-on and turn-off voltage of the D-mode GaN become different from each other. The experiments show that the traces of the turn-on process remain the same as the low frequency one and the turn-on voltage is −4 V, i.e., $V_{Tg(on)} = 4$ V. On the other hand, the turn-off voltage yields a different trace and the turn-off voltage is −7 V, i.e., $V_{Tg(off)} = 7$ V. The experiment also shows that the reverse recovery charge process during the turn-off time causes an overshoot voltage on $v_{DS}$. As a matter of fact, Switching Test (II) will be symmetric to Switching Test (I) with respect to the $v_{GD} = v_{GS}$ axis; therefore, the drain and source terminals are perfectly symmetric to the gate on the D-mode GaN MIS-HEMT. In summary, the characteristics of the GaN HEMT and TO220 packaging are displayed in Table 1. The stray inductance of the TO220 packaging measured from the RLC meter GWINSTEK LCR819 at the drain (high) to source (low) and the source (low) to drain (high) is around 100 nH.

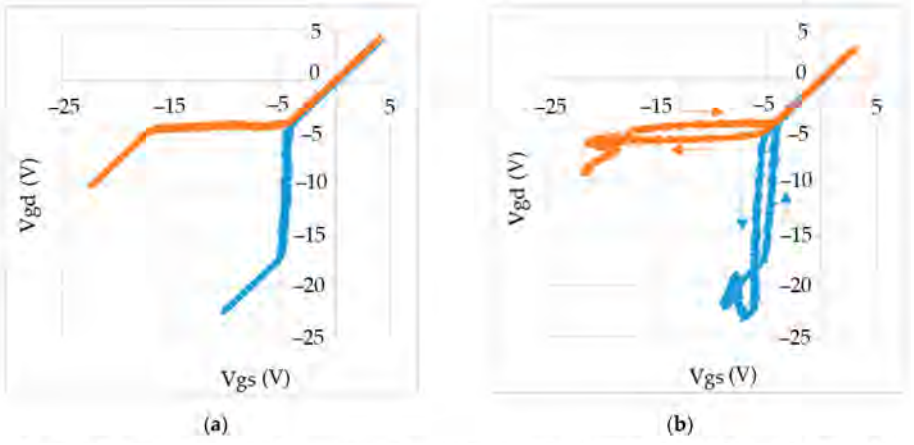


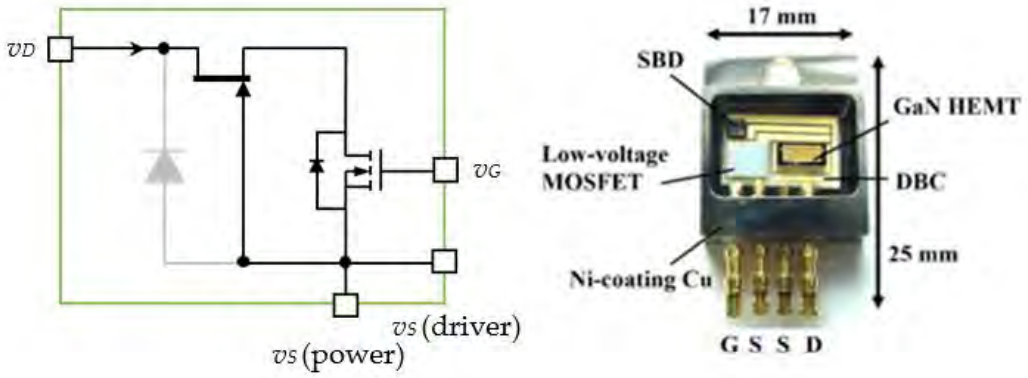

**Figure 5.** Results of the triangular wave on–off experiment of GaN HEMT at (**a**) 1 kHz and (**b**) 800 kHz.

**Table 1.** Characteristics summary of the D-mode GaN HEMT.

| Symbol | Unit | Description | Value | $v_{DS}$ | |
|---|---|---|---|---|---|
| | | | | **0 V** | **12 V** |
| $v_{GS,ON}$ (or $-V_{Tg}$) | V | Turn-on voltage (All) | −4 | | |
| | | Turn-off voltage (800 kHz switching) | −4 | | |
| | | Turn-off voltage (1 kHz switching) | −7 | | |
| $C_{DS}$ | pF | Parasitic capacitance | | 75 | 70 |
| $C_{GD}$ | pF | Parasitic capacitance | | 245 | 220 |
| $C_{GS}$ | pF | Parasitic capacitance | | 140 | 140 |
| $V_{GS,max}$ | V | Maximum gate-source voltage | 8 | | |
| $V_{DS,BD}$ | V | Drain-source breakdown voltage | 35 | | |
| $i_{d,max}$ | A | Maximum drain current | 60 | | |
| $L_d + L_s$ | nH | Stray Inductance, drain to source (100 kHz) | 80 | | |
| $L_d + L_s$ | nH | Stray Inductance, source to drain (100 kHz) | 120 | | |

### 2.2. Cascode GaN HEMT Module as an E-Mode Switch

A cascode configuration that comprises a high-voltage, normally-on GaN HEMTs device and a low-voltage silicon NMOS is shown in Figure 6 [16–22].




(**a**) (**b**)

**Figure 6.** Cascode GaN HEMT: (**a**) the cascode circuit; (**b**) the packaged device.

AlGaN/GaN HEMTs function in the depletion mode, limiting their range of applications. Normally-off operation is required in industrial power drive circuits to satisfy the fail-safe criteria and provide a simple gate drive configuration. A popular means of satisfying the normally-off requirement is to use a cascode configuration that comprises a high-voltage, normally-on GaN HEMTs device and a low-voltage silicon NMOS, as shown in Figure 6. In order to control the ON/OFF state of the normally-on GaN switch behaving as a normally-off device that is compatible with the commercial gate driver, a cascoding 80 mm D-mode GaN device, SiC SBD, and a low-voltage NMOS was achieved in NCTU [16–22].

The cascode GaN HEMT is using the NMOS as a switch to turn on and off the power path from drain to source when $v_{DS}$ is forward biased. When $v_{DS}$ is reverse biased, the gate-source voltage of the D-mode GaN is $v_{SD}$ according to the result from Figure 5, where the power path from the NMOS body diode to the D-mode GaN is naturally on. Therefore, the SiC SBD is unnecessary in the power module. The cascode GaN HEMT power module worked as an E-mode transistor that can endure a high breakdown voltage; however, the switching frequency is limited by the NMOS switch. In a particular application, such as a

synchronous buck converter such as the MTK pump express®, the body diode of the high side E-mode transistor is not preferred because of the returning current flow from the load to the power source is prevented. Thus, it was practical to use two E-mode transistors side by side. Reverting the drain and source of one transistor eliminates the body diode effect. However, it imposes an extra cost on the buck converter fabrication.

### *2.3. P-Cascode GaN HEMT Module as a Double Throw Switch*

In contrast with the cascode GaN HEMT, the P-Cascode GaN HEMT, as shown in Figure 7, with a cascoding 200 mm D-mode GaN HEMT device and a low-voltage P-MOS, is proposed in this paper. The P-Cascode GaN HEMT employs four terminals, including the source (*S*), drain (*D*), gate (*G*), and the output (*O*), in which $v_{OG}$ is the source-gate voltage of the PMOS, $v_{OS}$ is the source-drain voltage of the PMOS, $v_{GD}$ is the gate-source voltage of the GaN HEMT, and $v_{OD}$ is drain-source voltage of the GaN HEMT.

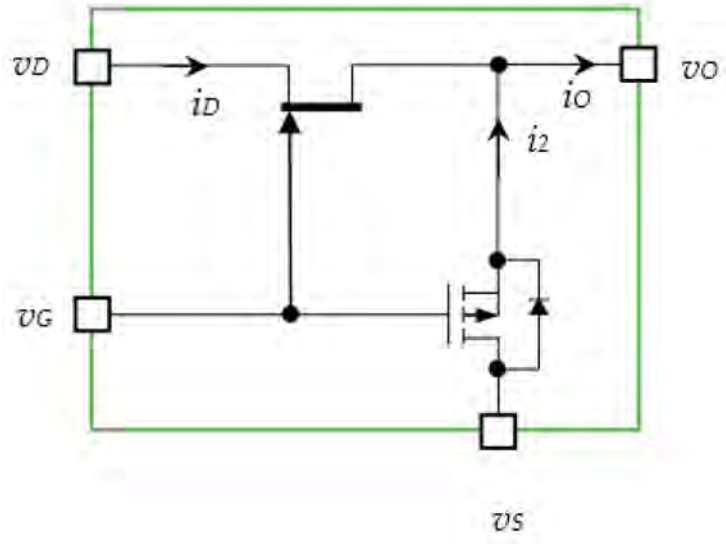



**Figure 7.** P-Cascode GaN HEMT Module.

We have performed the same on–off experiment according to Figure 3. The result shows that the threshold voltage $V_{Tp}$ of the PMOS turn-off is slightly higher than that of the turn-on. There is no significant bifurcation between turn-on and turn-off. The turn-off threshold voltage denoted by $V_{Tp(off)}$ is 4.0 V and the turn-on threshold voltage denoted by $V_{Tp(on)}$ is 3.8 V (Figure 8).

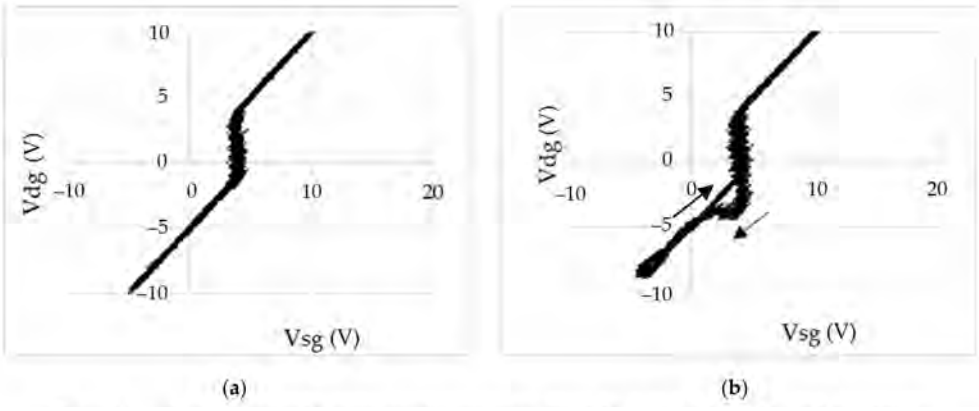



**Figure 8.** Result of the triangular wave on–off experiment (II) of the PMOS at (**a**) 1 kHz and (**b**) 800 kHz.

In the operation of $v_{DO} > 0$, the characteristics of the module in the linear ohmic region may be simplified as follows.

$$\begin{matrix} i_d = K_{GaN}((v_{GD} + V_{Tg})\, v_{DO} - {v_{DO}}^2/2) = v_{DO}/r_{on,GaN} & \text{if } \min(v_{GD}, v_{GO}) > -V_{Tg}, \\ i_d = 0 & \text{else} \end{matrix} \quad (5)$$

The on-resistance of GaN HEMT denoted by $r_{on,GaN}$ is a function of both $(v_{GD} + V_{Tg})$ and $v_{DO}$. In general, the resistance $r_{on,GaN}$ is also a function of the junction temperature of the GaN HEMT in the module. In this study, the GaN HEMT is a depletion mode device implying $-V_{Tg} < 0$. On the other hand, the characteristics of PMOS yields that

$$\begin{matrix} i_2 = K_{PMOS}((v_{OG} - V_{Tp})\, v_{OS} - {v_{OS}}^2/2) = v_{OS}/r_{on,PMOS} & \text{if } v_{OG} > V_{Tp}, \\ i_2 = 0 & \text{else} \end{matrix} \quad (6)$$

The on-resistance of PMOS denoted by $r_{on,PMOS}$ is a function of both $(v_{OG} - V_{Tp})$ and $v_{OG}$. Let $v_O$ be toggled between two states $v_{OH}$ and $v_{OL}$, which corresponds to the output voltage when the GaN HEMT and PMOS is turned on, respectively. The transistors GaN HEMT and PMOS shall be turned alternatively. To prevent the situation of both switches being simultaneously turned on is known as "shooting through". The situation where both transistors are turned on will cause the shooting through from the voltage source connected to $v_D$ to the ground connected to $v_S$. Thus, the output voltage may be shown as follows.

$$\begin{matrix} v_O = V_{OH} = v_D - i_d\, r_{on,GaN} & \text{if } \min(v_{GD}, v_{GO}) > -V_{Tg}, \\ v_O = V_{OL} = v_S - i_2\, r_{on,PMOS} & \text{if } v_{OG} > V_{Tp} \end{matrix} \quad (7)$$

In a particular application, such as the synchronous buck converter, we have $v_D = V_{DD}$ and vs. = 0 V. Since GaN HEMT and PMOS are turned on alternatively, $i_d = i_2 = i_o > 0$. The output voltage may be expressed as follows.

$$\begin{matrix} V_{OH} = V_{DD} - i_o\, r_{on,GaN} & \text{if } \min(v_{GD}, v_{GO}) > -V_{Tg}, \\ V_{OL} = -i_o\, r_{on,PMOS} & \text{else} \end{matrix} \quad (8)$$

The gate must be rapidly changed in order to make only one transistor on at a time. The required gate voltage to turn off the PMOS is $V_{GH} \geq V_{OH} - V_{Tp}$. The gate voltage to turn off the GaN is $V_{GL} \leq V_{OL} - V_{Tg}$. The swing of the gate voltage is

$$V_{GG} = V_{G,swing} = V_{GH} - V_{GL} \geq V_{OH} - V_{OL} - V_{Tp} + V_{Tg}, \quad (9)$$

In a practical case of $V_{OH}$~$V_{DD}$ and $V_{OL}$~0, if we select $V_{Tg} = V_{Tp}$, then the minimum gate swing $V_{GG} \geq V_{DD}$ is seen. In case of $V_{Tg(off)} > V_{Tp(on)}$, as shown in Figure 9, when the gate driver turns on to $V_{GH}$ and turns off to $V_{GL}$ cyclically, there will be time periods that both the GaN HEMT and PMOS are simultaneously turned on. This shooting through problem becomes more serious when at a higher frequency switching, where $V_{Tg(off)}$ increases, as referred to in the result in Table 1. To prevent this shooting through problem, it is recommended to choose a PMOS whose $V_{Tp(on)} > V_{Tg(off)}$ and also $V_{Tp(off)} > V_{Tg(on)}$.

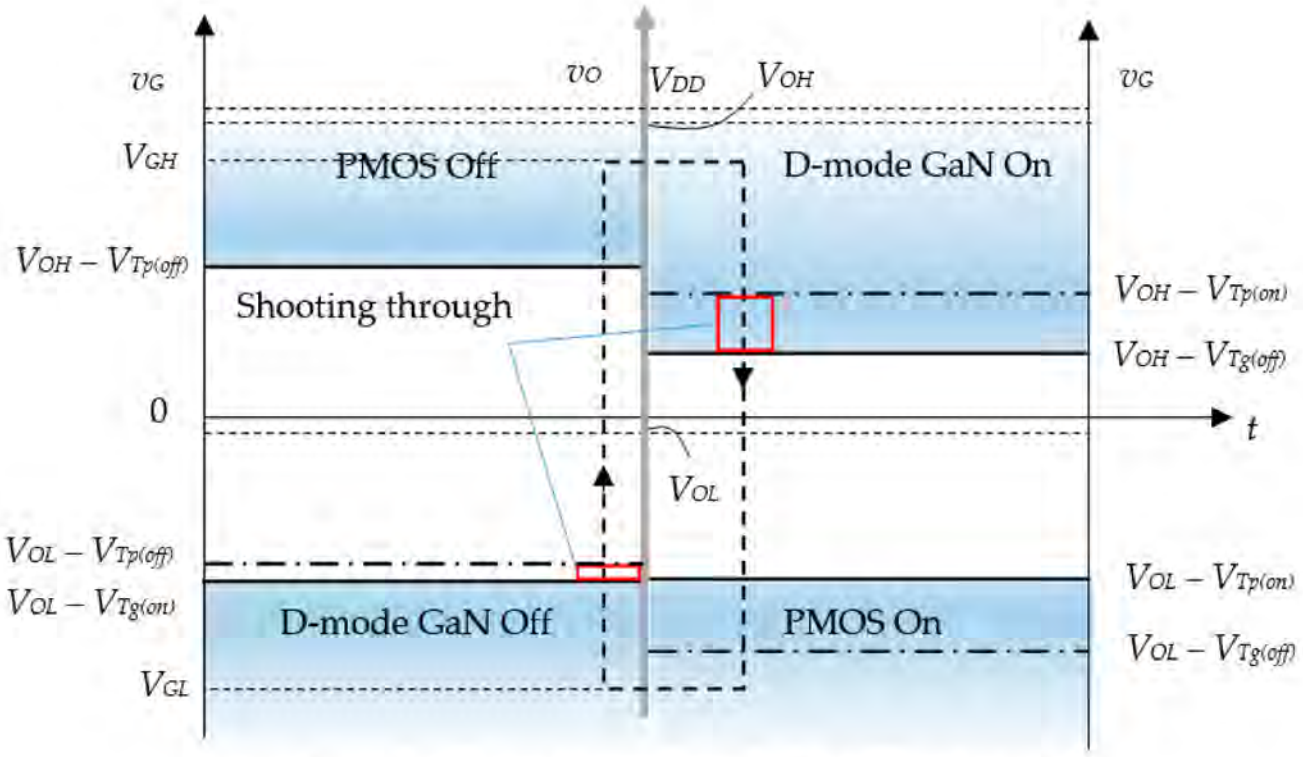



**Figure 9.** Operational region of the gate voltage for P-Cascode GaN HEMT.

In case that a PMOS failed to fulfill only the condition that $V_{Tp(on)} > V_{Tg(off)}$, we can add a capacitor in front of the gate of the PMOS, as shown in Figure 10. In such an arrangement, the gate signal can fulfill these two requirements.

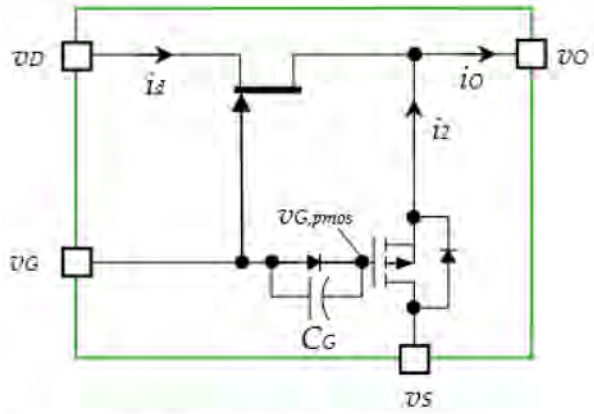



**Figure 10.** P-Cascode GaN HEMT Module.

The ratio ρ < 1 is a function that

$$\begin{gathered} V_{G,pmos}(t) = v_G(t) \quad \text{if } v_G > 0 \\ V_{G,pmos}(t) = \rho v_G(t) \text{ else } (\rho = C_{GS}/(C_G + C_{GS})) \end{gathered} \tag{10}$$

It shall note that $v_{G,pmos}(t)$ is in synchronous with $v_G(t)$, hence the circuit shown in Figure 10 is proposed to prevent the shooting through problem during only $v_G < 0$. In Figure 10, we added a single direction capacitor $C_G$ in front of the gate of the PMOS. The single direction capacitor is used as a voltage divider to take only a part of the gate voltage $v_G$ into the gate in the PMOS; the voltage relation is as follows.

$$v_{G,pmos}(t) = [C_{GS}/(C_G + C_{GS})]\, v_G \tag{11}$$

One other phenomenon that can occur is the gate voltage $v_g$ is also bonded by $V_{GL} \leq v_G \leq V_{OH}$ and the voltage $v_O$ is bounded by $V_{OL} \leq v_O \leq V_{OH}$, when GaN HEMT is turning off at time $t$:

$$v_G = V_{GH}(1 - t) + V_{GL}\, t \tag{12}$$

The output voltage $v_O$ after a time delay $t_D$ will follow the gate signal to go to a low voltage $V_{OL}$:

$$v_O = v_{OH}(1 - \gamma t) + v_{OL}\,.\gamma t, \text{ when } t > t_D \tag{13}$$

This time delay is known as the recovery charge process plus the time required for $v_G$ to fall below $V_{OH} - V_{Tg}$, as shown in Figure 11. After time $t_D$ when $v_G$ falls, the output voltage $v_O$ falls simultaneously. It may occur when $v_O$ rushes down to $V_{OL}$ faster than $v_G$ falls to $V_{GL}$ so that $v_G < v_o - V_{Tg}$ and the GaN HEMT turns off again, which will cause the output ringing. To prevent this, we need to reduce the gate resistance and, equivalently, to increase $\gamma$ in Equation (13).

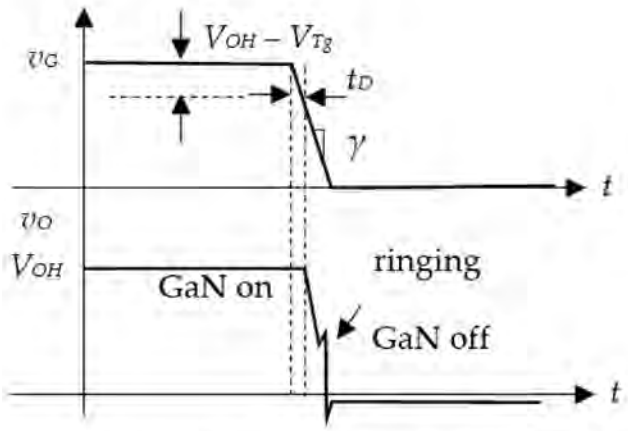



**Figure 11.** Operational region of gate voltage for P-Cascode GaN HEMT.

*2.4. Biased Charge-Pump Gate Drive Design*

The kind of charge-pump gate drive presented by Ishibashi [25] for the D-mode devices is useful for driving the D-mode GaN MIS-HEMT. The biased charge-pump circuit in Figure 12 uses $C_C$ to shift the gate voltage level. To reduce ringing, resistors $R_{G,p}$ and $R_{G,n}$ in series with the capacitor are used to slow down the turn-on of the GaN HEMT and turn-on of the PMOS.

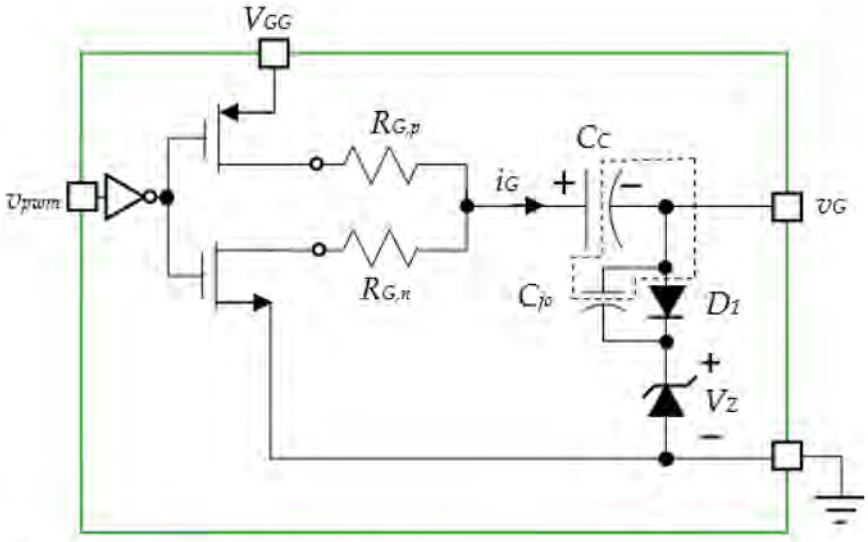



**Figure 12.** The biased charge-pump gate drive.

The charge-pump circuit in Figure 12 uses $C_C$ to lower the gate supply below the supply voltage of the gate power stage. Resistors $R_{G,p}$ and $R_{G,n}$ in series with the capacitor can reduce ringing by slowing down the turn-on of the GaN HEMT and turn-on of the PMOS. The slower turn-on allows more time for the parasitic network to discharge, limiting the ringing. The value of the boot resistor is determined empirically; starting at 0 Ω, and then increasing the resistance until the ringing is reduced to the desired level. Ideally, the charge-pump gate drive converts the output of $V_{GG}$ to a 0 V gate signal into a 0 to $-V_{GG}$ gate signal. The swing of the gate drive signal remains $V_G$ before and after the capacitor and a diode is added toward the normal gate drive circuit. In order to further shift the signal to above 0 V, a Zener diode with the reverse breakdown voltage $V_Z$ is used to clamp the gate signal. The output of the gate drive in the steady state is

$$\begin{array}{c} v_G = v_{GH} = V_Z \quad \text{if } v_{pwm} = 5 \text{ V} \\ v_G = v_{GL} = V_Z - V_{GG} \text{ if } v_{pwm} = 0 \text{ V} \end{array} \tag{14}$$

As mentioned in the previous section, $v_{GH} \geq V_{DD} - V_{Tp}$ and $v_{GL} \leq V_{Tg}$, and the choice for the $V_Z$ is as follows.

$$V_{Tg} + V_{GG} \geq V_Z \geq V_{DD} - V_{Tp} \tag{15}$$

When we have a close look at the equivalent circuit of a p-n junction diode, two types of capacitance take place: transition capacitance ($C_T$) and the diffusion capacitance ($C_D$).

$$C_{jo} = C_T + C_D \tag{16}$$

In a forward biased diode, diffusion capacitance is much larger than the transition capacitance. Hence, diffusion capacitance is considered in forward-biased diodes. When the gate drive $v_{pwm}$ is high, the current $i_G$ goes through $V_{GG}$ to the ground. The current $i_G$ goes through the ground back to the ground when vs is low. In Figure 12, we first assume that $R_{G,p} = R_{G,n} = R_G$. In the steady state when the gate signal $v_{pwm}$ is high, the diode $D_1$ is in the forward bias, the charge on the diode $D_1$ is

$$Q_{G,h1} = C_D \left(v_{G,h} - V_Z\right) \tag{17}$$

The charge on the capacitor's $C_C$ side is

$$Q_{G,h2} = C_C \left(V_{GG} - v_{G,h}\right) \tag{18}$$

If the charge conservation law is applicable in the dotted box shown in Figure 9 during the time when the gate signal $v_{pwm}$ is low, the diode $D_1$ is in the reverse bias, and the charge on the diode's $D_1$ side is

$$Q_{G,h1} + \Delta Q = C_T \left(v_{G,l} - V_Z\right) \tag{19}$$

The charge on the capacitor's $C_C$ side is

$$Q_{G,h2} + \Delta Q = C_C \left(0 - v_{G,l}\right) \tag{20}$$

It is obtained that

$$(C_D + C_C)v_{G,h} - (C_C + C_T)v_{G,l} = C_C V_{GG} + (C_D - C_T)V_Z \tag{21}$$

In case that $C_C >> C_D >> C_T$ and the diode drains out of the charges during the reverse bias session, so that $Q_{G,h1} + \Delta Q \cong 0$, then

$$v_{G,h} - v_{G,l} = V_{GG} \tag{22}$$

$$v_{G,l} = V_Z \tag{23}$$

The Zener diode is then used instead of a DC battery to lift the charge pump output voltage by an amount of the Zener diode's breakdown voltage.

### *2.5. Synchronous Buck Converter*

Buck converters can be highly efficient (often higher than 90%), making them useful for tasks such as converting a computer's main (buck) supply voltage (often 12 V) down to lower voltages needed by USB (5 V) and DRAM or (1.8 V or 1.25 V or less) using a high-side (HS) MOSFET switch with an adjustable duty. A synchronous buck converter is a modified version of the basic buck converter circuit topology in which the flyback diode is replaced by a low-side (LS) switch, typically another MOSFET switch. Conventional buck converters will delay the turn-on and bring forward the turn-off time to overcome the shooting-through problem; however, it will require two gate drives and a microprocessor to maintain the delay time $t_D$ (Figure 13). The sorting according to the gate drive IC and MOSFET is required to improve the reliability of the synchronous buck converter products. There are gate-driving techniques other than dead-time control, including the zero voltage switching (ZVS) or the zero current control (ZCS), which are useful in high-voltage applications such as the flyback converter [26] and class-E amplifier [27]. For the low input voltage applications, such as the buck converter, the ZVS or ZCS is useful in the discontinuous current mode (DCM), which supplies only low power output. In the context of this paper, we focused only on the continuous current mode (CCM) application using the synchronous buck converter for maintaining the stable voltage output.

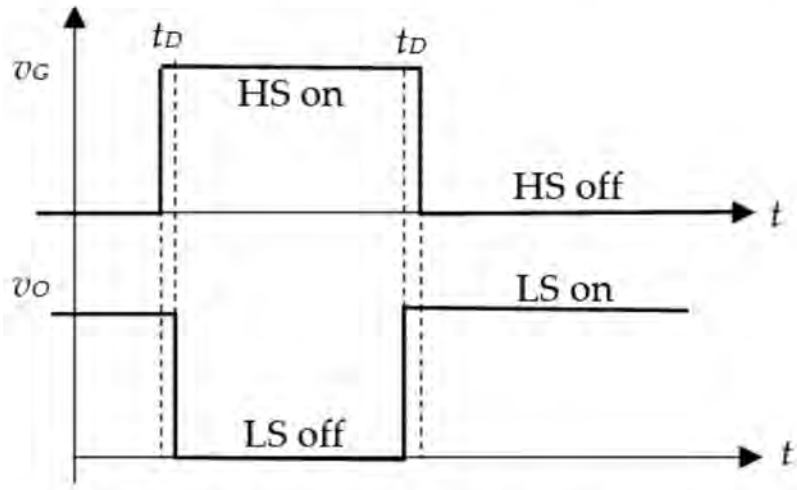



**Figure 13.** The conventional interlock switching to prevent the shooting-though problem.

The proposed buck converter, as shown in Figure 14, consists of a P-Cascode GaN HEMT switch module, the body diode of the PMOS, output inductor $L_1$, and output capacitor $C$, within which only a single gate drive is needed to control both transistors. Features of the proposed synchronous buck converter include (a) it can simplify the gate drive control for only a single gate used; (b) it has no need for two opposite MOSFETs to block the bi-directional current flow on the high side as the GaN HEMT has no body diode (or flyback diode); and (c) the P-Cascode GaN HEMT can be packaged as a whole, reducing the stray inductance and parasitic capacitance. A GaN HEMT with no body diode makes it suitable for half-bridge hard switching, which means no additional hard commutation due to zero reverse recovery. This makes the EMI design simpler and boosts performance. It is especially helpful in compact designs where power conversion and signal processing are on the same small PCB.

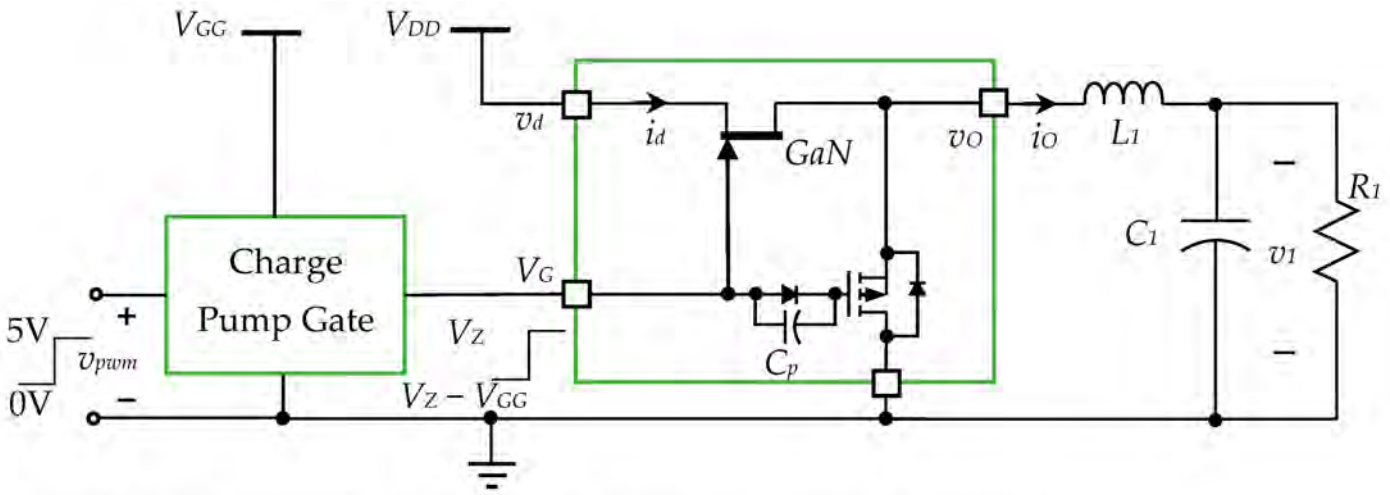



**Figure 14.** Synchronous buck converter using the P-Cascode GaN HEMT.

The GaN HEMT switches between the on and off states during operation. When GaN HEMT is on, the input voltage is connected to the load through the inductor. The capacitor is charging, and the output voltage begins to rise toward the input voltage. The body diode of the PMOS is reverse-biased.

During operation, the GaN HEMT alters between the closed (on) and open (off) states. When GaN HEMT is closed, the input voltage is connected to the load through the inductor, which stores energy in its magnetic field. The capacitor is charging, and the output voltage begins to rise toward the input voltage. The body diode of the PMOS is reverse-biased. The synchronous buck converter improves efficiency by substituting the PMOS switch for the body diode conduction. When a PMOS is used for the lower switch, some diode losses may occur during the time between the turn-off of the high-side GaN and the turn-on of the low-side PMOS, when the body diode of the low-side PMOS conducts the output current.

When GaN HEMT turns on in the duty $\delta$ of a period time $T_S$, the inductor current $i_o$ rises from $i_{o,min}$, to

$$i_{o,max} = (V_{DD} - V_1 - I_o r_{on,GaN})\, \delta T_S / L_1 + i_{o,min} \tag{24}$$

$I_o$ denotes the average current of $i_o$. When GaN HEMT turns off, the inductor current $i_o$ falls from $i_{o,max}$

$$i_{o,min} = (-I_o r_{on,PMOS} - V_1)\, (1 - \delta) T_S / L_1 + i_{o,max} \tag{25}$$

Comparing to Equation (25) with (26), we have

$$V_1 = \delta V_{DD} - I_o\, (\delta(r_{on,GaN} - r_{on,PMOS}) + r_{on,PMOS}) \tag{26}$$

By selecting properly $r_{on,GaN} \approx r_{on,PMOS}$, the above equation yields that

$$V_1 = \delta V_{DD} - I_o\, r_{on,PMOS} \tag{27}$$

Equation (25) yields that

$$i_{o,max} = \delta(1 - \delta) V_{DD} T_S / L_1 + i_{o,min} \tag{28}$$

The energy stored in the magnetization inductor $L_1$ is sent to the resistor during the turn-off time, which is

$$(1/2) L_1 ({i_{o,max}}^2 - {i_{o,min}}^2) = (1 - \delta) T_S ({V_1}^2 / R_1) \approx (1 - \delta) T_S \delta V_{DD}\, (\delta V_{DD} - 2 I_o\, r_{on,PMOS}) / R_1 \tag{29}$$

From Equations (25) and (29), we obtain that

$$((1-\delta)\,V_{DD}\delta T_S/L_1 + i_{o,min})^2 - {i_{o,min}}^2 = 2(1-\delta)\,\delta V_{DD}T_S(\delta V_{DD} - 2I_o\,r_{on,PMOS})/L_1R_1 \quad (30)$$

When $i_{o,min} >> (1-\delta)\,V_{DD}\delta T_S/L_1$, the above equation can be simplified into

$$i_{o,min} = (\delta V_{DD} - 2I_o\,r_{on,PMOS})/R_1 \quad (31)$$

The average output current $I_o$ is

$$I_o = (i_{o,max} - i_{o,min})/2 = \delta(1-\delta)V_{DD}T_S/2L_1 + (\delta V_{DD} - 2I_o\,r_{on,PMOS})/R_1 \quad (32)$$

The above equation can be simplified into

$$I_o = \delta V_{DD}\,(1 + (1-\delta)\,R_1T_S/2L_1)/(R_1\,(1 + 2r_{on,PMOS}/R_1)) \quad (33)$$

In applications where $r_{on,PMOS}/R_1 << 1$, the above equation is simplified into the following by defining $\beta = R_1T_S/2L_1$.

$$I_o = \delta V_{DD}\,(1 + \beta(1-\delta))/R_1 \quad (34)$$

In terms of the switching frequency, the time factor $\beta$ may be written as

$$\beta = R_1/2L_1f_s \quad (35)$$

The power loss on the transistors consists of two parts: (1) the on-resistance loss; and (2) the switching loss of the GaN HEMT. Again, assuming that $r_{on,GaN} \approx r_{on,PMOS}$, the total power loss

$$P_{Loss} = P_{L,on} + P_{L,switching} = (\delta {I_o}^2 r_{on,GaN} + (1-\delta)\,{I_o}^2 r_{on,PMOS}) + \alpha I_o V_{DD} = I_o(I_o r_{on} + \alpha V_{DD}) \quad (36)$$

Comparing with the total power input, we obtain the conversion efficiency $\eta$ as follows.

$$\eta = (1 - P_{Loss}/P_{in}) \times 100\% = ((1 - \alpha/\delta) - I_o r_{on}/V_{DD}) \times 100\% \quad (37)$$

In practice, $r_{on}$ is a monotonic increasing function of $I_o$ and $I_o$ is a monotonic increasing function of the duty ratio. The switching loss factor $\alpha$ is dependent on duty $\delta$. Equation (37) implies that the switching loss at a low duty ratio and the on-resistance loss at the high duty ratio are the dominant factor of the conversion efficiency. Furthermore, the higher $V_{DD}$ means the switching loss becomes more dominant in the conversion efficiency.

The ORCAD PSPICE simulation model for the synchronous buck converter is shown in Figure 15. Instead of using a Zener diode, a DC voltage with 10 V to present the reverse break down voltage of the Zener diode is used. The D-mode GaN HEMT is also replaced by a Power NMOS whose VTO is set to be −4 V to simulate the D-mode GaN HEMT. The gate drive is also simplified by directly driving the BJT's; thus, the input voltage shall be higher than 5 V of the real input gate voltage. The circuit model is simplified that the features from the stray inductance, as indicated in Table 1, and parasitic capacitances are ignored and the Zener diode is replaced by a voltage source. The result from the simulation subjected to different $R_1$ loadings will be reported in the later section with the experiment and Equation (33).

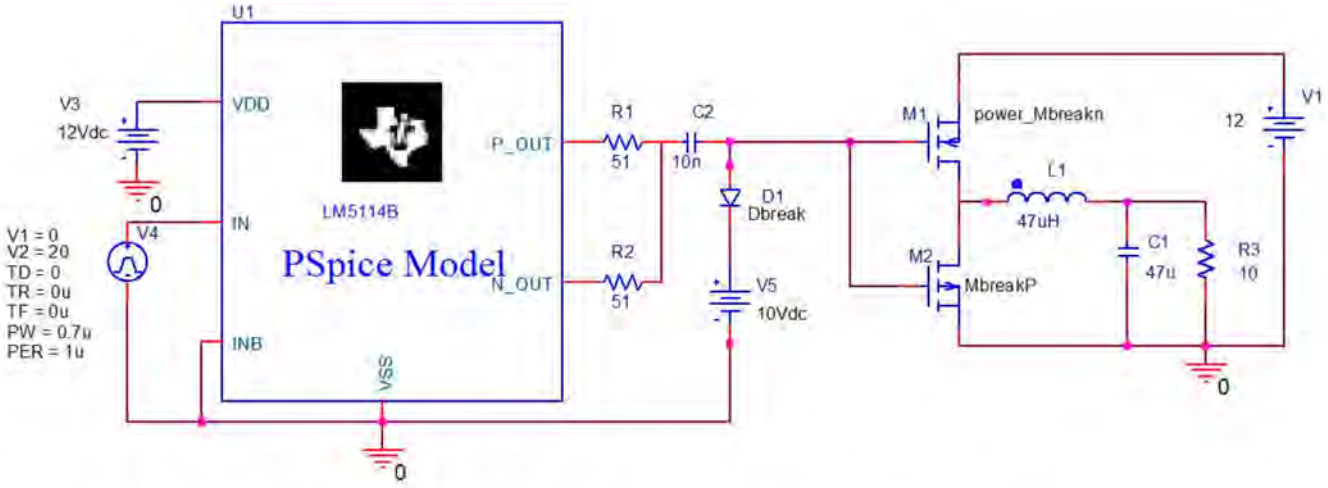



**Figure 15.** SPICE simulation model for the synchronous buck converter.

## 3. Results

We have performed experiments of the synchronous buck converter using P-Cascode GaN HEMT to convert 12 V into an output of 5 V. The experiments follow the circuit shown in Figure 14, with the parameters indicated in Table 2. The power delivery is controlled by the duty ratio $\delta$ from the function generator Tektronix AFG31054. The experiment output for a switching frequency of 500 kHz and $\delta$ = 50% is shown in Figure 16, in which the drain-source voltage $v_{sd,GaN}$ (the orange line) of the GaN and the output voltage $v_1 = v_{sd,MOS}$ (the blue line) are shown. Zooming in on the responses in the dotted rectangle area of the photo in Figure 16a, we draw the individual signals of the voltage and current measurements in Figure 16b,c. It is observed where there is still a minor shooting-through problem in Figure 16b, in that the PMOS turned on before the GaN turns off. It can also be observed that before PMOS turns off, the GaN HEMT is turned on at the synchronous time tick at around 700, as shown in Figure 16b,c. The shooting-through problem will induce the drain-source voltage to ring to the highest value, nearly 25 V, which is double the input voltage of 12 V. It is also observed for the switching loss in Figure 16d that the instantaneous power loss can be as high as 13.14 W although the shooting through persists only for ten nanoseconds. The switching loss is 0.04 W, calculated from taking integration of the multiplication of $v_{sd,GaN}$ of Figure 16b and $i_d$ of Figure 16c within the time tick from 696 to 706, and then dividing the integration by the number of ticks for a switching period, which is one thousand in this case. It is due to the parasitic capacitance of both GaN HEMT and PMOS being small when they are in the off-state, as shown in Table 3. Furthermore, the single direction capacitor $C_G$ shown in Figure 10 in series with the gate of the PMOS has also reduced the input capacitance when it turns on. As a result, it yields a 98.3% efficiency.

**Table 2.** Summary of the synchronous buck converter.

| Symbol | Unit | Description | Value |
|---|---|---|---|
| $L_1$ | µH | Buck Converter | 47 |
| $C_1$ | µF | | 47 |
| $R_1$ | Ω | | 5 |
| PMOS | STD10P6F6 | P-Cascode GaN HEMT Module | - |
| GaN HEMT | NCTU | | Table 1 |
| $C_p$ | pF | | 1000 |
| $C_G$ | nF | | 100 |
| $R_{G,p}$ | Ω | Gate driver | 30 |
| $R_{G,n}$ | Ω | | 51 |
| $C_C$ | nF | | 100 |
| Zener $V_z$ | V | Gate driver, Break down voltage | 10 |
| $V_{DD}$ | V | Voltage Source | 12 |
| $V_{GG}$ | V | | 20 |

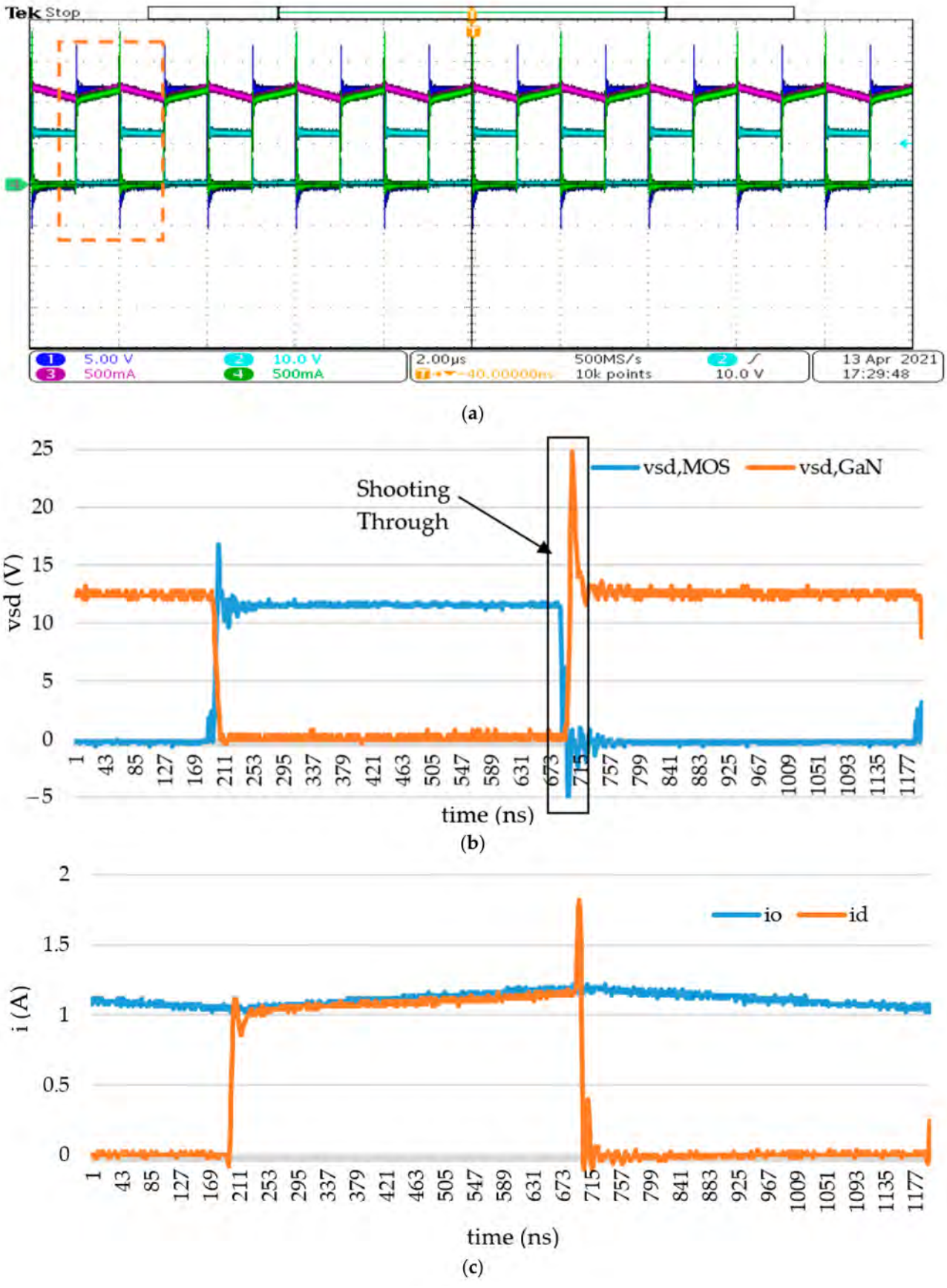



**Figure 16.** *Cont*.

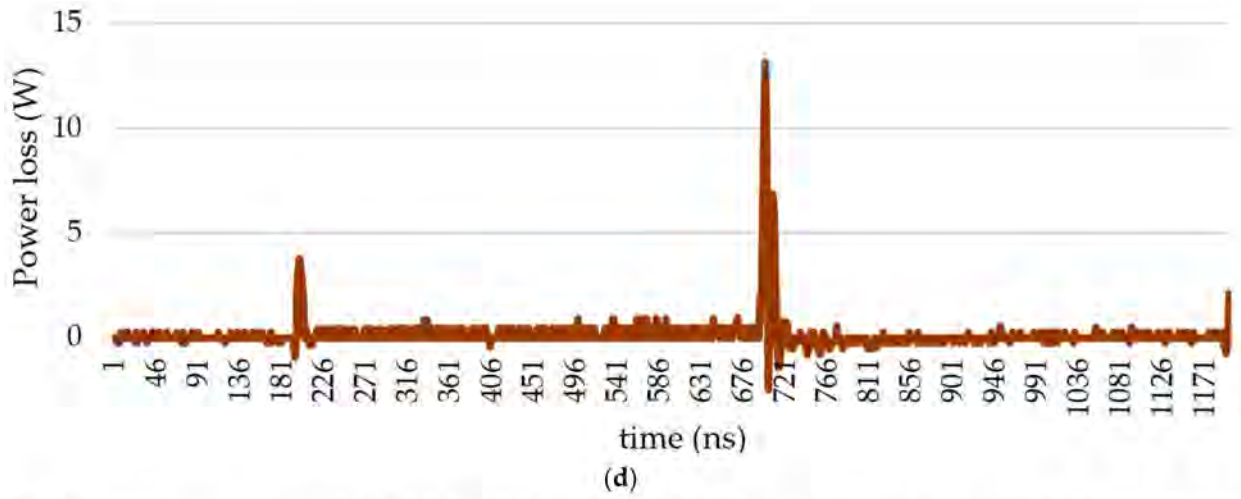



**Figure 16.** The experimental result for 12 V to 6.5 V step down at a switching frequency of 500 kHz and $\delta$ = 50%: (**a**) oscilloscope photo; (**b**) $v_{sd}$ of PMOS and $v_{sd}$ of the GaN HEMT data plot; (**c**) current $i_o$ and $i_d$ plot; and (**d**) the instantaneous power loss ((**b**–**d**): 2 ns per tick).

**Table 3.** The input parasitic capacitance *Ciss* at a switching frequency of 1 MHz.

| Symbol | Unit | Description | Value | |
|---|---|---|---|---|
| | | | 0 V | 12 V |
| *Ciss* | pF | GaN HEMT | 390 | 270 |
| *Ciss* | pF | PMOS | 450 | 370 |

The other experiment for switching frequency at 1 MHz and $\delta$ = 50% is shown in Figure 17 in which the drain-source voltage $v_{sd,GaN}$ (the orange line) of the GaN, the input current $i_D$ (the green line), and the gate voltage $v_G$ (the blue line) are shown. It is shown that GaN is turning on around $v_G = -7$ V at the time tick around 583 (0.8 ns per tick). It is shown that GaN is turning off at the time tick around 1844. Before the GaN is turned-off, the PMOS was turned on and hence the current surged, resulting in a shooting-through problem. This experiment is via a Zener diode with a higher reverse breakdown voltage $V_Z$ to 11 V in Equations (17)–(23). As shown in Figure 17b, equivalently we had clamped the gate voltage $v_G$ up by 1 V relative to the threshold voltage $V_{Tg}$ and $V_{Tp}$ when $V_Z$ = 11 V. This will cause the output ringing according to Equations (12) and (13) and Figure 11. This output ringing will induce the input current to ring simultaneously during the GaN turning off, which results a larger switching loss. In Figure 18, with each time tick on the horizontal axis being 0.8 nanosecond, the switching losses for different Zener diodes are compared. All of the three configurations have a similar width on the top, but they are different on the bottom. As a result, the switching loss coefficient $\alpha$ in Equation (36) will be different when a different Zener diode is used. In our case study, the switching loss of $V_Z$ = 11 V is the worst of the three choices. It is also worth noting that no matter what the value of $V_Z$, it can never find a snappy recovery nor uncontrolled high $dI_{rr}/dt$ when GaN turns on, as shown in Figure 17a,b. In the future, there may be implementation of the synchronous buck converter using two cascode D-mode GaNs to further reduce the EMI since, in some applications, the cost and weight of the filter can nullify the benefits of power efficiency improvement.

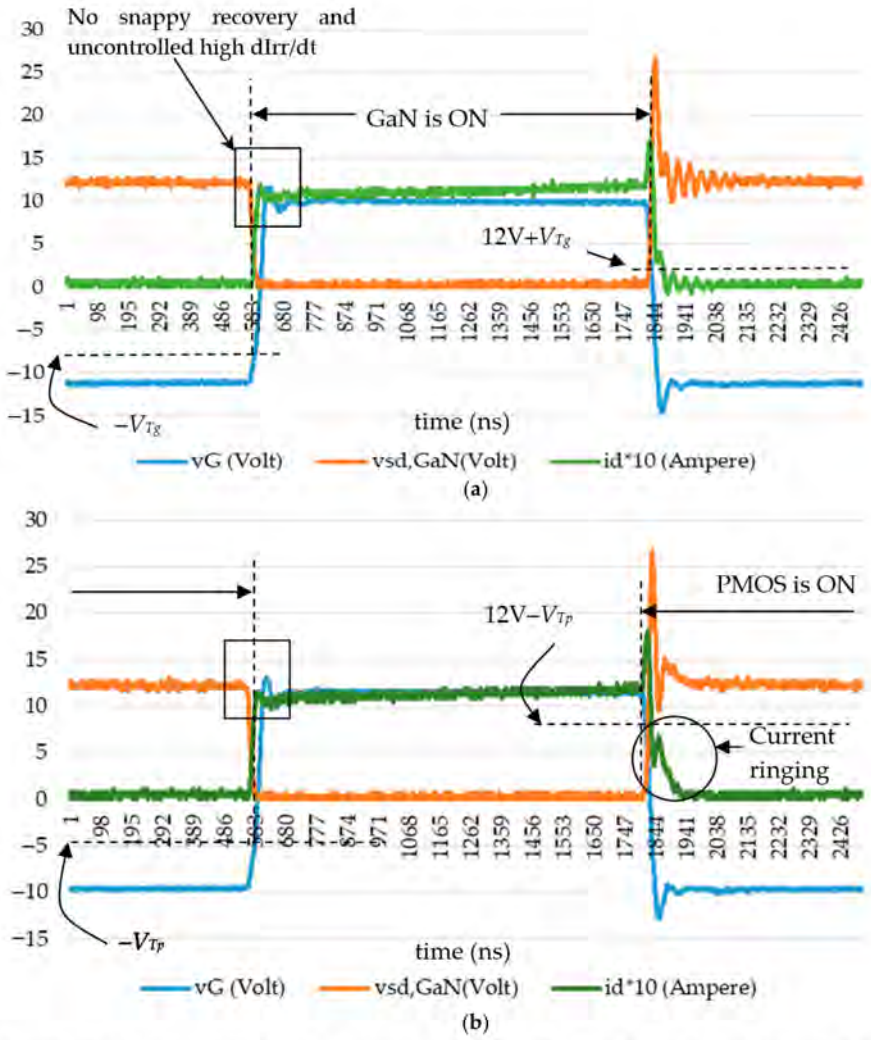



**Figure 17.** The experimental result for the 12 V to 6 V step down at a switching frequency of 1 MHz with (**a**) $V_Z$ = 10 V and (**b**) $V_Z$ = 11 V (0.8 ns per tick).

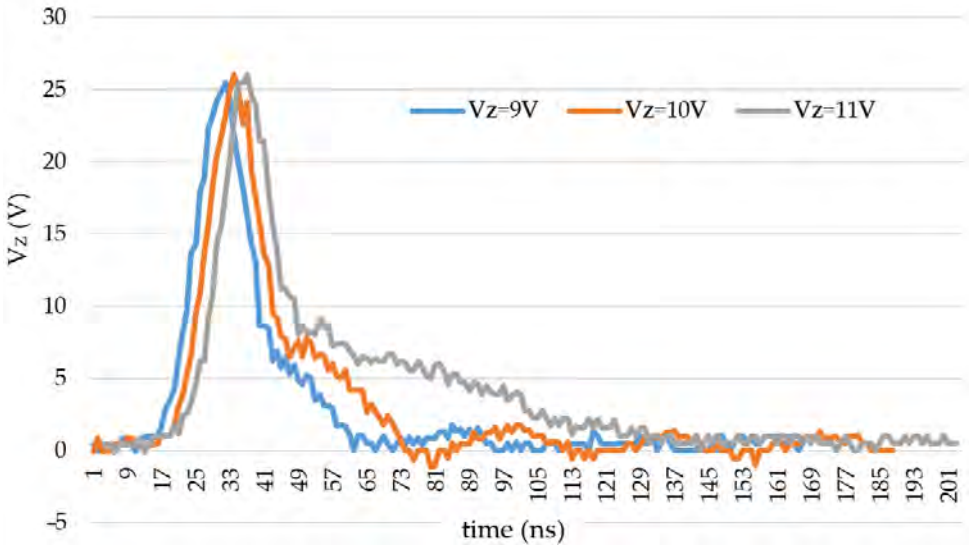



**Figure 18.** Comparison of the switching losses due to different Zener diodes (0.8 ns per tick).

More experiments due to a different duty ratio $\delta$ at 500 kHz are summarized into Figure 19. There is a sink after a duty ratio of 60% that comes back again at a higher duty ratio. From Equation (34), we obtain that

$$\beta = 5/(2 \times 47 \times 10^{-6} \times 500 \times 10^{3}) = 0.11, \quad (38)$$

$$I_o = (12/5)\delta(1 + 0.11(1 - \delta)) \quad (39)$$

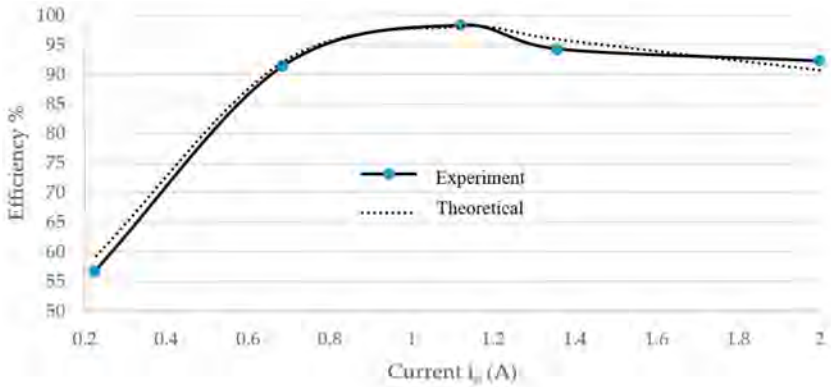



**Figure 19.** The P-Cascode GaN HEMT efficiency at a 500 kHz switching frequency vs. a different output current via duty control.

When the duty ratio is 10%, the current is measured as 223 mA and the efficiency is 56%, the $r_{on}$ is estimated around 200 mΩ at the deep saturation region, and $V_{DD}$ = 12 V. Compared to Equation (37), it is concluded that the switching loss factor $\alpha$ is around 0.044 from the following equation.

$$((1 - \alpha/0.1) - 0.223 \times 0.2/12) \times 100 = 56 \quad (40)$$

Substituting $\alpha = 0.01 + 0.1 \times |\delta - 0.5|$ and $r_{on} = (0.1 + 0.1\delta)$ Ω into Equation (37) and providing that $(r_{on,PMOS}/R_1)$ in Equation (33) reduced the actual amount of the current, we used the following equation to estimate the efficiency and compare the theoretical result also in Figure 19.

$$\eta = ((1 - \alpha/\delta) - 0.83 \cdot I_o r_{on}/V_{DD}) \times 100 \quad (41)$$

In the experimental results analysis shown in Figure 20, we excluded the coil loss and capacitor loss because we want to clarify the P-Cascode GaN HEMT. When we actually calculate the power of the load, the output power is calculated from

$$P_{out} = {I_O}^2 R_1 \quad (42)$$

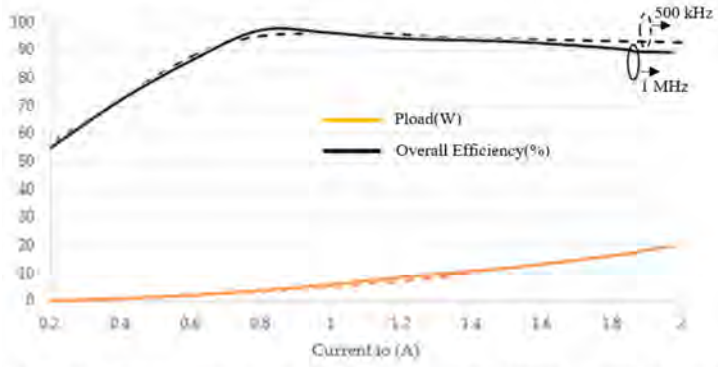



**Figure 20.** The power to load and overall efficiency at the 500 kHz and 1 MHz switching frequencies vs. the different output currents via duty control.

The efficiency is calculated from the power output divided by the power input, which is same as that of Figure 19. The result of the experiments subjected to the same load $R_1$ = 5 Ω with 500 kHz and 1 MHz switching frequencies were compared and shown in Figure 20. The overall efficiency for 500 kHz is more than 92% at 20 W output and the overall efficiency for 1 MHz is 89% at 20 W output; however, it yields a better overall efficiency, which is 97% compared to 95% from the 500 kHz switching, at 5 W output. The reason why they are not compared in the same figure is because they were obtained by adjusting the duty ratio from 10% to 90% and the current readings for a different frequency are different according to Equations (34) and (35). The higher the frequency is applied to the switching, the lower the current output is.

The standard efficiency evaluation is measured by varying the load when fixing the switching frequency and the duty cycle. The result of the experiments subjected to different $R_1$ loads with fixed duty at 50% are compared and shown in Figure 21. It can be observed from Equation (36) that the total power loss increases when the output current increased. It is also observed that the switching loss factor $\alpha$ in Equation (36) will increase as the switching frequency increases. The power output in the experiment can be calculated by Equation (42), which are from 1 to 10 W. The standard efficiency evaluation based on a 1 MHz switching frequency was also used to compare the simulation shown in Figure 15 and Equation (33). A comparison among the experiment, simulation, and Equation (33) is shown in Table 4. The Equation provides a higher output current than both the experiment and simulation do. The efficiency predicted by the simulation is lower than the experiment, which may be as a result of the output from the gate driver, which is the LM5114 PSpice model downloaded from TI Instrument®, not responding as fast as the practical ones subjected to the switching of the input signal $v_{pwm}$.

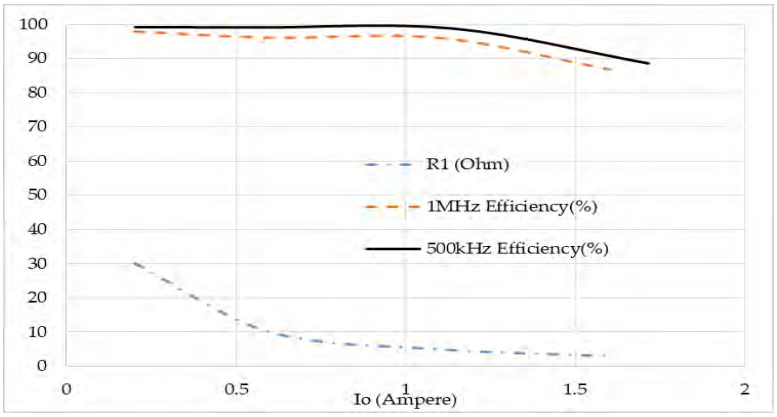



**Figure 21.** The power efficiency of the 500 kHz and 1 MHz switching frequencies with $\delta$ = 50% vs. different loadings.

**Table 4.** Comparison among the experiment, simulation, and Equation (33).

| $R_1$ (Ohm) | $I_o$ (Ampere) | | |
|---|---|---|---|
| | **Experiment** | **Simulation Figure 15** | **Equation (33)** |
| 30 | 0.20135 | 0.192 | 0.199 |
| 10 | 0.549 | 0.56 | 0.594 |
| 5 | 1.111 | 1.097 | 1.176 |
| 3 | 1.614 | 1.76 | 1.935 |
| $R_1$(Ohm) | **Efficiency** | | |
| | **Experiment** | **Simulation Figure 15** | **-** |
| 30 | 98 | 92 | - |
| 10 | 96.1 | 93.3 | - |
| 5 | 96.2 | 86.4 | - |
| 3 | 86.9 | 81.5 | - |

The oscilloscope we used in the experiment is a Tektronix MDO 3054, which has four inputs: we used two voltage probes and two current probes, measuring simultaneously the signals. The efficiency evaluation is influenced both by the error on the measured input power and on the measured output power despite the measure data being synchronized. In the literature [28], dealing with extreme efficiency in power electronics, the measurement data are acquired in the two-chamber calorimeter that handles the temperature control. In this paper, we only use the air conditioner to maintain a stable room temperature and performed the experiments intermittently to reduce the temperature effect on the experiments. As indicated in Figure 22a, we measured four signals, including $v_{sd,GaN}$, $v_{sd,PMOS}$, $i_d$, and $i_o$, and added the two measures $v_{sd,GaN}$ and $v_{sd,PMOS}$ together into the voltage input. The power input is calculated by the average of the multiplication on the 10,000 samples of 6 to 10 periods of switching, as follows.

$$P_{in} = \sum i_d \left(v_{sd,GaN} + v_{sd,PMOS}\right) \tag{43}$$

and

$$P_{out} = \sum i_O \times v_{sd,PMOS} \tag{44}$$

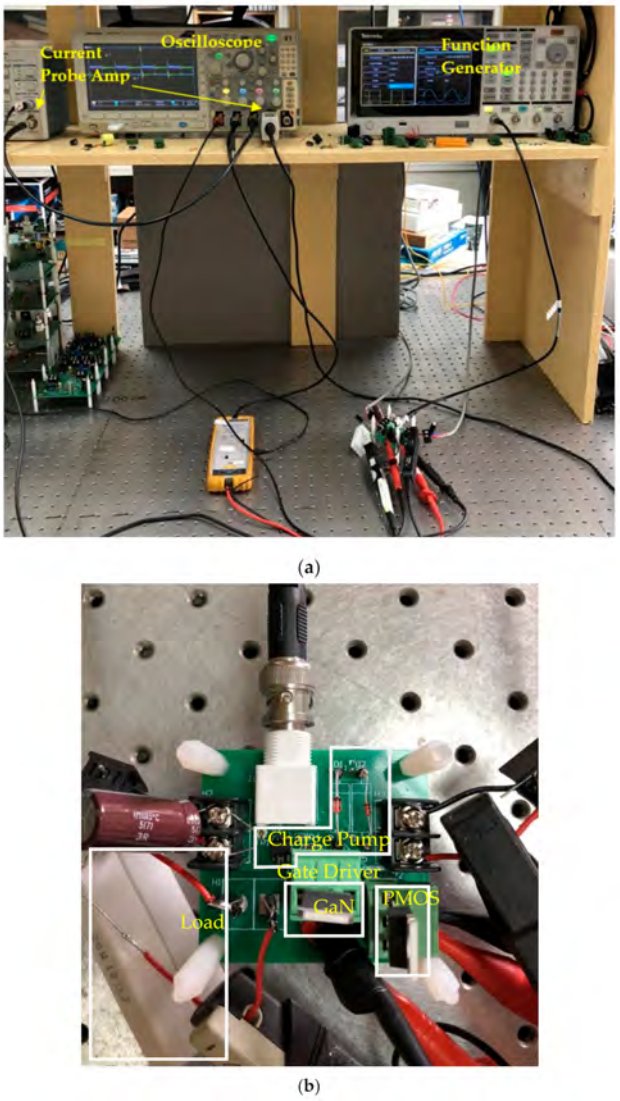



**Figure 22.** (**a**) Experimental setup and (**b**) photo of the circuit in the experiment.

The high efficiency part of the experiment is done by averaging the efficiency calculations from different experiments with the identical setting. In was hopeful, at least theoretically, that the variance of the efficiency measure be reduced by the number of times of measurements.

The photo of the circuit in the experiment is shown in Figure 22b. Since all of the components used are rather standard and handy for the SiP packaging, it may be implemented in an IC form factor later.

## 4. Conclusions

An innovative design of a new GaN HEMT synchronous buck converter is proposed. This synchronous buck converter is associated with a PMOS transistor; thus, it will need only one single gate drive to perform the DC/DC conversion, which is suitable for the point of load (POL) applications. In order to solve the shooting-through problem when only a single gate drive is used, the characteristics of both GaN HEMT and the PMOS must be studied. To compensate for the differences between GaN HEMT and the PMOS, an additional gate drive design is necessary. To fulfill the transistor matching, we used a single direction capacitor that prolonged the turn-on delay time in the PMOS. Furthermore, to prevent the output spike of the GaN HEMT during the turn-on period, we needed to reduce the gate resistance and equivalently to increase $\alpha$ in the above equation. Since the GaN HEMT is used on the high side, a Zener diode is used instead of a DC battery to lift the voltage, which is identical to the breakdown voltage of the Zener diode from the original charge-pump gate drive output. The circuit was implemented and tested. The result in the proposed circuit specification shows that the P-Cascode GaN HEMT efficiency is higher than 98% at a switching frequency 500 kHz and duty ratio $\delta$ = 50%. When the output is up to 20 W, the overall efficiency can be higher than 92%. In the future, we will find a better-matched PMOS to achieve a higher switching frequency for the NCTU GaN HEMT; i.e., the turn-on and turn-off voltage must have a good match for the D-mode GaN HEMT and the parasitic capacitance of the PMOS must be made smaller to match the parasitic capacitance of the GaN HEMT. Nevertheless, the SPICE simulation model must also be carefully studied in order to predict the better design requirements.

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