Non-Integer Order Approximation of a PID-Type Controller for Boost Converters

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Abstract: In this work, the voltage regulation of a boost converter is addressed. A non-integer order PID controller is proposed to deal with the closed-loop instability of the system. The average linear model of the converter is obtained through small-signal approximation. The resulting average linear model is considered divided into minimum and normalized non-minimum phase parts. This approach allows us to design a controller for the minimum phase part of the system, excluding temporarily the non-minimum phase one. A fractional-order PID controller approximation is suggested for the minimum phase part of the system. The proposal for the realization of the electrical controller is described and its implementation is used to corroborate its effectiveness when regulating the output voltage in the boost converter. The fractional-order PID approximation achieves regulation of the output voltage in the boost converter by exhibiting the iso-damping property and using a single control loop, which confirmed its effectiveness in terms of controlling non-minimum phase/variable parameter systems.

Keywords: DC–DC boost converter; fractional-order controller; iso-damping property; non-minimum phase system; PID controller

1. Introduction

DC–DC power converters are one of the most studied and applied devices of power electronics. From elementary configurations of DC–DC converters, the boost conversion mode is one of the most used and implemented, mainly because of its ability to step up the converter power supply, which allows interconnecting higher voltage demanding loads with lower-level power sources. The application range includes high-efficiency power supplies [1], DC motor drives [2], and renewable energy conversion systems [3], to mention the most relevant.

The main drawback of DC–DC boost converters is related its closed-loop instability, caused by the presence of a right-half plane zero in the model, and the difficulties it produces when regulating the output voltage. This control problem has attracted the attention of researchers, who have proposed a significant amount of techniques attempting to regulate the voltage/current in boost converters. Some of the most recent and relevant results can be summarized as follows: In [4,5], disturbance rejection approaches were suggested. Either by state-feedback linearization or a linear quadratic regulator, the output voltage of boost converter was regulated. The strategies resulted in fast recovery, zero steady-state error, and good disturbance rejection. In [6–9], a sliding mode technique, in combination with two switching surfaces, a twisting algorithm, or an adaptive back stepping approach, was suggested. Either to minimize current/voltage overshoot or chattering reduction, the strategies achieved acceptable dynamics, zero steady-state error, fast convergence, and high robustness.

In [10], a multi-loop predictive control strategy was proposed. The outer voltage loop employed the reference generated by a maximum power point tracking (MPPT) to calculate the current reference. The inner current loop minimized the error through inductor current variation rates for the two states of the switch. The results showed a reduction in the settling time, steady-state error, and overshoot. In [11], a non-linear tracking control with an energy-shaping approach was proposed to regulate the voltage in a boost converter. A self-tuner was suggested to update the invariant surface according to the output tracking error. The strategy proved the exponential convergence and performance recovery properties of the output without steady-state error.

In [12,13], voltage regulation of a boost converter was achieved using a non-linear passivity-based control. The synthesized controllers worked on the principle of energy shaping plus damping injection over the plant, which resulted in Lyapunov-stable systems with small ripple, acceptable error characteristics, and time constants. In [14–18], PI/PID controllers, based on either quantitative feedback theory, neural networks, or a particle swarm/genetic algorithm optimization-based control were suggested. Robustness was required considering the non-minimum phase nature and bandwidth limitations of the system. The strategies resulted in response enhancement, decrement in switching losses due to fewer on–off switch operations, and a disturbance rejection improvement for several operating conditions.

Recently, fractional calculus has been considered as an alternative to improve modeling, performance, and efficiency when controlling DC–DC converters. With the aim of mainly improving the transient and permanent response, the velocity of regulation, and robustness, many strategies have been adapted to integrate the definition of the fractional-order derivative/integral to the control objective. The main advantages of using fractional calculus are as follows [19,20]:

- Reduced levels of noise due to lower order derivatives;
- Robustness against parameters variations;
- Better description of certain system frequency response;
- Ladder and fractal arrangements of typical electrical elements are used to implement fractional relations.

Some recent results summarizing the use of fractional calculus in converters control are as follows: Robust-optimal controllers to improve output error-tracking were suggested in [21,22]. Optimized fractional-order PI controllers to eliminate oscillations, steady-state variations, and overshoots were used. A non-linear error-modulator, to improve convergence in the transient response, and different optimization algorithms were considered. The scheme produced a rapid transient response and improved damping with disturbance rejection, robustness, and time optimality. In [23], a fractional-order PI controller was proposed for output voltage regulation. The design consisted of a load variation-tracking scheme to ensure output regulation with a high tolerance to load variability. The controller demonstrated robust behavior against unknown load variations and stability. A typical fractional-order PID controller was proposed in [24]. Output capacitance and input inductance characterization was used to approximate the closed-loop transfer function with a first-order system. Its digital implementation demonstrated less overshoot and faster recovery. In [25,26], an adaptive sliding mode controller with a fractional-order approach was suggested for tracking the inductor current in a boost converter. The adaptation rules were based on Lyapunov functions and state observers. The speed of the transient response and robustness were improved.

In this paper, the approximation of a non-integer order PID-type controller to regulate the output voltage in a DC–DC boost converter is proposed. Besides modeling accuracy and good robustness in the presence of parameter variations from fractional calculus, the approach is suggested for its ability to control non-minimum phase systems. The controller design and approximation procedure focus on the minimum phase part of the extended model of the system. Since the proposed control strategy draws on fractional calculus, it is expected to produce a system frequency response that exhibits the iso-damping property.

The approximation procedure takes into account the robustness and desired closed-loop characteristics, to deliver a structure of a band-limited flat phase response. The output transient and permanent behavior exhibited a good performance and stable regulation. The experimental results corroborate the effectiveness and viability of the resulting fractional-order approximation in controlling non-minimum phase systems.

The paper is organized as follows: Section 2 provides the preliminaries concerning topics related with the scope of this work, i.e., the boost converter model, the method to approximate fractional-order differentiator, and the synthesis of the controller structure. In Section 3, the algorithm to approximate the fractional-order PID controller is provided step-by-step. The control problem and electrical implementation of the fractional-order PID controller are also provided in this section. A discussion on the obtained results is provided in Section 4 and the most relevant conclusions are presented in Section 5.

2. Materials and Methods

2.1. Boost Converter Model

The DC–DC boost converter is an electronic device with the ability to step up its input voltage to provide a higher and continuous power supply. This makes it ideal to interconnect higher voltage demanding loads with low-voltage sources. In Figure 1, the electronic diagram of the boost converter is shown. On the assumption of ideal components and a continuous conduction mode (CCM), the continuous average model of the boost converter is obtained as follows [27]:

$$
\begin{aligned}
L\frac{di_L}{dt} &= V_g - (1-\bar{D})v_C, \\
C\frac{dv_C}{dt} &= (1-\bar{D})i_L - \frac{v_C}{R},
\end{aligned}
\tag{1}
$$

where $\bar{D} \in [0,1]$ stands for the average of the duty cycle D; V_g denotes the DC power supply; and L, C, and R are the inductance, capacitance, and resistance, respectively.
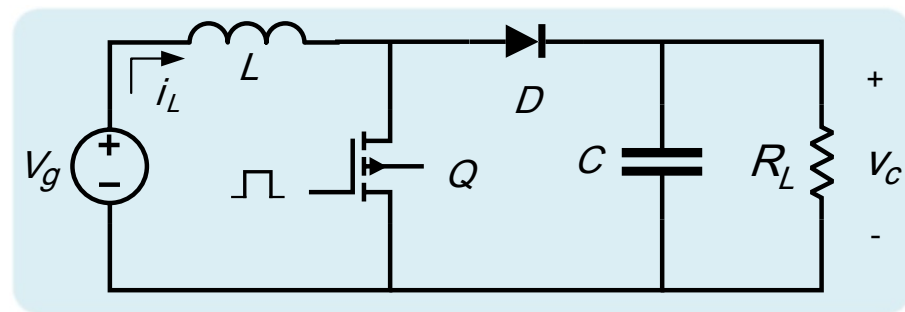

Figure 1. Electrical diagram of DC–DC boost converter.

By linearizing (1) and obtaining the transfer function of the boost converter, the small-signal representation is obtained. This technique consists of perturbing every signal of the original model to generate its DC and AC components [28]. The state space representation $\dot{x} = Ax + Bu$ and $y = Cx$ of the linearized small-signal average model of the boost converter around the equilibrium point, $[i_L, v_C] = \left[V_g/(R(1-\bar{D})^2), V_g/(1-\bar{D})\right]$, is given as follows [28]:

$$
\begin{bmatrix} \dot{\hat{i}}_L \\ \dot{\hat{v}}_C \end{bmatrix} = \begin{bmatrix} 0 & \frac{-(1-\bar{D})}{L} \\ \frac{(1-\bar{D})}{C} & \frac{-1}{RC} \end{bmatrix} \begin{bmatrix} \hat{i}_L \\ \hat{v}_C \end{bmatrix} + \begin{bmatrix} \frac{V_g}{L(1-\bar{D})} & \frac{1}{L} \\ \frac{-V_g}{RC(1-\bar{D})^2} & 0 \end{bmatrix} \begin{bmatrix} \hat{d} \\ \hat{v}_g \end{bmatrix},
\tag{2}
$$

and

$$
y = \begin{bmatrix} 0 & 1 \end{bmatrix} \begin{bmatrix} \hat{i}_L \\ \hat{v}_C \end{bmatrix},
\tag{3}
$$

where $\hat{i}_L$, $\hat{v}_C$, $\hat{d}$, and $\hat{v}_g$ are the perturbation terms of i_L, v_C, $\bar{D}$, and V_g, respectively.

The relation $\hat{d}$-to-$\hat{v}_c$ corresponds to the boost converter transfer function $G_p(s)$ as follows:

$$G_p(s) = C(sI - A)^{-1}B_1, \tag{4}$$

where $B_1 = \left[\frac{V_g}{L(1-\bar{D})} \quad \frac{-V_g}{RC(1-\bar{D})^2}\right]^T$. Thus, the extended transfer function of the system is given by

$$G_p(s) = \frac{\left(\frac{V_g}{CL}\right) - \left(\frac{V_g}{RC(1-\bar{D})^2}\right)s}{s^2 + \left(\frac{1}{RC}\right)s + \frac{(1-\bar{D})^2}{CL}}, \tag{5}$$

which is a non-minimum phase transfer function due to the right-half plane (RHP) zero. The extended boost converter transfer function (5) can be divided into factors as follows:

$$G_p(s) = G_{pm}(s)G_{nm}(s), \tag{6}$$

where

$$G_{pm}(s) = \frac{\left(\frac{V_g}{RC(1-\bar{D})^2}\right)\left(\frac{R(1-\bar{D})^2}{L} + s\right)}{s^2 + \left(\frac{1}{RC}\right)s + \frac{(1-\bar{D})^2}{CL}}, \tag{7}$$

$$G_{nm}(s) = \frac{\frac{R(1-\bar{D})^2}{L} - s}{\frac{R(1-\bar{D})^2}{L} + s}, \tag{8}$$

are the minimum phase and normalized non-minimum phase parts of $G_p(s)$, respectively. Note that (8) is an all-pass system, i.e., $|G_{nm}(j\omega)| = 1$, which resembles the Padé approximation of the delay [29],

$$e^{-s\tau} \approx \frac{2/\tau - s}{2/\tau + s}, \tag{9}$$

thus, the converter dynamic is given by the minimum phase part $Gpm(s)$.

The methodology to approximate the non-integer PID controller is described in the next section.

2.2. The Approximation of Non-Integer Order for Laplacian Operator

The so-called integro-differential operator, $s^{\pm\alpha}$, for $0 < \alpha < 1$, can be approximated as follows [30,31]:

$$s^\alpha \approx T\left(\frac{s}{\omega_c}\right) = \frac{a_0\left(\frac{s}{\omega_c}\right)^2 + a_1\left(\frac{s}{\omega_c}\right) + a_2}{a_2\left(\frac{s}{\omega_c}\right)^2 + a_1\left(\frac{s}{\omega_c}\right) + a_0}, \tag{10}$$

where (10) is a biquadratic module that produces a flat phase curve, ω_c is the center frequency, and a_0, a_1, a_2 are real constants defined as

$$\begin{aligned} a_0 &= \alpha^\alpha + 3\alpha + 2, \\ a_2 &= \alpha^\alpha - 3\alpha + 2, \\ a_1 &= 6\alpha \tan\frac{(2-\alpha)\pi}{4}. \end{aligned} \tag{11}$$

The approximation (10) behaves as differentiator of fractional-order around ω_c for $a_0 > a_2 > 0$. The derivative effect can be corroborated by assuming $\omega = \omega_c = 1$ and computing that the phase contribution of (10) is $\arg\{T(j1)\} > 0$, which produces a flat phase curve as long as [30,31]

$$\arg\{T(s/\omega_c)|_{j\omega_c}\} = \pm\alpha\pi/2. \tag{12}$$

In the next section, the procedure to obtain the fractional-order PID controller structure is described.

2.3. The Synthesis of the Approximation of a Fractional-Order PID Controller

The structure of the fractional-order $PI^\alpha D^\mu$ controller is described as [32]

$$G_c(s) = k_p \left(1 + \frac{1}{T_i s^\alpha} + T_d s^\mu \right), \tag{13}$$

where $\alpha, \mu \in (0, 1)$, k_p, T_i, T_d are the proportional gain, integral, and derivative time constants, respectively.

T_i and T_d are related through $T_i = \eta T_d$, where η is a constant, which was investigated through different design and optimization strategies to determine its effect in finding unique solutions for (13) [33,34]. A slight modification in (13) allowed us to create a perfect square trinomial and, by setting $\alpha = \mu$, $\eta = 1$, (13) can be expressed as follows:

$$G_c(s) = \frac{k_c (T_i s^\alpha + 1)^2}{s^\alpha}, \tag{14}$$

which is a common way to simplify the PID structure [35], where $k_c = k_p / T_i$.

By manipulating (10) as $s^\alpha \approx T(s) \equiv N(s)/D(s)$ and then substituting in (14), $G_c(s) = k_c(N(s)/D(s))$ as $T_i \to \infty$, or $G_c(s) = k_c(D(s)/N(s))$ as $T_i \to 0$, which confirms the differentiator (integrator) effect of the fractional-order operator s^α, $\phi_c = \pm \alpha \pi / 2$ is the controller phase contribution.

It is well known that the phase of the plant to be controlled, which in this case is given by ϕ_{pm}, the controller phase ϕ_c, and phase margin ϕ_m, are related as $\phi_c + \phi_{pm} = -\pi + \phi_m$ at the phase crossover frequency ω_{pc}, which implies that $\phi_c = \phi_m - \pi - \phi_{pm}$; thus,

$$\alpha = \frac{(-\pi - \phi_{pm} + \phi_m)}{(\pi/2)}. \tag{15}$$

Since (10) exhibits a flat phase response, the system frequency response is expected to exhibit the iso-damping property once the controller is applied; thus, investigating different values for gains T_i and k_c is suggested in order to obtain those that produce the required effect, since, as previously explained, the effect of (14) can be varied from integrator ($T_i \to 0$) to differentiator ($T_i \to \infty$).

In the following section, the controller design is described step-by-step. Numerical simulations are provided to corroborate the effectiveness of the fractional-order PID controller approximation.

3. Results

In this section, the synthesis and design process to obtain the approximation of a PID controller is described. Numerical and experimental results are provided. An electrical representation of the controller is obtained to validate its effectiveness over the complete system.

3.1. Control Design

The non-integer order approximation of the PID controller for the boost converter is synthesized in the following steps:

1.　Consider the boost converter transfer function divided into minimum/non-minimum phase parts $G_{pm}(s)$ and $G_{nm}(s)$, respectively;
2.　Consider the minimum phase transfer function $G_{pm}(s)$ as the uncontrolled plant;
3.　Determine the phase contribution of the uncontrolled plant ϕ_{pm} with no control effort;
4.　Compute the controller phase contribution $\phi_c = \phi_m - \pi - \phi_{pm}$;
5.　Compute the corresponding fractional order α through (15);
6.　Compute the fractional-order Laplacian operator through (10);
7.　Compute the controller structure $G_c(s)$ as a function of T_i and k_c gains;
8.　Obtain the closed-loop transfer function and evaluate the stability margins;

9. Determine the regulation and tracking performance of the closed-loop response.

The control strategy and controller design are developed under the following conditions: the descriptions of the boost converter transfer function (5) and (6) with the parameter values in Table 1 and the equilibrium point $[i_L, v_C] = [2.572, 25]$, which means that the desired output voltage is $v_C = v_o = 25$ V.

Table 1. Values for the parameters of the boost converter shown in Figure 1.

Element	Notation	Value
DC voltage source	V_g	18 V
Capacitor	C	20 μF
Inductor	L	22 mH
Resistance (Load)	R_L	13.5 Ω
Switching frequency	f_s	20 kHz

Acceptable robustness is achieved by ensuring a phase margin within 30–60° [29]. For this case, $g_m \geq 10$ dB and the desired phase margin $\phi_m = 50°$. From step 1 to 3, by considering the boost converter minimum phase transfer function $G_{pm}(s)$, the parameter values in Table 1, and $\bar{D}_{25\,V} = 0.28$, the uncontrolled plant phase contribution is $\phi_{pm} = -157.7°$. From step 4, the controller phase contribution to achieve the required phase margin is $\phi_c = 27.7°$. From step 5, the fractional order for the PID controller (14) computed through (15) is $\alpha = 0.3078$. From step 6, the fractional-order Laplacian operator is given as follows:

$$s^\alpha \approx \frac{N(s)}{D(s)} = \frac{3.619s^2 + 1.605 \times 10^6 s + 8.141 \times 10^{10}}{1.772s^2 + 1.605 \times 10^6 s + 1.662 \times 10^{11}}, \tag{16}$$

which produces the frequency response in Figure 2 for the approximation (10), where the phase contribution of 27.7° from the fractional-order controller can be corroborated.
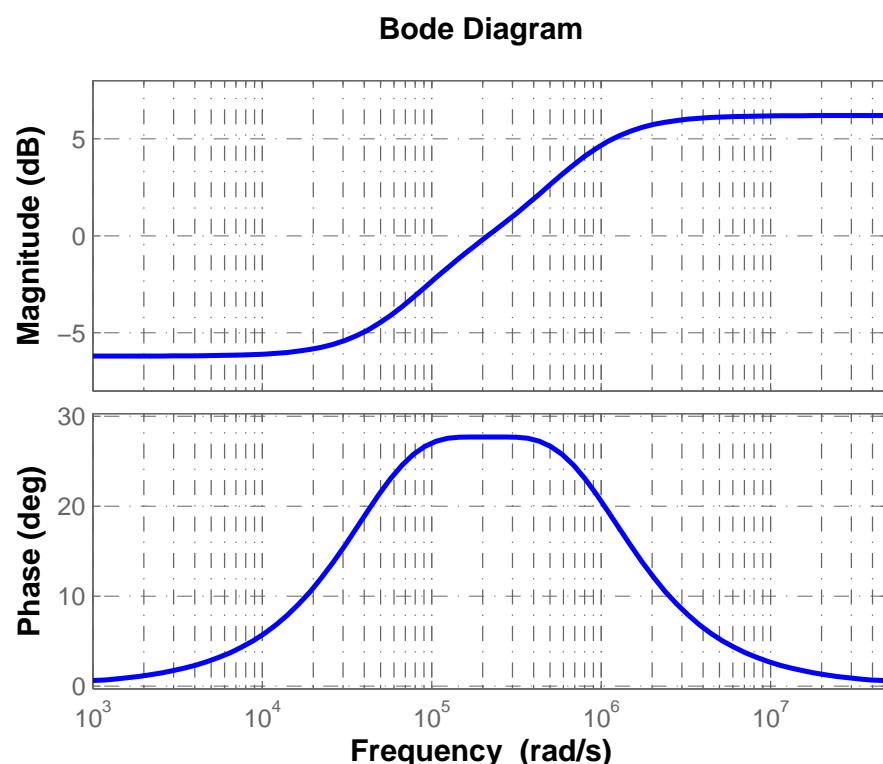
Figure 2. Frequency response for the approximation (10) with the fractional order $\alpha = 0.3078$.

From step 7, the controller structure (14) is given by

$$G_c(s) = \frac{k_c(T_i N(s) + D(s))^2}{N(s)D(s)}, \tag{17}$$

where $N(s)$ and $D(s)$ are the numerator and denominator of approximation (10), respectively. The controller's most significant effect is obtained within the range $[0, 5]$ of T_i and k_c. From step 8, several conditions, summarized in Table 2, were found to reach the desired phase margin with different output performances.

Table 2. Values of T_i and k_c to achieve the phase margin of $\phi_m = 50°$ in a typical unit feedback closed-loop system.

T_i	k_c	ϕ_m	T_i	k_c	ϕ_m
0.001	5.5	50.4°	1	0.185	50.4°
0.01	5.2	50.4°	1.5	0.075	50.8°
0.0894	3.3	50.3°	2	0.035	50.6°
0.3	1.3	50.6°	2	0.8	50.2°

The most relevant characteristics of the data from Table 2 are the phase margin invariability for different values of gains T_i and k_c, which confirms the presence of the iso-damping property when using fractional calculus [36]. This results in an additional advantage when using this type of controllers, as different values of T_i and k_c allow one to modify the time response for the same phase margin. Please note from Table 2 that the controller produces the same phase margin for either the derivative ($T_i \to \infty$) or integral ($T_i \to 0$) effect, as previously explained. The iso-damping property allows one to achieve the same stability margin in the presence of gain variations due to the frequency response flatness around the crossover frequency [37].

The controller parameters were set at $T_i = 2$ and $k_c = 0.8$ to minimize oscillations and achieve acceptable time constants; thus, the fractional-order controller of PID-type (17) is given as follows:

$$G_c(s) = \frac{\rho_1 s^4 + \rho_2 s^3 + \rho_3 s^2 + \rho_4 s + \rho_5}{\psi_1 s^4 + \psi_2 s^3 + \psi_3 s^2 + \psi_4 s + \psi_5}, \tag{18}$$

where $\rho_1 = 64.96$, $\rho_2 = 6.943 \times 10^7$, $\rho_3 = 2.33 \times 10^{13}$, $\rho_4 = 2.535 \times 10^{18}$, $\rho_5 = 8.662 \times 10^{22}$ and $\psi_1 = 6.415$, $\psi_2 = 8.655 \times 10^6$, $\psi_3 = 3.323 \times 10^{12}$, $\psi_4 = 3.975 \times 10^{17}$, $\psi_5 = 1.353 \times 10^{22}$.

Figure 3 shows the closed-loop step response in which the output regulation can be confirmed. From step 9, it is determined that the response reaches the reference in a short period of time, where the time constant is $\tau \approx 1.08$ µs, the peak time is $t_p \approx 4.5$ µs, the overshoot is %M ≈ 20 %, and the negligible steady-state error is $e_{ss} \approx 0$.

The robustness of the closed-loop system in the presence of parameter uncertainties was investigated through a μ-analysis, which allowed us to analyze the feedback systems, separating what is known from what is unknown, where μ is the structured singular value. Bounds of structured singular values μ_Δ provide information about the uncertainty magnitude and frequency in which system destabilization occurs, where Δ is the set of possible uncertainties [38]. The considered parameter uncertainty is $\pm 30\%$ its nominal value. Figure 4 shows the upper and lower bounds of μ_Δ. Since stability margins are the reciprocal of structured singular values μ_Δ, the upper bound of μ_Δ located at the peak $\mu_\Delta = 0.34$ provides the lower bound of the stability margin, which means that the closed-loop system becomes unstable for uncertainties above 295% the specified value.
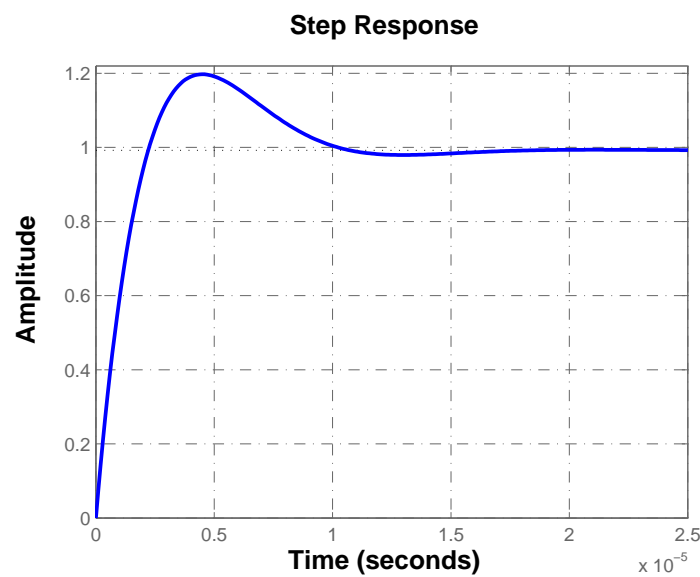
Step Response

Figure 3. Closed-loop step response of the boost converter produced by the synthesized fractional-order controller (18).
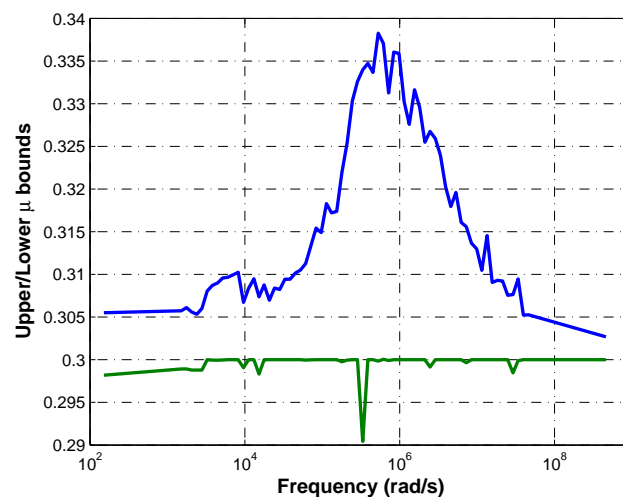
Figure 4. Upper/lower bounds for structured singular value μ_Δ to investigate the closed-loop robustness in the presence of parameter uncertainties.

Up to this point, the proposed fractional-order PID approximation effectively regulated the output of the system model (7) with a fast and robust response, which exhibits a stable tracking characteristic.

In the remainder of this section, the viability of the proposed approach is investigated. The electrical implementation of the controller was generated and validated to determine its viability as an alternative to regulate the voltage in boost converters.

3.2. Results of Electrical Implementation

To synthesize the electrical arrangement of the fractional-order controller, consider the following: the effect of the controller (14) can be modified through T_i; thus, it can be predicted that its time domain representation is given in terms of real poles, since its final structure can be either $G_c(s) = k_c T_i^2 N(s)/D(s)$ ($T_i \to \infty$), $G_c(s) = k_c D(s)/N(s)$ ($T_i \to 0$), or $G_c(s) = k_c(T_i N(s) + D(s))^2/N(s)D(s)$ (any other T_i), which depend on the numerator/denominator of the approximation (10).

Determining all possible values of the approximation parameters $a_0(\alpha)$, $a_1(\alpha)$, $a_2(\alpha)$ and noting that its numerator/denominator is a quadratic polynomial, real poles are

obtained as long as $a_1^2 > 4a_2a_0$. Figure 5 shows the evolution of $a_0(\alpha)$, $a_1(\alpha)$, $a_2(\alpha)$ for all possible values of α; thus, the condition $a_1^2 > 4a_2a_0$ holds for all α.
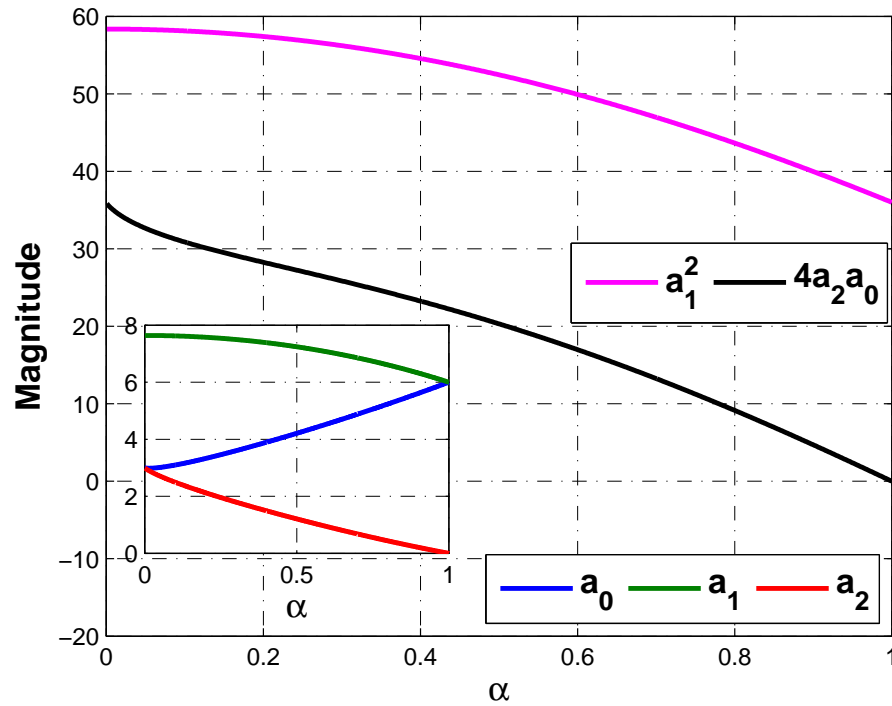

Figure 5. Parameters a_0, a_1, a_2 and values a_1^2 and $4a_2a_0$ to ensure the condition $a_1^2 > 4a_2a_0$ holds.

To generate the electrical configuration of non-integer order approximation (18), its partial fraction expansion representation, which is given in terms of real poles, is given as follows:

$$G_c(s) = A_1\left(\frac{1}{\gamma_1 s + 1}\right) + A_2\left(\frac{1}{\gamma_2 s + 1}\right) + A_3\left(\frac{1}{\gamma_3 s + 1}\right) + A_4\left(\frac{1}{\gamma_4 s + 1}\right) + A_5, \quad (19)$$

where constants A and coefficients γ are listed in Table 3.

Table 3. Coefficients and constants for partial fractional expansion (19) of the fractional-order approximation (18).
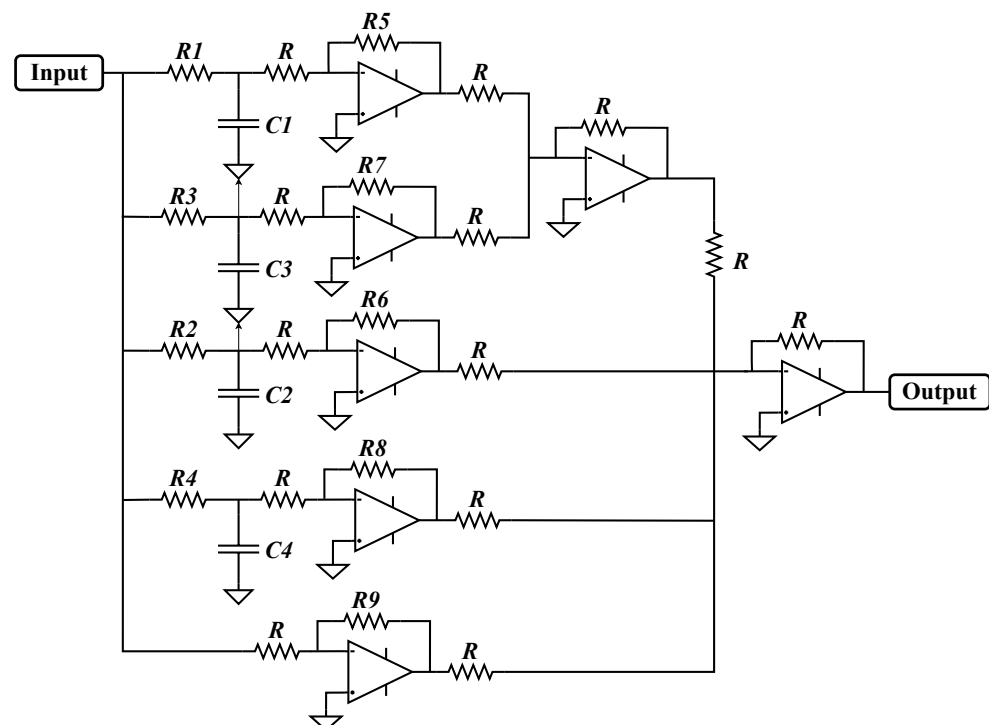
Constant	Coefficient
$A_1 = -4.5478$	$\gamma_1 = 1.2716 \times^{-6}$
$A_2 = 0.4152$	$\gamma_2 = 2.5965 \times 10^{-6}$
$A_3 = -1.6609$	$\gamma_3 = 8.3849 \times 10^{-6}$
$A_4 = 1.1369$	$\gamma_4 = 1.7121 \times 10^{-5}$
$A_5 = 12.6574$	

The mathematical term $A/(\gamma s + 1)$ resembles the transfer function of a first-order system; thus, an RC circuit is used to generated it. The controller (19) is electrically implemented with capacitors, resistors, and operational amplifiers.

The electrical diagram for the partial fractional expansion (19) of the PID controller approximation (18) is shown in Figure 6, the parameter values of which are provided in Table 4. Note that the parameter values of the resistances and capacitors in Table 4 are all commercial; thus, the proposal for electrical implementation in Figure 6 of non-integer order approximation of the PID-type controller (18) is achievable.

Table 4. Component values for the electronic diagram of the controller in Figure 6 for the experimental implementation of partial fractional expansion (19).

Parameter	Value 1	Parameter	Value
R_1	6.62 Ω	R_8	1.1 kΩ
R_2	7.64 Ω	R_9	12.7 kΩ
R_3	9.7 Ω	R	1 kΩ
R_4	16 Ω	C_1	0.2 μF
R_5	4.5 kΩ	C_2	0.34 μF
R_6	0.4 kΩ	C_3	0.9 μF
R_7	1.7 kΩ	C_4	1.1 μF

**Figure 6.** Electrical diagram to generate the partial fraction expansion (19).

Prior to validating the effectiveness of the proposed controller, simulation results from PSIM are shown in Figure 7. The regulation of the output voltage $v_o(t)$ for the reference signal $v_r = 25$ V and its average value are shown. The inductor current in also shown in this figure in order to corroborate the CCM operation. Notice that the fractional-order PID controller approximation (18) successfully regulates the voltage of the boost converter from Figure 1. It took approximately 1 ms for the proposed controller (18) to make the plant reach the reference signal.
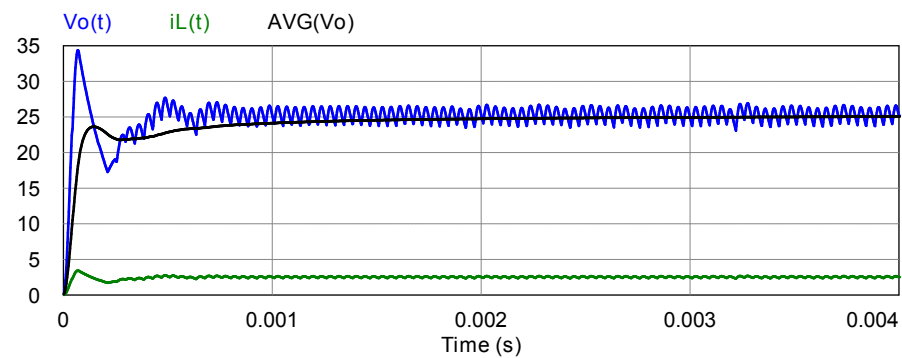
Figure 7. Output voltage $v_o(t)$, its average value, and the inductor current $i_L(t)$ for reference signal $v_r = 25$ V.

A comparison between the fractional-order PID approximation and the typical PID controller allowed us to determine that the former outperforms the latter. The PID controller was tuned through the pole placement of the closed-loop transfer function to ensure a compromise between stability and output performance. Recalling that an increase in stability margins decreases the performance parameters and vice versa, the tuning of the typical PID balanced the process to achieve acceptable values of time constants, such as τ, t_s, t_r, t_p, or $\%M$ and e_{ss} for the desired stability margins. The MatLab PID tuning algorithm was used to corroborate the obtained controller parameters, which targets a phase margin of 60° and a compromise between performance, providing a solid and neutral alternative to avoid biased tuning that could purposefully highlight the performance of the proposed approach. The similarity of both results led us to conclude that the former values were appropriate. The PID controller parameters are $[k_p, \ T_i, \ T_d] = [5, \ 0.1797, \ 0.2 \times 10^{-6}]$. The derivative and integral modes can be electrically generated with operational amplifiers in those configurations and the parameter values $[R_d, \ C_d] = [1 \ \Omega, \ 0.2 \ \mu\text{F}]$ and $[R_i, \ C_i] = [10 \ \text{k}\Omega, \ 17.97 \ \mu\text{F}]$, respectively. The proportional mode was achieved with a unit gain adder. The summation of the modes was performed through an adder with feedback and input resistors of 5 kΩ and 1 kΩ, respectively.

Figure 8 shows a comparison of the step response for both synthesized controllers applied to the minimum phase part of the boost converter (7). In order to quantify the improvement achieved through the fractional-order PID controller approximation, the performance parameters for the responses are provided in Table 5. One concludes, comparing the settling time t_s, that the response of fraction-order approximation settles in half the time it took for the response with the PID controller. The rise time t_r, time constant τ, and overshoot $\%M$ demonstrate a similar behavior, i.e., they are all smaller for the proposed non-integer order PID controller approximation.
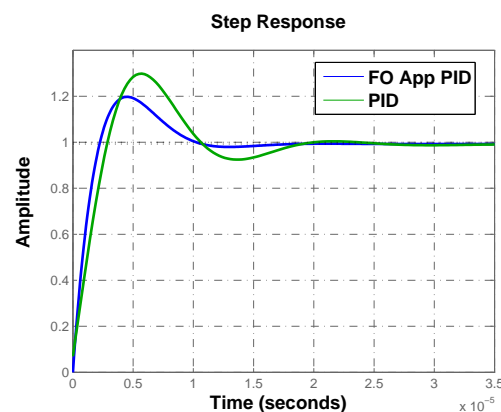

Figure 8. Comparison of the step response of the minimum phase part of the boost converter (7) when fractional-order PID controller approximation and typical PID controller are applied.

Table 5. Closed-loop step response performance parameters for the minimum phase part of the boost converter (7).

Parameter	Notation	Proposed PID	Typical PID
Steady-state error	e_{ss}	0.001	0
Time constant	τ	1.09 μs	1.58 μs
Rising time	t_r	1.68 μs	2.24 μs
Peak time	t_p	4.48 μs	5.71 μs
Settling time	t_s	9.65 μs	18.1 μs
Overshoot	%M	20%	29.8%

The implementation results that corroborate the effectiveness of the suggested approach are provided in Figures 9 and 10. The experiment was performed to obtain the desired output voltage of $v_C = v_o = 25$ V, while the converter operates with the specified load of $R_L = 13.5$ Ω. The prototype is made up of: a fixed ferrite inductor AGP4233-233ME of 22 mH, 20%, 24 A, a typical series resistance of 2.95 mΩ, and magnetic shielding to minimize EMI; a metallized polypropylene film capacitor of 20 μF, a maximum DC voltage of 500 V, 10% tolerance, and an ESR of 11 mΩ with the commercial number EZP-E50206LTA; the selected switch is a silicon Carbide (SiC) power MOSFET SCT3120ALHRC11, with a maximum drain-source voltage of 650 V, a continuous drain current of 21 A (at 25 °C), and an ON resistance of 156 mΩ; and lastly, a diode MUR 1520 with forward voltage of 1 V. For controller implementation, the low cost, high speed, 4 MHz wide-bandwidth quad JFET inputs operational amplifier LF347N was selected. The traditional TL494 was used for the PWM signal. Resistances and capacitors with commercial values and a tolerance of ±1% were used to achieve the parameter values for the controller. Figure 9a shows the worktable with the implementation of the boost converter regulated with the synthesized fractional-order PID controller approximation. Figure 9b shows the electrical diagram of the closed-loop control system composed of the converter, the fraction-order PID controller approximation, and the measuring device.

(a)

Figure 9. *Cont.*
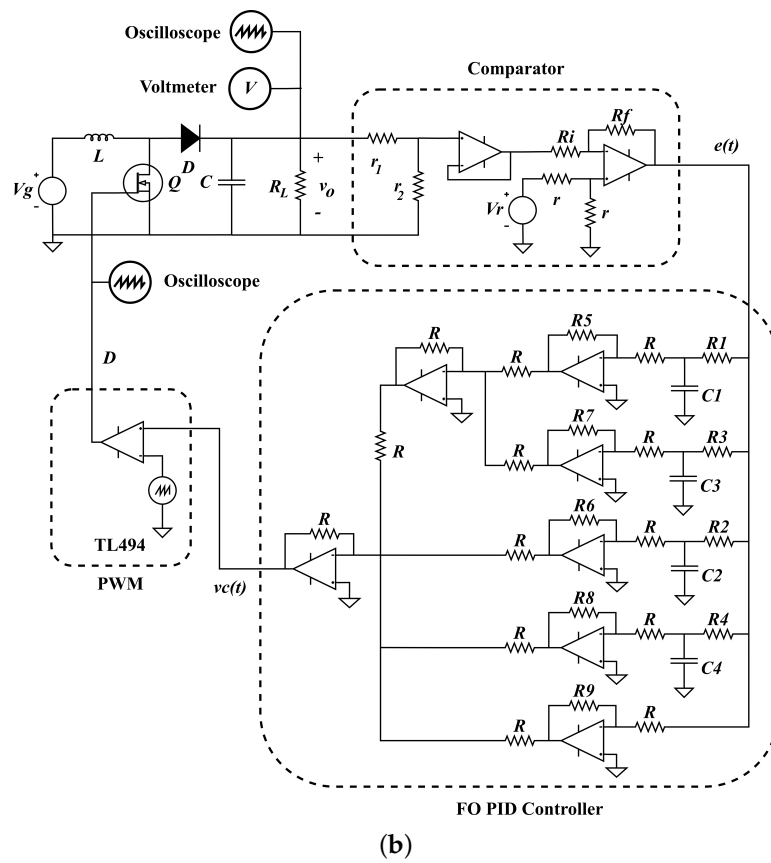
(b)
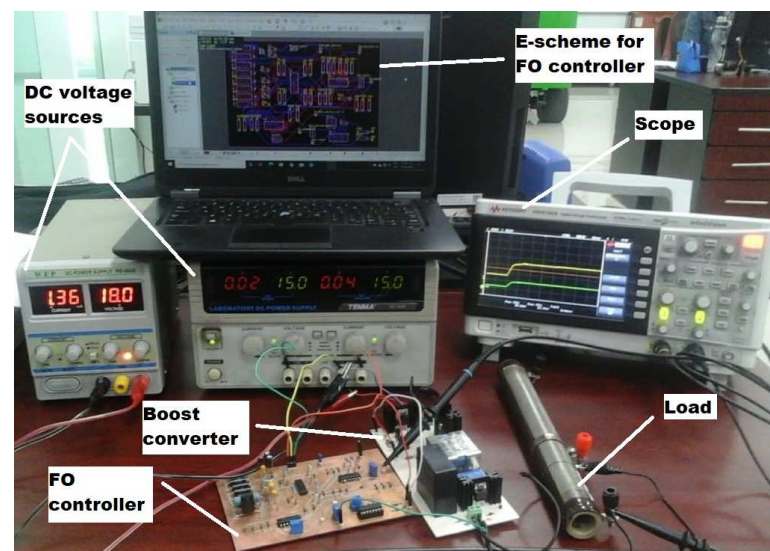
Figure 9. (**a**) Worktable with the implementation of the non-integer order PID controller approximation. (**b**) Electrical representation of the experiment of voltage regulation in a boost converter.
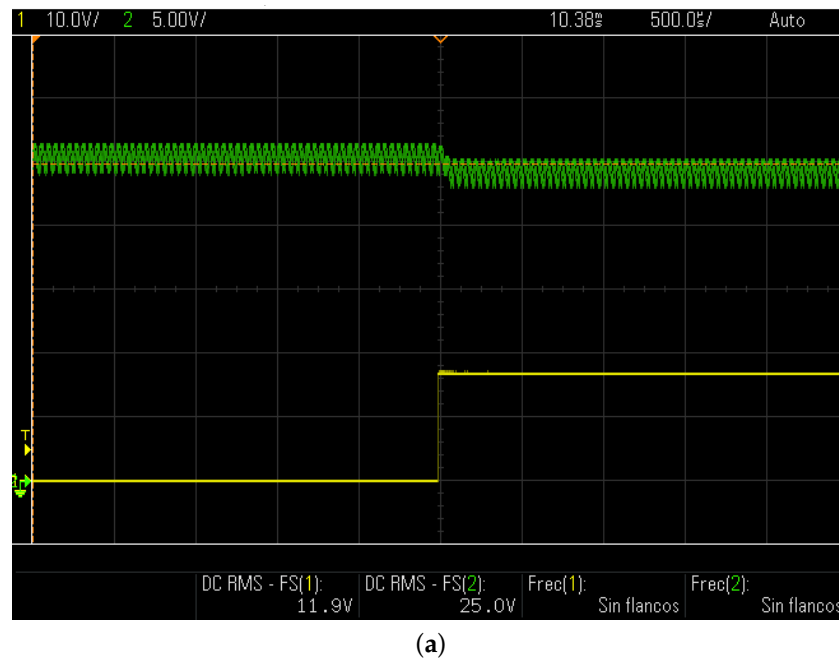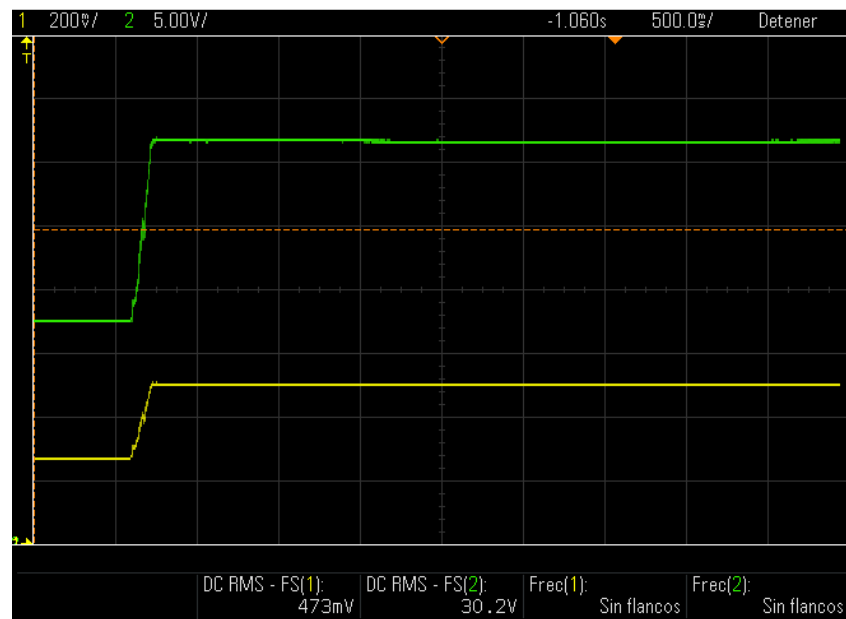

(a)

Figure 10. *Cont.*

(b)

Figure 10. Effective regulation of synthesized non-integer order PID controller. (**a**) Voltage regulation (top line) in the presence of load variation (bottom line). (**b**) Tracking characteristics of the output voltage (top line) for reference changes (bottom line).

Figure 10a shows the effectiveness of the proposed controller at regulating the output voltage in the boost converter. In addition, to determine the controller's ability to maintain regulation, a small load variation from $R_L = 13.5\ \Omega$ to $R_L = 18\ \Omega$ was introduced. One can see that, in spite of increment of the load (bottom line), the output voltage (top line) slightly varies, oscillating around the reference value. In Figure 10b, the tracking characteristics of the controller can be corroborated, since the output voltage (top line) behaves in a very similar way to the reference signal (bottom line) when it changes from $v_r = 20$ V to $v_r = 30$ V.

Finally, in Figure 11, the experimental measurement of the phase contribution of arrangement in Figure 6 is shown. One can see that the proposed electrical arrangement behaves with a derivative effect as expected, with its phase contribution center being around 2 kHz.

The advantages of the proposed fractional-order PID controller approximation can be summarized as follows:

- As a linear technique, it regulated the output voltage in a non-linear system;
- Effective regulation in a non-minimum phase system;
- Closed-loop instability caused by the RHP zero was avoided effectively;
- Acceptable stability margins and good robustness;
- Fast regulation velocity;
- Simplicity in structure;
- Viability for implementation.

In the next section, we discuss the presented results.
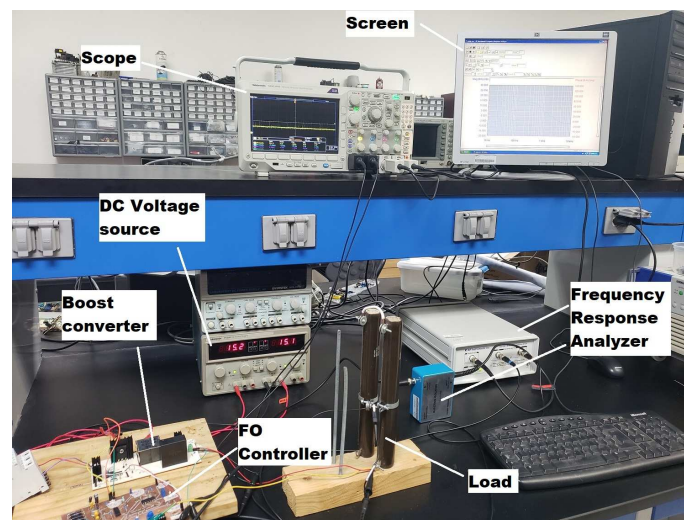
(**a**)
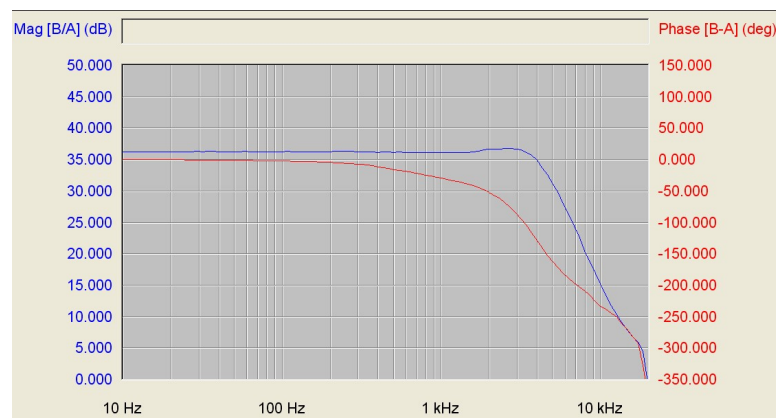
(**b**)

Figure 11. Frequency response of the proposed PID controller approximation. (**a**) Worktable with the equipment for the experiment. (**b**) Experimental measurement of controller phase contribution from the arrangement in Figure 6 obtained with the Frequency Response Analyzer, Model 300, 0.01 Hz/30 MHz, AP Instruments.

4. Discussion

In this paper, voltage regulation in a boost converter was performed. The system model was considered divided into minimum and non-minimum phase parts. The approximation of a non-integer order PID controller was suggested in order to achieve the control objective. The controller design considered the minimum phase part of the system, yet it successfully achieved the output voltage regulation of the complete system. This is the most remarkable result and confirms that fractional-order controllers perform acceptably when controlling variant-parameter or non-minimum phase systems.

The effectiveness of the controller approximation was validated through its electrical implementation. The experimental results corroborated that the output voltage of the boost converter was effectively regulated, demonstrating a fast and stable tracking characteristics. The experimental results were provided and described to corroborate the effectiveness and viability of the proposed approach.

The following things are worth mentioning: firstly, the presence of the iso-damping property produced by the controller confirms that, even though it results from an approximation, the property was inherited from fractional calculus; secondly, the simplicity of the suggested approach is noteworthy, as the control objective was achieved through a single control loop. The common method to address the voltage regulation of a boost

converter is through multi-loop control, i.e., one loop for regulating the voltage and another for regulating the current, in combination with minimization/optimization algorithms. Certain other techniques utilize a non-linear approach, mainly due to the closed-loop instability of the system.

A similar approach applied to a buck converter was reported in [39]. The main difference between both results lies in the way the control strategy was designed, since the boost converter is described by a non-minimum phase transfer function of varying parameters. In addition, the main objective of the control strategy in this manuscript was to avoid the closed-loop stability caused by a right-half plane zero, while appropriately regulating output voltage. Herein, we present a simpler electrical diagram of the controller than the one reported for the buck converter. Moreover, our design produced a stable and fast response, while achieving the desired stability margins.

5. Conclusions

The viability of a fractional-order PID controller for regulating the voltage in a boost converter was investigated. The non-integer approach was introduced into the controller design to exploit the ability of fractional calculus to control non-minimum phase systems. A biquadratic module with a flat phase response was used to approximate the fractional-order Laplacian operator. The tuning process was reduced to determine the controller's required effect through the time constant T_i. The performance parameters of both the proposed approach and a typical PID controller indicate the superiority of the former. The response velocity, determined through time constants τ, t_r and t_s, suggested its viability for analog implementation.

The controller representation in partial fractional expansion allowed us to directly generate its electrical equivalence through an *RC* circuit. The resulting electronic arrangement regulated the output voltage in the boost converter with a fast response and stable tracking characteristics.

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