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A Systematic Study on the Harmonic Overlap Effects for DC/AC Converters under Low Switching Frequency Modulation

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Abstract: In most high power industrial applications, the low switching frequency modulations (LSFM) are usually implemented to reduce power loss and heat dissipation pressure. However, there are some unexpected influences caused by the low order harmonic sinusoidal pulse width modulation (SPWM), such as the imbalanced submodule power in cascaded half-bridge inverter (CHB) and limited output power capability in H-bridge neutral-point-clamped (HNPC) converter. This paper starts by generalizing the basic characteristic of two-level SPWM, then deeply investigates the influences of low-frequency modulation on the operation of the circuits. They are classified into three mechanisms and generally named as harmonic overlap effect (HOE). The corresponding solutions to copy with the mechanisms are proposed and verified in some topologies through high-power simulations in simulations. In addition, a comprehensive summary of the influences and solutions of these effects on typical high power converters is drawn. The design rules of the modulation schemes for multilevel voltage source converters (VSCs) at low switching frequency are also proposed.

Keywords: high power conversion; low switching frequency modulation; multilevel converters; harmonic overlap effect

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1. Introduction

Medium-to-high (>1 MW) power conversions are essential for many industrial applications. To reduce heat dissipation pressure and improve system efficiency, the low switching frequency (<1 kHz) is usually utilized in the modulation process [1]. For example, the switching frequency of two-level (2 L) inverter in the Chinese railway of high-speed CRH5 is limited to 250 Hz [2]. However, it brings troublesome harmonic problems on the motor side. To avoid these problems, at the lower carrier ratio (*Cr*, the ratio of carrier frequency over the fundamental output frequency), optimized modulation methods [3] are often used to avoid or minimize the influence of low order harmonics. For example, Figure 1 shows the whole modulation method for Chinese railway of high-speed HXD1. When fundamental frequency rises to medium-and high-speed ranges, carrier ratio will drop, making the asynchronous modulation in the low-speed zone no longer applicable. Thus, the selective harmonic elimination PWM (SHEPWM) is often used to eliminate low-order harmonics. If the speed further increases, the motor will step into square wave mode. There will be only one switching in one fundamental period. Nevertheless, SHEPWM and the square wave mode are difficult to be compatible with the vector control, which has better dynamic performance [4]. Moreover, SHEPWM is more complicated to realize because it needs pre-calculated angles.

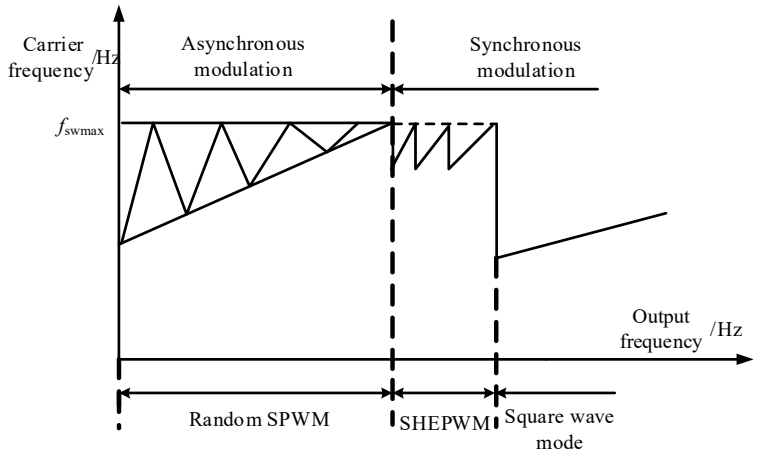


Figure 1. The modulation scheme for a traditional 2 L traction converter.

To further increase the voltage and power level, multilevel converters like cascaded half-bridge (CHB) [5,6] and modular multilevel converter (MMC) [7,8] are proposed and implemented in many applications, and have drawn ever increasing attention. However, in terms of modulation methods, the simplest phase disposition PWM (PDPWM) [9,10] and carrier phase shift PWM (CPS) [11] are still used because of their simpleness. When the switching frequency is low, the equivalent switching frequency is high on the output side, and low-order harmonics are canceled out, which avoids their influence on the dc and ac sides. However, in each submodule, due to the reduction of Cr, the low-order harmonics will impact the device stress and the submodule dc side itself. In [12], it is found that different phase shifted angles in the submodule in CHB will bring imbalanced active power under LSFM. The author of [13] proposes that in order to use low-frequency CPS in MMCs, the optimal Cr should be selected as 2.5 when Cr $\leq$ 5. In the increasingly mature industrial applications, a summary of the switching frequency and modulation method for common industrial high power products is listed in Table 1, where f_{sw} is the switching frequency, and f_0 is the fundamental output frequency.

Table 1. Switching frequency and modulation method for industrial high power converters.

Product	Topology, Maximal Power (MW)	Maximal f_{sw}/Hz	Maximal f_o/Hz	Modulation Method
HXD1 [14]	2L-VSC 0.817	250	116	Piecewise SPWM to SHEPWM
HXD2 [15]	2L-VSC 1.275	800	220	Piecewise SPWM to SHEPWM
HXD3 [16]	2L-VSC 1.25	450	120	Piecewise SPWM to SHEPWM
ConverteamMV7000 [17]	NPC 40	500	250	PDPWM and SVPWM
Perfect Harmonic [18]	CHB 132	250	120	CPS-PWM
GH150 [19]	MMC 13.7	1000	120	CPS-PWM
M2 L-3000 [20]	MMC 7.466	600	60	CPS-PWM
Siemens SimovertD	CC 27	Line frequency	24	Commutation by load and line voltage
GL150 [19]	LCI 75	Line frequency	0–105	Commutation by load

When the multilevel converter is used in medium voltage drive (MVD), the piecewise synchronous modulations used in two-level locomotive traction drives are hard to implement because of their complexity. Theoretically, SHEPWM can be implemented in a multilevel converter for ultra-low switching frequency. However, its calculation is more complicated than that in two-level converters, because it requires more precisely calculated angles, which is computationally intensive. The author of [21] proposes the

overmodulation method for 3L-NPC in high-speed range to get through the low pulse range. Still, it needs about 1 kHz switching frequency, and the vector control is also hard to use in the deep over-modulation range and square wave area.

As for the limited dynamic performance due to SHEPWM and other optimized PWMs, the stator flux trajectory tracking method (SFTC) [22,23] can be used in 2L-VSCs to adjust the pre-calculated angles dynamically. However, no similar research has been found in multilevel converters (more than three levels), because they are much more complicated. Therefore, it is necessary to study in-depth how LSFM affects the regular operation of high power converters, especially multilevel converters. This paper focuses on VSC on dc/ac applications, so the analyses are based on SPWM, while other kinds of conversion, such as dc/dc converters, are not considered here.

The contributions of this paper are stated as follows: this author systematically investigated the influence of LSFM on different VSCs, and proposed solutions to alleviate the influence. The analyzed influences are classified into three mechanisms, comprehensively named as harmonic overlap effect (HOE). Mechanism one reveals that when $Cr \leq 5$, the left harmonic of the first harmonic cluster will be superimposed on the fundamentals or even the output dc component. Thus, it will affect the fundamental output and power balance of the two-level module or the corresponding paired switchers. Mechanism two happens when Cr goes to a relatively higher integer. It is revealed that changing the initial carrier angle will periodically change the THD and device stress in the bridge, which will further affect the output capability and cause different heat sink pressure. The corresponding solutions are proposed and verified in NPC and HNPCs [24].

For the clamped multilevel converter, such as NPCs, and five-level hybrid clamped converter (5L-HC) [25], in addition to the above two mechanisms, there is another mechanism because of the nonlinear operation of switching function in the dc clamped point model. It is found when Cr is close to an even number, the asymmetry in the first and second half-periods in each independent PWM unit is obvious. Then the nonlinear operation, such as getting absolute value, will generate an undesired harmonic. It will bring the divergence of the upper and lower capacitor voltages and increase the balance burden.

Because the specific performance of each mechanism on each topology is different, the impacts of three harmonic overlap mechanisms on different topologies are systematically summarized, and the corresponding solutions for typical topology are verified and summarized in a table. To the best of the author's knowledge, such kind of research on LSFM has never been done before. Besides, methods are given to design the modulation scheme for those converters in low switching frequency.

The rest of this paper is organized as follows. Preliminaries on the classic two-level SPWM are concluded in Section 2, and the harmonic overlap mechanism is classified into three parts and presented separately in Sections 3–5. The summary of the harmonic overlap phenomenon on different high power converters is drawn in Section 6. The whole paper is concluded in Section 7. Since the research aims at the basic knowledge of circuit operation under LSFM and various topologies are studied, due to the limited space, the language is concise and sometimes a second consideration may be needed to get full understanding.

2. Preliminaries on the Classic Two-Level SPWM

The traditional two-level SPWM process is presented here to provide fundamentals for further analyses. The double Fourier transformation of the output switching function can be expressed as [26]:

$$\begin{aligned} u_{\mathrm{ao}} &= u_{\mathrm{dc}}\left(\tfrac{1}{2} + \tfrac{M}{2}\cos(\omega_0 t) + \tfrac{4}{\pi}\sum_{m=1}^{\infty}\tfrac{1}{m}J_0\left(m\tfrac{\pi}{2}M\right)\sin m\tfrac{\pi}{2}\cos m(\omega_{\mathrm{c}}t+\theta_{\mathrm{c}})\right. \\ &\left. + \tfrac{4}{\pi}\sum_{m=1}\sum_{\mathrm{n}=-\infty}^{\infty}\tfrac{1}{m}J_0\left(m\tfrac{\pi}{2}M\right)\sin[(m+n)\tfrac{\pi}{2}]\cos[m(\omega_{\mathrm{c}}t+\theta_{\mathrm{c}})+n(\omega_0 t+\theta_0)]\right) \end{aligned} \quad (1)$$

where J_0 is the Bessel function, u_{ao} is the output voltage, u_{dc} is the dc voltage, M is the modulation index, ω_{c} is the carrier frequency, ω_0 is the fundamental frequency. θ_{c} and θ_0

are the initial angle of carrier and fundamental voltage. It can be assumed that θ_0 is zero. m and n are the order of carries and their nth nearby fundamental order. The corresponding frequency spectrum is shown in Figure 2.

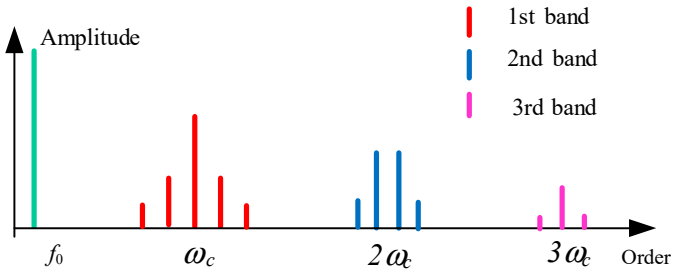


Figure 2. Frequency spectrum for classic two-level SPWM.

As inferred from (1), for the m-th harmonic cluster, the nearby harmonic order can be expressed as m $\times$ Cr $\pm$ n, where m $\pm$ n is odd, and Cr = ω_c/ω_0. For example, in the second harmonic cluster, the central sideband order is 2 $\times$ Cr $\pm$ 1. It can be inferred that when Cr is large, different harmonic clusters have no interaction with each other. When the switching frequency decreases and Cr decreases, the harmonics will move close with different speeds. Some characteristics can be concluded from (1) [27]:

1. When Cr is an odd number, it can ensure that the pulses are symmetrical around the zero crossing points in one period. The spectrum of the PWM output will be free of dc components and low order even harmonics.
2. When Cr is the multiples of three, the sideband of some harmonics in the symmetrical system will be in phase. Thus, the line voltage and current will be free of these harmonics, THD will be improved [28].
3. The decimal Cr will cause a subharmonic around the fundamental order [29], which is very harmful to the load. For example, in motor drive applications, it will cause severe low-frequency oscillation, which will cause great damage to the motor bearings.

The above principles can guide the modulation selection of a high-power two-level converter at low Cr. As for the multilevel converters using CPS-PWM, low-order harmonic clusters will encounter each other because of the carrier interleaving. However, the state of each SM (e.g., in CHB) and the paired switchers (e.g., in NPC) will still be affected by the lower-order harmonics, which will be explained in Sections 3–5. To sum up all these unexpected influences, they are concluded as harmonics overlap effect in this paper. It is rigorously defined as: in the high-power and low-switching frequency modulation inverters, the approach or superposition of harmonic clusters to the lower-frequency region will potentially exert a significant impact on the output or the operating state of circuit components. They can be classified into three different mechanisms, which will be presented separately in the following three sections.

3. Mechanism One—The Harmonic Overlap in DC and Fundamental Component When *Cr* $\leq$ 5

For a traditional two-level converter, when Cr = 3, the harmonic component will have the same frequency as the expected output voltage, as shown in Figure 3. It will affect the fundamental output and power balance of the two-level module or the corresponding paired switchers.

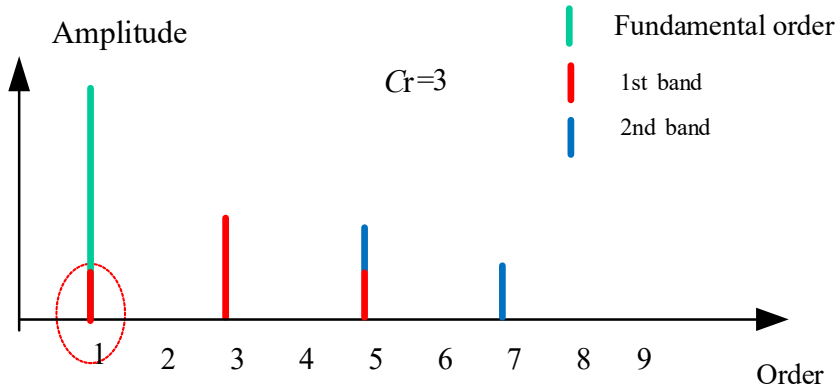


Figure 3. Frequency spectrum for two-level SPWM output when *C*r = 3.

The mathematics expression of the overlap component can be written as (2), where u_{a1} is the harmonic component with $m = 1$, $n = -2$. Thus, u_{a1} has the same angular frequency as the fundamental voltage. Such kind of the harmonic overlap in dc and fundamental component when $Cr \leq 5$ is called the mechanism one of the LSFM. Such mechanism occurs when $Cr \leq 5$. When *C*r is an integer, the left side harmonics of the first harmonic cluster will be superimposed on the fundamentals or even the dc output.

This conclusion can be applied to all converters using basic SPWM. Although the equivalent switching frequency of the multilevel output is relatively high, the frequency design of each carrier is still limited by this mechanism when using CPS-PWM.

$$\begin{cases} u_{a1} = -\frac{4}{\pi} J_0(\frac{\pi}{2}M)\cos[(\omega_c t + \theta_c) - 2(\omega_0 t + \theta_0) \\ \omega_c = 3\omega_0 \end{cases} \quad (2)$$

To verify this conclusion, simulations are conducted on a two-level VSC to compare the amplitude of the fundamental voltages at different *C*rs. The fundamental frequency is 50 Hz and the reference fundamental voltage is 1000 V. It is worth noting that the switching frequency should be no less than the Nyquist frequency (double of the fundamental frequency), so the lower carrier ratio is no longer simulated. It can be seen from Table 2 that for *C*r > 5, the output is almost the same with reference, but when it decreases to 3, the output amplitude diverges obviously.

Table 2. Output voltage in 2 L inverter when carrier ratio decreases (1000 V is the referenced output).

Cr	Output Fundamental Voltage Amplitude (V)	Error%
27	999.9	0
21	999.9	−0.01
15	999.6	−0.04
9	999.1	−0.09
7	998.5	−0.15
5	996.9	−0.31
3	1057	5.7

For the multilevel converter using two-level submodules, for example, in CHB and MMC, when *C*r = 3, the first left harmonic of the first harmonic cluster (50 Hz) will be superimposed on the fundamental. When *C*r = 4, it can be further inferred from (1) that the second harmonic on the left side will act as a dc component to the output, though the magnitude is tiny. For the high-capacity chain STATCOM using CHB, this mechanism will cause the unbalanced submodule capacitor voltages. For the CHB-MVD system, it will bring differences on the active power distribution of different power units, resulting in uneven heat dissipation.

An 8-module cascaded multilevel CHB model was built in Simulink by the SimPowerSystem toolbox to verify this conclusion, and the CPS-PWM modulation method was used. Under carriers of 150 Hz and 350 Hz, comparisons of the initial angle of fundamental voltage in each module are listed, which is shown in Table 3. The independent variable is the phase-shift-angle between the reference voltage and the carriers in different submodules. The data are obtained by extracting the FFT spectrum of the output voltage in each module. Since the submodule current is the same, the output power of each module will be different if their voltage angles are different. From the data in Table 3 it can be found that the voltage angles corresponding to the 350 Hz carrier is almost the same. However, the situation under 150 Hz is much worse. The angles vary from 10 to 49 degrees. Thus, the external power balancing control should be added in this case.

Table 3. The initial phase angles in different submodules voltage with different switching frequencies.

Different Submodule	**150 Hz**	**350 Hz**
Phase shift angle in different submodules (°)	Initial angle of the fundamental output voltage (°)	Initial angle of the fundamental output voltage (°)
0	47.9	29.8
45	39.5	29.7
90	29.9	29.8
135	20.2	29.9
180	13.0	29.8
225	10.5	29.8
270	29.9	30.1
315	49.1	29.9

As for the solution for this mechanism, for the two-level motor drive system, when the carrier ratio is low (Cr < 10) during the high-speed range, synchronous modulation can be selected to ensure a relatively stable output harmonic and ensure the smooth operation of the motor. Synchronous modulation is implemented by adjusting the PWM period according to the fundamental frequency, to keep the Cr constant in a certain period of time. When the carrier ratio is extremely low (Cr < 5), traditional SPWM should be avoided, and optimized PWM, such as SHEPWM, current harmonic minimum PWM (CHMPWM) [2] can be used.

However, for CHB, the implementation of optimized PWM is complicated. In order to avoid the power imbalance problem caused by overlap, Cr can be selected as a decimal. Because the equivalent switching frequency is high, low-order subharmonic will not be free on the ac side. It will cause a ting pulsation on the submodule capacitors because of the subharmonic. Since its amplitude is low, the resulting voltage fluctuation is negligible than the original dc side pulsating power.

4. Mechanism Two—The Overlap in Sideband Harmonics When $Cr \leq 9$

When Cr goes to a relatively higher integer, the cluster of harmonic moves to the righter side; some frequency in the spectrum containing two or more components coming from different harmonic clusters will appear. For example, when Cr = 5, there will have the same frequency at the 5th (5 + 0 = 9 − 4) and 7th (5 + 2 = 9 − 2) harmonics, as shown in Figure 4. It is worth noting that the central harmonic in the second cluster is 9th and 11th, not 10th. The mathematics expression of the overlap component can be written as (3), where u_{a51} corresponds to m = 1 and n = 0 of (1) when Cr = 5, and u_{a52} corresponds to m = 2, n = −4. As seen from (3), u_{a51} and u_{a52} have the same angular frequency but different initial angle. Thus, the amplitude of their sum is directly dependent on the initial angle

difference. Such kind of overlap in sideband harmonics when $Cr \leq 9$ is called mechanism two in this paper.

$$\begin{cases} u_{a51} = -\frac{4}{\pi} J_0(\frac{\pi}{2} M) \cos[(\omega_c t + \theta_c)] \\ u_{a52} = \frac{4}{\pi} J_0(\frac{2\pi}{2} M) \cos[(\omega_c t + \theta_c) - 4(\omega_0 t + \theta_0)] \\ \omega_c = 5\omega_0 \end{cases} \quad (3)$$

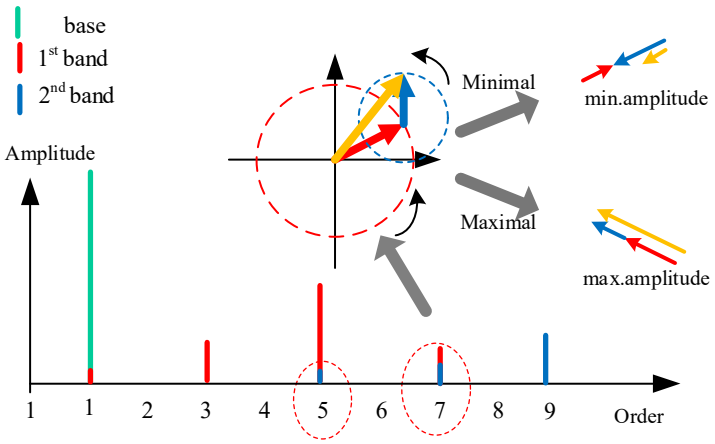
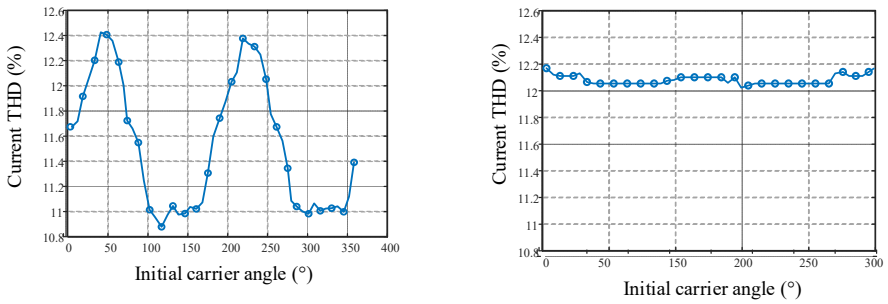


Figure 4. Frequency spectrum for two-level SPWM output when $Cr = 5$.

This phenomenon is not obvious when $Cr > 9$ because different harmonic clusters lie too far, and the overlapped component amplitudes are not at the same level. The most troublesome point is that the vector sum of these components depends on the initial angle between the carrier and the reference voltage. The largest summed amplitude is the direct addition of amplitude, and the smallest is their subtraction.

It can be further concluded that when the initial carrier angle changes from 0–2π, the amplitude will vary periodically. There will be multiple superimposed harmonic frequency points (such as the 5th, 7th) of similar phenomena. Therefore, the THD and RMS value of the output voltage and current will change periodically with the initial angle. Whereas the RMS value of the current affects the heat generation of the device, so the output capability of the device will also change periodically.

A 2MW NPC converter was built in Simulink by the SimPowerSystem toolbox to verify the above conclusion. The THD of output current in one phase with changing initial angles is drawn in Figure 5. It can be seen that the THD changed in a range of 6%, the varying period of THD is about π, which is half of the period because the equivalent switching frequency doubled in the line current.



(**a**) (**b**)

Figure 5. Output current THD with changing initial carrier angels. (**a**) $Cr = 7$ (**b**) $Cr = 7.3$.

For industrial application, such a mechanism can be utilized or eliminated. The method of utilization is: for a single NPC bridge, the best angle can be found to achieve the

maximum power output. However, for the HNPC bridges, it is not easy to find the angle that enables both bridges to the maximum output power. Therefore, this effect needs to be eliminated. As for the elimination method, the misposition of the sideband harmonics of different carrier clusters can be achieved by changing the carrier ratio to a decimal. It is very easy and can be implemented on a micro control unit based on pre-calculted PWM frequency. Thus, the output THD will be constant, and the RMS value of the output current and the thermal stress of the device can also be free of the influence. Simulation of *C*r = 7.3 is conducted on the same NPC converter. As can be seen from Figure 5b, the current THD stays almost unchanged under different initial angles. Similar results are obtained in HNPC simulation.

Not only NPCs, but all the other converters containing SPWM parts, including 2L-SPWM and CPSPWM, will be somehow influenced by this mechanism. It will have a great impact on the 2 L inverter. However, the impact on the other topologies using CPSPWM, such as MMC and CHB, are almost negligible. Since the overlapped component is tiny compared to the submodule output voltage, even though there will be different tiny harmonic power in devices, the influence on the heat dissipation pressure is negligible.

5. Mechanism Three—The Undesired Harmonic Order When *C*r Nears an Even Integer

The overlapped harmonic in the above two mechanisms comes from the direct superimposition of the harmonics in the frequency spectrum. In addition, there is another emerging undesired harmonics because of the LSFM, which is usually founded in the circuit containing nonlinear operation of the switching function. This phenomenon has little relation with which kind of multilevel modulation is adopted. It appears even for the most commonly used CPSPWM. This section will focus on a newly popular five-level converter 5L-HC to deeply illustrate this mechanism, on which CPSPWM is adopted.

5.1. Operating Principle of the 5L-HC

Phase x (x = a, b, c) circuit of the 5L-HC is shown in Figure 6. N1 and N2 are the clamping points on the dc side. These two points are connected to the other two phases, which are not shown here. Each phase contains 10 switches. In normal operation, S_{x1} and S_{x5} have the same gating signals. Gating signals of S_{x1}' and S_{x5}' are complementary to S_{x1} and S_{x5}, respectively. This ensures $u_{\mathrm{AB}} = 3E$. Gating signals of S_{x1} to S_{x4} are independent, corresponding to different carriers in CPS-PWM. The current of S_{x4} can be expressed as:

$$i_{sx4} = S_{gx4} \cdot i_{ox} \tag{4}$$

i_{ox} is the output current, and S_{gx4} is the switching function of S_{x4}. It means that when S_{x4} is turned on, its current is the output current. $i_{\mathrm{n1}x}$, $i_{\mathrm{n2}x}$ are the extracted currents from clamping points N1 and N2. The current of S_{x1}' ($i_{\mathrm{n1}x}$) can be expressed as:

$$i_{n1x} = (1 - S_{gx1}) \cdot S_{gx2} \cdot i_{ox} \tag{5}$$

N1, N2 can be regarded as one node in the dc-link. Thus, the balance of u_{d1} and u_{d3} is determined by the sum of the extracted currents from the two midpoints, as shown in (6), where $d_{\mathrm{n}x}$ is the extraction factor, which means the duty cycle of $|S_{gx2} - S_{gx1}|$.

$$\begin{aligned} i_{\mathrm{d2}x} &= i_{n1x} + i_{n2x} = ((1 - S_{gx1}) \cdot S_{gx2} + (1 - S_{gx2}) \cdot S_{gx1}) \cdot i_{ox} \\ &= \left|S_{gx2} - S_{gx1}\right| \cdot i_{ox} \\ &= d_{\mathrm{n}x} \cdot i_{ox} \end{aligned} \tag{6}$$

$$i_{d2} = \sum_{x=\mathrm{a,b,c}} i_{d2x} \tag{7}$$

As seen from (4), the balance of the upper and lower capacitor is directly related to $|S_{gx2} - S_{gx1}|$. Since there is no fundamental component in $|S_{gx2} - S_{gx1}|$ under a high carrier ratio, the average value of i_{d2x} is zero.

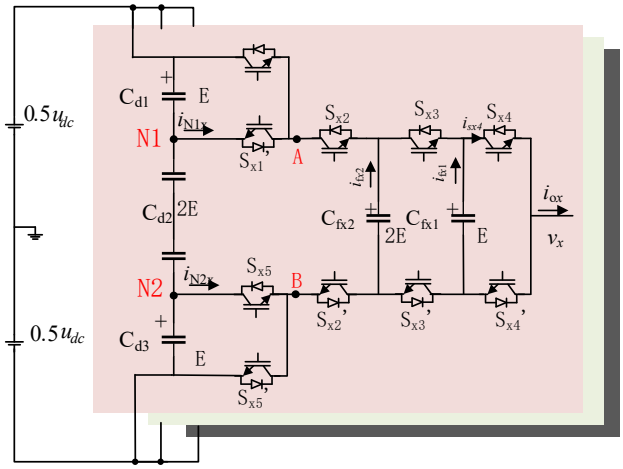
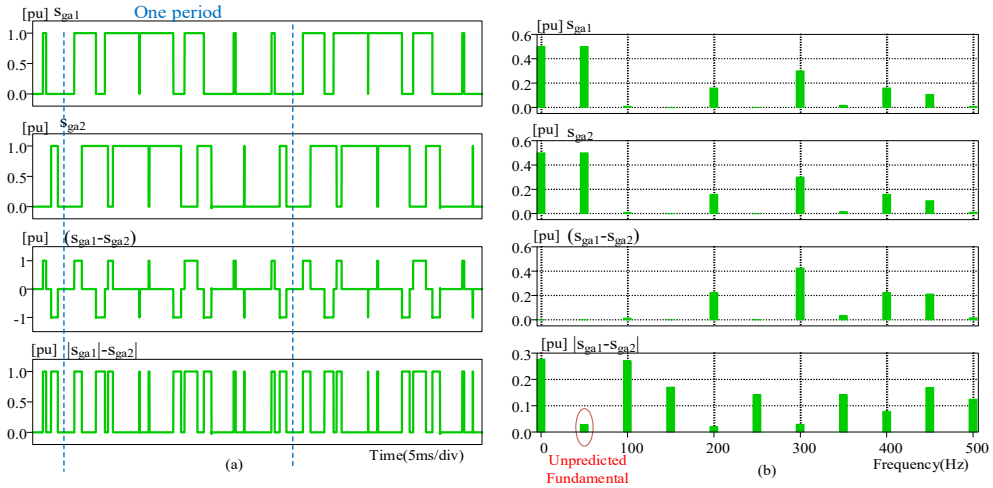


Figure 6. The circuit of the 5L-HC (showing only one phase) [25].

A simulation is conducted to investigate the influence caused by the absolute operation in (4). The waveforms of s_{ga1}, s_{ga2}, (s_{ga1}–s_{ga2}), and $|s_{ga1}$–$s_{ga2}|$ under Cr = 6 are shown in Figure 7, and the Fourier transformation is conducted to show their spectrum.



(**a**) Pluses and their operations. (**b**) Spectrum of the variable.

Figure 7. Pluses and their spectrum when *Cr* = 6.

As seen from Figure 7, the pulses in the former and latter half-cycles in one period are not completely symmetrical. Because the corresponding carriers have a 90-degrees delay, the S_{gx1} and S_{gx2} are different. The smaller the carrier ratio is, the larger inconsistency there will be. Therefore, after the subtraction, the pulse sequence is different between the two halves, but the difference between the positive and the negative pulse in the former (latter) half cycle is not that much. Therefore, the fundamental component is not obvious, as seen from Fourier analysis in Figure 7. The process of taking absolute value will flip the negative pulse, which increases the pulse inconsistency between the two halves, so the unpredicted fundamental component appears in $|s_{ga1}$–$s_{ga2}|$. If the carrier ratio changes to a smaller even integer, there will be a larger fundamental component in $|s_{ga1}$–$s_{ga2}|$.Thus, there will be an obvious dc component in i_{d2x} to deviate u_{d1} and u_{d3}. In [25], the balancing of dc capacitors is a tough problem.

5.2. Solution for Mechanism Three

For converters in fixed frequency applications, the carrier ratio can be chosen as an odd number to avoid this mechanism. For the motor drive system, when the carrier is changed with speed, synchronous modulation can be used to avoid the sensitive carrier ratios. However, under the requirement of not exceeding the maximum switching frequency, it is necessary to adopt a synchronous modulation similar to the high-speed area in 2 L inverters, which will also bring about the harmonic mutation problem in the switching process.

It is also valid to use closed-loop feedback if not changing the modulation CPS-PWM to compensate for the defects of the harmonic overlap process. The zero-sequence injection method used to eliminate the 3rd order ripple in dc capacitors [25] can be used here because it is also aimed at unbalancing the upper and lower dc capacitor voltages.

5.3. Simulation of Mechanism Three and the Solution

The simulation results on a 3MW 5L-HC are shown in Figure 8 to verify mechanism three and the solutions; the simulation parameters are listed in Table 4 When discontinuously changing the output frequency, the carrier ratio changes. Ia is the output current in phase a, u_{d1-3} are the dc capacitor voltages. As seen in Figure 8, when *Cr* is 6, 5.5, 4.5, and 4, the dc component in i_{np} changes the balance of dc capacitors. Since the polarity of the dc components changed, alternate divergence and convergence appeared in u_{d1} and u_{d3}.

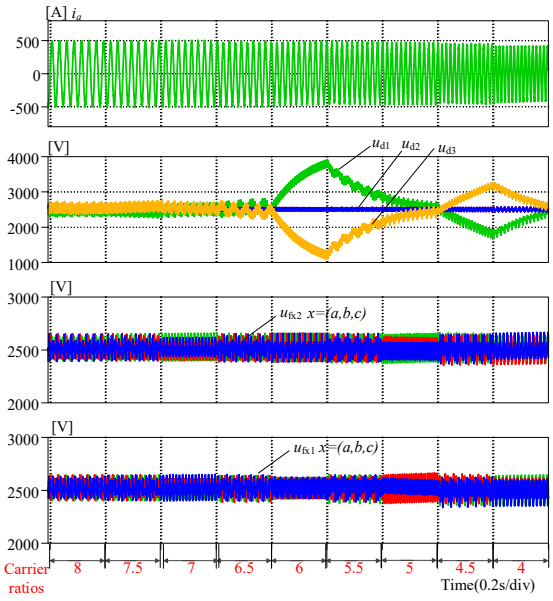


Figure 8. The circuit states of 5L-HC under different *Cr*.

Table 4. The simulation parameters for 5L-HC.

Items	Simulation Parameters
Apparent power	3 MVA
Dc bus voltages	10,000 V
Capacitors in the dc-link	C_{d1}/C_{d3} = 600 μF C_{d2} = 300 μF
Flying capacitors	C_{fx1} = 600 μF, C_{fx2} = 300 μF
Switching frequency	500 Hz
R–L Load	20 Ω/10 mH

Figure 9 shows the performance of using zero-sequence injection to close-loop balance the capacitor voltage when *Cr* = 6. It can be seen that when closed-loop control is not used before time 0.25 s, the capacitor voltages obviously diverge. It is worth noting that the

divergence of the capacitor will not be infinitely amplified. Divergence to a certain extent will deteriorate the waveform of output voltage and current, and then it will adjust i_{np} to 0 through the circuit feedback mechanism. The implement of balancing control (zero sequence injection method) in 0.25–0.45 s will maintain the mean value of u_{d1} and u_{d3} to the same.

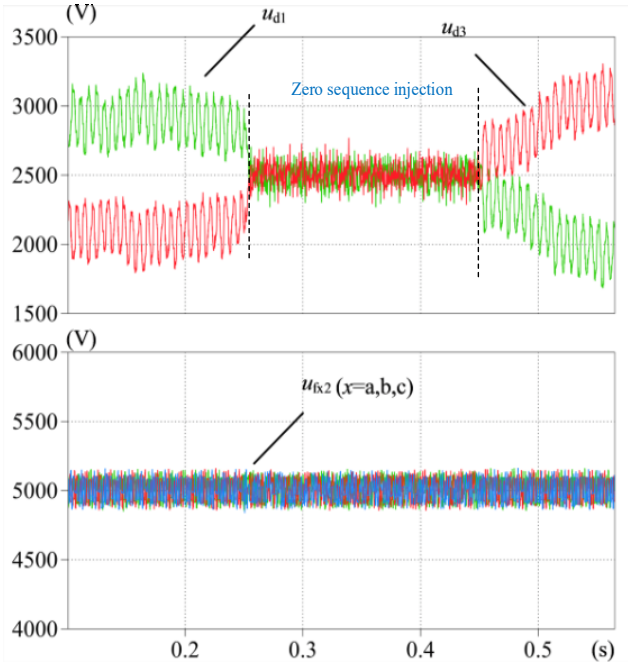


Figure 9. Performance of the feedback control to balance dc capacitor voltages caused by mechanism 3 when *Cr* = 6.

6. Summary of Harmonic Overlap Phenomenon on Different High Power Converters

After analyzing the above three harmonic overlap mechanisms, they can be summarized into the following characteristics:

1. The same mechanism on different topologies will exert different influences, so the solutions are different, which should be analyzed individually.
2. There will be one or more mechanisms in one converter.
3. The mechanisms do not conflict with the existing two-level and multi-level modulation theory. The traditional theory remains valid. For example, the carrier ratio should be odd (avoid even numbers), and better to be odd multiples of three in the three-phase system.

To sum up, the impacts of harmonic overlap on different topologies under typical modulations are summarized in Table 5. Due to limited space, this paper does not further discuss other new topologies. They can be synthesized according to the specific circuit model and modulation scheme, following the ideas in Sections 3–5.

Table 5. Influences and solutions of the three harmonic overlap mechanisms in typical topologies.

Mechanism / Topology / Influence	Modulation	Mechanism 1	Mechanism 2	Mechanism 3	Solutions
Brief description:		Dc and fundamental have changed, and the subharmonics affect the motor heating	Periodic changes of THD and thermal stress of devices caused by the overlap	Nonlinear operation produces unexpected harmonics	
Corresponding *Cr*		$Cr \leq 5$	$Cr < 10$ and *Cr* is an integer	$Cr \leq 9$	
2L -VSC	SPWM	Y	Y	N	1. Synchronous PWM; 2. Optimize PWM
3L-NPC	PDPWM	Y	Y	Y	Change *Cr* to decimals
CHB	CPS	Y	N	N	1. Change *Cr* to decimals 2. Optimized PWM
5L-FC	CPS	+	N	N	
MMC	CPS	Y	+	N	Change *Cr* to decimals
5L-HC	CPS	+	N	Y	Closed-loop feedback control combined with 3th ripple suppression
NNPC	PDPWM	Y	Y	Y	Closed-loop feedback combined with ripple suppression strategy
5L-ANPC	Improved CPS [30]	+	N	Y	Closed loop feedback control

N: No influence +: limited influence. Y: Strong influence.

Considering that modulations such as alternative phase opposition disposition PWM (APODPWM) and phase opposition disposition PWM (PODPWM) are similar to PDPWM in the harmonic characteristics, and they are rarely used in high-power industrial products, this paper does not pay much attention to them. The effect of LSFM can also be concluded by analyzing the frequency spectrum of the switching function.

7. Concluding Remarks and Future Works

This paper deeply investigates several unpredicted phenomena in high power VSC under low switching frequency modulation. They are classified into three mechanisms and summarized as the harmonic overlap effect. Mechanism one occurs when $Cr \leq 5$ and *Cr* is an integer. The left side of the first harmonic cluster will be superimposed on the fundamental component or even the dc output, which will affect the fundamental output and power balance of the two-level module or the corresponding paired switchers. Mechanism two will result in a periodically varying output current THD and current stress in the arm because of the overlap in some sideband harmonics. It happens when *Cr* goes to a relatively higher integer. Solutions for mechanism one and two are proposed by changing the carrier ratio and optimizing the PWM approach. Mechanism three is usually found in the circuits which have a nonlinear operation of the switching function. It will generate an undesired or unbalanced component in the circuit state. Feedback control to balance the dc capacitors is introduced here to handle this mechanism. A summary of these HOE on different topologies is drawn for comprehensive analyses. The overall research provides guidance for modulation design in different high power topologies. In the future, the author plans to investigate the mechanics on more high-power multilevel topologies and tries to promote a universal solution for them.

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