

## Article

# Seven-Level Inverter with Reduced Switches for PV System Supporting Home-Grid and EV Charger

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**Abstract:** This paper proposes a simple single-phase new pulse-width modulated seven-level inverter architecture for photovoltaic (PV) systems supporting home-grid with electric vehicle (EV) charging port. The proposed inverter includes a reduced number of power components and passive elements size, while showing less output-voltage total harmonic distortion (THD), and unity power factor operation. In addition, the proposed inverter requires simple control and switching strategies compared to recently published topologies. A comparative study was performed to compare the proposed inverter structure with the recent inverter topologies based on the number of components in the inverter circuit, number of components per output-voltage level, average number of active switches, THD, and operating efficiency as effective parameters for inverter performance evaluation. For design and validation purposes, numerical and analytical models for a grid-tied solar PV system driven by the proposed seven-level inverter were developed in MATLAB/Simulink environment. The inverter performance was evaluated considering grid-integration and stand-alone home with level-2 AC EV charger (3–6 kW). Compared with recently published topologies, the proposed inverter utilizes a reduced number of power components (7 switches) for seven-level terminal voltage synthesis. An experimental prototype for proposed inverter with the associated controller was built and tested for a stand-alone and grid-integrated system. Due to the lower number of ON-switches, the inverter operating efficiency was enhanced to 92.86% with load current THD of 3.43% that follows the IEEE standards for DER applications.

**Keywords:** DC-AC converter; electric vehicles; home grid; maximum power point tracking (MPPT); multilevel inverter; photovoltaic (PV) system; seven-level inverter



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## 1. Introduction

Recently, the world witnessed several storms and crises that disturbed most of the energy sources around the world, which forced them to switch to standstill energy sources allowing only emergency supplies. Therefore, many industries were been brought to a standstill during supply interruption and fuel lack. For such scenarios, renewable energy, especially the solar photovoltaic (PV) energy, stand out for making up the energy balance. Additionally, negative environmental impacts, along with the unsustainable nature associated with conventional energy resources, i.e., fossil fuels, provoke the development of new and clean energy resources to satisfy the increased global energy demand [1,2]. Among the different renewable energy resources, solar PV and wind energy are the most popular resources [3–5] which have been exploited by different companies and countries. Moreover, the renewable energy trend relies on electrical energy production from commercial and residential buildings using PV systems that help to enhance the power system resilience. Given the flexibility associated with PV systems, they are an ideal source of electricity for remote areas, which are located far away from local utility-grids [2,6]. Hence, energy can be produced by installing PV panels on household rooftops for direct consumption,

where the excess energy can be stored or sold to the grid if the system is grid-connected. In addition, PV systems can be used to support new emerging loads, e.g., electric vehicle (EV) charging [7]. Considering energy generation, storage, and self-consumption, EVs production arises as a crucial part of smart offices and residential buildings [8,9]. In addition to reducing CO<sub>2</sub> emissions and costs, EVs have the potential to significantly enhance self-supplying and consumption [10,11].

A critical component to integrate renewable energy sources with other systems is the power electronics interface converter, which is witnessing rapid development in conjunction with the widespread use of these new technologies. Due to the intermittent DC-power of the PV systems, power converters are vital to regulate the system output and facilitate their integration with the grid and other loads, e.g., AC charging ports for EV [12,13]. The multilevel inverters (MLIs) evaluation has been initiated in [14], based-on the neutral-point clamped structure (NPC) for medium/high power applications. MLI architectures offer many features compared to conventional topologies such as low voltage-stress on the switches, low voltage-ratings, reduced THD, reduced electromagnetic interference (EMI), voltage boosting capability in single-stage operation, and enhanced power-quality of the grid-integrated system with reduced filter passive elements [13,15]. The conventional topologies of MLIs are divided into three categories: cascaded H-bridge (CHB-MLI) [16,17], NPC-MLI [18,19], and flying capacitor (FC-MLI) [20,21]. Despite the large number of output-voltage levels that are synthesized from these topologies, many power switches are needed, which surges the converter's power loss and complicates the control circuit design and implementation in addition to negatively impacting the inverter reliability.

To mitigate the former drawbacks, modified MLI architectures are introduced based-on a reduced number of components [22–32]. In [22], a seven-level pulse-width-modulation (PWM) inverter is presented considering external DC input sources and suitable circuit combination for switches and THD reduction. However, it required a comparatively increased number of switches and external DC-sources, which increased the inverter footprint and cost. In [23], a staircase MLI is presented to decrease the number of power components and the inverter losses. However, this topology considers an even larger number of switches. In [24], the number of external DC-sources is reduced without voltage division over input split-capacitors. However, this topology can be used for up to five-level synthesis without modular extension capability. For further reduction of switches, MLI with reduced switches is presented in [25], but it requires a large number of separated DC-sources for output voltage synthesis. In [26], a new inverter structure basic cell is presented considering a reduced number of switches to a competitive level. However, this architecture still requires a large number of separate DC-sources, and it is only applicable for high output-voltage levels that complicate the control scheme and switching pattern. In [27], a new single-phase MLI inverter was introduced with a voltage-boosting capability for low voltage PV systems. However, it is applicable for low power applications and it incorporates two conversion stages, which increases the power losses. In [28], a compact MLI is presented considering a reduced number of external DC-sources using two-capacitors in each module for staircase multilevel output-voltage. However, this increases the inverter power density and footprint for high power applications. New MLI topologies for single/three-phase applications considering a reduced number of components and a single DC-source are recommended for renewable energy applications [29,30]. Different MLI topologies are developed to reduce the inverter power loss, voltage-stress, and overall footprint using different switching and commutation techniques [33,34]. In addition, several MLI structures are proposed to improve the stand-alone and grid-integrated renewable energy and EV applications at improved operating efficiency.

Motivated by the literature survey, this paper proposes a new single-phase 7-level PWM inverter, considering a reduced power component count, for stand-alone and grid-integrated PV systems. The proposed inverter reduces the required number of components to a competitive level for efficiency, footprint, and cost improvements. The proposed MLI is divided into two circuits: the main and auxiliary. The main circuit is a simple H-bridge

inverter circuit, which is responsible for output-voltage polarity control, and the auxiliary circuit is a combination of switches to synthesize each output-voltage level. In addition, a boost converter (BC) is internally integrated with the PV-array for maximum power point tracking (MPPT) at the front-end of the 7-level inverter, as indicated in Figure 17. A simple sinusoidal level shifted PWM switching technique is used for gating the power switches of the proposed inverter for a less complex control technique. The output-voltage levels that can be synthesized are:  $+V_{dc}$ ,  $+2V_{dc}/3$ ,  $+V_{dc}/3$ ,  $0$ ,  $-V_{dc}/3$ ,  $-2V_{dc}/3$ , and  $-V_{dc}$ .

The rest of the paper is organized as follows. Section 2.1 deliberately illustrates the proposed inverter circuit configuration, and the switching pattern, control algorithm, and switching logical combinations are demonstrated in Section 2.2. In addition, a comparative study of the proposed 7-level inverter with the recent inverter topologies is interpreted and discussed in Section 3 to show the features of the proposed inverter for industrial applications. The proposed system control scheme is discussed in Section 4. The proposed 7-level inverter simulation and experimental validations for grid-integrated PV system supporting L2 AC EV charging are analyzed in Section 5. Finally, Section 6 concludes the paper findings.

The circuit diagram of the proposed 7-level inverter is depicted in Figure 2. The inverter circuit is divided into two portions: the main and auxiliary circuit. The main involves an H-Bridge inverter that incorporates four power switches ( $S_1$ ,  $S_2$ ,  $S_3$ , and  $S_4$ ) and is responsible for generating the positive and negative half cycles. On the other side, the auxiliary circuit of the 7-level inverter consists of three power switches ( $Q_f$ ,  $Q_1$ , and  $Q_2$ ), two batteries ( $V_{dc1}$  and  $V_{dc2}$ ), and a single power diode ( $D_A$ ), as illustrated in Figure 2. The main purpose of the auxiliary circuit is to synthesize the different output-voltage levels and deliver these voltage levels to the front-end of the H-bridge inverter. Hence, the switching device of the auxiliary circuit is operating at the switching-frequency similar to the other stage.

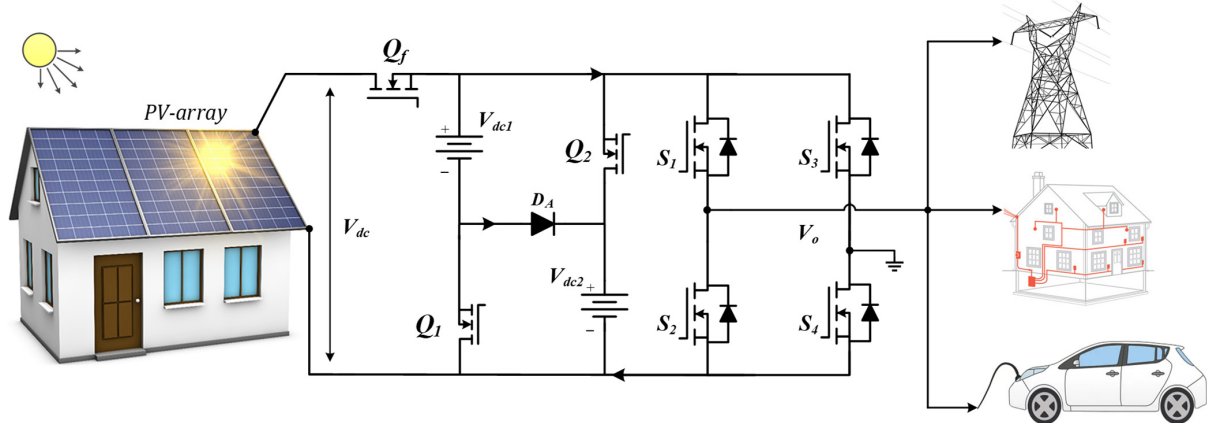


**Figure 1.** Circuit configuration of solar PV system integrated with the grid and EV loads via the proposed 7-level inverter.

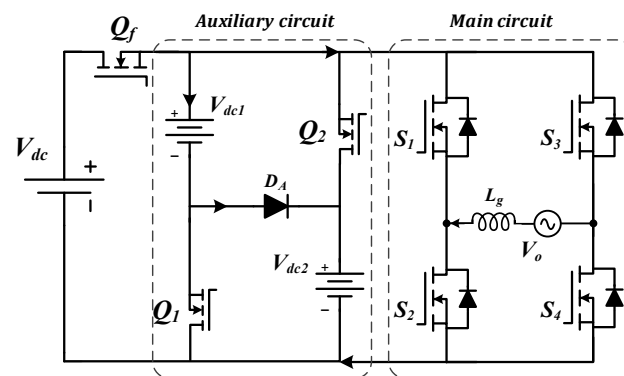


**Figure 2.** Power circuit of the proposed 7-Level inverter.

## 2. Proposed Multilevel PWM Inverter

### 2.1. Circuit Configuration and Operation Principal

The front-end of the inverter auxiliary circuit is connected to the main DC source, which is the output DC voltage from BC in a PV system that will be clearly illustrated later in this paper. The MLI operation is simply demonstrated as appeared in Figures 3 and 4. Switching-ON  $Q_f$  results in having the total DC-voltage  $V_{dc}$  ( $V_{dc} = V_{dc1} + V_{dc2}$ ) applied to the front-end of H-bridge circuit and the two batteries charge in series at the same time through diode forward biasing ( $D_A$ ) where:

$$V_{dc1} = \frac{1}{2}V_{dc2} = \frac{1}{3}V_{dc} \quad (1)$$

On the other side, switching-OFF the series switch ( $Q_f$ ) isolates the input DC-source from the H-bridge front-end allowing the charged series batteries to discharge during an adequate duration determined by the control strategy to supply the utility grid. The circuit operation can be divided into seven modes illustrated in Figures 3 and 4 and described as follows:

Mode 1, the series switch ( $Q_f$ ) is ON to connect the DC-source  $V_{dc}$  to the front-end of H-bridge circuit. By switching-ON of the two switches  $S_1$  and  $S_4$ , the inverter output voltage becomes  $+V_{dc}$ . At the same time, the two batteries ( $V_{dc1}$  and  $V_{dc2}$ ) charge through the diode ( $D_A$ ), as described in Figure 3a. Then, the reverse current path is illustrated in Figure 3b.

Mode 2, switching-OFF  $Q_f$  isolates the DC supply. At the same time, the switch ( $Q_2$ ) is turned on to apply a voltage of  $2V_{dc}/3$  to the H-bridge circuit and the second battery is disconnected from the circuit and diode  $D_A$  is reversed. Turning-ON switches  $S_1$  and  $S_4$  of the main inverter results in generating output-voltage of positive  $+2V_{dc}/3$ , as clarified in Figure 3c. The reverse current path is depicted in Figure 3d.

Mode 3, the series switch ( $Q_f$ ) as well as ( $Q_2$ ) are OFF-stated. Switch ( $Q_1$ ) is turned-ON to apply a DC-voltage of  $V_{dc}/3$  to the H-bridge circuit. Similarly, turning-ON switches  $S_1$  and  $S_4$  of main circuit synthesizes output-voltage of  $+V_{dc}/3$ , as depicted in Figure 3e. The reverse current path is shown in Figure 3f.

Mode 4, the zero output-voltage can be generated by voltage cancellation through the main H-bridge inverter. Voltage cancellation occurs by switching-ON ( $S_1$  and  $S_3$ ) or ( $S_2$  and  $S_4$ ) as shown in Figure 3g,h.

Mode 5, the series switch ( $Q_f$ ) as well as ( $Q_2$ ) are OFF-stated same as to mode (3). The switch ( $Q_1$ ) is turned-ON to deliver DC voltage of  $V_{dc}/3$  to H-Bridge input side. Turning-ON switches  $S_2$  and  $S_3$  of the main inverter generates an output-voltage of  $-V_{dc}/3$ , as shown in Figure 3i, where the reverse current path is depicted in Figure 3j.

Mode 6, turning-OFF the series switch ( $Q_f$ ) and switching-ON ( $Q_2$ ) delivers a voltage of  $2V_{dc}/3$  to the H-bridge inverter similar to Figure 3c. At the same time, switching-ON switches ( $S_2$  and  $S_3$ ) of the main inverter synthesizes a negative output-voltage of ( $-2V_{dc}/3$ ), as clarified in Figure 3k. The reverse current path is portrayed in Figure 3l.

Mode 7, turning-ON the series switch ( $Q_f$ ) applies the total DC-voltage  $V_{dc}$  to front-end of H-Bridge inverter. By turning-ON the two switches  $S_2$  and  $S_3$ , MLI output-voltage becomes  $-V_{dc}$ . At the same time, the two batteries ( $V_{dc1}$  and  $V_{dc2}$ ) are charging in series through diode ( $D_A$ ) similar to mode (1), as shown in Figure 3m. Besides, the current path of the reverse direction is shown in Figure 3n.

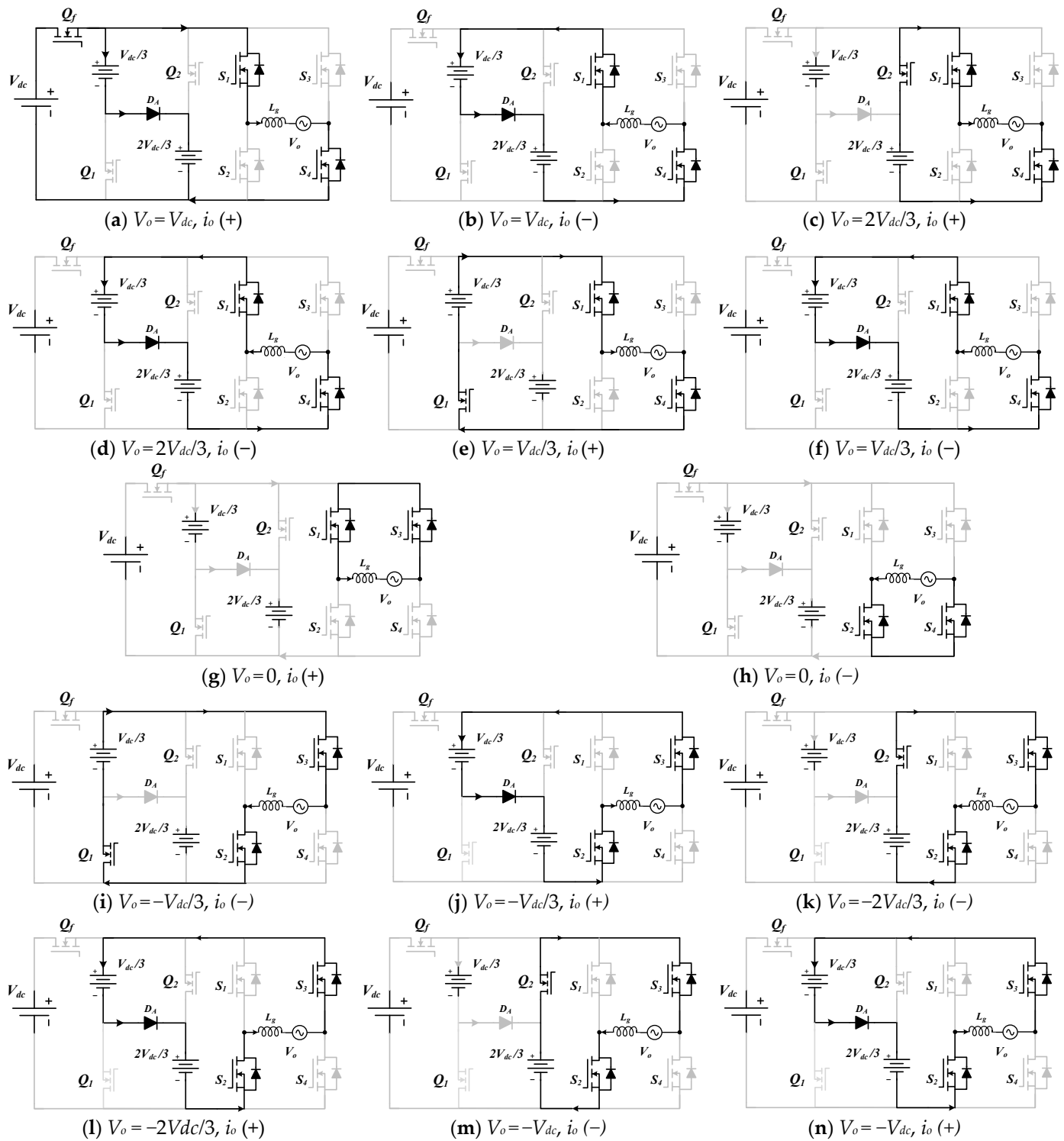


**Figure 3.** Operational modes of the 7-level inverter to synthesize the multilevel output-voltage.

The logical combination of switching patterns of the auxiliary circuit and H-bridge inverter switches simplifies the switching pattern of the proposed inverter. Using a suitable control strategy, 7-levels output-voltage of  $+V_{dc}$ ,  $+2V_{dc}/3$ ,  $+V_{dc}/3$ ,  $0$ ,  $-V_{dc}/3$ ,  $-2V_{dc}/3$ , and  $-V_{dc}$  can be synthesized from the proposed inverter that enhances the power quality of the grid-integrated operation.

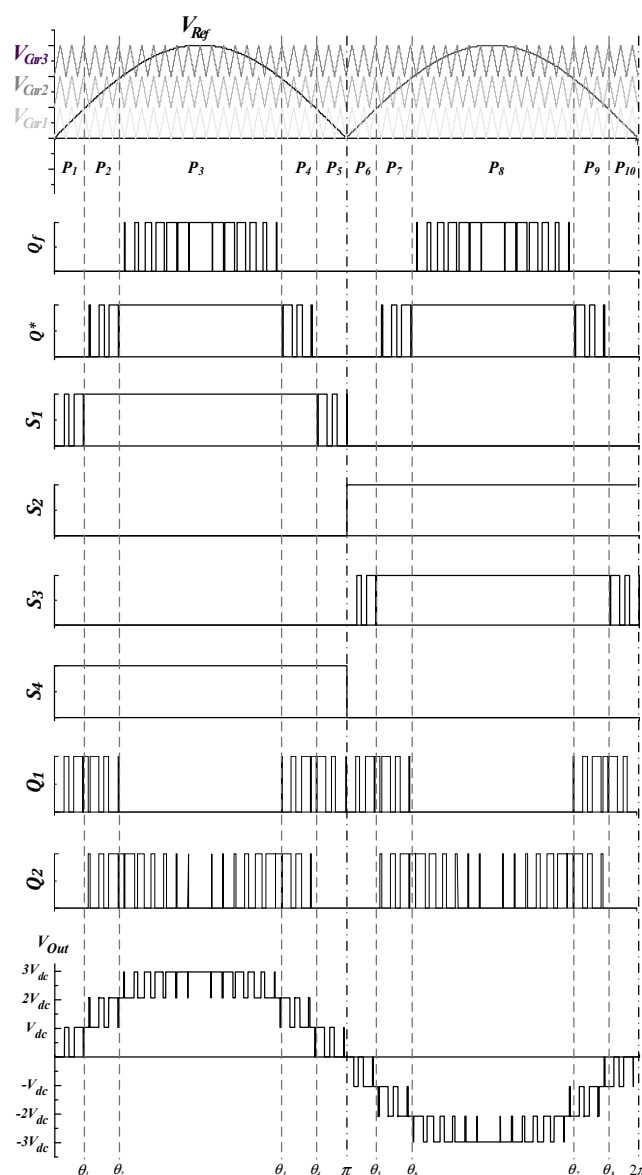


**Figure 4.** Switching strategy of the 7-Level PWM inverter.

## 2.2. The Switching Patterns and Control Strategy

The pulse-width modulated switching scheme of the 7-level inverter is depicted in Figure 4. The switching pattern of the proposed inverter uses a rectified sinusoidal waveform reference signal and three high-frequency carrier-signals. The reference signal has the same power-frequency as the required output voltage. The carrier waveforms have the same frequency and amplitude with different offset (level-shifted PWM) to generate the appropriate switching pattern of the power switches. By comparing the reference signal with level-shifted carrier waveforms, the gating signals of each inverter switch can be generated, as shown in Figure 4; when  $V_{Car1}$ ,  $V_{Car2}$ , and  $V_{Car3}$  are lower than  $V_{Ref}$ , the switching functions of all switches are OFF. During the positive half-cycle and when  $V_{Ref}$  is higher than  $V_{Car1}$  and lower than  $V_{Car2}$  as well as  $V_{Car3}$ , it represents operational mode (3), as shown in Figure 3e. Similarly, during the negative half-cycle and when  $V_{Ref}$  is higher than  $V_{Car1}$  and lower than both  $V_{Car2}$  and  $V_{Car3}$ , it describes operational mode (7), as indicated in Figure 3i. When  $V_{Ref} > V_{Car1}$  and  $V_{Car2}$  and lower than  $V_{Car3}$ , it represents the operational mode (2), as depicted in Figure 3c. Along the same vein, when  $V_{Ref} > V_{Car1}$  and  $V_{Car2}$  and lower than  $V_{Car3}$ , that describes mode (6), as shown in Figure 3k. Finally, when  $V_{Ref}$  is higher than  $V_{Car3}$ , the switch  $Q_f$  is turned-ON to deliver the total input DC-voltage

to the H-bridge circuit to synthesize the third output-voltage level, as described in modes (1) depending on the H-bridge inverter switching, as portrayed in Figure 3a,b, respectively.

Considering one output-voltage/reference signal cycle, the switching functions are divided into six modes of operation related to the output-voltage levels, where the full switching states based on the comparison between the reference and carrier waveforms are listed in Table 1, and the corresponding operating periods are determined by:

$$\text{Mode 1: } P_1 \rightarrow 0 < \omega t < \theta_1 \text{ and } P_5 = \theta_4 < \omega t < \pi \quad (2)$$

$$\text{Mode 2: } P_2 \rightarrow \theta_1 < \omega t < \theta_2 \text{ and } P_4 = \theta_3 < \omega t < \theta_4 \quad (3)$$

$$\text{Mode 3: } P_3 \rightarrow \theta_2 < \omega t < \theta_3 \quad (4)$$

$$\text{Mode 4: } P_6 \rightarrow \pi < \omega t < \theta_5 \text{ and } P_{10} = \theta_8 < \omega t < 2\pi \quad (5)$$

$$\text{Mode 5: } P_7 \rightarrow \theta_5 < \omega t < \theta_6 \text{ and } P_9 = \theta_7 < \omega t < \theta_8 \quad (6)$$

$$\text{Mode 6: } P_8 \rightarrow \theta_6 < \omega t < \theta_7 \quad (7)$$

By logical combinations of the different switching functions ( $Q_f, Q_1, \dots$  etc.) and the operational modes ( $P_1, P_2, \dots, P_n$ ), the switched gating pulses can be generated for each switch ( $S_n$ ). Also, application of gate pulses to the switches during each fractional period depends on the switching angle ( $\theta_n$ ) and the modulation index/ratio ( $M_a$ );

$$M_a = \frac{A_m}{3A_c} \quad (8)$$

where;  $A_m$  is the reference-signal amplitude, and  $A_c$  is the amplitude of carrier waveforms. The synthesized output-voltage can be formulated as follows:

$$v_{out} = M_a \sin(\omega t) \quad (9)$$

Consequently, the switching functions of the auxiliary circuit switches can be simply generated based-on the aforementioned key switching waveforms using the appropriate combinations of logic-gates (AND, OR, and NOT) as follows:

$$Q_1 = (S_1 + S_3) \times Q^* \times \overline{S_1} \quad (10)$$

$$Q_2 = S_1 \times Q^* \quad (11)$$

**Table 1.** Output voltage levels according to switching states.

| Comparison                                                           | Auxiliary Circuit Switching |       |       | $Q^*$ | Main Circuit Switching |       |       |       | Output-Voltage       |
|----------------------------------------------------------------------|-----------------------------|-------|-------|-------|------------------------|-------|-------|-------|----------------------|
|                                                                      | $Q_f$                       | $Q_1$ | $Q_2$ |       | $S_1$                  | $S_2$ | $S_3$ | $S_4$ |                      |
| $V_{Car1} < V_{Ref}$<br>$V_{Car2} < V_{Ref}$<br>$V_{Car3} < V_{Ref}$ | 1                           | 0     | 0     | 1     | 1                      |       |       | 1     | $V_{dc}$             |
| $V_{Car1} < V_{Ref}$<br>$V_{Car2} < V_{Ref}$<br>$V_{Car3} > V_{Ref}$ | 0                           | 0     | 1     | 1     | 1                      |       |       | 1     | $\frac{2}{3} V_{dc}$ |
| $V_{Car1} < V_{Ref}$<br>$V_{Car2} > V_{Ref}$<br>$V_{Car3} > V_{Ref}$ | 0                           | 1     | 0     | 0     | 1                      |       |       | 1     | $\frac{1}{3} V_{dc}$ |
| $V_{Car1} > V_{Ref}$<br>$V_{Car2} > V_{Ref}$<br>$V_{Car3} > V_{Ref}$ | 0                           | 0     | 0     | 0     |                        | 1     |       | 1     | 0                    |

Table 1. Cont.

| Comparison                                                           | Auxiliary Circuit Switching |       |       | $Q^*$ | Main Circuit Switching |       |       |       | Output-Voltage<br>$V_{Out}$ |
|----------------------------------------------------------------------|-----------------------------|-------|-------|-------|------------------------|-------|-------|-------|-----------------------------|
|                                                                      | $Q_f$                       | $Q_1$ | $Q_2$ |       | $S_1$                  | $S_2$ | $S_3$ | $S_4$ |                             |
| $V_{Car1} > V_{Ref}$<br>$V_{Car2} > V_{Ref}$<br>$V_{Car3} > V_{Ref}$ | 0                           | 0     | 0     | 0     | 1                      |       | 1     |       | 0                           |
| $V_{Car1} < V_{Ref}$<br>$V_{Car2} > V_{Ref}$<br>$V_{Car3} > V_{Ref}$ | 0                           | 1     | 0     | 0     |                        | 1     | 1     |       | $-\frac{1}{3} V_{dc}$       |
| $V_{Car1} < V_{Ref}$<br>$V_{Car2} < V_{Ref}$<br>$V_{Car3} > V_{Ref}$ | 0                           | 0     | 1     | 1     |                        | 1     | 1     |       | $-\frac{2}{3} V_{dc}$       |
| $V_{Car1} < V_{Ref}$<br>$V_{Car2} < V_{Ref}$<br>$V_{Car3} < V_{Ref}$ | 1                           | 0     | 0     | 1     |                        | 1     | 1     |       | $-V_{dc}$                   |

To illustrate the effect of different modulation ratios on the output-voltage levels, different modulation indices are considered under different output-voltage levels. When  $M_a$  is lower than 0.33, the output-voltage has only three levels ( $+V_{dc}/3, 0, -V_{dc}/3$ ). For a modulation index between 0.33 and 0.67, the output-voltage shows five levels ( $+2V_{dc}/3, +V_{dc}/3, 0, -V_{dc}/3, -2V_{dc}/3$ ). For a modulation index between 0.67 and 1, 7-level output-voltage can be synthesized ( $+V_{dc}, +2V_{dc}/3, +V_{dc}/3, 0, -V_{dc}/3, -2V_{dc}/3, -V_{dc}$ ).

### 3. Comparative Study

This section introduces a comparative study between the proposed 7-level PWM inverter with the recent MLI structures based on different performance metrics, such as number of switching devices, number of components, number of components for each output-voltage level ( $N_{C/L}$ ), number of active switches per output-voltage pole ( $N_{AVG/Pole}$ ), output-voltage THD, inverter efficiency, and the applied PWM technique. The comparison illustrates that each MLI topology utilizes different number of components to obtain the same output-voltage level. As  $N_{C/L}$  increases, the MLI topology requires more components for same output-voltage level synthesis per pole. On the other side, when  $N_{C/L}$  has decreases, the required number of components decreases, which enhances the inverter efficiency. The factor ( $N_{C/L}$ ) can be formulated as follows [13]:

$$N_{C/L} = \frac{N_C + N_T + N_S + N_D + N_{PS} + N_X}{N_{Pole}} \quad (12)$$

where;

$N_{C/L}$ : Components per pole of output voltage level.

$N_{Pole}$ : Number of voltage levels per pole.

$N_C$ : Number of capacitors.

$N_D$ : Number of diodes.

$N_S$ : Number of switching devices.

$N_{PS}$ : Number of DC power supplies.

$N_T$ : Number of transformers.

$N_X$ : Number of additional components.

Table 2 illustrates a comparison between the proposed inverter topology and the recent topologies based-on the former metrics. As noted, the proposed MLI utilizes a smaller number of power switches, power components, and  $N_{C/L}$  compared to other topologies. This leads to fewer losses and less cost associated with the proposed inverter. In addition,  $N_{AVG/Pole}$  is compared for the different MLI topologies as an indication for the number of

active switches in the current path, which indicates the inverter power-losses. The factor  $N_{AVG/Pole}$  can be expressed as follows:

$$N_{AVG/Pole} = \frac{N_{level(0)} + N_{level(1)} + N_{level(2)}}{N_{Pole}} \quad (13)$$

where;

$N_{level(0)}$ : number of active switches for the zero output-voltage synthesis.

$N_{level(1)}$ : number of active switches for the first output-voltage level synthesis.

$N_{level(2)}$ : number of active switches number for the second output-voltage level synthesis.

Based-on Table 2, the proposed MLI exhibits a low  $N_{AVG/Pole}$  in compared with most of the recent added topologies, which decreases the inverter power losses and enhances its efficiency. In addition, the heat dissipated over the inverter components is reduced, which improves the system reliability. Figure 5 shows  $N_S$ ,  $N_{C/L}$ ,  $N_{AVG/Pole}$ , and  $THD$  for the proposed 7-level inverter in compared with the recent MLI structures.

**Table 2.** Comparison study of MLI topologies.

| In Cited Paper: |       | $N_{Pole}$ | $N_{PS}$ | $N_S$ | $N_D$ | $N_C$ | $N_T$ | $N_{C/L}$ | $N_{AVG/Pole}$ | THD (%) | Eff. (%) | PWM Technique       |
|-----------------|-------|------------|----------|-------|-------|-------|-------|-----------|----------------|---------|----------|---------------------|
| Reference       | Level |            |          |       |       |       |       |           |                |         |          |                     |
| [35]            | 7     | 4          | 2        | 6     | 2     | 0     | 0     | 2.5       | 3.6            | 4.8     | 94       | Fund. Frequency PWM |
| [14]            | 5     | 3          | 1        | 12    | 6     | 2     | 0     | 7         |                |         |          | SPWM                |
| [17]            | (a)   | 5          | 3        | 2     | 8     | 0     | 0     | 0         | 3.33           |         |          | Fund. Frequency PWM |
|                 | (b)   | 7          | 4        | 3     | 12    | 0     | 0     | 0         | 3.75           | 2.5     | –        |                     |
|                 | (c)   | 9          | 5        | 4     | 16    | 0     | 0     | 0         | 4              | 8       |          |                     |
| [36]            | 5     | 3          | 2        | 12    | 12    | 0     | 0     | 8.67      |                |         |          | MPC & SPWM          |
| [20]            | (a)   | 5          | 3        | 1     | 4     | 0     | 1     | 0         | 2              |         |          | PSC-PWM             |
|                 | (b)   | 7          | 4        | 1     | 6     | 0     | 2     | 0         | 2.25           |         |          |                     |
|                 | (c)   | 9          | 5        | 1     | 8     | 0     | 3     | 0         | 2.4            | 3       |          |                     |
| [21]            | 5     | 3          | 1        | 12    | 0     | 5     | 0     | 6         |                | 5       | –        | 3D-PWM              |
| [37]            |       | 6          | 0        | 9     | 4     | 3     | 0     | 2.67      | 5.4            |         |          | Fund. Frequency PWM |
| [38]            | (a)   | 5          | 3        | 2     | 6     | 0     | 0     | 0         | 2.67           | 2.67    | 3        | SPWM                |
|                 | (b)   | 7          | 4        | 3     | 8     | 0     | 0     | 0         | 2.75           |         | 88       |                     |
|                 | (c)   | 9          | 5        | 4     | 10    | 0     | 0     | 0         | 2.8            | 4.4     |          |                     |
| [39]            | (a)   | 5          | 3        | 2     | 8     | 0     | 0     | 0         | 3.33           | 3.33    |          | SHE-PWM & SPWM      |
|                 | (b)   | 7          | 4        | 3     | 10    | 0     | 0     | 0         | 3.25           | 6.84    | –        |                     |
|                 | (c)   | 9          | 5        | 4     | 12    | 0     | 0     | 0         | 3.2            | 5.2     |          |                     |
| [40]            |       | 5          | 4        | 8     | 4     | 0     | 0     | 3.2       |                | 4.24    | –        | Fund. Frequency PWM |
| [41]            |       | 3          | 2        | 8     | 0     | 0     | 0     | 3.33      | 4              | 3.67    | –        | SHE-PWM & SPWM      |
| [42]            |       | 4          | 1        | 12    | 0     | 2     | 0     | 3.75      | 4              | –       | 90       | CPS-SPWM            |
| [43]            |       | 3          | 2        | 6     | 0     | 0     | 0     | 2.67      | 3              | 3.9     | –        | SPWM                |
| [44]            |       | 4          | 3        | 7     | 1     | 0     | 0     | 2.75      | 3              | 5.48    | –        | SPWM                |
| [45]            |       | 3          | 2        | 5     | 1     | 0     | 0     | 2.67      | 3              | 4.97    | –        | SPWM                |
| [30]            | (a)   | 7          | 4        | 3     | 7     | 2     | 0     | 0         | 3              | 3.33    | 4.3      | SPWM                |
|                 | (b)   | 9          | 5        | 4     | 10    | 3     | 0     | 0         | 3.4            | 2.8     | 4        |                     |

Table 2. Cont.

| In Cited Paper: |         | $N_{Pole}$ | $N_{PS}$ | $N_S$ | $N_D$ | $N_C$ | $N_T$ | $N_{C/L}$ | $N_{AVG/Pole}$ | THD (%) | Eff. (%) | PWM Technique |
|-----------------|---------|------------|----------|-------|-------|-------|-------|-----------|----------------|---------|----------|---------------|
| Reference       | Level   |            |          |       |       |       |       |           |                |         |          |               |
| [15]            | (a)     | 5          | 3        | 2     | 5     | 1     | 0     | 0         | 2.67           | 2.33    | 3        | 88.5          |
|                 | (b)     | 7          | 4        | 3     | 6     | 2     | 0     | 0         | 2.75           | 2.75    | 2.9      | 90.3          |
|                 | (c)     | 9          | 5        | 4     | 7     | 3     | 0     | 0         | 2.8            | 3.2     |          |               |
| Proposed MLI    | 7-level | 4          | 1        | 7     | 1     | 0     | 0     | 2.25      | 2.75           | 3.73    | 92.86    | SPWM          |

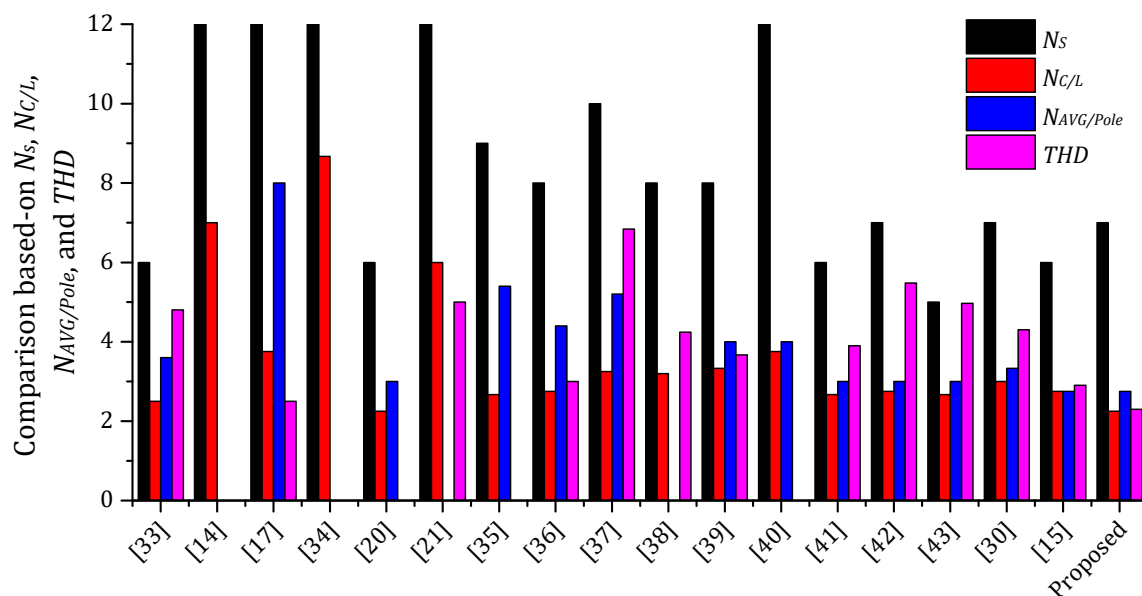


Figure 5. Comparison between the proposed 7-level inverter and the recent topologies.

#### 4. MLI Control Scheme

Control scheme of the proposed single-phase 7-level inverter with MPPT algorithm for stand-alone and grid-integrated operations is depicted in Figure 6. A single choke-coil was used as current filter for sinusoidal grid-integrated voltage and current. The conventional P&O algorithm was used for MPPT, in which the PV array voltage and current were sensed and used to define the BC duty cycle that matches MPP [2,46,47]. The MPPT controls the maximum power to the load/grid considering a constant (K) that defines the system tracking efficiency. Different linear and non-linear controllers can be used for load-voltage/grid-current regulation; however, the conventional PI-controller was used in this work due to their simplicity and linearity [48,49]. In both cases, the reference set point was usually used as a sinusoidal waveform [30,50]. In case of grid-integrated operation, the reference set point was used as the sinusoidal grid-voltage to ensure the unity power factor operation. Hence, the PV system power was divided by the grid voltage to produce the sinusoidal reference grid-current, as shown in Figure 6. In stand-alone operation, the reference set point was a sinusoidal waveform for the desired load voltage. A closed-loop current control using the conventional PI controller is used to regulate the actual grid-injected current ( $i_g$ ) to follow the reference value ( $i_g^*$ ) considering the proposed PWM switching pattern. The PI controller output-signal was considered as the modulation index signal ( $M_a$ ), which was compared with the level-shifted carrier waveforms to generate the key gating pulses ( $S_1$ ,  $S_2$ ,  $S_3$ , and  $S_4$ ). Then, the auxiliary circuit switching pulses could be derived based-on Equations (10) and (11).

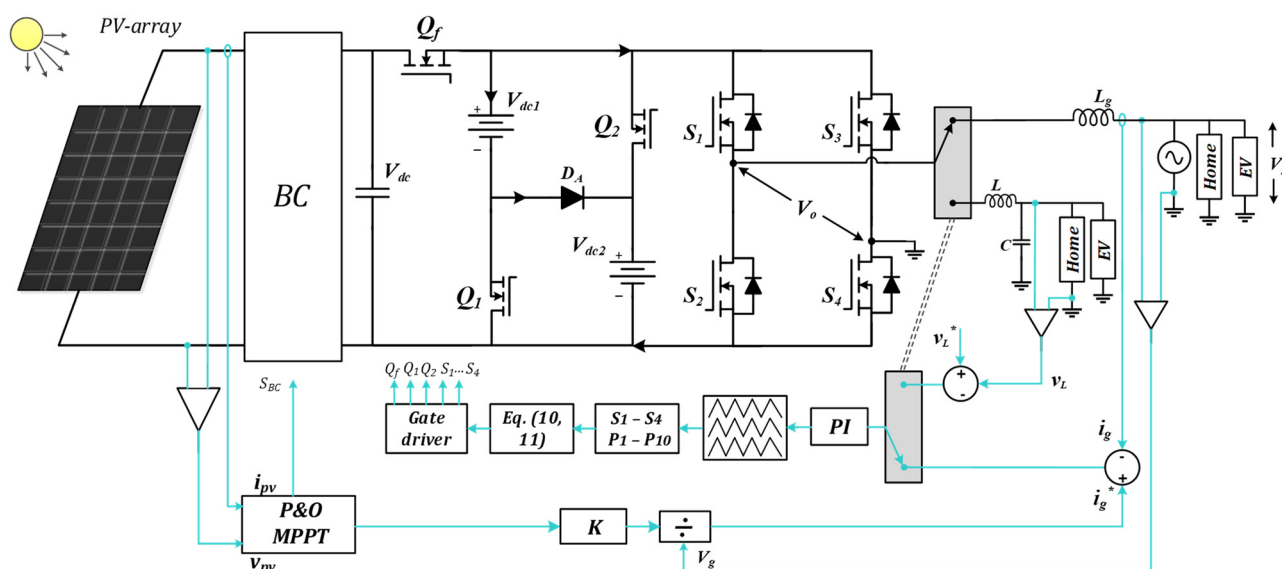


Figure 6. Control scheme of the grid connected PV system via the proposed 7-level inverter.

## 5. Simulation and Experimental Validations

### 5.1. Simulation Results

A MATLAB/Simulink model was developed for the entire PV system, including DC-DC BC with P&O MPPT and the proposed MLI with the associated controller. In this model, the main input source was a PV array and other sources were battery banks. The Canadian solar CS5P-220M PV module was considered in the model, which has the output characteristics at the standard test conditions listed in Table 3. The PV array consisted of five series modules ( $N_s = 5$ ) and ten parallel modules ( $N_p = 10$ ), which showed the characteristics listed in Table 4. The system was tested under stand-alone as well as grid-integrated operation. For stand-alone operation, the load-voltage was sensed and compared with the reference value where the error signal was fed to a conventional PI controller to generate  $M_a$ . Similarly, for the grid-integration, the phase angle of the grid voltage as well as grid current were sensed for power factor correction. The measured and reference grid currents were compared and regulated using a PI controller, as indicated in Figure 6. In both cases, the output signal from PI controller was compared with the level-shifted carrier waveforms to generate the main switching signals and control periods ( $Q_f, S_1, \dots, S_4$ ). Then, the auxiliary circuit switching signals were derived for the 7-level inverter. The PV grid-tied system was tested under different solar irradiance, which varies from 1000 ( $\text{W}/\text{m}^2$ ) to 700 ( $\text{W}/\text{m}^2$ ) to validate the performance of MPPT technique under uniform as well as step-changed solar irradiance as a hard tracking condition [2].

Table 3. The characteristics of Canadian solar CS5P-220M PV module at STC.

|                                    |          |
|------------------------------------|----------|
| Maximum Power ( $P_{mpp}$ )        | 220 (W)  |
| Voltage at MPP ( $V_{mpp}$ )       | 47 (V)   |
| Current at MPP ( $I_{mpp}$ )       | 4.68 (A) |
| Open circuit voltage ( $V_{oc}$ )  | 58.8 (V) |
| Short circuit current ( $I_{sc}$ ) | 5.01 (A) |

Table 4. The characteristics of PV array.

|                                    |          |
|------------------------------------|----------|
| Maximum Power ( $P_{mpp}$ )        | 11 (kW)  |
| Voltage at MPP ( $V_{mpp}$ )       | 235 (V)  |
| Current at MPP ( $I_{mpp}$ )       | 46.8 (A) |
| Open circuit voltage ( $V_{oc}$ )  | 294 (V)  |
| Short circuit current ( $I_{sc}$ ) | 50.1 (A) |

Figure 7 shows the PV panel output current, voltage, and power with a step-variation in irradiance profile from  $1000 \text{ W/m}^2$  to  $700 \text{ W/m}^2$  to ensure MPPT controller stability at different irradiance conditions. The constant voltage profile in Figure 7c proves that the PV array operates efficiently at the MPP, regardless the fluctuations in irradiance profile. In addition, the extracted power at  $1000 \text{ W/m}^2$  matches the listed maximum power at the standard test conditions presented in Table 4. On the grid side, Figure 8 exhibits the inverter output voltage. The inverter terminal-voltage is a high-frequency modulated at 7-levels before the grid-current filter with its fundamental component is in-phase with the grid-voltage, as depicted Figure 8. Figure 9 exhibits the change in the grid-voltage, grid-injected current, and grid-injected power with step variation of irradiation. The grid-injected current is sinusoidal waveform and in-phase with the grid-voltage for unity power-factor operation of grid-integrated PV-system. To prove the robustness of the grid-tied controller with minimum error, the reference and actual grid currents are depicted in Figure 10. The actual grid-current tracks the reference current with minimum error, low settling time, and enhanced system response.

The Fast Fourier Transform (FFT) harmonic analysis of the grid-injected current and inverter terminal-voltage are portrayed in Figure 11. The grid current harmonic orders are compared with IEEE-1547 harmonic standard limit for Distributed Energy Resources (DER). The grid current THD is 3.75% and its harmonic orders are below the standard individual order limits as shown in Figure 11a. Also, the FFT harmonic spectrum of the inverter terminal multilevel voltage is portrayed in Figure 11b and its THD is 24.35%.

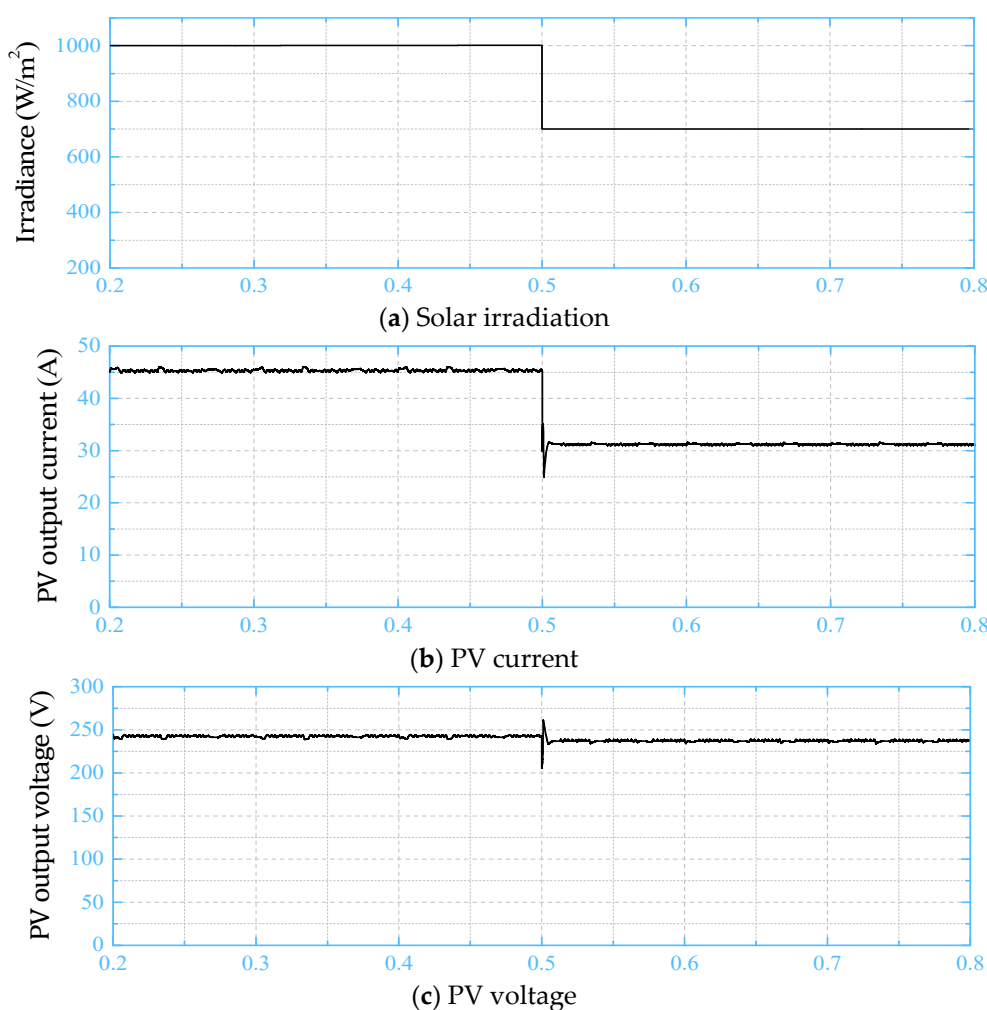


Figure 7. Cont.

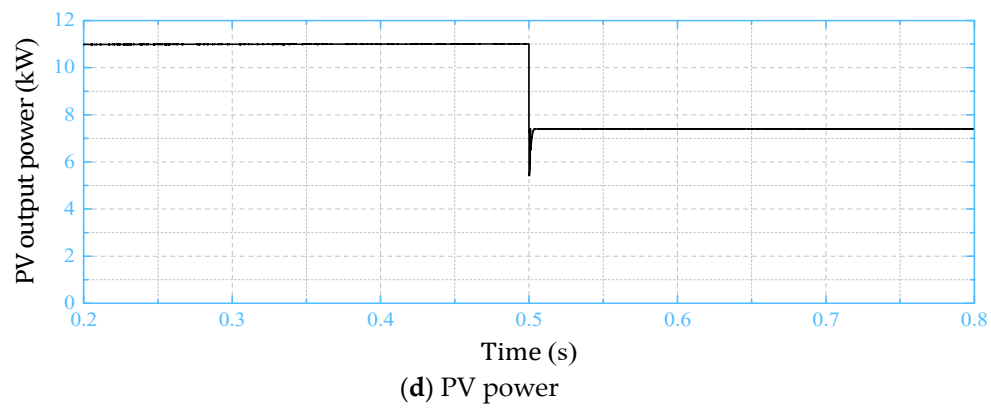


Figure 7. The PV panel current, voltage, and power.

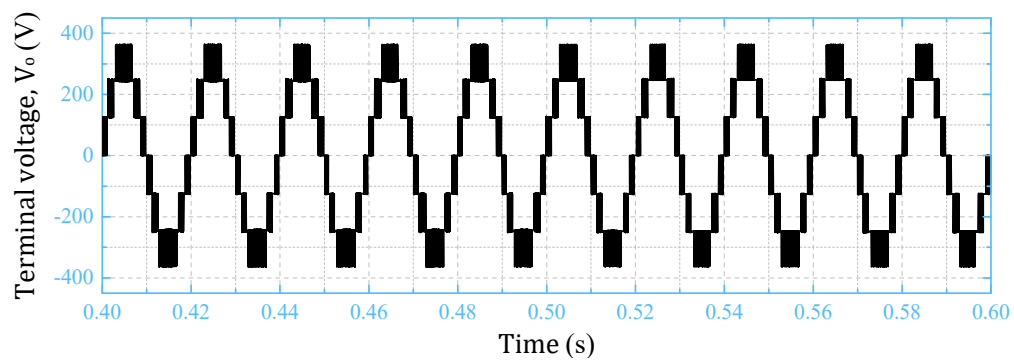


Figure 8. Multi-Level inverter output voltage.

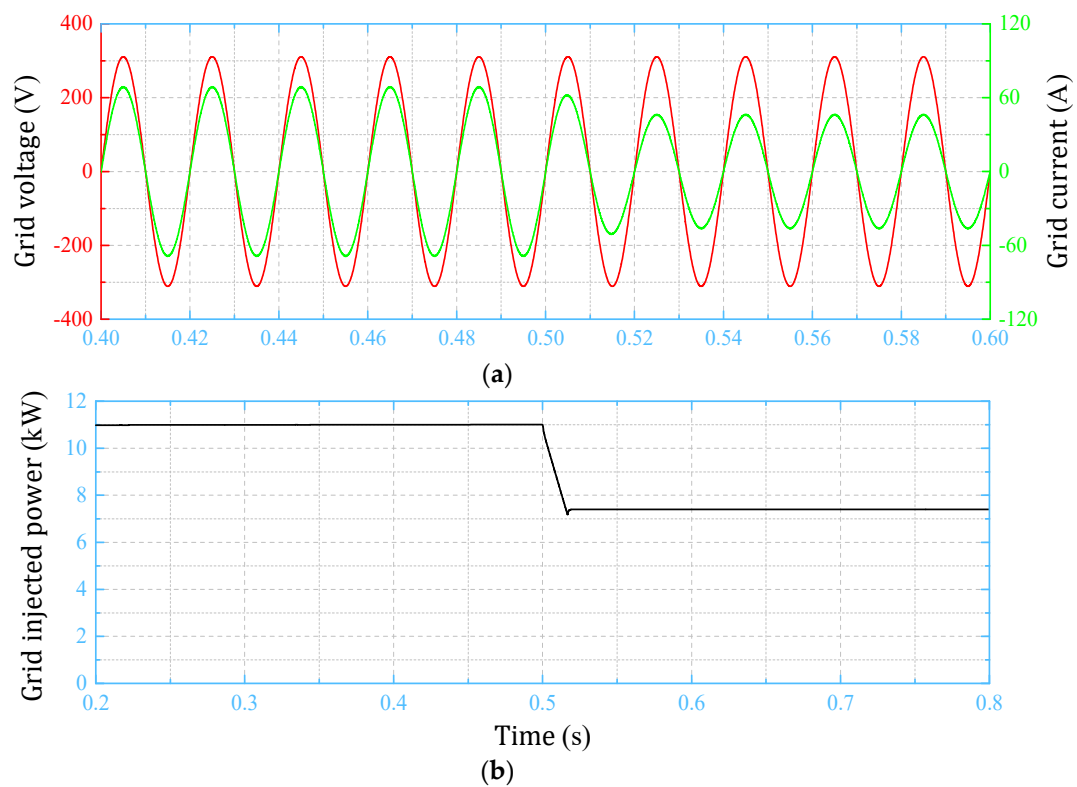


Figure 9. The injected current, voltage, and power variation. (a) Grid voltage and current; (b) Grid injected power.

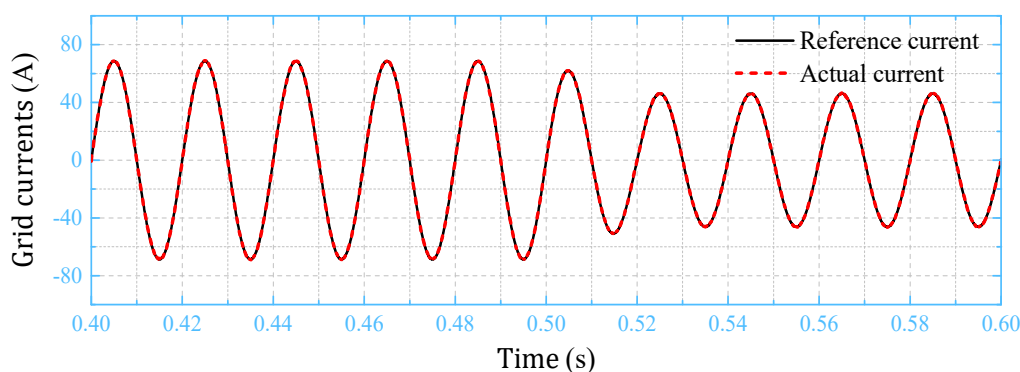


**Figure 10.** The reference and actual injected currents of the seven-level inverter at irradiance variation.

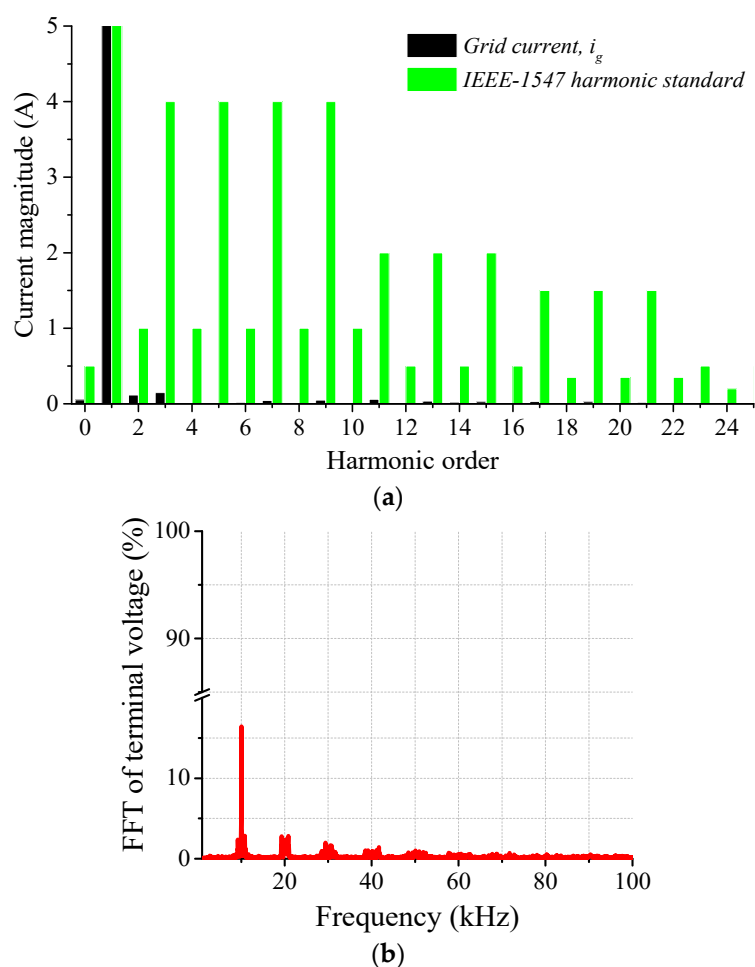


**Figure 11.** FFT analysis of inverter output voltage and grid injected current; (a) grid current, and (b) inverter voltage.

In addition, the grid integrated home/EV system is tested under uniform irradiance profile (fixed at  $1000 \text{ W/m}^2$ ) considering grid current pulsating change for EV charging, which considers base grid and home power of 3 kW and 2 kW, respectively, as depicted in Figure 12. Figure 12a shows the loading profile before and after EV charging connection and in case of the grid-integrated operation. The inverter multilevel output voltage with pulsating charging current of EV is shown in Figure 12b. The inverter terminal voltage has 7-levels even under load current/power variation. In addition, the grid voltage and load current based on the former loading profile is depicted in Figure 12c. Obviously, the base home and grid injected power are applied between starting time up to (0.1 s). Between

the time intervals (0.1 and 0.2 s), the EV is connected to the grid for EV charging and the grid power is increased from 5 kW to 11 kW, as cleared in the grid pulsating current in Figure 12c.

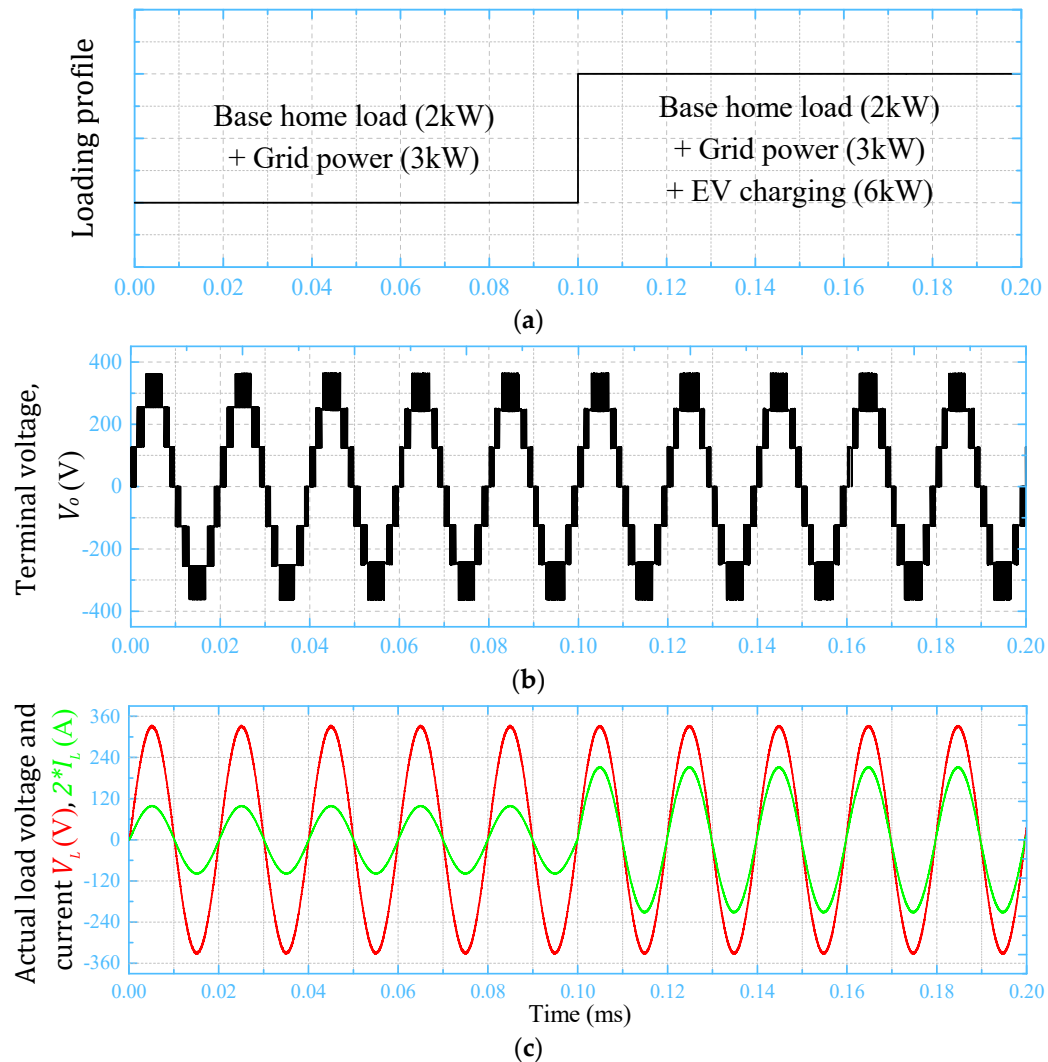


**Figure 12.** Simulation results of the proposed 7-level inverter as level-2 EV charger (240 V, 3:6 kW); (a) loading profile, (b) multilevel output voltage, and (c) inverter voltage/pulsating current.

For closed-loop load-voltage control of home/EV operation, the loading profile of the home/EV system considering home base load of 2 kW is depicted in Figure 13a. Figure 13b shows the 7-level terminal-voltage of the proposed inverter. Reference and actual load-voltages are portrayed in Figure 13c. Obviously, the actual load-voltage follows the reference value with reduced steady-state error and sinusoidal waveform with low THD for enhanced power-quality considering low passive elements. In addition, the load voltage and current waveforms, considering the loading profile in Figure 13a, are depicted in Figure 13d. The load current is sinusoidal waveform with reduced THD and unity power-factor operation. The FFT harmonic spectrum of the load current is analyzed in Figure 14. The THD of the load current is 2.3%, which enhances the power-quality of the load power that follows the IEEE-519 harmonic standard limits.

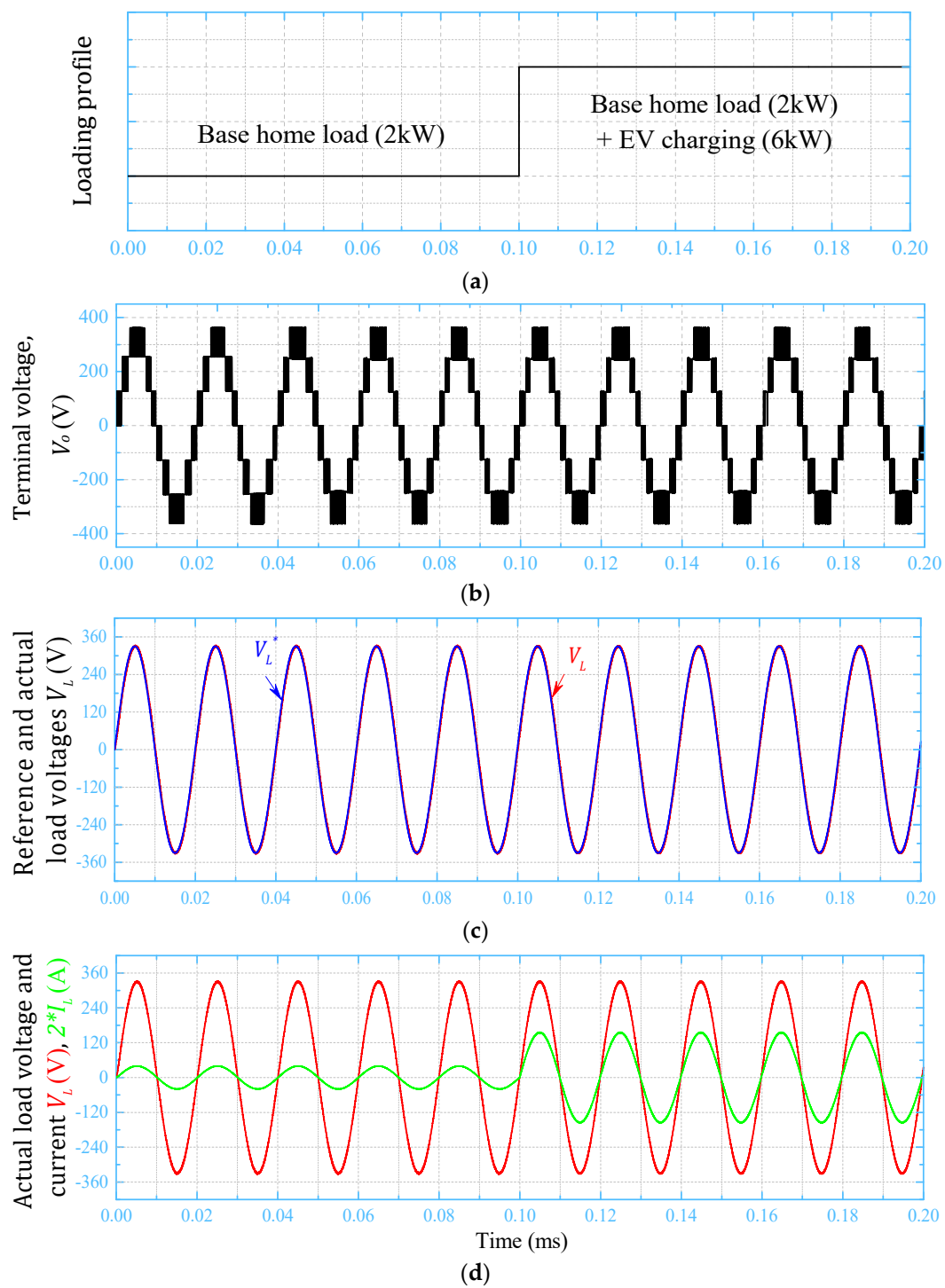


**Figure 13.** Simulation results of the proposed 7-level inverter for house loads voltage control (2 kW). (a) Load reference and actual voltages, (b) Load voltage and current.

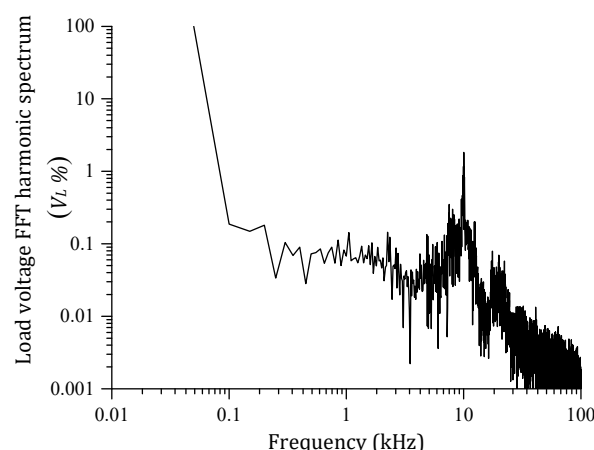


**Figure 14.** House load current FFT harmonic spectrum at 2 kW.

### 5.2. Experimental Results

An experimental prototype is built for the proposed MLI and the associated control to validate its performance. The proposed MLI is integrated and tested in a test platform considering the proper sinusoidal PWM switching strategy, as depicted in Figure 4. For simplicity, a DC supply is used to emulate the PV array, BC, and MPPT. Figure 15 shows the experimental prototype and the measured system parameters are listed in Table 5. The prototype consists of an input DC-source, two non-identical batteries, and the proposed MLI. The dc sources  $V_{dc1}$  and  $V_{dc2}$  at the input side of the experimental prototype have been implemented as ideal DC sources instead of batteries, which is acceptable given the large difference between time constants of batteries and converters. The main H-bridge inverter switches are implemented using IRFP264PBF MOSFETs and the auxiliary circuit switches are deployed using IGW50N65F4 IGBTs, for unidirectional power-flow, which are interfaced with Dspace DS-1103 controller via 6N137 gate-driver circuits. The SPWM switching technique is developed according to Table 1 and Figure 4. The switching-frequency of the proposed 7-level inverter is 10 kHz to synthesize the high-frequency modulated voltage at the inverter terminals. The proposed inverter is tested during stand-alone and grid-connected operations. In both cases, a conventional PI controller is used for error signal regulation to generate the modulation index to synthesize the inverter switching signals.

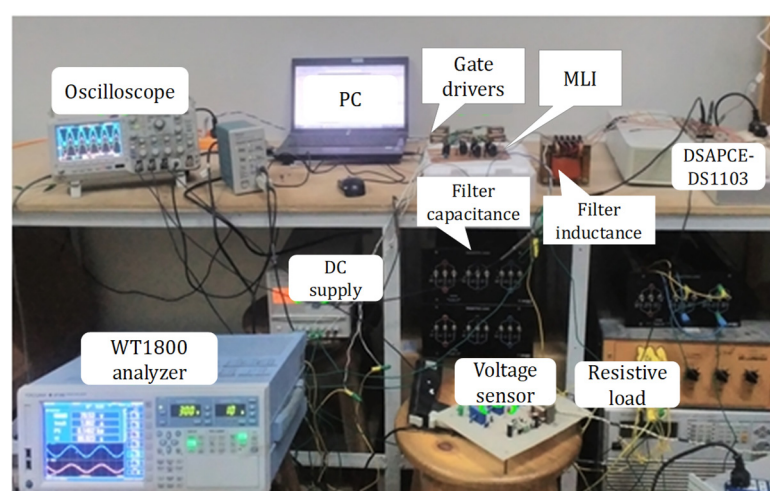
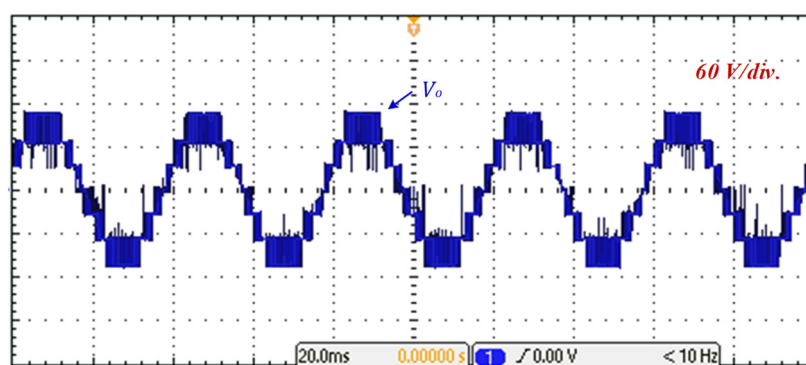
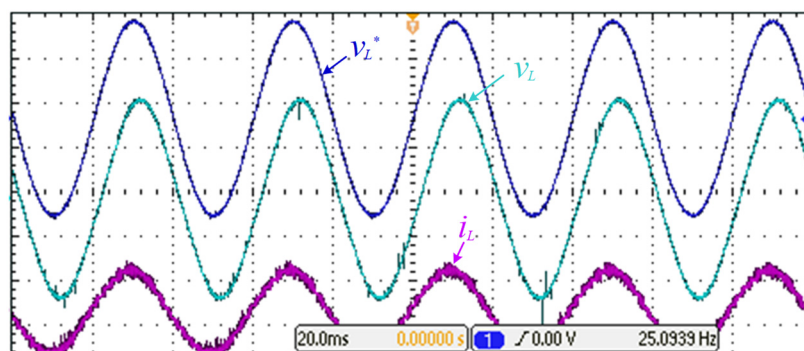


**Figure 15.** A photograph of the experimental system.

**Table 5.** Experimental system parameters.

|                                    |                                    |
|------------------------------------|------------------------------------|
| Input Voltage ( $V_{in}$ )         | 105 V                              |
| Grid voltage ( $V_g$ )             | 70 V, 50 Hz                        |
| Load resistance ( $R$ )            | 43 ( $\Omega$ )                    |
| LC filter                          | 1 mH, 10 $\mu$ F                   |
| AC line frequency                  | 50 Hz                              |
| Switching frequency ( $F_{SW}$ )   | 10 kHz                             |
| PI controller gains, $K_P$ , $K_I$ | 0.081 A/V, 200 $\text{rad s}^{-1}$ |

Figure 16 shows the measured terminal-voltage waveform of the proposed inverter. The inverter voltage realizes the seven levels like the simulation results. In addition, the proposed inverter is tested with a closed loop voltage control for stand-alone operation and the results are depicted in Figure 17. As noted, the actual voltage tracks the reference value with a small voltage error, which feeds the load with a sinusoidal current waveform, as indicated in Figure 17a. A small phase-shift is noticed between reference and actual load voltages due to the PI-controller steady state error [48], which has no effect on the converter control technique and its stability operation. FFT spectrum of the load voltage is displayed in Figure 17b, which shows a THD of 3.73%. The RMS values of load voltage, current, power, and efficiency of the proposed 7-level inverter are captured from the WT1800 power analyzer and presented in Figure 17c. The proposed inverter exhibits a high operating efficiency of 92.5% compared to most of the topologies presented in the literature.

**Figure 16.** Measurement of the 7-level inverter terminal-voltage at stand-alone load-voltage control.**(a)** Reference and actual load voltage ( $V_L^*$ ,  $V_L$ ) and the load current ( $I_L$ ).**Figure 17.** Cont.

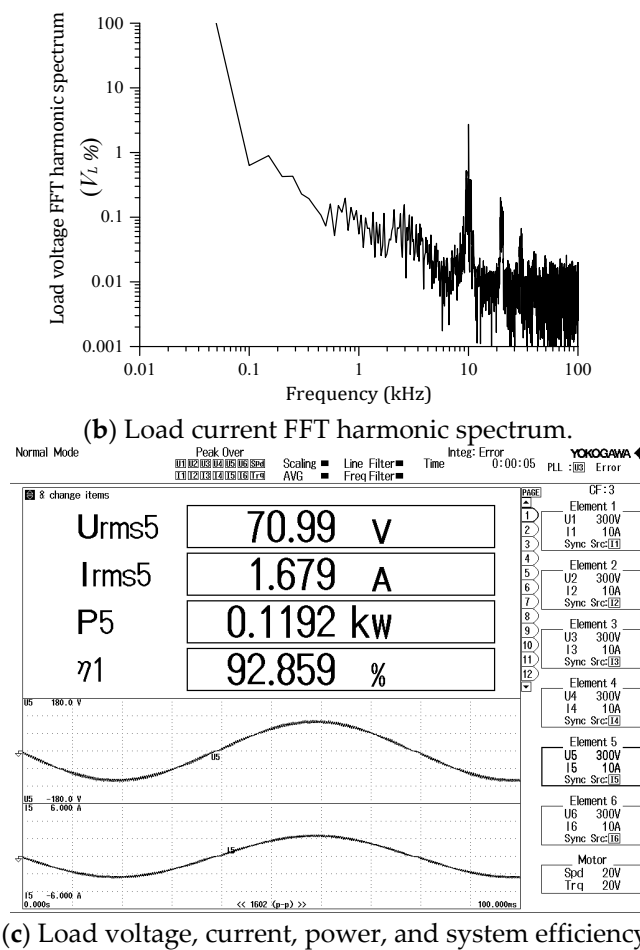


Figure 17. Measurement of the 7-level inverter terminal-voltage at stand-alone load-voltage control.

To reveal the system validation of the proposed inverter for grid-integrated applications, the inverter was tested under grid-connected operation and the results are presented in Figure 18. The figure shows a comparison between the actual grid injected current and the reference value, which indicates the accuracy of the controller and inverter to track the reference current with a clean sinusoidal waveform. The THD of the measured grid current is 3.43%, which is within the standard limits defined by the IEEE-1547 standard for DER.

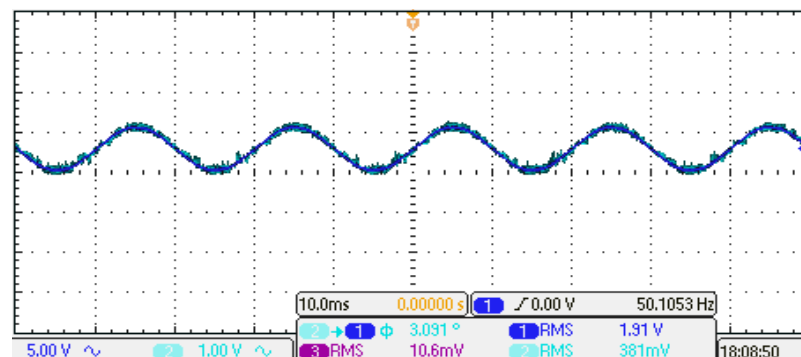


Figure 18. The 7-level inverter experimental results under grid-tied current control.

## 6. Conclusions

This paper has presented a new topology of a single-phase seven-level inverter as an interface for grid-integrated and stand-alone solar PV systems. The circuit configuration and operation principle of the proposed inverter have been presented in detail along with

the switching patterns and control strategy. A comparative study between the proposed inverter structure and the recent MLI topologies is enriched to reveal the features of the proposed inverter. The proposed MLI structure considers a reduced number of power switches,  $N_{C/L}$ , and  $N_{AVG/Pole}$ , which enhances the inverter operating efficiency and decreases its cost. Only seven switches have been utilized to synthesis voltage waveform of seven levels at the output terminals. The performance of the proposed inverter and associated control was investigated for grid-integrated and stand-alone PV systems based on simulation and experimental tests. The test platform includes a boost converter with MPPT control, which feeds the front-end of the proposed MLI. The results show that the proposed inverter exhibits an improved steady state response, and minimum settling time (i.e., 5 ms). THD of both voltage and current waveforms during grid-integration and stand-alone operations is 3.43%, which follows the IEEE-1547 harmonic standards for DER applications. In addition, the inverter offers a high operating efficiency of 92.86%, compared to most of the recently published topologies surveyed in this paper.

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## Abbreviations

|                |                                         |
|----------------|-----------------------------------------|
| $M_a$          | Modulation index                        |
| $N_{PS}$       | Number of DC power supplies             |
| $N_S$          | Number of switching devices             |
| $N_D$          | Number of diodes                        |
| $N_C$          | Capacitors Number                       |
| $N_T$          | Transformers Number                     |
| $N_X$          | Number of other additional components   |
| $N_{Pole}$     | Voltage levels number per pole          |
| $N_{C/L}$      | Number of components per level          |
| $N_{AVG/Pole}$ | Average number of ON-switches per pole  |
| $A_m, A_c$     | Reference and carrier signal amplitudes |
| $P_n$          | Modes of operation                      |
| $\theta_n$     | Switching angle                         |
| PV             | Photovoltaic                            |
| EV             | Electric vehicle                        |
| MLI            | Multilevel inverter                     |
| THD            | Total harmonic distortion               |
| EMI            | Electromagnetic interface               |
| CHB-MLI        | Cascaded H-bridge MLI                   |
| NPC-MLI        | Neutral Point Clamped MLI               |
| FC-MLI         | Flying Capacitors MLI                   |
| SPWM           | Sinusoidal pulse-width-modulation       |

|         |                                    |
|---------|------------------------------------|
| MPPT    | Maximum power point tracking       |
| BC      | Boost converter                    |
| SHE-PWM | Selective harmonic elimination PWM |
| P&O     | Perturb and observe                |
| FFT     | Fast Fourier transform             |
| DER     | Distributed energy resources       |

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