energies

MDPI

Article

Novel Five-Level ANPC Bidirectional Converter for Power Quality Enhancement during G2V/V2G Operation of Cascaded EV Charger

Jorge Lara [1,*], Lesedi Masisi [2], Concepcion Hernandez [1], Marco A. Arjona [1] and Ambrish Chandra [3]

[1] División de Estudios de Posgrado e Investigación, TNM Instituto Tecnológico de La Laguna, Torreón 27000, Mexico; coni.hernandez@ieee.org (C.H.); marjona@ieee.org (M.A.A.)
[2] School of Electrical and Information Engineering, University of the Witwatersrand, Johannesburg 2000, South Africa; lesedi.masisi@wits.ac.za
[3] Department of Electrical Engineering, École de Technologie Supérieure (ÉTS), Montreal, QC H3C 1K3, Canada; ambrish.chandra@etsmtl.ca
* Correspondence: jorge_lara_c@yahoo.com

Abstract: This paper presents a novel single-phase (SP) active-neutral point clamped (ANPC) five-level bidirectional converter (FLBC) for enhancing the power quality (PQ) during the grid-to-vehicle (G2V) and vehicle-to-grid (V2G) operation of an electric vehicle (EV) charger connected in series. This EV charger is based on a dual-active half-bridge DC-DC converter (DAHBC) with a high frequency isolation transformer. Unlike the comparable ANPC topologies found in literature, the proposed one has two more switches, i.e., ten instead of eight. However, with the addition of these components, the proposed multilevel converter not only becomes capable of properly balancing the voltage of the DC-link split capacitors under various step-changing conditions but it achieves a better efficiency, a lower stress of the switching devices and a more even distribution of the power losses. The resulting grid-tied ANPC-SPFLBC and DAHBC are accurately controlled with a cascaded control strategy and a single-phase shift (SPS) control technique, respectively. The simulation results obtained with MATLAB-SimPowerSystems as well as the experimental results obtained in laboratory validate the proposed ANPC-SPFLBC for a set of exhaustive tests in both V2G and G2V modes. A detailed power quality analysis carried out with a Fluke 43B alike demonstrates the good performance of the proposed topology.

Keywords: single-phase five-level converter; ANPC topology; DC-link split capacitors voltage balancing; power quality enhancement; electric vehicle charger; G2V/V2G operation modes

Citation: Lara, J.; Masisi, L.; Hernandez, C.; Arjona, M.A.; Chandra, A. Novel Five-Level ANPC Bidirectional Converter for Power Quality Enhancement during G2V/V2G Operation of Cascaded EV Charger. *Energies* **2021**, *14*, 2650. https://doi.org/10.3390/en14092650

Academic Editor: Sekyung Han

Received: 24 March 2021
Accepted: 27 April 2021
Published: 5 May 2021

1. Introduction

The detrimental environment pollution due to the use of conventional sources of energy, the continuous increases in the price of oil and the expected eventual exhaustion of fossil fuels have fostered the rapid development of electric vehicles, both battery-based (BEV), hybrid (HEV), plug-in (PEV) and fuel cell-based (FCEV) [1,2]. Some European countries, such as Norway and Sweden have scheduled banning all petrol-powered cars in the next 3–4 decades. The EVs inherently linking the transport and the electricity sectors have given rise to emerging technologies such as superchargers (G2V) and grid-support (V2G) [3–5]. These EVs are grid-connected through a power converter, hence requiring of advanced power conversion and control techniques and a deep analysis of the grid impact, the converter behavior, the stability, the harmonic emission and the electromagnetic interference (EMI) [6]. There exists a wide variety of EV battery charger topologies [7]. The dual active full bridge (DAFB) and the dual active half bridge (DAHB) DC-DC topologies are especially practical because they include a higher frequency (HF) transformer in between that provides a galvanic isolation for safely connecting the EV

batteries with the mains through the grid-tied power converter [8,9]. Furthermore, bearing in mind that the physical size and in turn the weight of the required transformer reduces with the increasing of the operating frequency [10], this topology is fairly attractive for EV applications where space and burden constraints are critical. Despite the fact that in the DAHB topology only the SPS control technique can be applied, it is widely utilized due to its low cost, volume and weight as well as its global reduction in switches, drivers and cooling system [11].

The interaction of modern power converters with the smart grid is a main issue regarding power quality aspects [12]. The use of multilevel power converters (ML) is increasingly preferred since they provide a high-quality output voltage with a lower harmonic content, a lower dV/dt, a lower switching frequency and consequently a higher efficiency [13]. The cascaded H-bridge (CHB), the flying capacitor (FC) and the neutral-point-clamped (NPC) including its subtopology of active-NPC (ANPC) are the main types of conventional multilevel topologies [14]. The NPC-based configurations have the advantage of requiring only one isolated DC source but also the inconvenient that its DC-link split capacitors undergo the voltage unbalance phenomenon and consequently they need implementing balancing compensation techniques [15–18]. It is possible to get rid of this unbalancing issue by using two independent DC voltage sources instead of capacitors but at the expense of a higher cost and a bigger system complexity [19] or well in certain photovoltaic (PV) applications [20].

Over the last years various topologies of single-phase ANPC five-level (FL) converters have been devised. In [21], authors propose a single-phase hybrid Si/SiC ANPC FL inverter with an improved modulation scheme for reducing the conduction losses. Although the inherent voltage unbalancing problem is not mentioned, its undesirable effect is present but it could have been reduced by considerably increasing the capacitance of the electrolytic split capacitors. Due to the absence of redundant vectors for the states that output half of the DC bus voltage, the voltage balancing in this topology is simply not possible. In [22], authors propose a single-phase ANPC FL inverter and its three-phase version. The modulation strategy is based on an unipolar pulse-width modulation (PWM) for the high-frequency switches and on the polarity of the modulating signal for the low-frequency switches. Owing to the consecutive alternation of the redundant switching states for the high-frequency switches, the split capacitors are equally charge and discharge at each switching period, thus accurately maintaining a zero average neutral current and consequently achieving a fairly good voltage unbalancing compensation. Nevertheless, the alternation of the redundant states at twice the switching frequency increases the power losses and the stress of the high frequency switches, thus reducing the overall efficiency.

In comparison with [21,22], the single-phase (SP) ANPC-FL converter proposed in this paper is based on a novel topology consisting of ten switches instead of eight. However, with the addition of these two switches, it not only becomes capable of properly balancing the voltage of the DC-link split capacitors under different step-changing conditions but it achieves a better efficiency, a lower stress of the switching devices and a more even distribution of the power losses. Thanks to this voltage balancing, the power quality of the proposed ANPC-FL converter output voltage and in turn of the grid current are considerably enhanced during the G2V and V2G operation of the cascaded DAHB converter working as a bidirectional EV charger.

This paper is organized as follows: Section 2 describes the topology details of the proposed ANPC SPFLBC, its current flowing paths and its voltage balancing strategy. Section 3 examines the cascaded control strategy for the proposed grid-tied SPFLBC while analyzes the DAHB converter and its SPS control technique. Section 4 shows the transient and steady state simulation results obtained with MATLAB-SimPowerSystems whereas the experimental results obtained in laboratory are presented in Section 5. For this, several tests and measurements under different conditions have been carried out including also the power quality and power losses distribution analyses. Section 6 provides the discussion. Finally, the conclusion and some important remarks are given in Section 7.

2. Proposed Single-Phase ANPC Five-Level Bidirectional Converter

Figure 1 shows the three five-level ANPC topologies analyzed in this paper. It can be noted that the proposed topology has ten switches whereas the other two topologies have only eight. However, these two extra switches allow it to carry out a fairly good voltage balancing of the split capacitors not only in inverter (V2G) and rectifier (G2V) modes but also achieving a higher efficiency, a lower stress of the switching devices and a more even distribution of the power losses. The ANPC FL converter presented in [21] is uncapable of balancing the capacitors voltage since it simply does not have redundant vectors for the states that output half of the DC bus voltage. Regarding the topology presented in [22], it has four switches withstanding with the full DC bus voltage and although they switch at the low frequency of the modulating signal, the remaining switches operating at the switching frequency concentrate big stress and large power losses. Unlike [22], in the proposed topology there are only two switches that withstand with the full DC bus voltage while the power losses are lower and more evenly distributed. In high power applications, this represents the advantage of a lower stress in the power devices, thus making possible the utilization of MOSFETs inherently capable of switching more efficiently and at higher frequencies than IGBTs [23]. Table 1 shows a comparison of these three topologies in terms of the number of components and the voltage balancing characteristics.

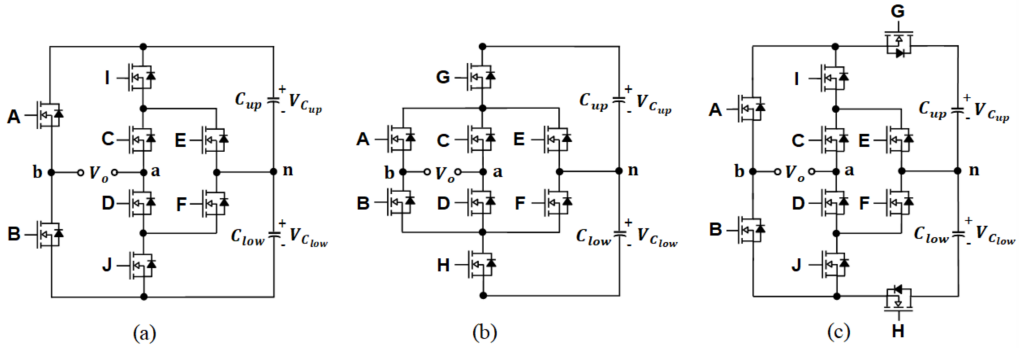

Figure 1. Topologies of single-phase ANPC five-level converters: (**a**) [21], (**b**) [22], (**c**) Proposed.

Table 1. Comparison of single-phase five-level ANPC topologies.

Five-Level ANPC Topology	Number of Components				Voltage Balancing		
	Split Capacitors	Power Switches	Clamping Diodes	Total	Capability	Stress	Efficiency
[21]	2	8	0	10	NO	LOWEST	HIGHEST
[22]	2	8	0	10	YES	HIGHEST	LOWEST
Proposed	2	10	0	12	YES	MIDDLE	MIDDLE

Current Flowing Paths of Proposed ANPC SPFLBC and Voltage Balancing Strategy of DC-Link Split Capacitors

Figure 2 shows the current flowing paths for the seven switching states of the proposed ANPC SPFLBC while Table 2 summarizes the states of the ten switches, the converter output voltage as well as the devised voltage balancing strategy. It can be noted that the unbalancing problem just arises in states where the current flowing path involves only one of the two capacitors, i.e., in states 2 and 4. This is because one of the capacitors charges/discharges and its voltage changes while the voltage of the other capacitor remains constant and unaltered. Given that in states 1 and 5, there is no neutral current and the same current flows through both capacitors, they charged/discharged equally and then there is no unbalancing.

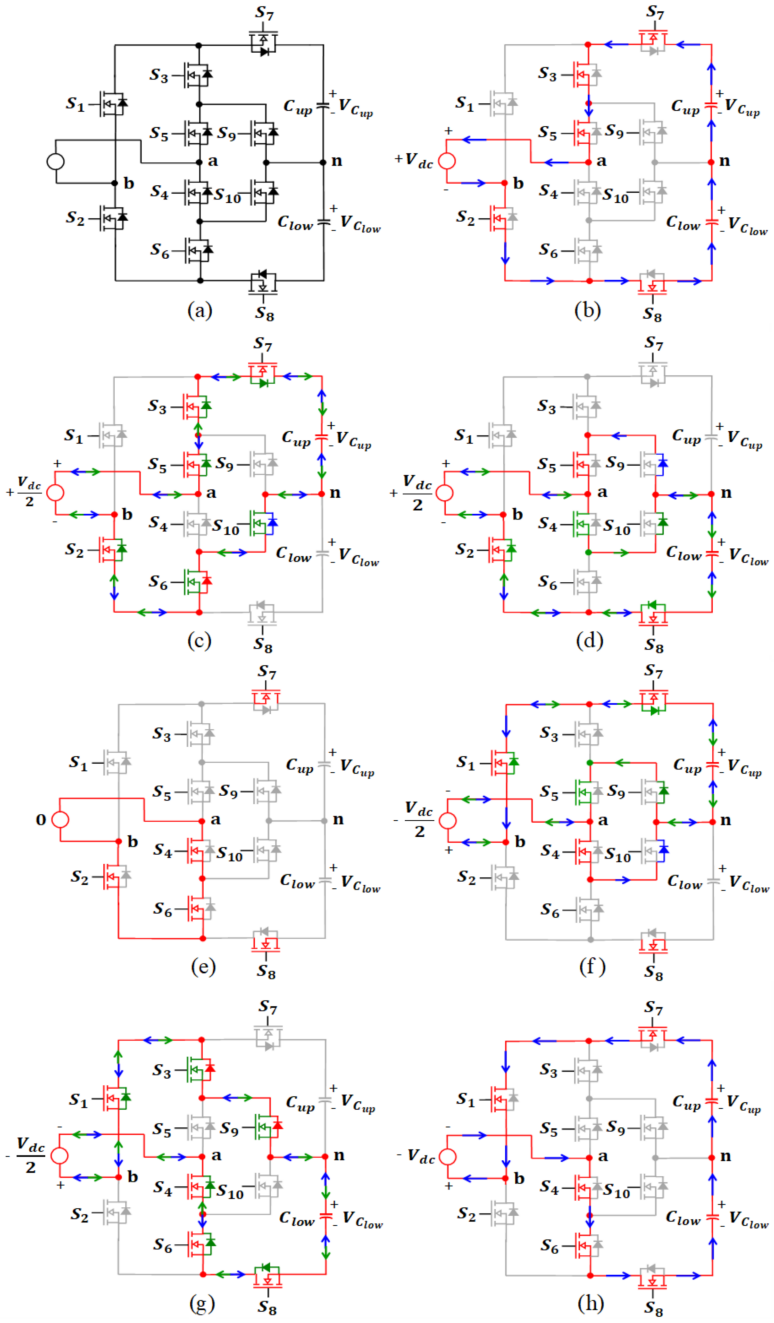

Figure 2. Current flowing paths for the seven switching states of the proposed ANPC SPFLBC. (**a**) Proposed topology, (**b**) State 1 $[+V_{dc}]$, (**c**) State 2U $[+V_{dc}/2]$ from upper capacitor, (**d**) State 2L $[+V_{dc}/2]$ from lower capacitor, (**e**) State 3 [0], (**f**) State 4U $[-V_{dc}/2]$ from upper capacitor, (**g**) State 4L $[-V_{dc}/2]$ from lower capacitor, (**h**) State 5 $[-V_{dc}]$.

Table 2. Switching states and voltage balancing strategy for the proposed ANPC SPFLBC.

Switching State	State of Switches										FLBC Output Voltage (V_{FLBC})	Voltage Balancing Algorithm Activated	Capacitors Unbalance Voltage (ΔV)$*[sgn(i_{bat})]$	FLBC Output Current (i_{FLBC}) $*[sgn(i_{bat})]$
	S_1	S_3	S_5	S_7	S_9	S_2	S_4	S_6	S_8	S_{10}				
1	0	1	1	1	0	1	0	0	1	0	$+V_{dc}$			
2U	0	1	1	1	0	1	0	1	0	1	$+V_{dc}/2$	YES	+	+
2L	0	0	1	0	0	1	1	0	1	0		NO/YES	OTHERWISE	
3	0	0	0	1	0	1	1	1	1	0	0			
4U	1	0	1	1	0	0	1	0	1	0	$-V_{dc}/2$	NO/YES	OTHERWISE	
4L	1	1	0	0	1	0	1	1	1	0		YES	−	−
5	1	0	0	1	0	0	1	1	1	0	$-V_{dc}$			

Likewise, in state 3, the split capacitors keep the same initial voltage since no current is flowing. For carrying out the balancing of the split capacitors in both inverter and rectifier modes, the following three factors have to be considered: (a) the voltage unbalance $\Delta V = V_{C_{up}} - V_{C_{low}}$, (b) the output current i_{FLBC} of the SPFLBC and (c) the current flow direction or sign (sgn) of the battery current i_{bat}. In state 2, if the balancing algorithm is activated and $\{(\Delta V) * [sgn(i_{bat})]\} \geq 0$ and $\{(i_{FLBC}) * [sgn(i_{bat})]\} \geq 0$, then the switching state 2U has to be applied, otherwise the 2L has to be selected. Similarly, in state 4, if the balancing algorithm is activated and $\{(\Delta V) * [sgn(i_{bat})]\} < 0$ and $\{(i_{FLBC}) * [sgn(i_{bat})]\} < 0$, then the switching state 4L has to be applied, otherwise the 4U has to be selected. By evaluating these simple conditions of Table 2, the proposed ANPC SPFLBC is capable of keeping the capacitors voltage at the same value even under step changing conditions of the battery current in V2G and G2V modes, under DC bus voltage sudden variations as well as under grid sags and swells phenomena as it will be demonstrated in simulation and experiments in Sections 4 and 5, respectively.

3. Control of Proposed Grid-Tied ANPC SP Five-Level Converter and Cascaded DAHBC

Figure 3 shows the block diagram of the proposed grid-tied ANPC SPFLBC and the EV charger based on the DAHB converter with HF isolation transformer. For ease of readability, the details of the cascaded control strategy block included in Figure 3 are shown in the diagram of Figure 4.

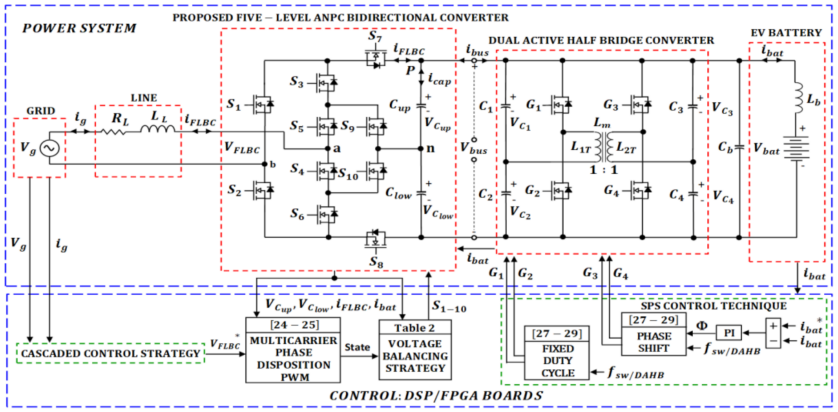

Figure 3. Block diagram of the proposed grid-tied ANPC SPFLBC, the cascaded DAHB converter as EV charger and their control strategies.

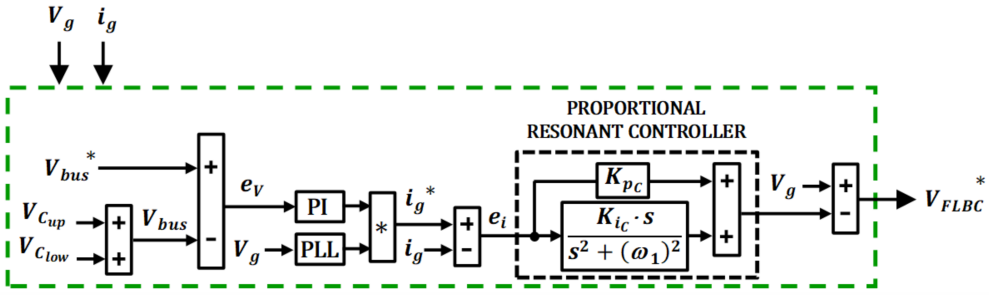

Figure 4. Detailed diagram of the cascaded control strategy block included in Figure 3.

Figure 5 shows the scheme of the cascaded control strategy carried out for regulating the DC bus voltage V_{bus} and the grid-current i_g using two controllers connected in series [24]. For this, the PLL first synchronizes with the grid voltage V_g and provides a unit sinusoidal reference signal. Then, it multiplies with the output from the $H_{C_V}(s)$ compensator of the outer voltage for generating the grid current reference $i_g{}^*$ that becomes the input of the cascaded current inner loop. Later, the output from the current compensator $H_i(s)$ is subtracted from the grid voltage for providing the reference $V_{FLBC}{}^*$ of the multicarrier phase-disposition PWM [24,25]. Finally, the resulting state is sent to the voltage balancing block that generates the ten switching signals S_{1-10} of the ANPC SPFLBC.

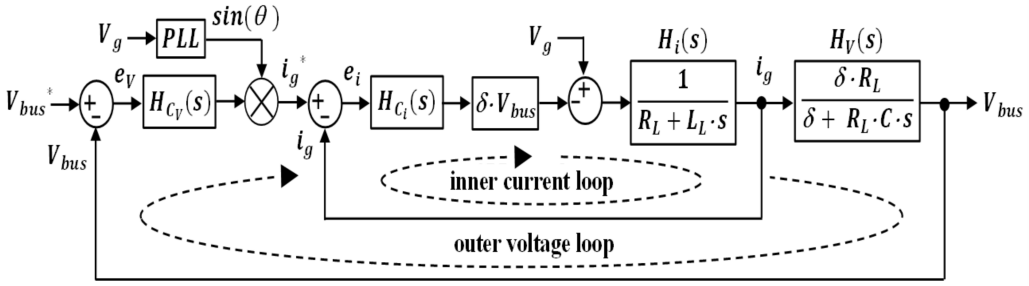

Figure 5. Block diagram of cascaded control strategy for the proposed grid-tied ANPC SPFLBC [24].

The maths behind the cascaded controller are described in the following. The outer loop voltage error e_V and the inner loop current error e_i are defined as:

$$e_V = V_{bus}{}^* - V_{bus} \tag{1}$$

$$e_i = i_g{}^* - i_g \tag{2}$$

where the superscript * means a reference signal. In the outer loop there is a proportional integral (PI) voltage compensator whereas in the inner loop there is a proportional-resonant (PR) current controller, respectively. By applying the Kirchhoff's voltage law (KVL) to the power circuit of Figure 3 consisting in the ANPC SPFLBC connected with the single-phase AC grid through an RL line, the following equation is obtained:

$$L_L \frac{di_g(t)}{dt} + R_L i_g(t) + V_{FLBC}(t) - V_g(t) = 0 \tag{3}$$

where the variables R_L and L_L represent the line resistance and line inductance while i_g, V_g and V_{FLBC} mean the grid current, the grid voltage and the ANPC SPFLBC output voltage, respectively. The converter output voltage can also be expressed as a function of the duty cycle δ as follows:

$$V_{FLBC}(t) = \delta(t) \cdot V_{bus}(t) \tag{4}$$

By substituting (4) in (3) and assuming an average value for the grid current and the respective duty cycle, the small signal model of the grid current is given by:

$$i_g(s) = \frac{V_g(s) - \delta \cdot V_{bus}(s)}{[R_L + L_L \cdot s]} \tag{5}$$

Assuming that the inner current loop is ten times faster than the outer voltage loop, V_g is seen as a constant value that does not vary with time and consequenlty $V_g(s) = 0$. Hence, the transfer function $H_i(s)$ for the inner current loop is written as:

$$H_i(s) = \frac{i_g(s)}{\delta} = \frac{-V_{bus}(s)}{[R_L + L_L \cdot s]} \tag{6}$$

Bearing in mind that the inner loop deals with the grid current that is an ac quantity, thus a proportional-resonant controller with a zero-steady state error and a theoretical infinite gain at the resonance frequency has been used [26]. The transfer function $H_{C_i}(s)$ of this current controller is given by:

$$H_{C_i}(s) = k_{p_C} + \frac{k_{i_C} \cdot s}{s^2 + {\omega_1}^2} \tag{7}$$

After applying the Kirchhoff's current law (KCL) at the node P in the power circuit of Figure 3, the following equations are obtained:

$$i_{bus}(t) - i_{cap}(t) - i_{FLBC}(t) = 0 \tag{8}$$

$$i_{bus}(t) = \delta(t) \cdot i_g(t) \tag{9}$$

$$i_{cap}(t) = C \cdot \frac{d[V_{bus}(t)]}{dt} \tag{10}$$

$$i_{FLBC}(t) = \frac{V_{FLBC}(t) - V_g(t)}{R_L} \tag{11}$$

where i_{cap} is the split capacitors current and $C = C_{up}/2 = C_{low}/2$. By substituting (4) into (11) and the resulting (9)–(11) into (8) while assuming an average value for the grid current and the duty cycle, the small signal model that links up the dc bus voltage with the grid current is found as:

$$\delta \cdot R_L \cdot i_g(s) - [R_L \cdot C \cdot V_{bus}(s)] \cdot s - V_{FLBC}(s) + V_g(s) = 0 \tag{12}$$

By considering in (12) the same assumption as in the inner loop, i.e., $V_g(s) = 0$, the transfer function $H_V(s)$ for the outer voltage loop is derived as:

$$H_V(s) = \frac{V_{bus}(s)}{i_g(s)} = \frac{\delta \cdot R_L}{[\delta + R_L \cdot C \cdot s]} \tag{13}$$

Bearing in mind that the outer loop deals with the bus voltage that is a dc quantity, thus a classical proportional-integral controller has been used. The transfer function $H_{C_V}(s)$ of this voltage controller is given by:

$$H_{C_V}(s) = k_{p_V} + \frac{k_{i_V}}{s} \tag{14}$$

By programming the transfer functions of the plants (6), (13) and the compensators (7), (14) in MATLAB code and using the single-input single-output (SISO) design tool, the gains of the controller have been accurately tuned until obtaining a good response [24].

Dual Active Half-Bridge DC-DC Converter

The EV bidirectional charger studied in this paper is based on the dual-active half-bridge DC-DC converter which has an advantageous isolation high-frequency transformer in between. As shown in Figure 3, the EV battery bank is connected on the low-voltage side of the DAHBC whereas the proposed ANPC SPFLBC is connected on the high-voltage side. The topology of this DAHB converter consists of one arm with two switches and another arm with two split capacitors. The set of these two arms are found at either side of the HF transformer [27]. The DAHBC can either increase or decrease the voltage from either side, thereby it is capable of working as a bidirectional Boost/Buck voltage converter. The direction and magnitude of the power flow is controlled by shifting the relative phase between the voltages on either side of the HF transformer. In comparison with the dual active full bridge converter (DAFBC), the DAHBC replaces four of its switches with four capacitors. This reduction in the number of power switches represents a limitation in terms of the available degrees of liberty for controlling the power flow. However, it becomes an important advantage regarding the inherent lower switching and conduction losses. Furthermore, in the DAHBC the unique four power switches available also experiment a lower stress since they have to endure only half of the DC bus voltage. Another advantage of this simplified topology is that in steady state, the magnetizing current of the HF transformer does not contain any dc component, thereby not increasing the core losses or giving rise to flux saturation [28].

The DAHB converter and its control blocks are shown in Figure 3. The switching signals G_1 and $G_2 = not(G_1) = \overline{G}_1$ as well as G_3 and $G_4 = not(G_3) = \overline{G}_3$ are obtained by comparing the triangular carrier signal $f_c = f_{sw}$ with zero, thus both sides of the DAHBC operate at a fixed-duty cycle of 50%. However, the phase of pulses G_3/G_4 are shifted with respect to G_1/G_2 within the SPS block in accordance to the desired battery current and its sign. During the V2G mode, the pulses G_1/G_2 lag G_3/G_4 whereas in the G2V mode, the pulses G_1/G_2 lead G_3/G_4. The current flowing paths for the different switching states of the DAHBC can be found in [29]. According to the experimental sizing of the ANPC SPFLBC, the DAHBC, the EV batteries bank and the variac connected to the grid, the main parameters of the HF transformer have been determined by simulation. Figure 6 shows the commercial off-the-shelf (COTS) HF transformer used in the prototype of the DAHBC built in the laboratory.

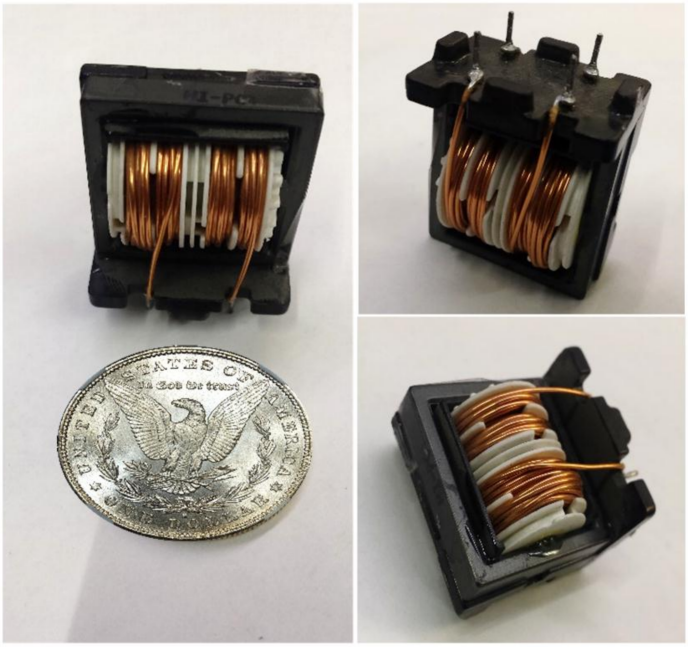

Figure 6. Various views of the HF transformer used in the DAHBC prototype and size comparison with a one-dollar morgan coin.

4. Simulation Results

With the aim of validating and evaluating the performance of the proposed grid-tied ANPC SPFLBC and the cascaded DAHBC, the full system presented in Figure 3 has been simulated in MATLAB-SimPowerSystems. For this, the following five tests have been carried out: (a) A step-change in the battery current under the V2G mode, (b) A step-change in the battery current under the G2V mode, (c) A grid voltage sag/swell under the V2G mode d) A DC bus voltage step-change under the G2V mode and (e) A swept of the capacitance of the DC-link split capacitors. The obtained results are presented in Figures 7–11.

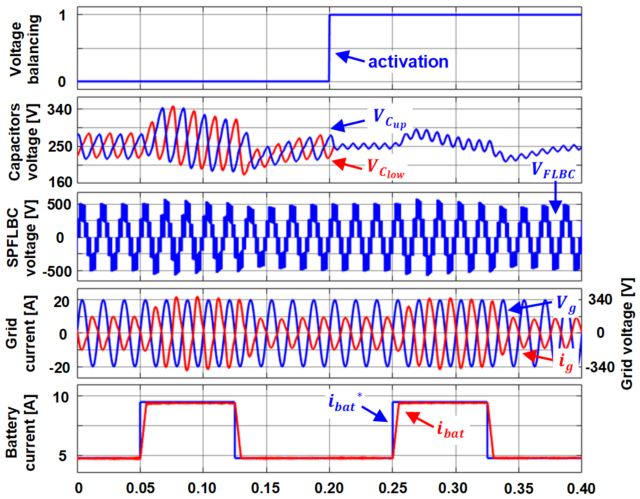

Figure 7. Performance of the voltage balancing strategy and the SPS control for the proposed grid-tied ANPC SPFLBC and the cascaded DAHBC during a step-change in the battery current under the V2G mode.

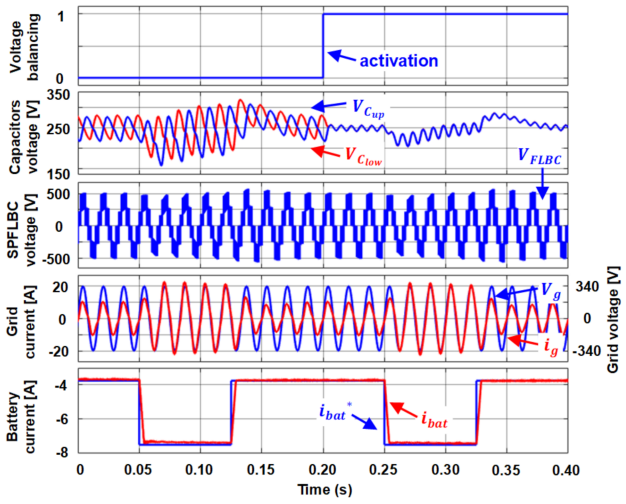

Figure 8. Performance of the voltage balancing strategy and the SPS control for the proposed grid-tied ANPC SPFLBC and the cascaded DAHBC during a step-change in the battery current under the G2V mode.

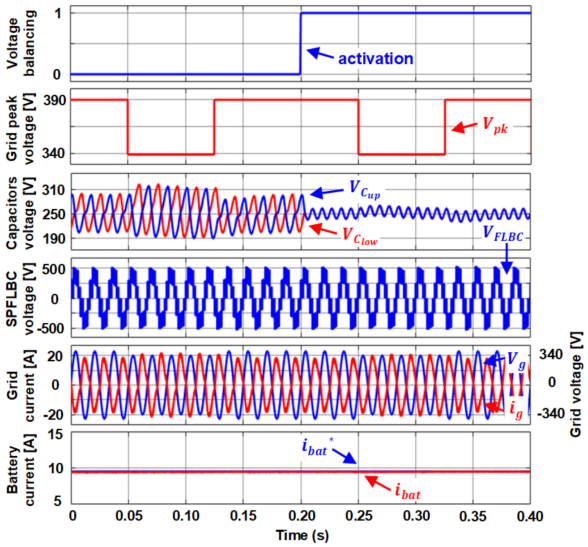

Figure 9. Performance of the voltage balancing strategy and the SPS control for the proposed grid-tied ANPC SPFLBC and the cascaded DAHBC during a grid voltage sag/swell under the V2G mode.

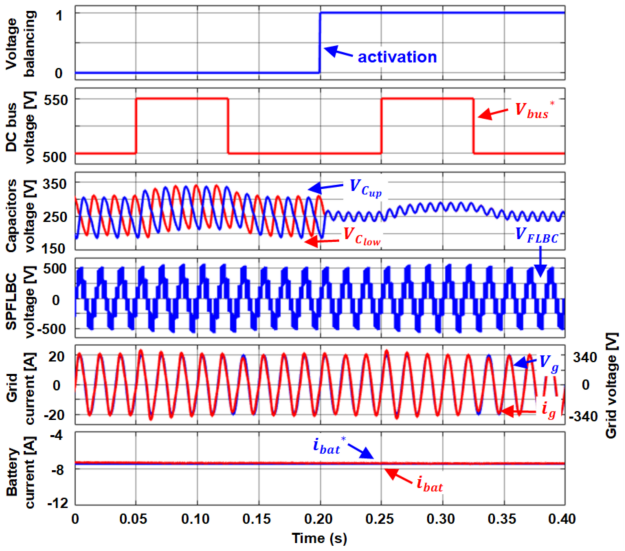

Figure 10. Performance of the voltage balancing strategy and the SPS control for the proposed grid-tied ANPC SPFLBC and the cascaded DAHBC during a DC bus voltage step-change under the G2V mode.

In the first test, as it is shown in Figure 7, the battery current reference $i_{bat}{}^*$ has been step-changed from +4.75 A to +9.5 A and back to +4.75 A after 75 ms. Bearing in mind that the sign of the battery current is positive, thus the power is flowing from the battery to the grid. i.e., V2G mode, and the grid current i_g is out-of-phase with the grid voltage V_g. It can be observed that from t = 0.2 s when the voltage balancing strategy is activated, the voltage of split capacitors becomes equal and thus the levels of the ANPC SPFLBC output voltage V_{FLBC} become symmetric and undistorted. Note also that the SPS control technique applied to the DAHBC properly regulates the battery current with a fast response, equivalent to a good dynamic on the grid side. The DC bus voltage is alike fairly good maintained at 500 V in spite of the abrupt changes in the current flowing through the five-level converter.

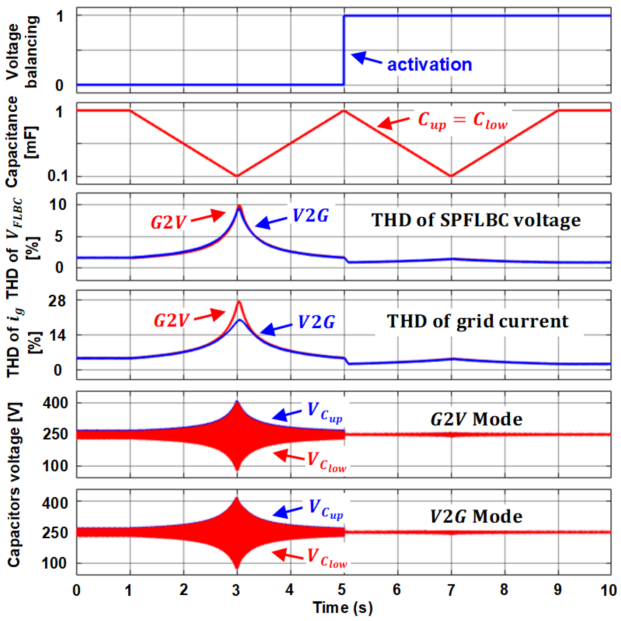

Figure 11. Dynamic response of the voltage balancing strategy and the vector control for the proposed grid-tied ANPC SPFLBC and the cascaded DAHBC during a swept of the capacitance of the DC-link split capacitors.

In the second test, as it is shown in Figure 8, $i_{bat}{}^*$ has been step-changed from −3.75 A to −7.5 A and back to −3.75 A after 75 ms. Bearing in mind that the sign of the battery current is negative, thus the power is flowing from the grid to the battery. i.e., G2V mode, and the grid current i_g is in-phase with the grid voltage V_g. Note that the −7.5 A from the battery is equivalent to a grid current with a peak value of around 20 A. This is due to the different voltage ratio between the DC bus and the AC grid. The parameters of the simulated and the experimental prototype can be consulted in Table 3. As in the V2G mode, the voltage balancing alike improves the power quality of V_{FLBC} and in turn of i_g while the DC bus voltage and the battery current are properly controlled.

In the third test, as it is shown in Figure 9, $i_{bat}{}^*$ is kept constant at +9.5 A (V2G mode) while the peak value of the grid voltage is first decreased from 390 V to 340 V and later increased back to 390 V. These sag and swell are equivalent to 12.8% and 14.7%, respectively. It can be noted how before t = 0.2 s, the voltage unbalance increases with the grid voltage reduction. However, once the voltage balancing strategy is activated, it makes equal the voltages of the upper $V_{C_{up}}$ and lower $V_{C_{low}}$ capacitors in spite of the grid voltage variations. Additionally, the effect on the DC bus voltage regulation becomes negligible.

In the fourth test, as it is shown in Figure 10, $i_{bat}{}^*$ is kept constant at −7.50 A (G2V mode) while the DC bus voltage reference $V_{bus}{}^*$ is step-changed from 500V to 550 V and back to 500 V. These variations are equivalent to 10% and 9.1%, respectively. As in the previous tests, the voltage balancing strategy also makes that the split capacitors voltages accurately match, and in turn it allows achieving a fairly good symmetry of V_{FLBC} and a considerable reduction in the harmonic distortion of i_g.

In the fifth test, as it is shown in Figure 11, the capacitance of the DC-link split capacitors $C_{up} = C_{low}$ has been linearly varied following the profile of a triangular wave with peak values of 1 mF and 100 µF. The total harmonic distortion (THD) as well as the split capacitors voltage waveforms for the V2G and G2V modes have been obtained with a battery current refence $i_{bat}{}^*$ of +9.5 A and −7.5 A, respectively. It can be observed that the highest THD and maximum capacitors unbalance occur when the capacitance is minimum, i.e., at 100 µF. However, it is important to remark how even under the worst conditions in both operation modes, the proposed voltage balancing strategy significantly narrows the capacitors voltage difference from around 200 V to less than 6 V. In the same way, the maximum THD of V_{FLBC} in the V2G and G2V operations modes quite decreases

from 9.4% and 10.0% to around 1.5% in both cases. Likewise, the highest THD of i_g in the V2G and G2V operation modes fairly reduces from 19.9% and 27.4% to only 4.3% and 4.5%, respectively.

Table 3. Parameters of simulation and experimental grid-tied ANPC SPFLBC and cascaded DAHBC.

Parameter	Symbol	Value		Units
		Simulation	Experimental	
Switching frequency of FLBC	$f_{sw/FLBC}$	5	5	kHz
Switching frequency of DAHB	$f_{sw/DAHB}$	50	10	
Line resistance	R_L	0.1	0.1	Ω
Line inductance	L_L	5	2.5	mH
HF transformer magnetization inductance	L_m	10	8.3	
HF transformer leakage inductances	L_{1T}, L_{2T}	0.01	0.082	
Inductance of the battery inductor	L_b	50	5	
Grid voltage (peak)	V_g	340	21 | 7 *	V
DC bus voltage	V_{bus}	500	24	
Battery nominal voltage	$V_{bat/nom}$	360	22	
Battery rated current capacity	$I_{bat/Ah}$	66	120	Ah
Grid frequency	f_g	60	60	Hz
Capacitance of FLBC split capacitors	C_{up}, C_{low}	350	128	μF
Capacitance of DAHB split capacitors	C_1, C_2	350	680	
	C_3, C_4	10	165	
Capacitance of battery side capacitor	C_b	1	100	
Sampling time/Time-step	T_s	20	100	μs

* Note: The grid voltage V_g is 21V in the G2V mode and 7V in the V2G mode, respectively.

5. Experimental Results

In order to validate and evaluate the performance of the voltage balancing and cascaded control strategies for the proposed grid-tied SPFLBC as well as of the SPS technique for the battery current control through the DAHBC, they have been built and tested on the same basis of the simulations described in Section 4. The parameters of these converters are summarized in Table 3. Figure 12 shows a photograph of the full experimental setup built in laboratory whereas Figures 13–19 show the obtained results.

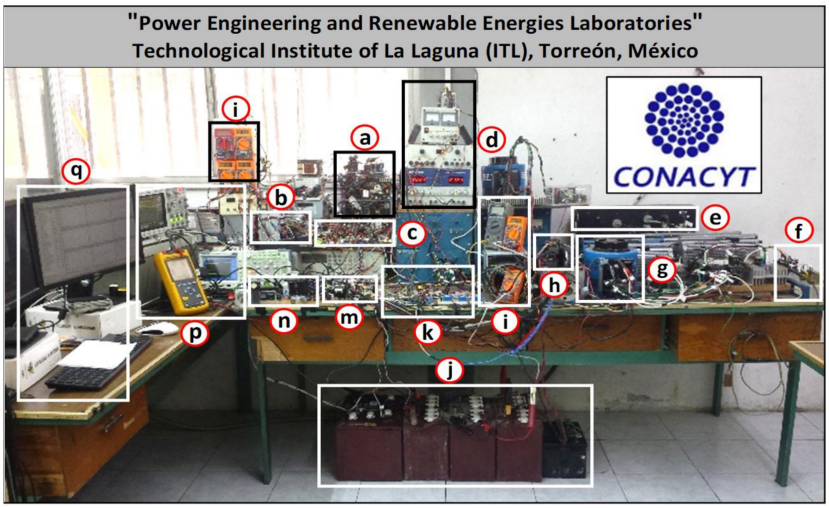

Figure 12. Experimental setup built in the laboratory: (**a**) Novel single-phase ANPC five-level bidirectional converter, (**b**) Dual active half-bridge DC-DC converter, (**c**) Drivers of power converters, (**d**) Auxiliary DC voltage sources, (**e**) Grid connectors board, (**f**) Line inductor, (**g**) Grid variable autotransformer, (**h**) Tektronix Hall current probes, (**i**) Multimeters, (**j**) Lead-acid rechargeable battery bank, (**k**) Voltage/current Hall sensors and signal conditioning stage, (**m**) DSP/FPGA-based control cards, (**n**) Control dashboard, (**p**) Tektronix/Agilent digital scopes and Fluke 43B, (**q**) PC-Windows 10/i7/8Gb RAM.

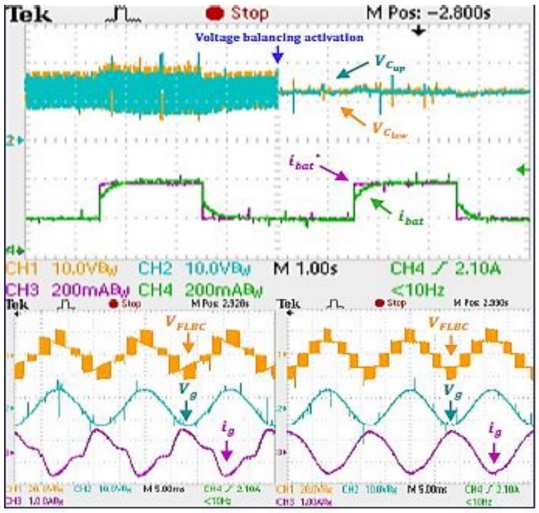

Figure 13. Performance of the voltage balancing strategy and the SPS control for the proposed grid-tied ANPC SPFLBC and the cascaded DAHBC during a step-change in the battery current under the V2G mode.

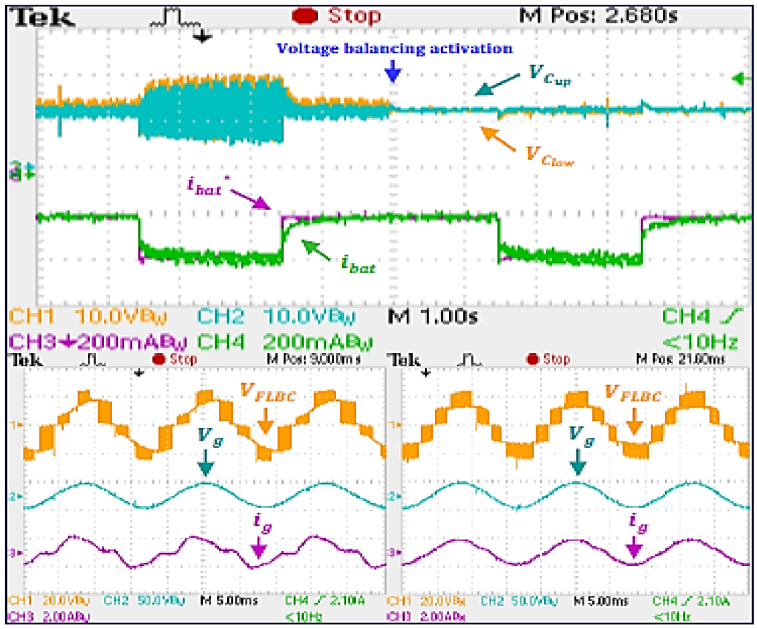

Figure 14. Performance of the voltage balancing strategy and the SPS control for the proposed grid-tied ANPC SPFLBC and the cascaded DAHBC during a step-change in the battery current under the G2V mode.

Figure 13 shows the performance of the ANPC SPFLBC and the DAHBC during a step-change in the battery current under the V2G mode. At t = 1.5 s, the battery current reference $i_{bat}{}^*$ is changed from +0.175 A to +0.350 A and back to +0.175 A after 2 s. This sequence repeats at half the full-time scale, i.e., at t = 5 s when the voltage balancing is activated. It can be observed how the voltage unbalance of split capacitors increases with the battery current. However, the voltage balancing strategy is very effective by making practically equals the voltages of the upper capacitor $V_{C_{up}}$ and the lower capacitor $V_{C_{low}}$.

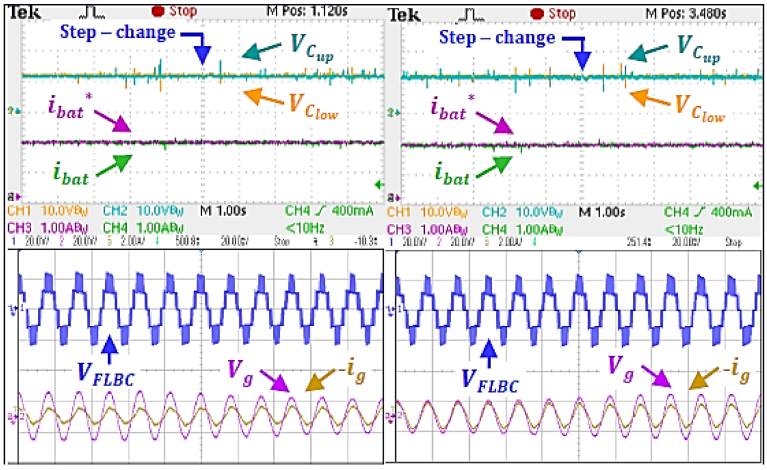

Figure 15. Performance of the voltage balancing strategy and the SPS control for the proposed grid-tied ANPC SPFLBC and the cascaded DAHBC during a grid voltage sag/swell under the V2G mode.

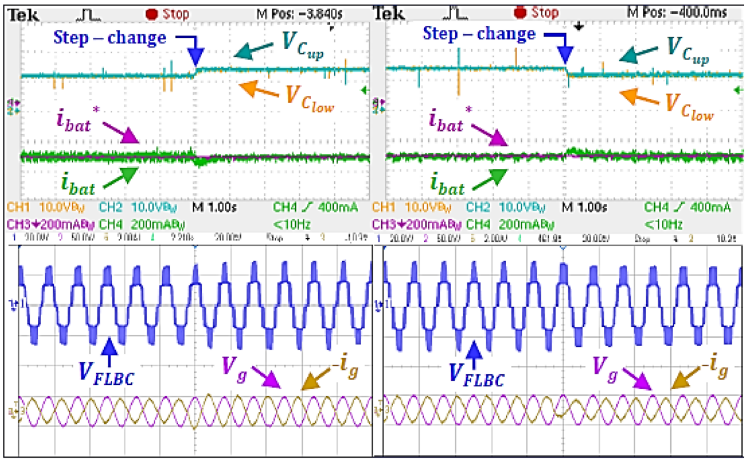

Figure 16. Performance of the voltage balancing strategy and the SPS control for the proposed grid-tied ANPC SPFLBC and the cascaded DAHBC during a DC bus voltage step-change under the G2V mode.

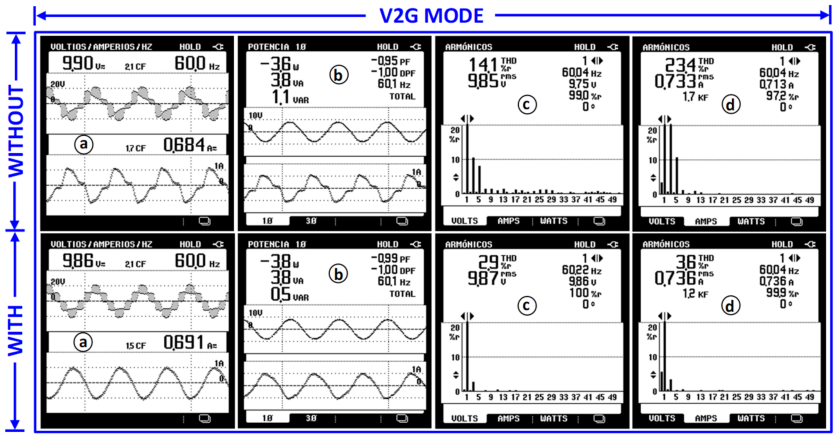

Figure 17. Fluke 43B-based power quality analysis of proposed grid-tied ANPC SPFLBC without (Top) and with (Bottom) DC-link split capacitors voltage balancing under the V2G mode. (**a**) SPFLBC output voltage V_{FLBC} and grid current i_g. (**b**) Grid powers, grid factors, V_g and i_g. (**c**) Spectrum of V_{FLBC}. (**d**) Spectrum of i_g.

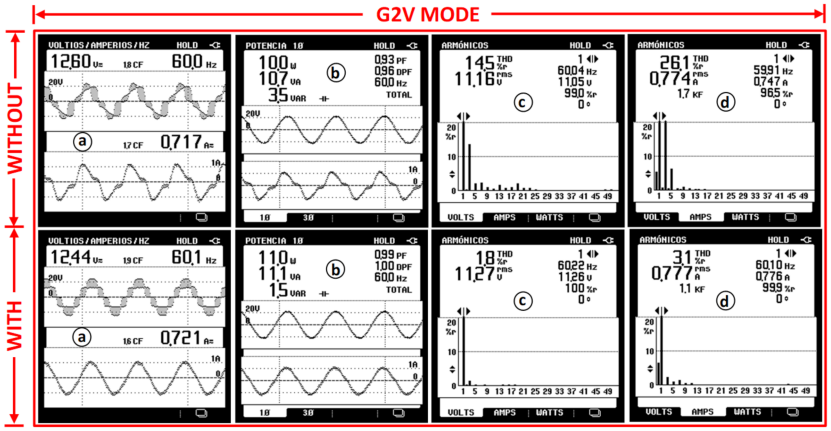

Figure 18. Fluke 43B-based power quality analysis of proposed grid-tied ANPC SPFLBC without (top) and with (bottom) DC-link split capacitors voltage balancing under the G2V mode. (**a**) SPFLBC output voltage V_{FLBC} and grid current i_g. (**b**) Grid powers, grid factors, V_g and i_g. (**c**) Spectrum of V_{FLBC}. (**d**) Spectrum of i_g.

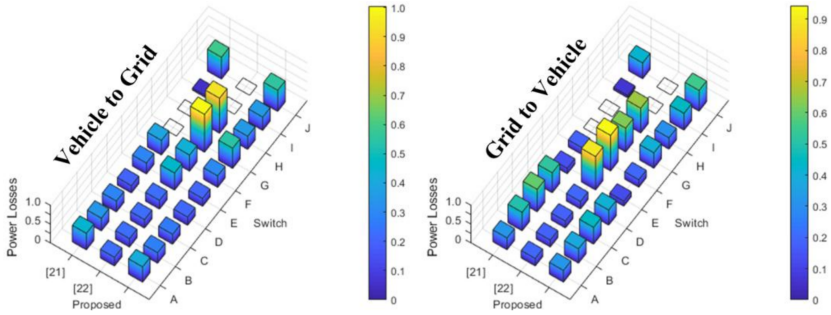

Figure 19. Normalized power losses distribution for the three different single-phase ANPC five-level topologies under study. (**Left**) V2G mode. (**Right**) G2V mode.

During this time, the DC bus voltage is accurately maintained at 24V in spite of the disturbances caused by the sudden variations in the current flow from the battery to the grid. It can also be noted that initially the output voltage waveform from the ANPC SPFLBC is asymmetric due to the unbalance in states 2 and 4 while the grid current is severely distorted. Thanks to the proposed voltage balancing, the ANPC SPFLBC provides a voltage signal with high symmetry that in turn allows flowing a high-quality grid current with very low harmonic content. Furthermore, i_g accurately remains out-of-phase with the grid voltage V_g since the grid is receiving the power from the battery. It is important to clarify that the voltage and current spikes observed in the waveforms do not belong to the real measurements but to the EMI induced in the probes of the TPS2024B Tektronix scope. Given that this instrument does not incorporate any kind of filtering, the displayed signals are purely raw.

Figure 14 shows the performance of the ANPC SPFLBC and the DAHBC during a step-change in the battery current under the G2V mode. At t = 1.5s, the battery current reference $i_{bat}{}^*$ is changed from -0.175 A to -0.350 A and back to -0.175 A after 2 s. It is noteworthy how after the activation of the voltage balancing strategy at t = 5 s, the voltage of split capacitors properly overlaps, the ANPC SPFLBC output voltage becomes symmetric and the grid current distortion fairly reduces. Also, i_g accurately remains in-phase with the grid voltage V_g since now the grid is sending the power to the battery.

Figure 15 shows the performance of the ANPC SPFLBC and the DAHBC during a grid voltage sag/swell under the V2G mode. The grid voltage variations have peak values of 15 V and 11 V. Therefore, the tested sag and swell are of approximately 27% and 36%, respectively. During the test the voltage balancing strategy is always on while the DC bus

voltage reference $V_{bus}{}^*$ and the battery current reference $i_{bat}{}^*$ remain at 24 V and +0.35 A, respectively. It is noteworthy how both of the split capacitors stay all the time at the same voltage in spite of the sag/swell disturbances, hence the SPFLBC continuously provides an output voltage with high symmetry and low distortion. It is also remarkable that the voltage sag as well as the voltage swell have an unnoticeable effect on the DC bus voltage regulation and the battery current control.

Figure 16 shows the performance of the ANPC SPFLBC and the DAHBC during a DC bus voltage step-change under the G2V mode. During the test the voltage balancing strategy is always on while the peak value of the grid voltage V_g and the battery current reference $i_{bat}{}^*$ remain at 25 V and −0.35 A, respectively. First, the DC bus voltage is increased from 24 V to 29 V and later decreased from 29 V to 24 V. These variations are equivalent to 21% and 17%, respectively. It is noteworthy how the DC bus voltage step-changes have a negligible influence on the battery current regulation and practically no effect on the voltage balancing of split capacitors. Thus, the SPFLBC output voltage always remains symmetric while the amplitude of its levels simply changes accordingly.

Figures 17 and 18 show the experimental results obtained from the power quality analysis of the ANPC SPFLBC output voltage V_{FLBC} as well as of the grid current i_g for the V2G and G2V operation modes. In each of these figures, the time signals and their resulting spectra are compared without and with the activation of the proposed voltage balancing strategy. It can be observed how in both V2G and G2V modes, when the voltage balancing strategy is off, the signals V_{FLBC} and i_g are severely distorted, the levels of V_{FLBC} are fairly unequal and the power factor is very poor. Once the voltage balancing is on, the following improvement are obtained: (a) In the V2G mode, the THD of V_{FLBC} and i_g reduces from 14.1% and 23.4% to only 2.9% and 3.6%, respectively, whereas in the G2V mode, it reduces from 14.5% and 26.1% to only 1.8% and 3.1%, respectively. (b) In the V2G mode, the reactive power reduces from 1.1 Vars to 0.5 Vars whereas in the G2 V mode, it reduces from 3.5 Vars to only 1.5 Vars. (c) In the V2G mode, the power factor increases from −0.95 to −0.99 whereas in the G2V mode, it increases from 0.93 to 0.99. In general, it is noteworthy that when the voltage balancing is on, the levels of V_{FLBC} become symmetric, the harmonic content of V_{FLBC} and i_g fairly reduces, the reactive power on the grid side decreases and the power factor notably improves.

The power losses distribution and the efficiency for the three different single-phase ANPC five-level topologies under study are shown in Figure 19 and Table 4, respectively. For ease of comparison, the set of graphs in both V2G and G2V modes has been normalized while the notation of the switches match with the letters A-J used in topologies of Figure 1. It can be observed that the ANPC-FLC of [21] with only eight switches is the more efficient with 96.4% in the V2G mode and 95.8% in the G2V mode. In spite of presenting the lower power losses, this topology is inherently uncapable of balancing the voltage of split capacitors because it does not count with redundant vectors for the states that generate an output of half the DC bus voltage.

Table 4. Comparison of efficiency for different five-level ANPC topologies.

Five-Level ANPC Topology	Efficiency (%)	
	V2G	G2V
[21]	96.4	95.8
[22]	93.5	94.1
Proposed	95.0	94.5

Unlike [21], the ANPC-FLC of [22] having also eight switches is capable of properly balancing the capacitors voltage. Nevertheless, although in this converter the four switches A–D that withstand the full DC bus voltage commutate at low frequency, such topology presents the lower efficiency due to the higher stress in the remaining switches, i.e., G-H in

the V2G mode and E-F in the G2V mode. According to Table 4, its efficiency in the V2G and G2V modes is 93.5% and 94.1%, respectively.

In comparison with [21,22], the proposed ANPC-FLBC has two more switches, i.e., a total of ten. However, unlike [21] it is capable of balancing the capacitors voltage whereas in contrast with [22], it not only achieves a better efficiency but a lower stress of the switching devices and a more even distribution of the power losses. The efficiency of the proposed topology is 95.0% in the V2G mode and 94.5% in the G2V mode.

6. Discussion

In comparison with the conventional two-level converters, the multilevel converters are characterized for providing a lower distortion voltage signal and achieve it with lower switching frequencies. These are two big advantages in terms of a lower cost and volume of the required output passive filter as well as a switching losses reduction. Thus, with the aim of increasing the efficiency of multilevel converters, the switching frequency must be kept low but not too much because it can deteriorate the fundamental output signal used for control purposes and compromise the performance of the converter application. In the present work, the switching frequency $f_{sw/FLBC}$ of the FLBC has been set to 5 kHz in both simulation and experiments. The results shown in Sections 4 and 5 validate the selection of this frequency by obtaining a good control performance and an efficiency even higher than with the topology proposed in [22]. A summary of the parameters for the proposed grid-tied ANPC SPFLBC is shown in Table 3. The selection of $f_{sw/FLBC}$ is also based on [24]. This research works deals with a single-phase five-level converter that implements the same multicarrier phase disposition method used in the present paper.

The parameter discrepancies and drifts due to temperature and aging of the inductive and capacitive components in the power system shown in Figure 3 do not have an influence on the accuracy and performance of the proposed voltage balancing strategy. Nevertheless, the gain and offset of the Hall-effect voltage sensors used for measuring the voltage of the upper and lower capacitors have a significant effect on the voltage balancing. In the same way, the parameter variations due to temperature in the resistors connected to the operational amplifiers in turn contained within the signal conditioning stage that interfaces the Hall-effect voltage sensors with the analog-to-digital converters of the DSP alike affect the voltage balancing.

With the aim of providing accurate voltage measurements of the split capacitors to the voltage balancing control loop, a digital calibration curve that compensates the nonlinearity and gain mismatch from the voltage sensors as well as an automatic routine that digitally removes their initial voltage offsets have been programmed within the DSP. It important to remark that before taking the initial voltage measurements, the split capacitors are first discharged through a resistor. In spite that the experimental results presented in Section 5 were obtained at various times in different days as well as under different conditions and scenarios, they exhibited repeatability since the initialization routine has been always performed before starting up the ANPC SPFLBC. Thanks to the nonlinearity, gain mismatch and offset compensations carried out on the voltage sensors, the remaining parameters variations undergone by the full power system during the days of tests have been minor and practically unnoticeable.

7. Conclusions

A novel single-phase ANPC SPFLBC that enhances the power quality during the G2V and V2G operation of a cascaded EV charger has been presented in this paper. The simulation and experimental results obtained from a set of exhaustive tests validate the good performance of the developed balancing strategy for keeping equal the split capacitors voltages even under step-changing disturbances. In the same way, the cascaded control and the SPS control strategies implemented with a DSP/FPGA for controlling in real-time the grid-tied ANPC SPFLBC and the DAHBC have alike shown a good performance. It has been also demonstrated that the proposed grid-tied ANPC SPFLBC not only is capable

of achieving a very low THD of the grid current but a higher efficiency, a lower stress of the switching devices and a more even distribution of the power losses in both V2G and G2V modes.

Author Contributions: Conceptualization, J.L., L.M., C.H., M.A.A. and A.C.; Formal analysis, J.L., L.M., C.H., M.A.A. and A.C.; Investigation, J.L., L.M., C.H., M.A.A. and A.C.; Methodology, J.L., L.M., C.H., M.A.A. and A.C.; Validation, J.L., L.M., C.H., M.A.A. and A.C.; Writing—review & editing, J.L., L.M., C.H., M.A.A. and A.C. All authors have read and agreed to the published version of the manuscript.

Funding: This work was funded by the National Council of Science and Technology of Mexico (CONACYT) through its "Postdoctoral Fellowship Program" under grants 2019-000006-01NACV-00062 and 2020-000022-01NACV-00108.

Institutional Review Board Statement: Not Applicable.

Informed Consent Statement: Not Applicable.

Data Availability Statement: Not Applicable.

Acknowledgments: Authors would like to thank TNM Instituto Tecnológico de La Laguna for its partial support in this research.

Conflicts of Interest: Authors declare no conflicts of interest.

References

1. Cheng, M.; Tong, M. Development status and trend of electric vehicles in China. *Chin. J. Electr. Eng.* **2017**, *3*, 1–13.
2. Falahi, M.; Chou, H.-M.; Ehsani, M.; Xie, L.; Butler-Purry, K.L. Potential Power Quality Benefits of Electric Vehicles. *IEEE Trans. Sustain. Energy* **2013**, *4*, 1–8. [CrossRef]
3. Mude, K.N. Battery charging method for electric vehicles: From wired to on-road wireless charging. *Chin. J. Electr. Eng.* **2018**, *4*, 1–15. [CrossRef]
4. Kwon, M.; Jung, S.; Choi, S. A high efficiency bi-directional EV charger with seamless mode transfer for V2G and V2H ap-plication. In Proceedings of the IEEE Energy Conversion Congress and Exposition (ECCE), Montreal, QC, Canada, 20–24 September 2015; pp. 5394–5399.
5. Zgheib, R.; Al-Haddad, K.; Kamwa, I. V2G, G2V and active filter operation of a bidirectional battery charger for electric vehicles. In Proceedings of the 2016 IEEE International Conference on Industrial Technology (ICIT), Taipei, Taiwan, 14–17 March 2016; pp. 1260–1265.
6. Verma, A.; Singh, B. AFF-SOGI-DRC Control of Renewable Energy Based Grid Interactive Charging Station for EV with Power Quality Improvement. *IEEE Trans. Ind. Appl.* **2021**, *57*, 588–597. [CrossRef]
7. Yilmaz, M.; Krein, P.T. Review of Battery Charger Topologies, Charging Power Levels, and Infrastructure for Plug-In Electric and Hybrid Vehicles. *IEEE Trans. Power Electron.* **2013**, *28*, 2151–2169. [CrossRef]
8. Tian, Q.; Bai, K. Widen the zero-voltage-switching range and secure grid power quality for an ev charger using variable-switching-frequency single-dual-phase-shift control. *Chin. J. Electr. Eng.* **2018**, *4*, 11–19.
9. Sha, D.; Xu, G.; Xu, Y. Utility Direct Interfaced Charger/Discharger Employing Unified Voltage Balance Control for Cascaded H-Bridge Units and Decentralized Control for CF-DAB Modules. *IEEE Trans. Ind. Electron.* **2017**, *64*, 7831–7841. [CrossRef]
10. Zhao, B.; Song, Q.; Liu, W.; Sun, Y. Overview of Dual-Active-Bridge Isolated Bidirectional DC–DC Converter for High-Frequency-Link Power-Conversion System. *IEEE Trans. Power Electron.* **2013**, *29*, 4091–4106. [CrossRef]
11. He, P.; Khaligh, A. Comprehensive Analyses and Comparison of 1 kW Isolated DC–DC Converters for Bidirectional EV Charging Systems. *IEEE Trans. Transp. Electrif.* **2017**, *3*, 147–156. [CrossRef]
12. Brenna, M.; Foiadelli, F.; Longo, M. The Exploitation of Vehicle-to-Grid Function for Power Quality Improvement in a Smart Grid. *IEEE Trans. Intell. Transp. Syst.* **2014**, *15*, 2169–2177. [CrossRef]
13. Fard, M.T.; Abarzadeh, M.; Noghani, K.A.; He, J.; Al-Haddad, K. Si/SiC hybrid 5-level active NPC inverter for electric air-craft propulsion drive applications. *Chin. J. Electr. Eng.* **2020**, *6*, 63–76. [CrossRef]
14. Abarzadeh, M.; Vahedi, H.; Al-Haddad, K. Fast sensor-less voltage balancing and capacitor size reduction in PUC5 converter using novel modulation method. *IEEE Trans. Ind. Inform.* **2019**, *15*, 4394–4406. [CrossRef]
15. Onar, O.C.; Kobayashi, J.; Erb, D.C.; Khaligh, A. A bidirectional high-power-quality grid interface with a novel bidirectional noninverted buck–boost converter for PHEVs. *IEEE Trans. Veh. Technol.* **2012**, *61*, 2018–2032. [CrossRef]
16. Awal, M.A.; Bipu, R.H.; Montes, O.A.; Feng, H.; Husain, I.; Yu, W.; Lukic, S. Capacitor Voltage Balancing for Neutral Point Clamped Dual Active Bridge Converters. *IEEE Trans. Power Electron.* **2020**, *35*, 11267–11276. [CrossRef]
17. Filba-Martinez, A.; Busquets-Monge, S.; Bordonau, J. Modulation and Capacitor Voltage Balancing Control of Multilevel NPC Dual Active Bridge DC–DC Converters. *IEEE Trans. Ind. Electron.* **2019**, *67*, 2499–2510. [CrossRef]

18. Moonem, M.; Duman, T.; Krishnaswami, H. Capacitor voltage balancing in a neutral-point clamped multilevel dc-dc dual active bridge converter. In Proceedings of the 2017 IEEE 8th International Symposium on Power Electronics for Distributed Generation Systems (PEDG), Florianopolis, Brazil, 17–20 April 2017; pp. 1–7.
19. Khan, S.A.; Islam, R.; Guo, Y.; Zhu, J. An Amorphous Alloy Magnetic-Bus-Based SiC NPC Converter with Inherent Voltage Balancing for Grid-Connected Renewable Energy Systems. *IEEE Trans. Appl. Supercond.* **2018**, *29*, 1–8. [CrossRef]
20. Sivakumar, K. A Fault-Tolerant Single-Phase Five-Level Inverter for Grid-Independent PV Systems. *IEEE Trans. Ind. Electron.* **2015**, *62*, 7569–7577. [CrossRef]
21. Zhang, L.; Zheng, Z.; Li, C.; Ju, P.; Wu, F.; Gu, Y.; Chen, G. A Si/SiC hybrid five-level active NPC inverter with improved modulation scheme. *IEEE Trans. Power Electron.* **2020**, *35*, 4835–4846. [CrossRef]
22. Ruiz-Caballero, D.A.; Ramos-Astudillo, R.M.; Mussa, S.A.; Heldwein, M.L. Symmetrical hybrid multilevel DC–AC converters with reduced number of insulated DC supplies. *IEEE Trans. Ind. Electron.* **2010**, *57*, 2307–2314. [CrossRef]
23. Buticchi, G.; Lorenzani, E.; Franceschini, G. A Five-Level Single-Phase Grid-Connected Converter for Renewable Distributed Systems. *IEEE Trans. Ind. Electron.* **2013**, *60*, 906–918. [CrossRef]
24. Vahedi, H.; Shojaei, A.A.; Chandra, A.; Al-Haddad, K. Five-Level Reduced-Switch-Count Boost PFC Rectifier with Multicarrier PWM. *IEEE Trans. Ind. Appl.* **2016**, *52*, 4201–4207. [CrossRef]
25. Calais, M.; Borle, L.J.; Agelidis, V.G. Analysis of multicarrier PWM methods for a single-phase five level inverter. In Proceedings of the 2001 IEEE 32nd Annual Power Electronics Specialists Conference (IEEE Cat. No.01CH37230), Vancouver, BC, Canada, 17–21 June 2001; pp. 1351–1356.
26. Teodorescu, R.; Blaabjerg, F.; Liserre, M.; Loh, P.C. Proportional-resonant controllers and filters for grid-connected voltage-source converters. *IEE Proc. Electr. Power Appl.* **2006**, *153*, 750–762. [CrossRef]
27. Fan, H.; Li, H. High-Frequency Transformer Isolated Bidirectional DC–DC Converter Modules with High Efficiency over Wide Load Range for 20 kVA Solid-State Transformer. *IEEE Trans. Power Electron.* **2011**, *26*, 3599–3608. [CrossRef]
28. Chakraborty, S.; Chattopadhyay, S. Minimum-RMS-Current Operation of Asymmetric Dual Active Half-Bridge Converters with and Without ZVS. *IEEE Trans. Power Electron.* **2016**, *32*, 5132–5145. [CrossRef]
29. Ngo, T.; Won, J.; Nam, K. A single-phase bidirectional dual active half-bridge converter. In Proceedings of the 2012 Twenty-Seventh Annual IEEE Applied Power Electronics Conference and Exposition (APEC), Orlando, FL, USA, 5–9 February 2012; pp. 1127–1133.