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Hybrid DC-DC Converter with Low Switching Loss, Low Primary Current and Wide Voltage Operation

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Abstract: A full-bridge converter with an additional resonant circuit and variable secondary turns is presented and achieved to have soft-switching operation on active devices, wide voltage input operation and low freewheeling current loss. The resonant tank is linked to the lagging-leg of the full bridge pulse-width modulation converter to realize zero-voltage switching (ZVS) characteristic on the power switches. Therefore, the wide ZVS operation can be accomplished in the presented circuit over the whole input voltage range and output load. To overcome the wide voltage variation on renewable energy applications such as DC wind power and solar power conversion, two winding sets are used on the output-side of the proposed converter to obtain the different voltage gains. Therefore, the wide voltage input from 90 to 450 V ($V_{in,max} = 5V_{in,min}$) is implemented in the presented circuit. To further improve the freewheeling current loss issue in the conventional phase-shift pulse-width modulation converter, an auxiliary DC voltage generated from the resonant circuit is adopted to reduce this freewheeling current loss. Compared to the multi-stage DC converters with wide input voltage range operation, the proposed circuit has a low freewheeling current loss, low switching loss and a simple control algorithm. The studied circuit is tested and the experimental results are demonstrated to testify the performance of the resented circuit.

Keywords: phase-shift PWM converter; resonant converter; ZVS; circulating current

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1. Introduction

For the elimination of the air pollution and emission of greenhouse gases, clean renewable energy sources with power electronic techniques have been investigated and developed for fuel cell [1,2], wind power [3,4], solar power [5,6] and battery storage system [7] applications. Solar power [8,9] is one of the most attractive clean energy sources. However, the problem of the solar panel output voltage is unstable. To solve this problem, DC-DC pulse-width modulation (PWM) converters with wide voltage variation capability were studied and researched. Full-bridge phase-shift pulse-width modulation (PSPWM) converter have been developed in [10] to have 4:1 (18 V–75 V) input voltage range operation. The synchronous rectifiers with the PSPWM scheme are adopted on the secondary side to control load voltage. The disadvantages of this circuit topology are a complicated control scheme and eight active switches. The other problems of this circuit topology are the output power and zero voltage switching (ZVS) range on active devices are related to the input voltage. In [11], the half-bridge PWM converter with multi-winding on the secondary side is proposed to control load voltage and have 2:1 (V_{in} = 250 V–400 V) voltage operation. Three active devices, four rectified diodes, four secondary windings and two filter inductors are adopted in this converter. The more component counts used in this converter will result in high cost and circuit reliability. In [12], a cascade DC-DC converter with PSPWM modulation is proposed to achieve wide input voltage operation (V_{in} = 600 V–800 V). However, the voltage range of this circuit topology is limited between 600 V–800 V. The conventional three-level duty cycle control or frequency control converters can achieve the same voltage range operation. In [13],

an asymmetric half-bridge resonant circuit with the buck-boost circuit and resonant circuit has been presented to have 2:1 (V_{in} = 36 V–72 V) voltage operation. The main problem of this circuit topology is the unbiased voltage stresses on active switches for both primary and secondary sides. In [14], a hybrid converter with a half-bridge PWM circuit and boost circuit was presented to achieve about 2:1 (V_{in} = 45 V–75 V) input voltage operation. The basic structure of this circuit topology is a kind of series-connected converter. In [15], the resonant converter operated at the half bridge or full bridge resonant circuit has been studied to realize V_{in} = 80 V–200 V voltage operation. However, the resonant frequency at low and high input voltage ranges are different due to the different resonant capacitances on half-bridge and full-bridge resonant tanks. Therefore, the wide switching frequency range will happen in this circuit topology. In [16], the PSPWM converter with two isolation transformers has been developed to have 4:1 input voltage operation. This circuit has four different operating sub-circuits under different input voltage conditions. However, the control algorithm of this circuit topology is too complicated to be implemented. In [17], the input-parallel output-series converter has been studied to have wide voltage range capability. Eight active devices and eight rectifier diodes are needed to have a 4:1 voltage operation. This circuit topology uses more power semiconductors that will reduce the circuit reliability and increase the cost.

A hybrid soft-switching DC-DC PWM converter is presented to reduce switching losses on active devices, achieve low primary current at the freewheeling state and have 5:1 (V_{in} = 90 V–450 V) wide input voltage operation. The PSPWM modulation is used to control active devices and have zero voltage turn-on characteristic. The presented converter contains a resonant circuit and a full-bridge PWM circuit. The resonant circuit can extend the ZVS operation range and also reduce the primary freewheeling current. To extend the input voltage operation range, two secondary winding sets are used on the low voltage side. Thus, a 5:1 (V_{in} = 90 V–450 V) wide input voltage range can be realized in the studied hybrid circuit. Compared to the conventional PWM converters, the advantages of the presented converter are low switching loss, low primary freewheeling current, wide input voltage operation and a simple control scheme. The circuit diagram of the proposed PWM circuit is discussed in Section 2. The principles of operation are provided in Section 3. In Sections 4 and 5, the circuit characteristic and experiments of the prototype circuit are discussed and presented to show the circuit performance. In Section 6, the conclusions of the studied hybrid PWM circuit are presented.

2. Circuit Diagram of the Proposed PWM Converter

The conventional PSPWM converter and main PWM signals are given in Figure 1a. Six power semiconductors (four active devices and two rectifier diodes), two magnetic cores (one isolation transformer and one filter inductor) and one filter capacitor are normally used in this circuit topology to realize medium or high power applications. The disadvantages of the PSPWM converter are the hard switching operation of active devices on lagging leg and high freewheeling current. The serious switching loss on active devices will result in serious switching losses at high-frequency operation and a high freewheeling current will reduce circuit efficiency. To solve these two problems, a half-bridge inductor–inductor–capacitor (*LLC*) converter can be added to a conventional full-bridge PSPWM converter as shown in Figure 1b remark in purple. The circuit elements of *LLC* converter include S_3, S_4, L_r, C_r, T_2, D_3, D_4, $C_{o,r}$ and D_r. The PSPWM converter and resonant circuit share the same active devices S_3 and S_4. Due to the ZVS operation characteristic of *LLC* converter, active devices S_3 and S_4 can achieve ZVS turn-on operation with a wide load range. Therefore, the hard switching drawback is improved. Diode D_r in Figure 1b is used to connect two dc voltage terminals $V_{o,r}$ (output terminal of *LLC* converter) and V_R (the secondary rectified voltage). During power transfer interval ($|v_{ab}|>0$), $V_R > V_{o,r}$ and D_r is reverse biased. However, D_r will be forward biased at the freewheeling duration (v_{ab} = 0 under S_1 and S_3 ON or S_2 and S_4 ON). Due to D_r is conducting, the power flow at the freewheeling duration is from $V_{o,r}$ (*LLC* converter) to V_o (load side) and the rectified voltage $V_R = V_{o,r}$. Under the freewheeling

state, the primary leg voltage $v_{ab} = 0$ and the secondary rectified voltage $V_R = V_{o,r}$. It can obtain the primary-side inductor voltage $v_{LP} = -n_{p1}V_{o,r}/n_{s1} < 0$ and the primary current i_{LP} will be declined to zero. Hence, the high circulating current drawback is overcome. In order to overcome and achieve wide voltage operation, four secondary windings are adopted in Figure 1b remark in blue. For low voltage input conditions ($V_{in,min} \sim 2.2V_{in,min}$), Q_1 turns on and Q_2 turns off (Figure 2a). Thus, D_2 and D_3 are reverse biased. The proposed circuit has a high voltage gain with transformer turns ratio $N_{T1} = n_{p1}/(n_{s1}+n_{s2})$. Under high voltage input case ($2.2V_{in,min} \sim 5V_{in,min}$), the switches Q_1 turns off and Q_2 turns on (Figure 2b). Therefore, D_1 and D_4 are reverse biased and the present circuit has low voltage gain with transformer turns ratio $N_{T1} = n_{p1}/n_{s2}$. Hence, the wide voltage operation, low freewheeling current and wide ZVS operation are realized in the presented hybrid PWM converter.

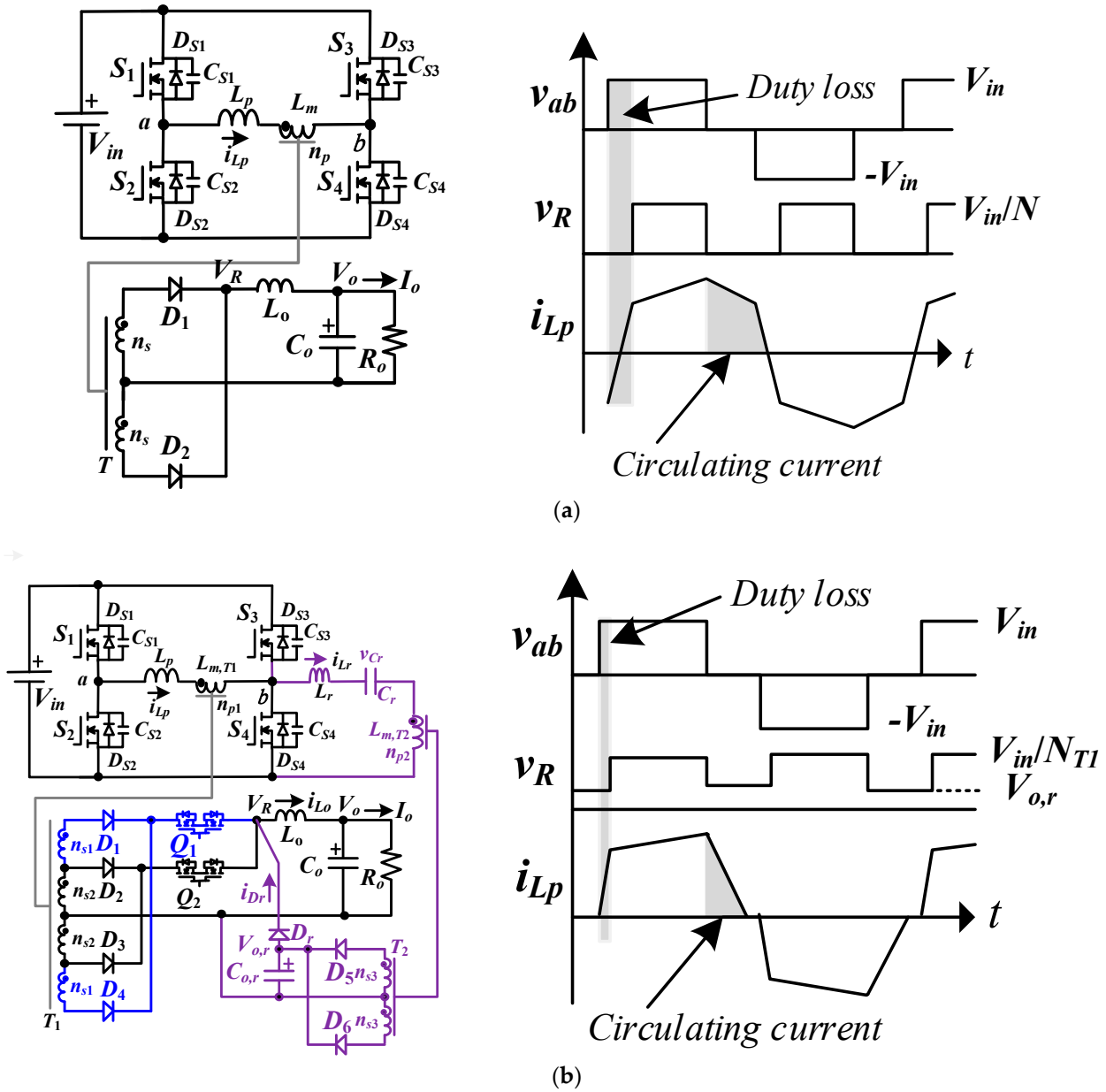


Figure 1. Circuit diagram (**a**) conventional phase-shift pulse-width modulation (PSPWM) converter and its pulse-width modulation (PWM) signals (**b**) presented circuit structure.

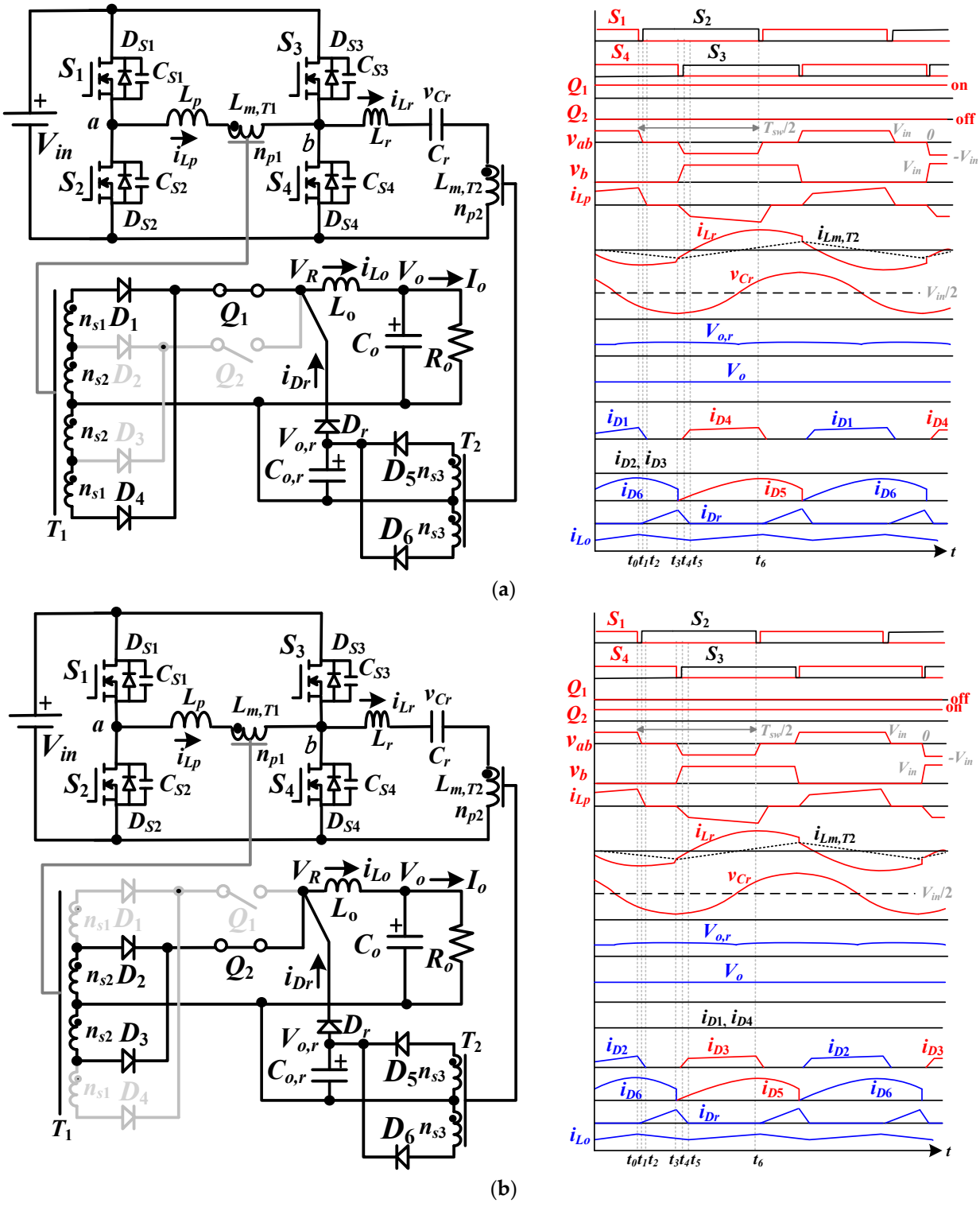


Figure 2. Equivalent sub-circuits and PWM signals under (**a**) low input voltage range (**b**) high input voltage range.

3. Operation Principle of the Present Circuit

On the basis of the input voltage range, two cub-circuits can be operated in the present converter. Figure 2a,b provide two sub-circuits under low and high input voltage regions. Under the low voltage region ($V_{in,min}$ ~ $2.2V_{in,min}$), the full-bridge PWM converter with high secondary turns is operated to obtain high DC voltage gain. To achieve high voltage gain, Q_1 turns on and Q_2 turns off. Thus, the transformer turns ratio in Figure 2a becomes

$N_{T1} = n_{p1}/(n_{s1}+n_{s2})$. Under the high voltage region ($2.2V_{in,min} \sim 5V_{in,min}$), the present converter only needs low voltage gain to control load voltage. Therefore, Q_1 turns off and Q_2 turns on to have fewer winding turns on the secondary side. The transformer turns ratio in Figure 2b becomes $N_{T1} = n_{p1}/n_{s2}$. Due to input voltage deviation, the PSPWM modulation is selected to control active devices and regulate the duty ratio of PWM signals. The resonant circuit is used in the presented circuit in order to improve the ZVS load range for lagging-leg switches. The output voltage $V_{o,r}$ of resonant converter is connected to the rectified terminal voltage V_R. Ths positive voltage $V_{o,r}$ can decrease the current i_{Lp} to 0 at a freewheeling state. Then, the freewheeling current loss is improved. In the adopted circuit, the inductance $L_R << L_{m,T1}$ and the output capacitances of $S_1 \sim S_4$ are $C_{S1} = C_{S2} = C_{S3} = C_{S4} = C_{oss}$

For the low voltage input case ($V_{in,min} \sim 2.2V_{in,min}$), the PWM signals are shown in Figure 2a. In the low input voltage region, Q_1 turns on and Q_2 turns off. It is obvious that the fast recovery diodes D_2 and D_3 are both reverse biased. In this equivalent operating circuit, the secondary turns of T_1 are equal to $n_{s1}+n_{s2}$. From Figure 2a, six states are operated in every half switching period. The equivalent state circuits for the first half switching period are provided in Figure 3.

State 1 [$t_0 \sim t_1$]: At t_0, $i_{LP} = i_{Lo}/N_{T1}$ and $i_{Dr} = 0$. Thus, D_r is reverse biased. S_1 and S_4 are ON so that D_1 conducts, the leg voltage $v_{ab} = V_{in}$ and $v_{Lo} \approx V_{in}/N_{T1}–V_o$. Thus, the primary current i_{Lp} and output inductor current i_{Lo} are increased and given in Equations (1) and (2).

$$i_{Lp}(t) \approx i_{Lp}(t_0) + (V_{in} - N_{T1}V_o)(t - t_0)/(N_{T1}^2 L_o) \quad (1)$$

$$i_{Lo}(t) \approx N_{T1} i_{Lp}(t) \quad (2)$$

Power transfer between input and output terminals is through a full-bridge PWM converter in this state. The resonant circuit is controlled at the resonant frequency. Since S_4 is ON, the inductor current i_{Lr} will decrease and i_{Lr} is less than the magnetizing current $i_{Lm,T2}$. Therefore, D_6 is forward biased and *LLC* converter will store energy on $C_{o,r}$.

State 2 [$t_1 \sim t_2$]: At t_1, S_1 is off. Prior to t_1, i_{Lp} is positive. After time t_1, i_{Lp} will discharge C_{S2}. If the energy $(L_p + N_{T1}^2 L_o) i_{Lp}^2(t_1) > 2C_{oss}V_{in}^2$, then v_{CS2} will decline to 0 at time t_2. The discharge time of C_{S2} is $\Delta t_{12} \approx 2V_{in}C_{oss}N_{T1}/I_o$. To ensure the ZVS operation, the other necessary condition is t_d (dead time between S_2 and S_1) > Δt_{12}. *LLC* circuit is still operated at resonant mode ($f_{sw} = f_r = 1/2\pi\sqrt{L_r C_r}$).

State 3 [$t_2 \sim t_3$]: $v_{CS2} = 0$ at t_2. Then i_{Lp} flows through D_{S2} and keeps $v_{CS2,ds} = 0$. Hence, S_2 can turn on to realize ZVS operation. The secondary rectified voltage V_R is decreased to $V_{o,r}$ so that diode D_r becomes forward biased and obtains $V_R = V_{o,r}$. The primary and secondary inductor voltages $v_{Lp} = -N_{T1}V_{o,r}$ and $v_{Lo} = V_{o,r} - V_o < 0$. It can obtain that i_{Lp} and i_{Lo} are both decreased in state 3.

$$i_{Lp}(t) \approx i_{Lp}(t_2) - N_{T1}V_{o,r}(t - t_2)/L_p \quad (3)$$

$$i_{Lo}(t) \approx i_{Lo}(t_2) + (V_{o,r} - V_o)(t - t_2)/L_o \quad (4)$$

In a traditional PSPWM converter, $v_{Lp} \approx 0$ and i_{Lp} almost constant at the freewheeling state. From (3), i_{Lp} in the proposed hybrid converter is decreased in this state. If the freewheeling time interval is large enough, i_{D1} or i_{Lp} can be decreased to zero.

$$\Delta t_{i_{LP}=0} \approx L_p I_o/(N_{T1}^2 V_{o,r}) \quad (5)$$

From Equation (5), one can be observed, the time $\Delta i_{Lp=0}$ is dependent on I_o and $V_{o,r}$. For full load condition, a more freewheeling time interval is needed to achieve no circulating current advantage.

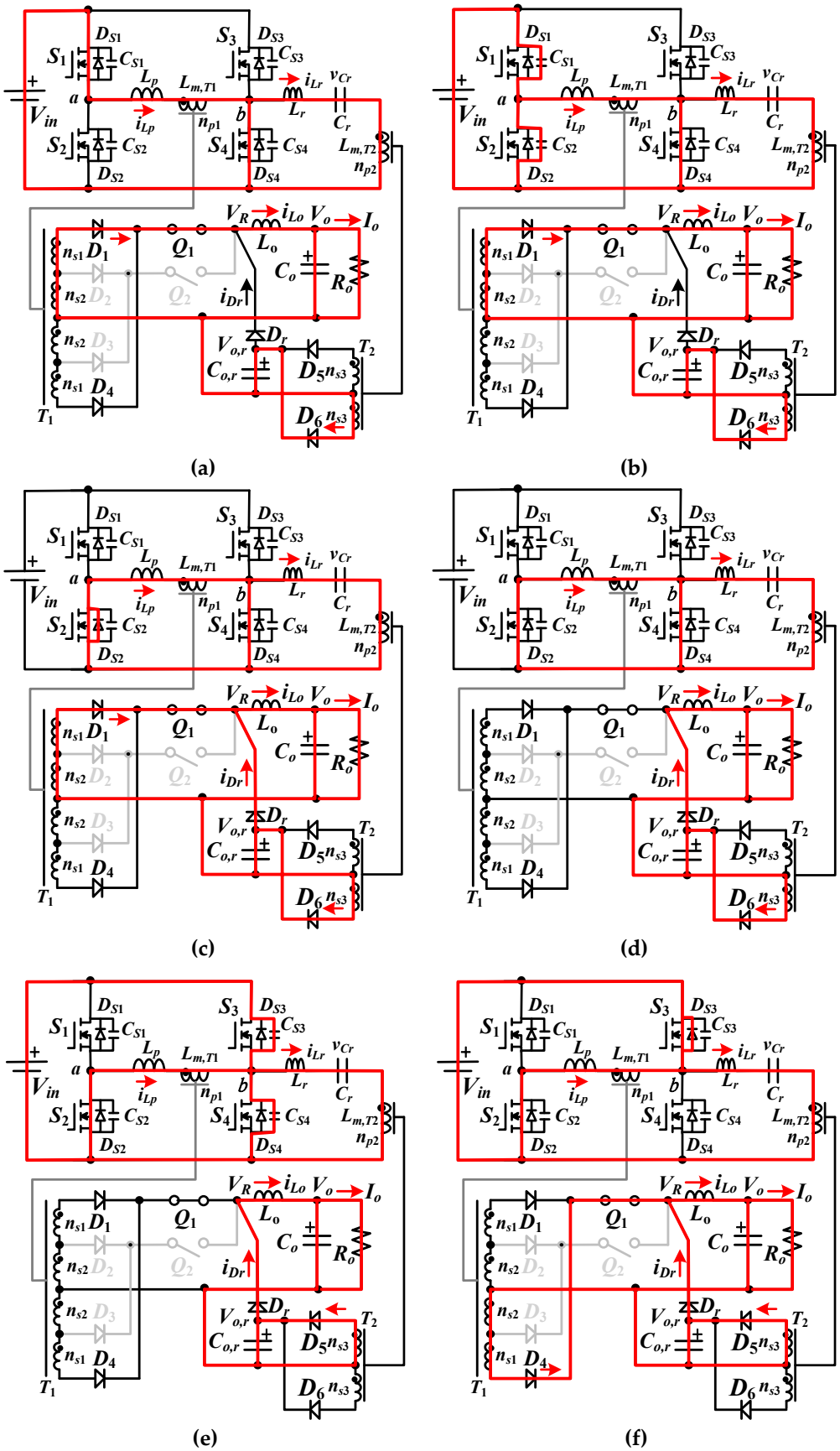


Figure 3. State circuits of the first half switching cycle under low voltage input operation (**a**) state 1 circuit (**a**) state 1 (**b**) state 2 (**c**) state 3 (**d**) state 4 (**e**) state 5 (**f**) state 6.

State 4 [$t_3 \sim t_4$]: At t_3, $i_{D1} = 0$, $i_{Lp} \approx 0$ and $i_{Dr} = i_{Lo}$. Hence, the circulating current is removed at a freewheeling state. In state 4, power transfer is from V_{in} to V_o through *LLC* circuit, D_r and L_o. The filter inductor voltage $v_{Lo} = V_{o,r} - V_o < 0$ and i_{Lo} is decreased in this state.

State 5 [$t_4 \sim t_5$]: At time t_4, S_4 turns off. Prior to t_4, $i_{Lr} - i_{Lp} < 0$. C_{S3} is discharged when S_4 is turned off. Diode D_5 becomes forward biased in *LLC* circuit. Owing to *LLC* operation, v_{CS3} can be easily decreased to 0 and S_3 can turn on at zero voltage at time t_5.

State 6 [$t_5 \sim t_6$]: At time t_5, C_{S3} is discharged to zero voltage. D_{S3} becomes forward biased and S_3 can turn on at zero voltage switching after time t_5. The leg voltage $v_{ab} = -V_{in}$ and D_4 become forward biased. Since $i_{D4} < i_{Lo}$, D_r is conducting. The inductor voltage $v_{Lp} \approx N_{T1}V_{o,r} - V_{in} < 0$ and i_{Lp} decreases. At time t_6, the diode current $i_{D4} = i_{Lo}$, $i_{Lp} = -i_{Lo}/N_{T1}$ and $i_{Dr} = 0$. The time interval of state 6 is expressed as $\Delta t_{56} \approx I_o L_p / [N_{T1}(V_{in} - N_{T1}V_{o,r})]$. Since D_r is conducting in this state, the duty ratio loss of PSPWM circuit at state 6 is calculated as $d_6 \approx f_{sw} I_o L_p / [N_{T1}(V_{in} - N_{T1}V_{o,r})]$. The current i_{Lo} is still decreased in state 6. This state is ended at time t_6.

The proposed circuit can also be operated at high voltage input conditions ($2.2V_{in,min} \sim 5V_{in,min}$). The PWM waveforms for high voltage input operation are provided in Figure 2b. Under high voltage input, Q_1 is controlled at OFF state and Q_2 is ON. Due to Q_1 is OFF, D_1 and D_4 become OFF. The full-bridge PWM converter has turns ratio $N_{T1} = n_{p1}/n_{s2}$. Since the switching frequency of *LLC* circuit is equal to the resonant frequency, active devices S_3 and S_4 are turned on at ZVS operation. Due to D_r is connecting $V_{o,r}$ and V_R, the primary current i_{Lp} can be decreased to 0 at the freewheeling state. Figure 4 provides the state circuits for first half switching period under high voltage input operation.

State 1 [$t_0 \sim t_1$]: i_{LP} is increased and equal to i_{Lo}/N_{T1} at time t_0. Thus, D_r becomes reverse biased. The leg voltage $v_{ab} = V_{in}$ and D_2 is forward biased. The currents i_{Lp} and i_{Lo} are increased. Power flow from V_{in} to V_o is finished by a full-bridge converter. Due to $i_{Lr} < i_{Lm,T2}$, D_6 is forward biased in state 1.

State 2 [$t_1 \sim t_2$]: At t_1, S_1 is turned off and $i_{Lp}(t_1) > 0$. i_{Lp} discharge capacitor C_{S2}. If $(L_p + N_{T1}^2 L_o) i_{Lp}^2(t_1) > 2C_{oss}V_{in}^2$, then v_{CS2} will decrease to zero at time t_2. *LLC* converter is controlled at resonant mode, v_{Cr} is decreased and D_6 is conducting.

State 3 [$t_2 \sim t_3$]: At t_2, $v_{CS2} = 0$ and D_{S2} is forward biased due to $i_{Lp} > 0$. Active device S_2 turns on at ZVS and leg voltage $v_{ab} = 0$. The secondary voltage V_R is clamped at $V_{o,r}$ due to D_r is forward biased. It can obtain $v_{Lp} = -N_{T1}V_{o,r}$ and $v_{Lo} = V_{o,r} - V_o < 0$. Both i_{Lp} and i_{Lo} are decreased in this state.

State 4 [$t_3 \sim t_4$]: At t_3, i_{D2} is decreased to 0 and $i_{Dr} = i_{Lo}$. Hence, diode D_2 is reverse biased. *LLC* converter will transfer power from V_{in} to V_o through D_r and L_o. The inductor voltage $v_{Lo} = V_{o,r} - V_o < 0$ and i_{Lo} is decreased in state 4.

State 5 [$t_4 \sim t_5$]: S_4 turns off at time t_4. Since $i_{Lr}(t_4) - i_{Lp}(t_4) < 0$, v_{CS3} is decreased after time t_4. Due to $i_{Lr} > i_{Lm,T2}$, D_5 becomes forward biased. *LLC* circuit is operated at inductive load so that v_{CS3} can be easily decreased to 0.

State 6 [$t_5 \sim t_6$]: At t_5, $v_{CS3} = 0$. Then, D_{S3} is on so that S_3 can turn on at this moment to achieve soft switching operation. In state 6, $v_{ab} = -V_{in}$ and D_3 is ON. Since D_r is still conducting, it can obtain $v_{Lp} \approx N_{T1}V_{o,r} - V_{in} < 0$ and i_{Lp} is decreased. At time t_6, $i_{D4} = i_{Lo}$ and D_r becomes reverse biased. The primary current $i_{Lp} = -i_{Lo}/N_{T1}$. Since $v_{Lo} = V_{o,r} - V_o < 0$, i_{Lo} is decreased. State 6 ends at time t_6.

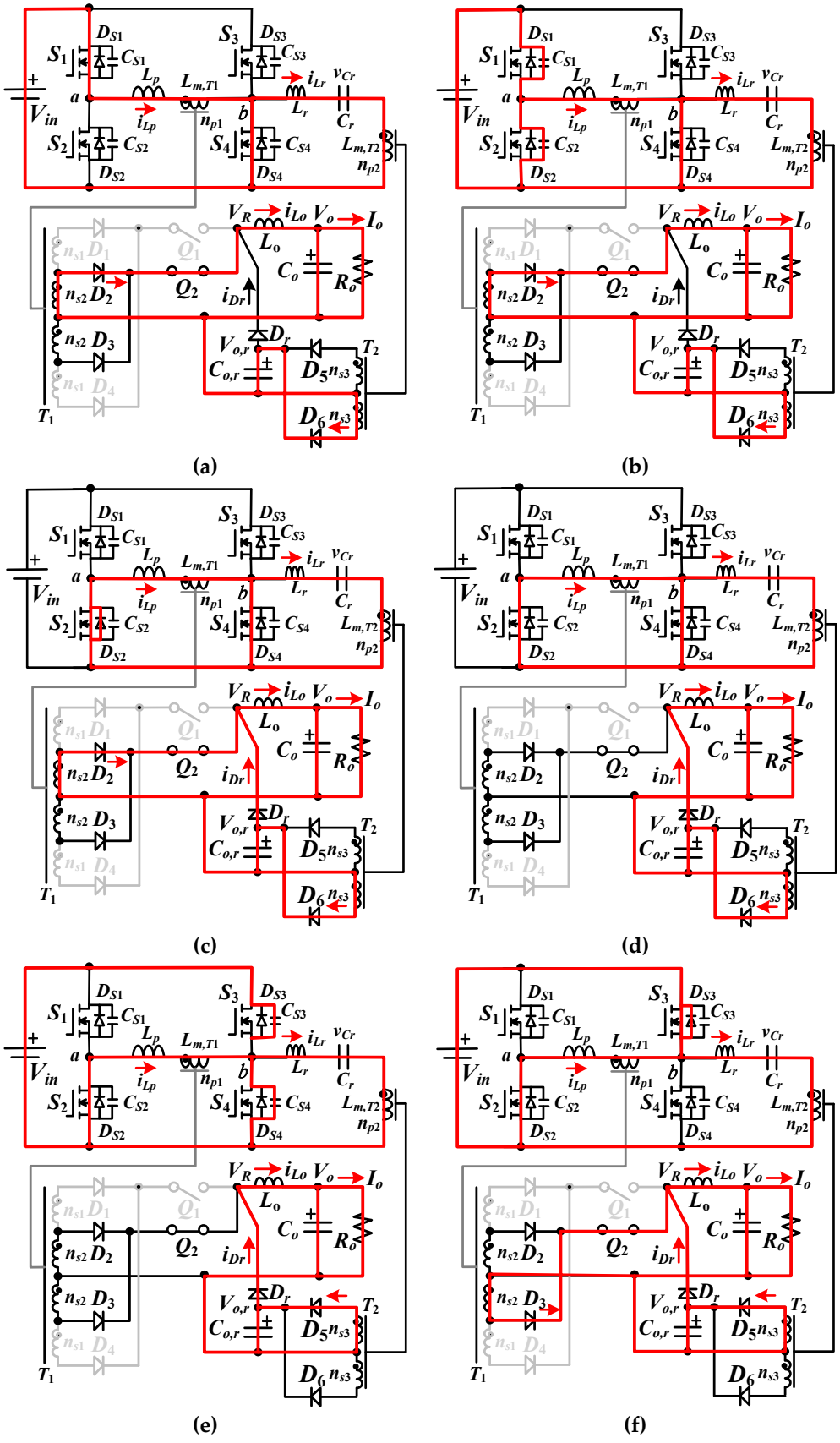


Figure 4. State circuits of the first half switching cycle under high voltage input operation (**a**) state 1 circuit (**a**) state 1 (**b**) state 2 (**c**) state 3 (**d**) state 4 (**e**) state 5 (**f**) state 6.

4. Circuit Analysis of the Presented Converter

The advantages of the studied hybrid PSPWM circuit are a wide load range of soft switching, less circulating current and wide input voltage operation. The hard switching drawback and high freewheeling current problem of conventional PSPWM converter are overcome by using an *LLC* converter in the proposed circuit. Since the switching frequency of *LLC* circuit is equal to the resonant frequency, active switches of the PSPWM converter can be turned on at ZVS. To realize a wide input voltage deviation problem, four winding sets and two switches are adopted on the low voltage side to control DC voltage gain. Under low input voltage conditions, the winding turns n_{S1}+n_{S2} are selected on the secondary side. Under a high input voltage case, the n_{S2} turns are used on the output side. In the presented circuit, the resonant circuit is controlled under constant switching frequency (equal series resonant frequency). Hence, $V_{o,r}$ is approximately equal to $V_{in}/(2N_{T2}) = V_{in}n_{S3}/(2n_{p2})$. In the presented phase-shift PWM converter, there is a duty loss in state 6. The inductor voltage v_{Lo} in states 1 and 2 is equal tp $V_{in}/N_{T1} - V_o$. However, v_{Lo} in states 3–6 is equal to $V_{o,r} - V_o = V_{in}/(2N_{T2}) - V_o$. Apply the voltage-second balance to L_o, the voltage V_o is derived as.

$$V_o \approx [d_e(1 - \frac{N_{T1}}{2N_{T2}}) + \frac{N_{T1}}{4N_{T2}}]\frac{2V_{in}}{N_{T1}} \tag{6}$$

where $d_e = d - d_6$ is the effective duty cycle and $N_{T1} = n_{p1}/(n_{s1}+n_{s2})$ or n_{p1}/n_{s2} for low or high voltage input condition, respectively. In a traditional PSPWM converter, the output voltage is expressed in Equation (7).

$$V_{o,con} = \frac{2d_eV_{in}}{N_{T1}} \tag{7}$$

Comparing Equations (6) and (7), it obtains $G_{dc} = N_{T1}V_o/(2V_{in}) > G_{dc,con} = N_{T1}V_{o,con}/(2V_{in})$. That means the presented circuit has larger DC gain than the traditional PSPWM converter. Due to the full-bridge circuit structure, $S_1 \sim S_4$ has $V_{in,max}$ voltage stress. The switches Q_1 and Q_2 have voltage stress $V_{in}n_{s1}/n_{p1}$. The voltage stresses on the fast recovery diodes $D_1 \sim D_6$ and D_r are obtained in Equations (8)–(11).

$$V_{D1,rating} = V_{D4,rating} = 2V_{in}(n_{s1} + n_{s2})/n_{p1} \tag{8}$$

$$V_{D2,rating} = V_{D3,rating} = 2V_{in}n_{s2}/n_{p1} \tag{9}$$

$$V_{D5,rating} = V_{D6,rating} = V_{in}n_{s3}/n_{p2} \tag{10}$$

$$V_{Dr,rating} = V_{in}/N_{T1} - V_{in}/(2N_{T2}) \tag{11}$$

The dc diode currents of $D_1 \sim D_6$ and D_r are $I_{D1} = I_{D2} = I_{D3} = I_{D4v} \approx d_eI_o$, $I_{D5} = I_{D6} \approx (0.5 - d_e)I_o$ and $I_{Dr} \approx (1 - 2d_e)I_o$. The inductor voltage $v_{Lo} = V_{in}/N_{T1} - V_o$ in states 1 and 2 and $v_{Lo} = V_{o,r} - V_o$ in states 3 ~ 6. Therefore, L_o in conventional full-bridge PWM converter and the proposed hybrid converter are expressed in Equations (12) and (13).

$$L_{o,con} > V_o(0.5 - d_e)/(f_{sw}\Delta i_{Lo}) \tag{12}$$

$$L_o > (V_o - \frac{V_{in}}{2N_{T2}})(0.5 - d_e)/(f_{sw}\Delta i_{Lo}) \tag{13}$$

Comparison of Equations (12) and (13), it is clear that the presented hybrid PWM circuit has less output inductance L_o. The output power of the resonant circuit is $P_{LLC} \approx (0.5 - d_{eff})I_oV_{in}/N_{T2}$ and the output power of the PSPWM circuit is $P_{PWM\ circuit} \approx 2d_eI_oV_{in}/N_{T1}$.

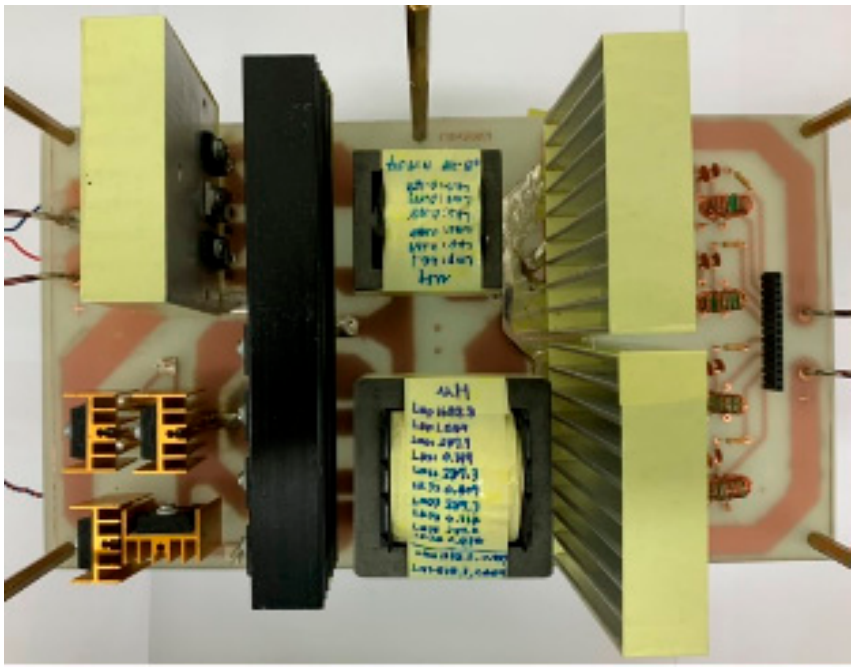
5. Experimental Results

The presented hybrid PSPWM circuit is investigated and confirmed by a prototype circuit. The rated power of the proposed circuit is $P_{o,max}$ = 800 W, the input and output

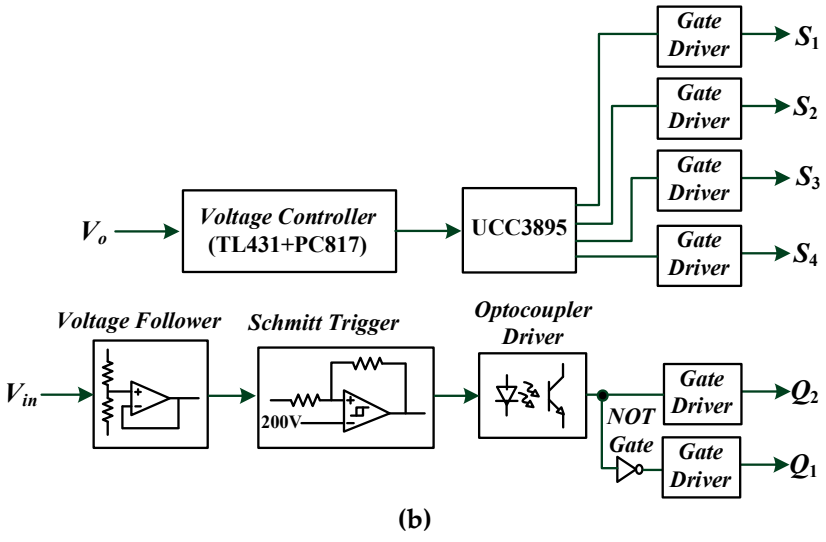
voltages are V_{in} = 90 V–450 V and V_o = 48 V. The switching frequency is f_{sw} = 70 kHz. In the presented circuit, Q_1 and Q_2 are ON and OFF under 90 V $\leq V_{in} <$ 200 V (low voltage input). Therefore, the transformer T_1 has turns ratio $N_{T1} = n_{p1}/(n_{s1} + n_{s2})$. On the other hand, Q_1 and Q_2 are OFF and ON under 200 V $< V_{in} \leq$ 450 V (high voltage input). Transformer T_1 has turns ratio $N_{T1} = n_{p1}/n_{s2}$. To present signal oscillation at V_{in} = 200 V, a Schmitt comparator with $\pm$ 10V tolerance is adopted in the control circuit to control Q_1 and Q_2. Hence, Q_1 is ON and Q_2 is OFF at 90 V $\leq V_{in} \leq$ 210 V, and Q_1 is OFF and Q_2 is ON at 190 V $\leq V_{in} \leq$ 450 V in the control algorithm. The general purpose PWM integrated circuit UCC3895 is selected to control S_1–S_4. The switches Q_1 and Q_2 are controlled by a voltage comparator. The component parameters of the laboratory prototype circuit are provided in Table 1. Figure 5a gives the picture of the prototype circuit. The control blocks of the presented converter are given in Figure 5b. The output voltage controller is based on the type III voltage control algorithm [18]. The output of the voltage controller is to regulate the phase shift angle between the leading-leg switches and lagging-leg switches. The gate drivers are used to turn on or off the switching devices S_1–S_4. In order to realize the wide input voltage operation, a Schmitt trigger comparator with 200 V reference voltage is adopted to select the low (Q_1 ON, if $V_{in} <$ 200 V) or high (Q_2 ON, if $V_{in} >$ 200 V) input voltage region. The measured waveforms of the proposed circuit for V_{in} = 90 V and 210 V under the low voltage region are illustrated in Figures 6 and 7. Similarly, Figures 8 and 9 provide the experimental waveforms under V_{in} = 190 V and 450 V at high voltage regions. The primary-side signals ($v_{S1,g}$, $v_{S4,g}$, v_{ab}, and i_{Lp}) of the full-bridge converter under V_{in} = 90 V, 210 V, 190 V and 450 V are illustrated in Figures 6a, 7a, 8a and 9a, respectively. One can observe that the proposed converter has a less effective duty ratio at V_{in} = 210 V (450 V) than V_{in} = 90 V (190 V). The circulating current of i_{Lp} at the freewheeling state (v_{ab} = 0) can be improved and reduced to zero at V_{in} = 210 V, 190 V and 450 V in Figures 7a, 8a and 9a. The primary-side waveforms ($v_{S3,g}$, $v_{S4,g}$, v_{Cr}, and i_{Lr}) of the resonant converter at V_{in} = 90, 210, 190 and 450 V are provided in Figures 6b, 7b, 8b and 9b, respectively. The resonant capacitor voltage v_{Cr} contains a dc voltage value that is equal to $V_{in}/2$. Figures 6c and 7c provide the measured output side waveforms of PSPWM converter at V_{in} = 90 V and 210 V. For the low voltage input region, Q_1 is ON and Q_2 is OFF. Therefore, D_2 and D_3 are reverse biased. At the freewheeling state (v_{ab} = 0), D_r is conducting to clamp $V_R = V_{o,r}$ and force $V_{Lo} = V_{o,r} - V_o < 0$. Therefore, i_{Lo} is decreased at this freewheeling state. Similarly, Figures 8c and 9c provide the measured waveforms of i_{D2}, i_{D3}, i_{Dr} and $V_{o,r2}$ at V_{in} = 190 V and 450 V under the high voltage region. The measured secondary-side waveforms of the resonant converter at V_{in} = 90, 210, 190 and 450 V are illustrated in Figures 6d, 7d, 8d and 9d, respectively. Figure 10 demonstrates the test results of S_1 (at leading-leg) and S_4 (at lagging-leg) at V_{in} = 90 V input for 20% load and full load conditions. Owing to the energy on L_o is adopted to discharge the leading-leg switch S_1, one can observe that switch S_1 in Figure 10a,b have ZVS turn-on operation. Due to the LLC circuit operation, S_4 can achieve ZVS turn-on operation shown in Figure 10c,d at 20% and 100% power conditions. Similarly, the measured waveforms of S_1 (at leading-leg) and S_4 (at lagging-leg) at V_{in} = 190 V, 210 V and 450 V under 20% load and full load are demonstrated in Figures 11–13, respectively. Due to the phase-shift PWM operation of the DC full-bridge converter, the PWM signals of S_2 and S_3 have the same operation characteristics as S_1 and S_4. From the experimental results in Figures 10–13, it is clear that all switches have ZVS characteristic from 20% load to full load for all input voltage range. Figure 14 provides the relationship between the signals of Q_1 and Q_2 and input voltage V_{in}. When $V_{in} >$ 90 V and $<$ 210 V (in low voltage input range), Q_1 turns on and Q_2 turns off. The $n_1 + n_2$ turns are selected to achieve high voltage gain. On the other hand, Q_1 turns off and Q_2 turns on, if $V_{in} >$ 210 V (in high voltage input range). The n_2 turns are selected to reduce voltage gain. If the input voltage V_{in} is declined from 450 V and $V_{in} <$ 190 V, then Q_1 will turn on and Q_2 turns off. The measured efficiencies of the prototype circuit are about 90%, 88%, 92% and 89% at V_{in} = 90 V, 210 V, 190 V and 450 V, respectively, under full load conditions.

Table 1. Circuit parameters in the laboratory prototype.

Items.	Parameter	Items	Parameter
V_{in}	90~450 V	V_o	48 V
L_o	32 μH	S_1~S_4, Q_1, Q_2	STF40N60M2
P_o	800 W	D_1~D_4	MSC015SDA120B
f_{sw}	70 kHz	D_5, D_6	STPS 30M80CFP
L_p	8 μH	D_r	SBR60A300CT
L_r	13 μH	n_{p1}:n_{s1}:n_{s2}	17:7:7
C_r	410 nF	n_{p2}:n_{s3}	19:2
$C_{o,r}$	330 μF/100 V	$L_{m,T2}$	66 μH
C_o	12800 μF/100 V		



(a)



(b)

Figure 5. Prototype circuit (**a**) picture of the proposed converter (**b**) control blocks.

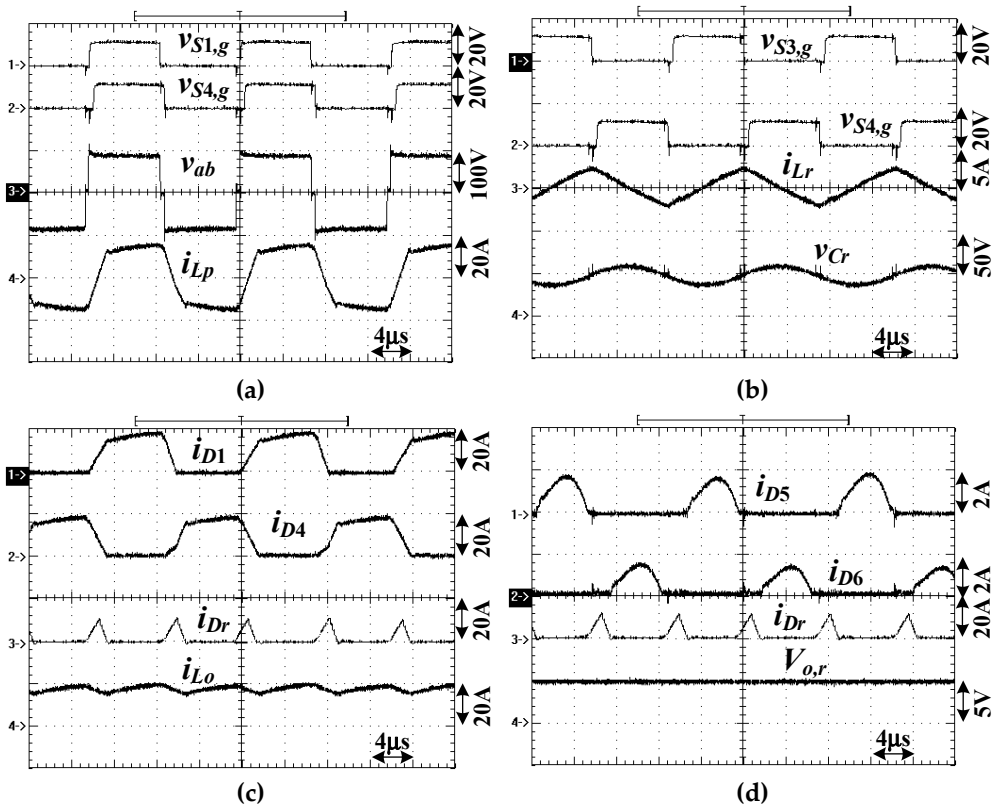


Figure 6. Experimental results at V_{in} = 90 V and full load under low voltage input region (**a**) $v_{S1,g}$, $v_{S4,g}$, v_{ab}, and i_{Lp} (**b**) $v_{S3,g}$, $v_{S4,g}$, v_{Cr}, and i_{Lr} (**c**) i_{D1}, i_{D4}, i_{Dr}, and i_{Lo} (**d**) i_{D5}, i_{D6}, i_{Dr}, and $V_{o,r}$.

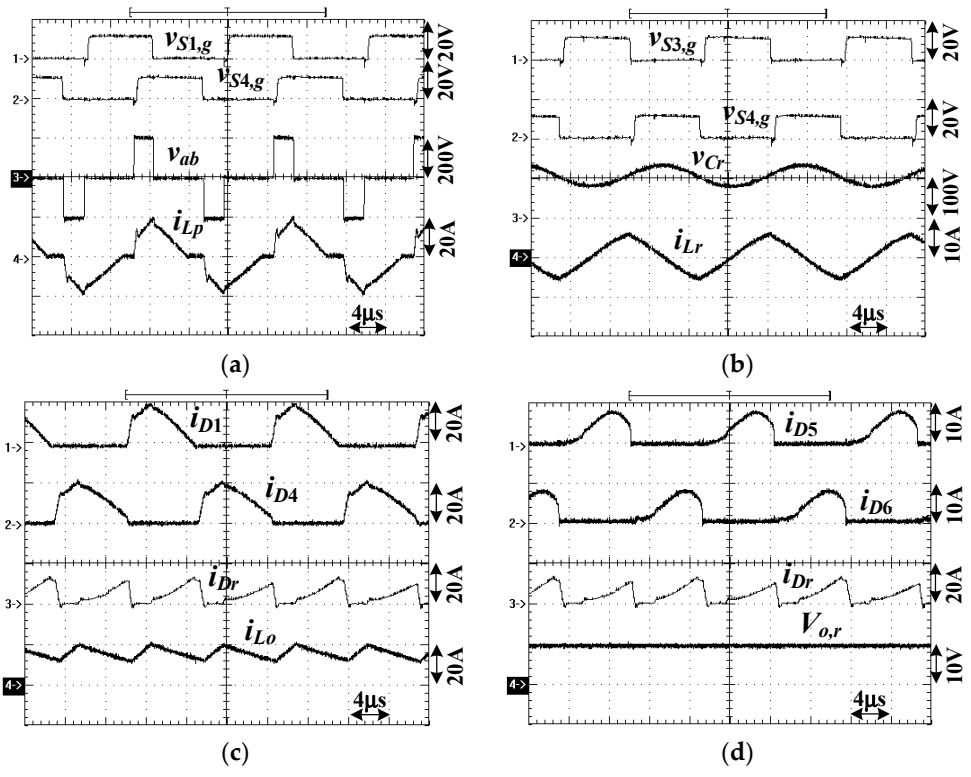


Figure 7. Measured results at V_{in} = 210 V and full load under low voltage input region (**a**) $v_{S1,g}$, $v_{S4,g}$, v_{ab}, and i_{Lp} (**b**) $v_{S3,g}$, $v_{S4,g}$, v_{Cr}, and i_{Lr} (**c**) i_{D1}, i_{D4}, i_{Dr}, and i_{Lo} (**d**) i_{D5}, i_{D6}, i_{Dr}, and $V_{o,r}$.

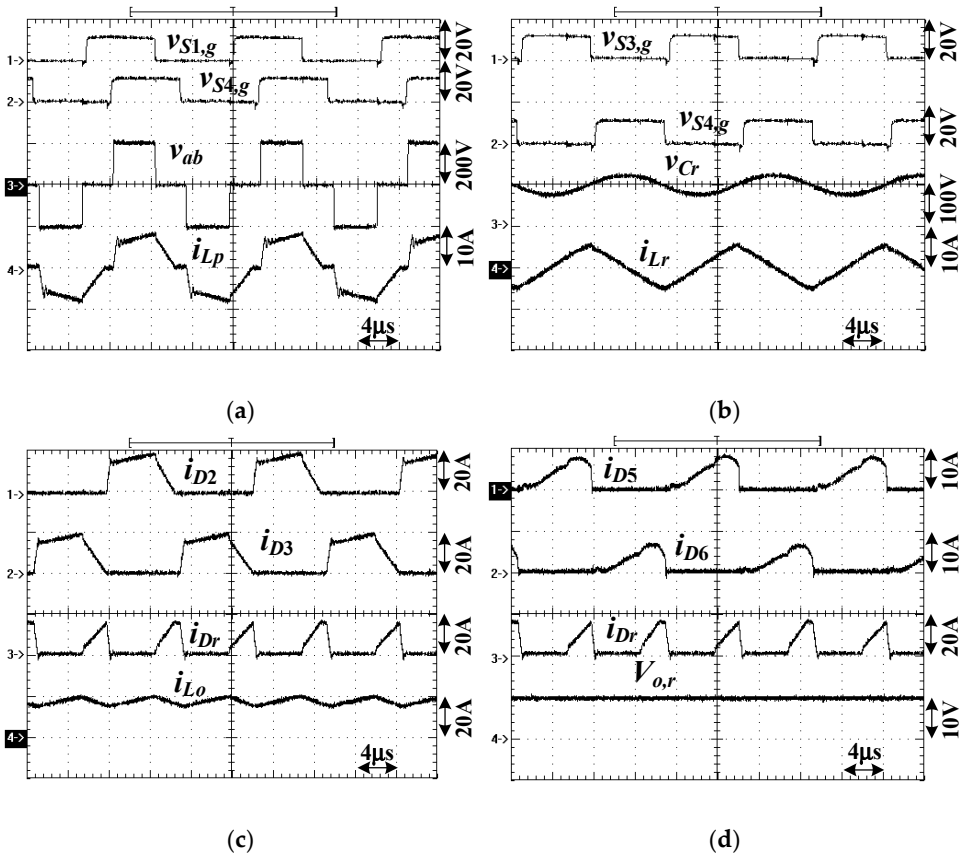


Figure 8. Measured results at V_{in} = 190 V and full load under high voltage input region (**a**) $v_{S1,g}$, $v_{S4,g}$, v_{ab}, and i_{Lp} (**b**) $v_{S3,g}$, $v_{S4,g}$, v_{Cr}, and i_{Lr} (**c**) i_{D2}, i_{D3}, i_{Dr}, and i_{Lo} (**d**) i_{D5}, i_{D6}, i_{Dr}, and $V_{o,r}$.

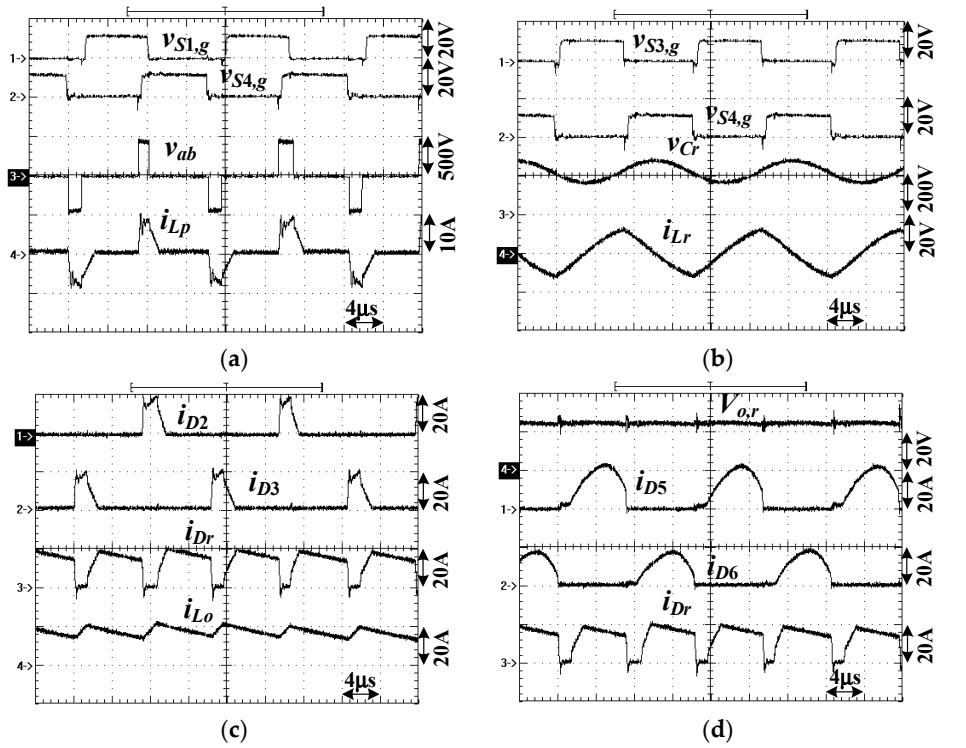


Figure 9. Measured results at V_{in} = 450 V and full load under high voltage input region (**a**) $v_{S1,g}$, $v_{S4,g}$, v_{ab}, and i_{Lp} (**b**) $v_{S3,g}$, $v_{S4,g}$, v_{Cr}, and i_{Lr} (**c**) i_{D2}, i_{D3}, i_{Dr}, and i_{Lo} (**d**) i_{D5}, i_{D6}, i_{Dr}, and $V_{o,r}$.

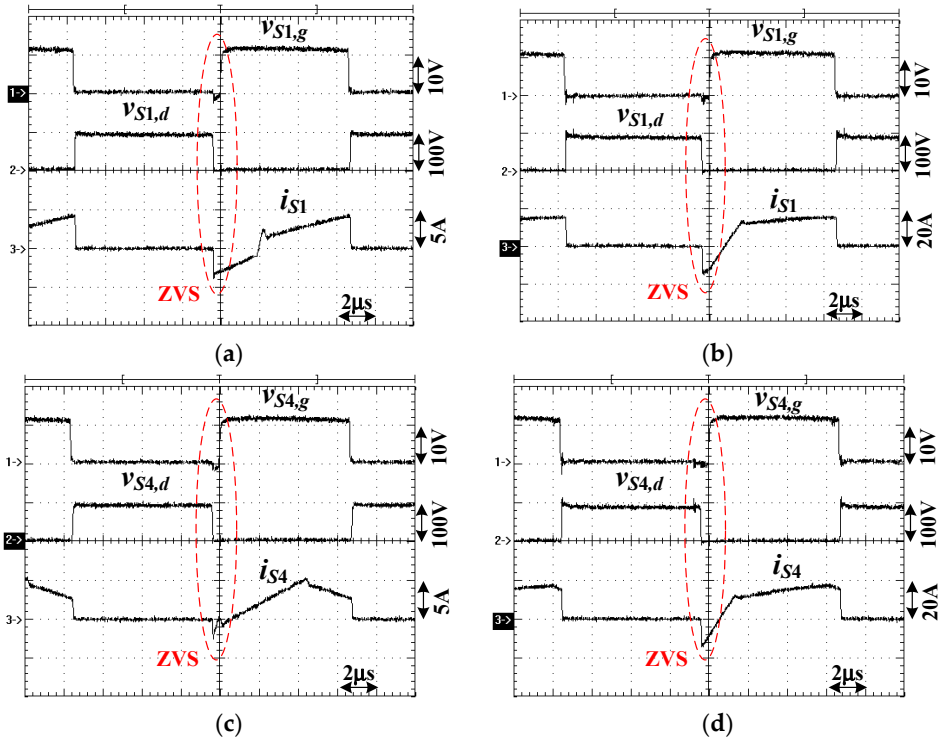


Figure 10. Measured results of S_1 and S_4 at V_{in} = 90 V input (**a**) S_1 waveforms at 160 W (20% load) (**b**) Scheme 1. waveforms at 800 W (full load) (**c**) S_4 waveforms at 160 W (20% load) (**d**) S_4 waveforms at 800 W (full load).

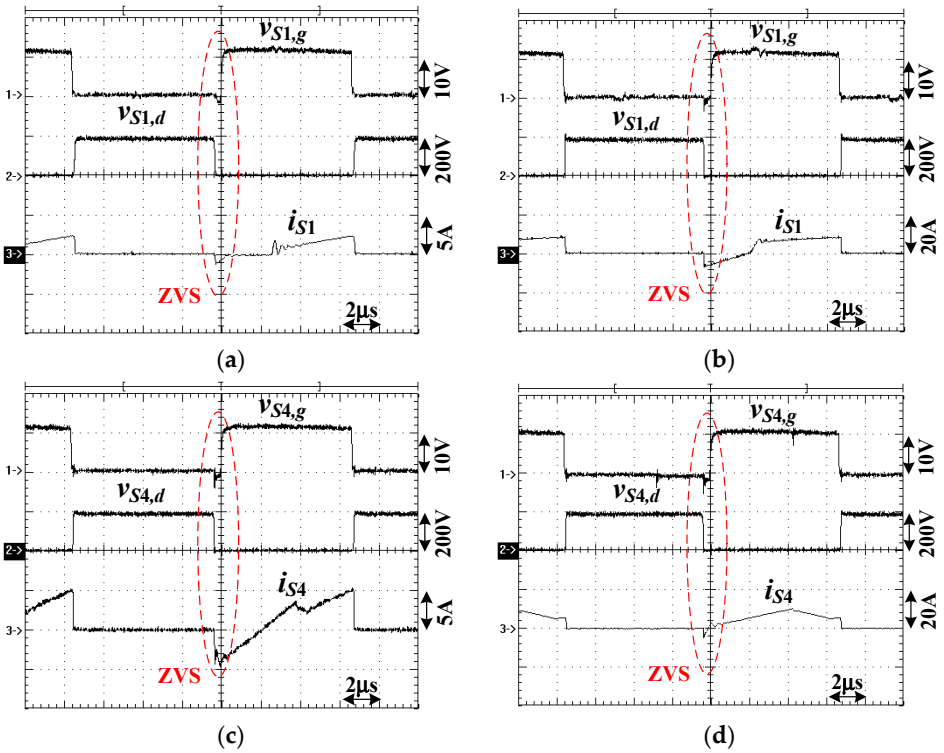


Figure 11. Measured results of S_1 and S_4 at V_{in} = 190 V input (**a**) S_1 waveforms at 160 W (20% load) (**b**) Scheme 1. waveforms at 800 W (full load) (**c**) S_4 waveforms at 160 W (20% load) (**d**) S_4 waveforms at 800 W (full load).

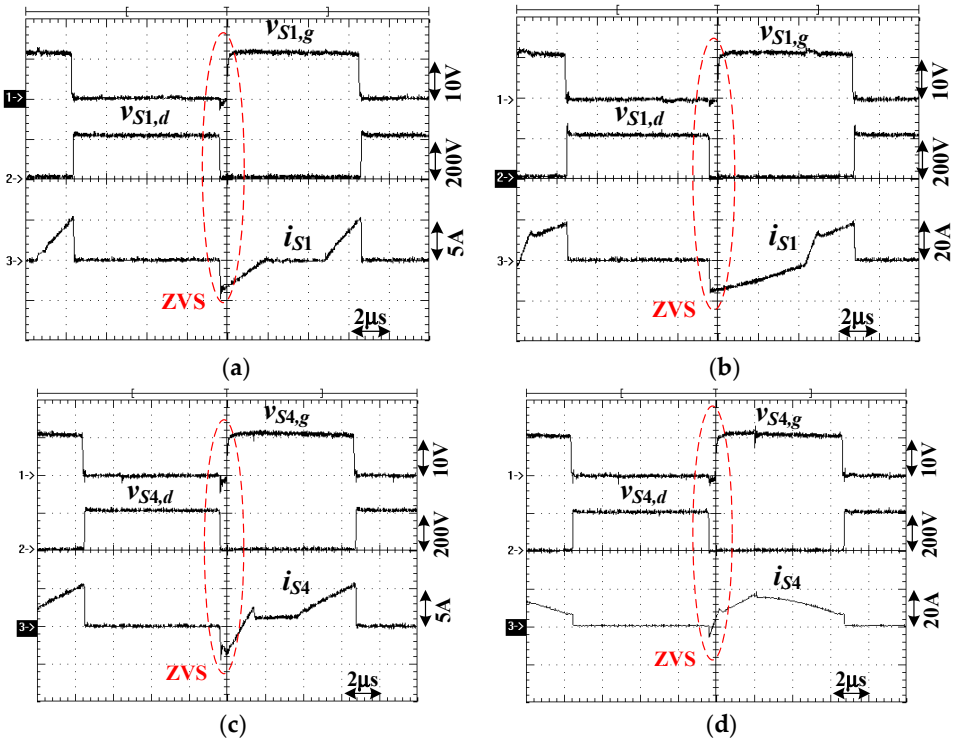


Figure 12. Measured results of S_1 and S_4 at V_{in} = 210 V input (**a**) S_1 waveforms at 160 W (20% load) (**b**) Scheme 1. waveforms at 800 W (full load) (**c**) S_4 waveforms at 160 W (20% load) (**d**) S_4 waveforms at 800 W (full load).

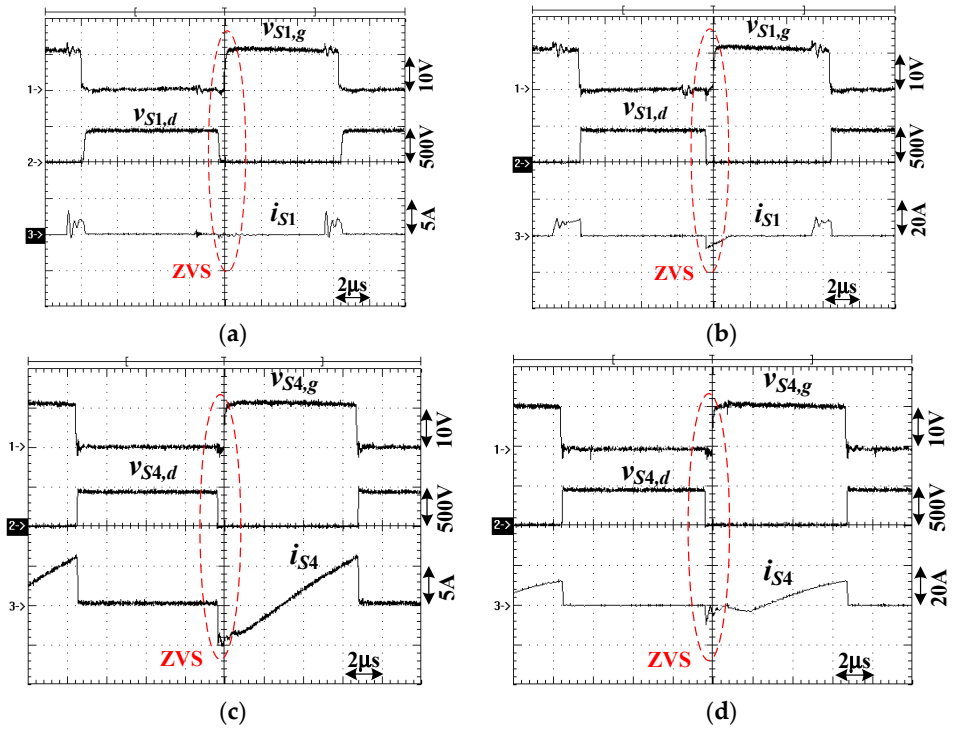


Figure 13. Measured results of S_1 and S_4 at V_{in} = 450 V input (**a**) S_1 waveforms at 160 W (20% load) (**b**) Scheme 1. waveforms at 800 W (full load) (**c**) S_4 waveforms at 160 W (20% load) (**d**) S_4 waveforms at 800 W (full load).

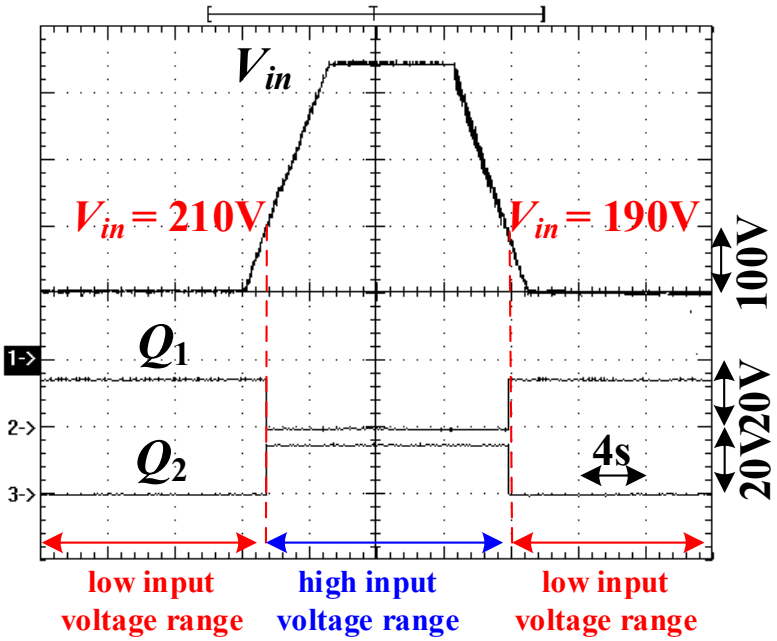


Figure 14. Measured waveforms of input voltage and PWM signals of Q_1 and Q_2 under 100% load.

6. Conclusions

A hybrid PWM converter is discussed and implemented to improve the drawbacks of the traditional PSPWM converter. The advantages of the presented circuit are low primary current stress at the freewheeling state, low switching losses at the lagging-leg switches and more wide input voltage operation for PV power renewable energy applications. Compare to the conventional PWM converters in [10–17] with wide input voltage or output voltage operation, the proposed circuit has fewer power switches on the primary side. The LLC resonant converter is used on the lagging-leg of the conventional PSPWM converter to reduce the switching loss. Thus, the switching losses on the proposed converter are improved. The high freewheeling current loss of conventional phase-shift PWM converter is also improved by the connection of the output DC voltage of the resonant circuit to the rectified terminal of the PSPWM circuit. However, the proposed converter has more circuit components compared to the other wide input voltage PWM converters. The performance of the presented hybrid PWM circuit is provided from the experiments with an 800 W prototype circuit. Further work will consider reducing the active or passive components in the presented converter, decreasing the circuit cost and maintaining the same converter performance.

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