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Analysis of Instability Behavior and Mechanism of E-Mode GaN Power HEMT with p-GaN Gate under Off-State Gate Bias Stress

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Abstract: In this study, we investigate the degradation characteristics of E-mode GaN High Electron Mobility Transistors (HEMTs) with a p-GaN gate by designed pulsed and prolonged negative gate (V_{GS}) bias stress. Device transfer and transconductance, output, and gate-leakage characteristics were studied in detail, before and after each pulsed and prolonged negative V_{GS} bias stress. We found that the gradual degradation of electrical parameters, such as threshold voltage (V_{TH}) shift, on-state resistance ($R_{DS\text{-}ON}$) increase, transconductance max ($G_{m,\,max}$) decrease, and gate leakage current ($I_{GS\text{-}Leakage}$) increase, is caused by negative V_{GS} bias stress time evolution and magnitude of stress voltage. The significance of electron trapping effects was revealed from the V_{TH} shift or instability and other parameter degradation under different stress voltages. The degradation mechanism behind the DC characteristics could be assigned to the formation of hole deficiency at p-GaN region and trapping process at the p-GaN/AlGaN hetero-interface, which induces a change in the electric potential distribution at the gate region. The design and application of E-mode GaN with p-GaN gate power devices still need such a reliability investigation for significant credibility.

Keywords: enhancement-mode GaN power device; p-GaN; high electron mobility transistor (HEMT); negative gate bias stress; p-GaN; electron traps

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1. Introduction

High electron mobility transistors (HEMTs) based on Gallium Nitride (GaN) are certainly becoming superior devices for high-frequency, high-voltage, and high-power applications with respect to their excellent physical properties [1] such as wide bandgap (3.4 eV), high breakdown voltage (3.3 MV/cm), and low permittivity. In addition, the GaN HEMT devices have low on-resistance [2], high power densities [3], and high breakdown voltages [4], which help design compact high-power RF and high-efficiency amplifiers [5]. Meanwhile, these excellent device performances are obtained with an AlGaN/GaN hetero-junction and the formation of a 2-dimensional electron gas (2DEG) between hetero-junctions, which has comparatively high charge density and high mobility at room temperature [6]. Moreover, these GaN power devices have an important role in power electronic applications (PEAs), which includes their usage in power adapters, battery chargers, load converters, PV, and motor drives [7–9]. With this wide range of applications for the GaN power electronic technology, the basic characteristic requirements such as good controllability, high efficiency, cost-effectiveness, and reliability are simultaneously increasing for power devices [10].

In the GaN HEMT power device structure, the 2DEG (with respect to the piezoelectric and spontaneous polarization of the GaN) [11] forms without any gate voltage, which confirms that the GaN devices are naturally depletion-mode (D-mode) or normally-on. Further,

the fabrication of enhancement-mode or normally-off (E-mode) GaN HEMT power devices is implemented by several methods: the combination of a metal-insulator-semiconductor (MIS) stack with the use of gate recess [12]; the integration of a series connection between the normally-on GaN HEMT and low-voltage Si Metal Oxide Semiconductor Field Effect Transistor (MOSFET) cascode package [13,14]; the fluorine implantation [15]; the oxide charge engineering [16]; and the use of a p-AlGaN [17] or p-GaN as p-type gate material [18], where the conduction band shifts towards up, and results a depletion for the channel of negative gate voltages. Among D-mode and E-mode GaN HEMTs, the E-mode device is preferred for most PEAs as it requires to evince a normally-off condition with large power range [19]. In recent years, the E-mode GaN with p-GaN gate power devices achieved very low resistance 10 mΩ for a 90 A commercial transistor (GaN—GS61008T) and with very low leakage current (100 nA at 650 V [20]). Typically, these achievements demand the E-mode GaN HEMT with p-GaN gate device to maintain efficient operation at high frequencies and hard switching conditions, which leads to device instability and low reliability. The reliability of the p-GaN gate HEMTs is one of its most considerable problems at present.

In this study, for the conditions of fail-safe and easy gate-control operation in use as power switches, a normally-off device is demonstrated by the use of a p-GaN layer. Figure 1 shows the most favorable schematic diagram of an E-mode GaN HEMT with a p-GaN gate. Even though the p-GaN demonstrates easy gate control V_{TH}, this method still lacks enough negative gate bias experiment studies to verify the V_{TH} stability and device degradation. Meantime, the p-GaN demonstrated E-mode GaN HEMT device instability behavior induced by the positive gate bias stress and off-state drain bias stress, and under hard switching operations, was well discussed and reported in several studies [21–23]. In this paper, we focused on studying the degradation and instability behavior of the device, which was induced by the negative gate bias stress in the form of pulsed and prolonged stress conditions at room temperature.

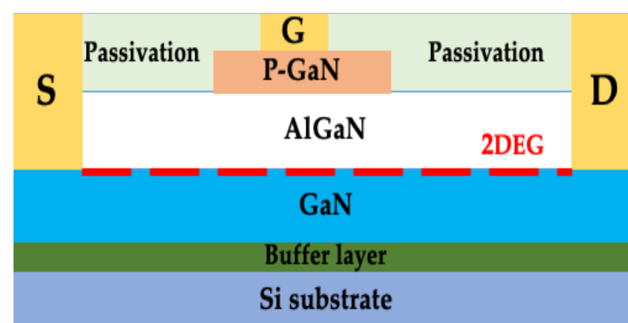

Figure 1. Most favorable schematic cross section of the E-mode GaN High Electron Mobility Transistor (HEMT) with p-GaN gate.

1.1. Gate-Lag Effect

The pulsed negative gate bias stress (Gate-Lag effect) is a phenomenon where the drain current shows slow transients for the sudden change in gate voltage, which results in a critical problem in both digital and analog applications. Under the short duty cycle of negative gate bias stress, the variation and degradation of device electrical parameters were reported for different power devices such as GaN- and SiC-based FETs [24,25]. In this case, the leakage of electrons from the gate channel for the respective pulsed negative V_{GS} bias stress is trapped and de-trapped by surface states, which is considered as a mechanism behind device degradation and instability issues. This pulsed negative V_{GS} bias stress modulates the negatively charged trap density with an increase in V_{GS} bias stress and increase in stress pulse (t_{stress}). However, the p-GaN gate HEMT device structure has no oxide layer compared with the MIS-HEMT device, which tells us that the reported surface state trapping mechanisms with oxide layer are not applicable here, although some

research on the reliability of commercialized E-mode GaN HEMT with p-GaN gate under reverse electrostatic discharge stress and repetitive short circuit stress has reported that the degradation mechanism could be addressed by the formation of traps at the barrier layer, p-GaN/AlGaN hetero-interface, and AlGaN/GaN interface [26,27]. At the present work, we studied the degradation behavior and mechanism for the impact of various negative gate stress voltage pulses without drain stress bias at room temperature.

1.2. Prolonged Negative Gate Bias Stress

Negative bias temperature instability (NBTI) was found to be the most important reliability issue for power transistors, such as GaN FET, HEMT and MIS-HEMT, and Si, SiC MOSFETs [28,29]. Negative gate bias (NBTI) studies on the MIS-HEMT devices already show that the V_{TH} instability is characterized by positive charge trapping at interface states or near interface traps. During NBTI stress conditions, the electron injection from the metal region into the gate dielectric region has been proven from dynamic and static measurements. The p-GaN HEMTs hold no dielectric layer above the p-GaN cap, indicating that the MIS-HEMT oxide layer quality issues are not considerable in the p-GaN gate HEMT structure for NBTI experiments. Further, the gate channel of p-GaN gate HEMTs represented as a back-to-back series connection between a Schottky junction ($J_{Schottky}$) and a p-i-n junction. In this p-GaN gate case, a peculiar conduction mechanism under prolonged negative gate bias stress conditions could cause device instability and degradation issues. However, few researches on device degradation and instability of p-GaN gate device under negative V_{GS} bias stress and off-state drain stress have been reported where the hole deficiency or positive charge deficiency in the p-GaN region has considered as a mechanism behind device degradation [30,31]. In this experiment, we focused on the relations between pulsed and prolonged stress induced device degradations and instability issues. Therefore, an in-depth investigation and comparison of p-GaN gate device degradation and instability under both pulsed and prolonged negative gate stress is of significance to accelerate the developments of emerging GaN power device technology.

This study aims to investigate the physical mechanisms behind the electrical parameter instabilities of the E-mode GaN with p-GaN under negative gate (V_{GS}) bias stress. In this paper, the dynamic trapping phenomena from the instability and degradation of E-mode GaN with p-GaN gate transistors under V_{GS} negative bias stresses are as follows: (i) double-pulsed V_{GS} bias stress, which might occur in a typical practical application such as half-bridge circuits, and (ii) prolonged V_{GS} bias stress (negative bias instability test), which continuously performed as a qualification reliability tests in semiconductor industries (High-Temperature Gate Bias). The device capability to withstand conditions over the negative gate bias with parameter degradation is one of the critical reliability issues. This paper contributes to an understanding of the dynamics of trapping process in E-mode GaN power switch with p-GaN under pulsed and prolonged negative V_{GS} bias stress.

2. Experimental Details

A commercially available E-mode HEMT with p-GaN gate switches (200 V breakdown voltage) was used to investigate the dynamic instability and static reliability. The device under test (DUT) made up of AlGaN barrier layer, p-GaN layer, GaN transition layer, and a GaN buffer layer is shown in the schematic diagram of p-GaN gate HEMT in Figure 1. At present, we have studied the footprint of negative gate stress conditions through the device electrical parameters defined in the linear and saturation operating regions at V_{DS} = 3 V. We focus our interest on the stability of V_{TH}, increase of $R_{DS\text{-}ON}$, degradation of $G_{m,\ max}$, and $I_{GS\text{-}Leakage}$. A fresh device is used in this study to exhibit electrical characteristics, which includes output characteristics (I_{DS}-V_{DS}), transfer characteristics (I_{DS}-V_{GS}), and gate leakage characteristics ($I_{GS\text{-}Leakage}$-V_{GS}) before the negative gate (V_{GS}) stress conditions, which are shown in Figure 2a,b. Thermally stable values of V_{TH} = 1.6 V (observed at linear region of I_{DS} = 0.05 A), $R_{DS\text{-}ON}$ = 25 mΩ (observed at saturation region of $I_{DS,\ Max}$ with V_{DS} = 3 V and V_{GS} = 6 V), $G_{m,\ max}$ =1.5 S (defined at V_{DS} = 3 V) and $I_{GS,\ Leakage}$ versus

V_{GS} characteristics (observed at V_{DS} = 3 V and V_{GS} from 0 V to 6 V) are confirmed with the data sheet. Further, fresh devices are put through to an extensive study of trapping or detrapping effect analysis under negative V_{GS} bias stress at room temperature. All double-pulsed and prolonged V_{GS} bias stress experiments were done with the Keithley 2651 A and 2601 A source meter systems.

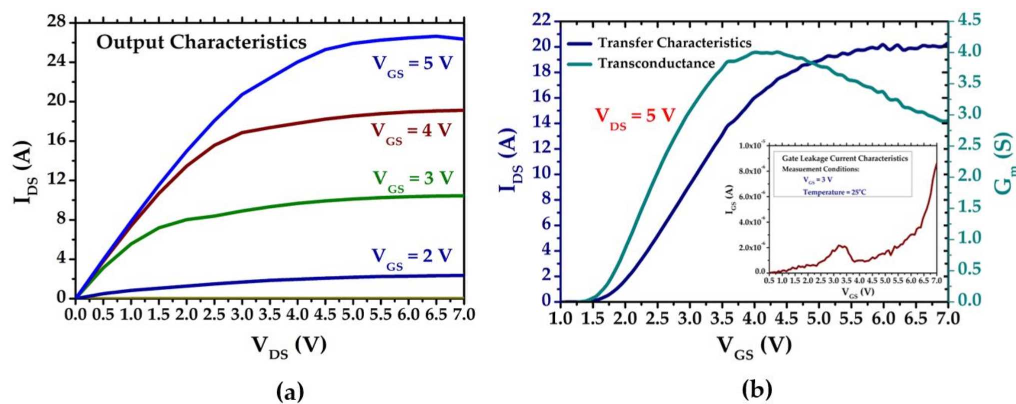

Figure 2. Representative of commercialized 200 V E-mode GaN power HEMT switch fresh electrical characteristics at room temperature: (**a**) output characteristics and (**b**) transfer characteristics.

In the pulsed negative V_{GS} bias stress experiment, we studied the effect of pulsed negative gate bias stress conditions from the device parameter instability and degradation. A double pulse experiment technique was explored and used in the pulsed negative V_{GS} bias stress experiment [32,33]. Device electrical parameters, such as V_{TH} shift, $I_{DS, Max}$ or $R_{DS\text{-}ON}$ degradation, $I_{GS\text{-}Leakage}$ increase, and $G_{m, max}$, were investigated under pulsed V_{GS} bias stress through two regimes of stress conditions. In the first regime, the influence of low pulsed V_{GS} stress on the device electrical parameters of the DUT was obtained, where the pulsed stress V_{GS} bias = −1 to −3 V and V_{DS} = 3 V at room temperature. At the another regime, an increase in mid/high-stress voltages is studied for DUT, where the pulsed V_{GS} bias stress = −5 V to −30 V and V_{DS} = 3 V at room temperature. The reason for the large or harsh negative gate bias stress experiments is to observe the gate terminal stability level and variations in degradation phenomena of the device. Using a double pulse technique for each negative V_{GS} pulse on DUT, the device stressed at Off-State for 300 ms and the on-state V_{GS} pulse given for 300 µs. During each negative V_{GS} bias pulse, both drain and source terminals are grounded with V_{DS} = 0 V. The waveform for pulsed negative V_{GS} bias stress experiments on the p-GaN gate HEMT device is shown in the Figure 3a.

In the prolonged negative V_{GS} bias stress experiment, the stress time (t_{stress}) of mid/high stress voltages was increased to observe device instability and degradation [34]. The negative gate bias instability on the E-mode GaN with p-GaN device at room temperature was studied. Under prolonged negative V_{GS} bias stress, both the drain and source terminals are grounded with V_{DS} = 0 V. From the studies of pulsed V_{GS} stress experiment, the device is selectively subjected to the mid/high V_{GS} bias stress from −10 V to −20 V. From the literature, under high negative gate bias stress, GaN-based powered devices have shown significant variation in degradation phenomena as stress voltage increases [28,34]. Based on previous studies, in this experiment the devices are subjected and studied with high stress voltage to ensure the gate terminal withstandability and degradation phenomena under harsh stress conditions. As we show below, for a harsh stress condition (such as −20 V), there is non-recoverable damage at room temperature after stress compared to low/mid stress conditions. For each prolonged negative V_{GS} bias stress, different devices are used. Similar to the pulsed V_{GS} stress experiment, the device initially characterized for fresh/virgin transfer characteristics with V_{DS} = 3 V. Further, the device was subjected to V_{GS} bias stress for 10,000 s. During the DUT stress phase, transfer characteristics were obtained at every 1000 s interval to extract V_{TH} shift, $I_{DS, Max}$ or $R_{DS\text{-}ON}$ degradation, $G_{m, max}$

degradation, and $I_{GS\text{-}Leakage}$ characteristics. The waveform for prolonged negative V_{GS} bias stress experiments on the E-mode GaN power HEMT device is shown in Figure 3b.

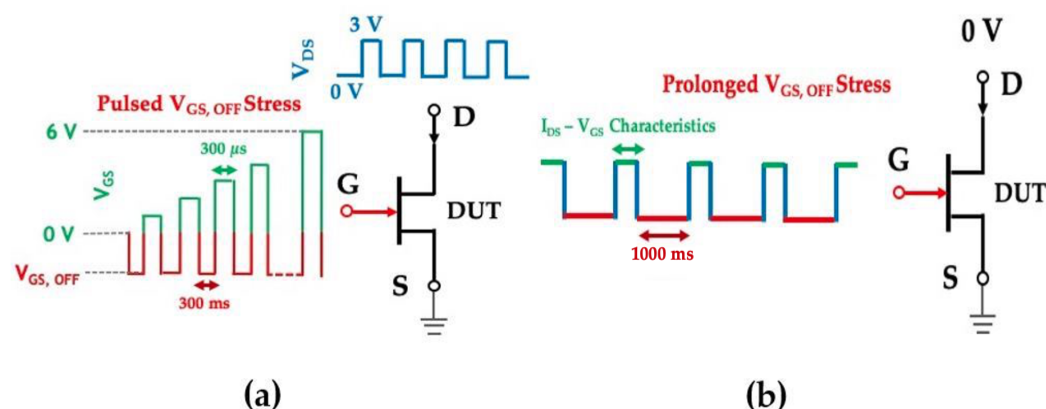

Figure 3. Schematic stress waveform of negative gate stress applied on E-mode GaN power HEMT with p-GaN device under test: (**a**) Pulsed Negative Gate Bias Stress and (**b**) Prolonged Negative Gate Bias Stress.

3. Results and Discussion

3.1. Degradation of Electrical Parameters under Pulsed V_{GS} Bias Stress

Figure 4a shows the extracted $\triangle V_{TH}$ and $\triangle G_{m,\,max}$ for different pulsed negative V_{GS} bias stress (V_{GS} bias = −1 V to −5 V & V_{DS} = 3 V, room temperature) according to the preliminary data sheet standards. $\triangle R_{DS\text{-}ON}$ and $I_{GS\text{-}Leakage}$ were extracted and shown in Figure 4b. The degradation parameters $\triangle V_{TH}$, $\triangle G_{m,\,max}$, and $\triangle R_{DS\text{-}ON}$ are normalized values of V_{TH}, $G_{m,\,max}$, and $R_{DS\text{-}ON}$ (defined at V_{TH} stress/VTH fresh), respectively. The transfer characteristics curve shifts in the positive direction with minimal significance under the low-voltage stress conditions, which results in an increase in the $\triangle V_{TH}$ from 1 V to 1.11 V with respect to change in stress voltage. At the same time, the $\triangle G_{m,\,max}$ of the device decreases from 1 S to 0.90 S and $\triangle R_{DS\text{-}ON}$ increases from 1 Ω to 1.04 Ω. Overall, the p-GaN gate HEMT, under the low stress voltage condition, show negligible and easily recoverable degradation at room temperature.

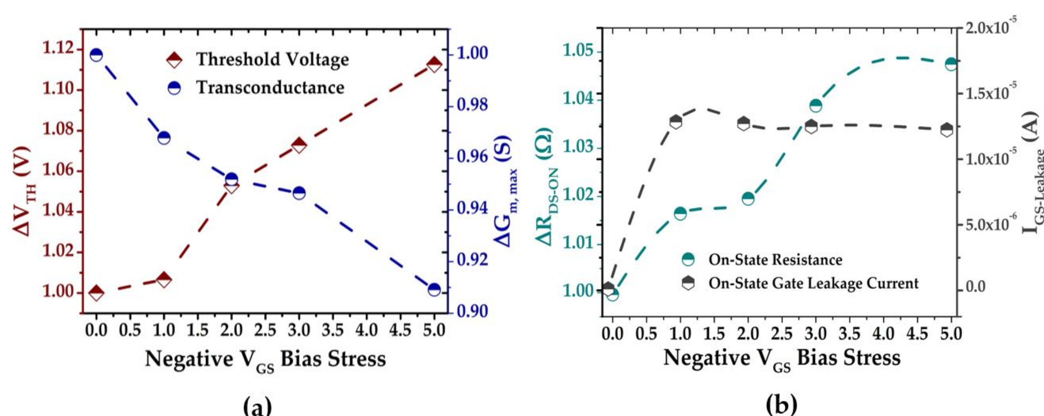

Figure 4. Extracted (**a**) $\triangle V_{TH}$ and $\triangle G_{m,\,max}$ and (**b**) $\triangle R_{DS\text{-}ON}$ and $I_{GS\text{-}Leakage}$ under low-voltage pulsed stress conditions.

In parallel, the impact of high negative pulsed V_{GS} bias stress (V_{GS} Bias = −10 to −30 V and V_{DS} = 3 V at room temperature), investigated through the transfer curve characteristics, is shown in Figure 5a. Further, the extracted $\triangle V_{TH}$ and $\triangle G_{m,\,max}$ under constant voltage (V_{DS} = 3 V) is shown in Figure 5b. The transfer characteristics curve shows the shifts towards positive direction quickly for the increase in negative V_{GS} bias stress, and the

normalized $\triangle V_{TH}$ shift from 1 V to 1.71 V. From Figure 5b, the normalized $\triangle G_{m,\ max}$ degrades rapidly from 1 S to 0.61 S after the increase in stress. In general, the V_{TH} of p-GaN gate HEMT device varies based on the inflow of holes from the $J_{Schottky}$ (Schottky junction) to outflow of holes through PN junction (p-GaN/2DEG). Therefore, the V_{TH} shift obtained due to the trapping effect is close to the gate region for the V_{GS} bias stress. In addition, Figure 5c shows the variation of $\triangle R_{DS\text{-}ON}$ under high stress conditions, which is extracted at V_{GS} = 6 V (On-State). The conductivity of the device decreases very rapidly with increase in negative stress voltage, whereas the normalized $\triangle R_{DS\text{-}ON}$ increases from 1 Ω to 1.36 Ω after −30 V stress. Usually, the degradation of the $R_{DS\text{-}ON}$ could be caused by influence of traps in the gate region. It can be addressed that the dynamic trapping or detrapping process takes place in the gate channel region under negative V_{GS} bias stress which causes the increases in $R_{DS\text{-}ON}$ with the shift of V_{TH}. Figure 5d shows the gate leakage current characteristics of the device were studied with different negative V_{GS} bias stress (V_{GS} bias = −10 V to −30 V and V_{DS} = 3 V at room temperature). Up to V_{GS} = 1.5 V, the $I_{GS\text{-}Leakage}$ is very minimal and negligible. Moreover, the gate leakage current increases slightly for each step gate voltage under the device's semi-on- and on-state.

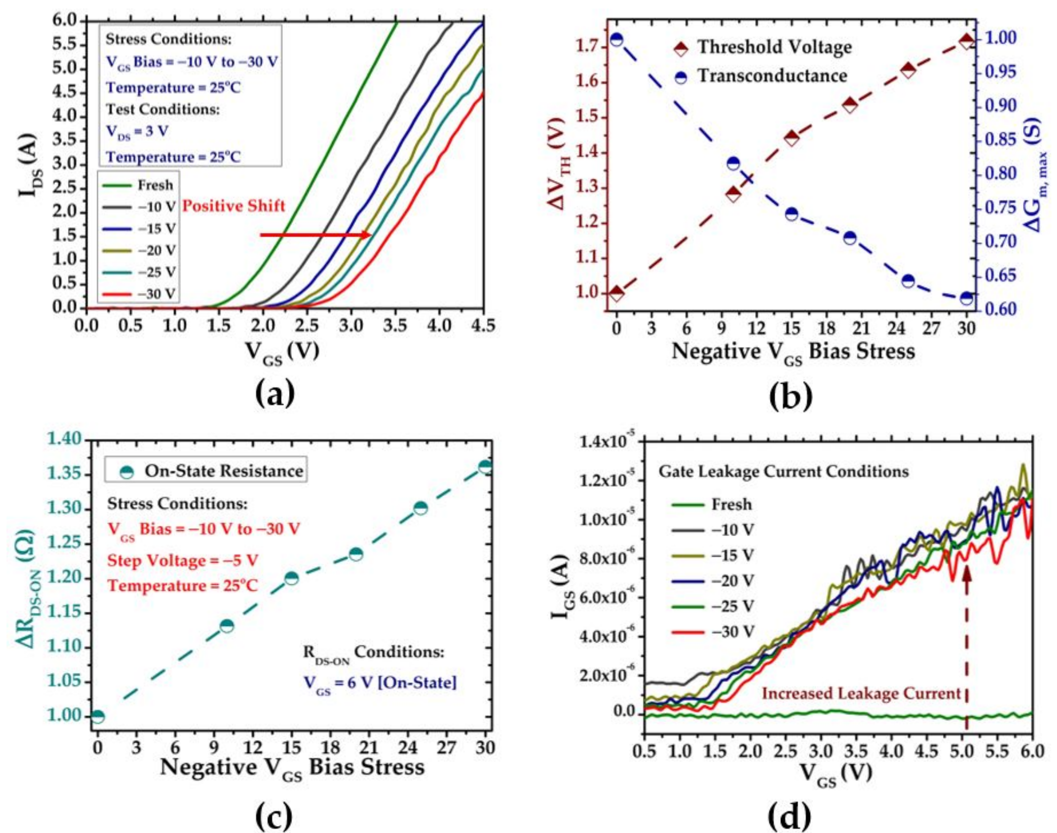

Figure 5. (**a**) Extracted Transfer Characteristics of p-GaN HEMT, (**b**) extracted $\triangle G_{m,\ max}$ and $\triangle V_{TH}$, (**c**) extracted $\triangle R_{DS\text{-}ON}$ and (**d**) $I_{GS\text{-}Leakage}$ under high voltage pulsed stress conditions.

3.2. Influence of Stress Time Evolution on Negative V_{GS} Bias Stresses

The gate stress investigations show the influences of the mentioned instability and degradation of the device on the designers, which could directly affect the reliability of the system. At this experiment, the impact of various negative V_{GS} bias stresses with respect to stress time evolution was investigated. Usually, the high negative gate bias stress (V_{GS} bias = −10 V, −15 V, and −20 V) phases are not carried always in the most of the systems. However, these high values of gate bias stress show a notable effect on the device degradation and stability due to the trapping or detrapping task, which needs to be studied.

Figure 6a,b shows the extracted normalized $\triangle V_{TH}$ shift and recovery, and Figure 6c,d shows the extracted normalized $\triangle R_{DS\text{-}ON}$ degradation and recovery. The instability of V_{TH} and degradation of $R_{DS\text{-}ON}$ are very minimal and fully recoverable at −5 V stress conditions. Further, these two electrical parameters are shown to be increasing as the magnitude of negative V_{GS} bias stress increases. However, with increasing stress time, the device shows a gradual increase in $\triangle R_{DS\text{-}ON}$ and the saturation of V_{TH} degradation at each stress bias. In this, the $\triangle V_{TH}$ initially shows the strong increase from 1 V to 1.6 V after 10^3 s stress and further increased minimal from 1.6 V to 1.98 V after 10^3 s to 10^4 s stress under a −20 V stress condition. The rapid increase in V_{TH} at beginning shows the device's strong dependence on stress voltage over stress time. At such a high stress voltage condition, the device does not show full recovery under room temperature compared to other stress voltage conditions. Similarly, the conductivity of the device is strongly affected by high stress condition, whereas the $\triangle R_{DS\text{-}ON}$ increased from 1 Ω to 2.17 Ω within 10^4 s of stress. The $\triangle R_{DS\text{-}ON}$ of the device shows full recovery under room temperature, which is shown in Figure 6d. The influence of stress time evolution on the gate leakage characteristics under mid/high prolonged negative V_{GS} bias stresses is shown in the Figure 7a. Figure 7b shows the influence of stress voltage on $I_{GS\text{-}Leakage}$ versus gate bias with V_{DS} = 3 V at room temperature. The gate current leakage over stress time for various stress voltages reveals that the $I_{GS\text{-}Leakage}$ has no changes with respect to increase in stress time. Further, a very minimal and negligible increase in the $I_{GS\text{-}Leakage}$ versus gate bias for various stress voltages is shown in Figure 7b. The pulsed negative V_{GS} bias stress shows the strong impact on the device $I_{GS\text{-}Leakage}$ compared to the prolonged stress conditions.

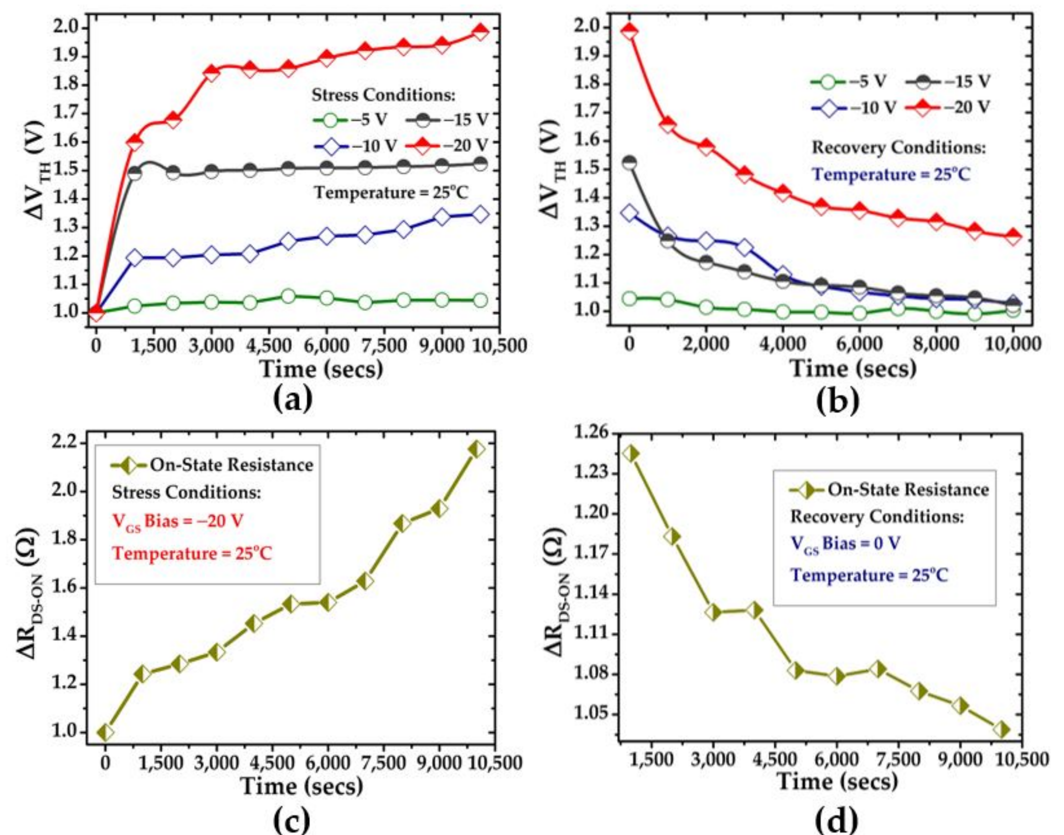

Figure 6. Extracted (**a**) $\triangle V_{TH}$ shift under stress conditions , (**b**) $\triangle V_{TH}$ recovery under room temperature, (**c**) extracted $\triangle R_{DS\text{-}ON}$ degradation under stress conditions, and (**d**) $\triangle R_{DS\text{-}ON}$ recovery under room temperature.

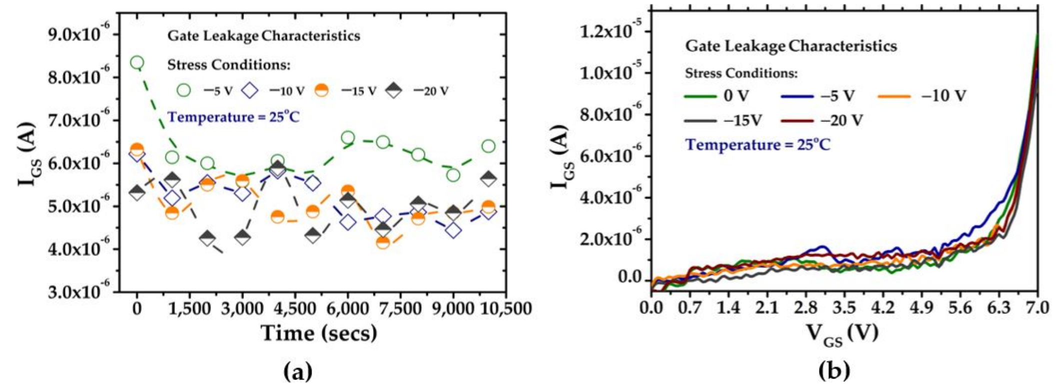

Figure 7. The gate leakage characteristics of p-GaN gate HEMT as a function of (**a**) stress time and (**b**) stress voltages during prolonged negative V_{GS} bias stress.

3.3. *Influenced Degradation Mechanism and Analyzations*

The GaN-based HEMT device holds several kinds of traps, which exist in the p-GaN region, the AlGaN barrier layer of the device, and the hetero-structure interface [35,36], such as G_a vacancy (VG_a), Ga-N divacancy (VG_a-V_N) or oxygen impurity centers (O_N), gallium antisite (NG_a), or N vacancy (V_N) [37]. Figure 8 shows the schematic p-GaN gate HEMT device diagram with trap states before stress conditions. According to the degraded electrical parameters under the negative V_{GS} bias stress conditions in the p-GaN gate device, the degradation mechanisms are significantly influenced by trapping process under the gate region. The keen degradation and instabilities of electrical parameters under negative gate bias stress take place at room temperature, which could to be caused by hole deficiency and p-GaN/AlGAN interface traps. Therefore, the p-GaN gate-modeled HEMT structure is further subjected to in detail investigation for the above-mentioned device degradation mechanisms.

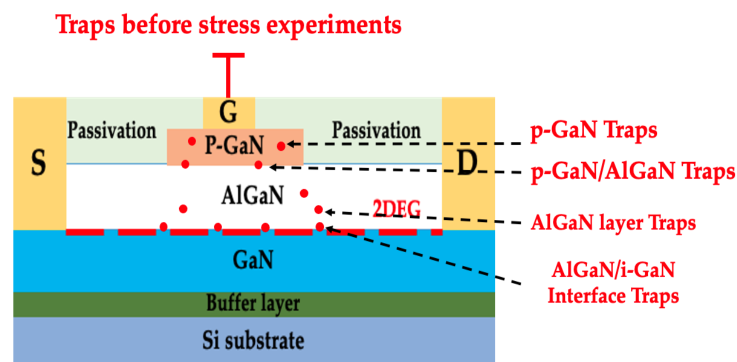

Figure 8. Schematic cross section of p-GaN HEMT device with traps in fresh device before stress conditions.

The physical mechanism behind the degradation effects for pulsed and prolonged V_{GS} bias stress on the p-GaN gate HEMT is explained in the Figure 9a,b. In view of the Schottky gate contact of the studied device, where the metal/p-GaN hetero-structure acts as Schottky junction diode and the p-GaN/AlGaN/GaN structure acts as p-i-n junction diode, and respective junction capacitances [38,39]. Under negative gate bias, the $J_{Schottky}$ is forward biased, with small voltage drop on it. The p-i-n junction has reverse bias under negative gate bias stress, and all the voltage drops on the p-i-n junction (p-GaN/AlGaN/GaN). A small depletion takes place under stress conditions, where p-GaN is nearby the barrier layer AlGaN. As a result, the removal of holes flows from the depletion region in p-GaN to the gate region, and the p-i-n junction capacitor is charged which is shown in Figure 9a. Some of the donor-type holes at the p-GaN/AlGaN interface trao state also released under this charge process. When the gate bias switched to the positive level, the reduced charges

at the p-GaN and interface of p-GaN/AlGaN are not immediately restored, which plays a strong role in the positive shift of threshold voltage (V_{TH}), increase of on-state resistance ($R_{DS\text{-}ON}$), and degradation of transconductance ($G_{m,\,max}$). As the magnitude of stress voltage is increased, the high order of hole deficiency takes place in the strong instability and degradations. As the stress time increases, the formation of the built-in electric potential by ionizing the donor-type holes will reduce the holes' deficiency from the trap state, which leads to the saturation of the V_{TH} shift degradation degree. Under the negative gate bias stress condition, the release of donor type holes from the p-GaN/AlGaN interface trap state by the reverse biased p-i-n junction capacitor charge process is not modulated due to the lack of an electron injection or recombination process under V_{GS} stress bias. Meanwhile, the acceptor-like traps at the AlGaN/i-GaN interface and the buffer layer are also very difficult to activate as the electric potential is very low at buffer layer and the drain bias is zero during negative gate bias stress. At this point, detrapping the activated donor-type traps from the interface (p-GaN/AlGaN) and holes from gate region could primarily influence the electrical parameters degradation and instabilities. If the gate bias increases more negative, the number of released holes from the p-GaN and p-GaN/AlGaN trap state will be increased, which results in more significant degradations and instabilities. This agrees with the results shown in both pulsed and prolonged negative gate bias stress experiment as shown in the Figures 5 and 6.

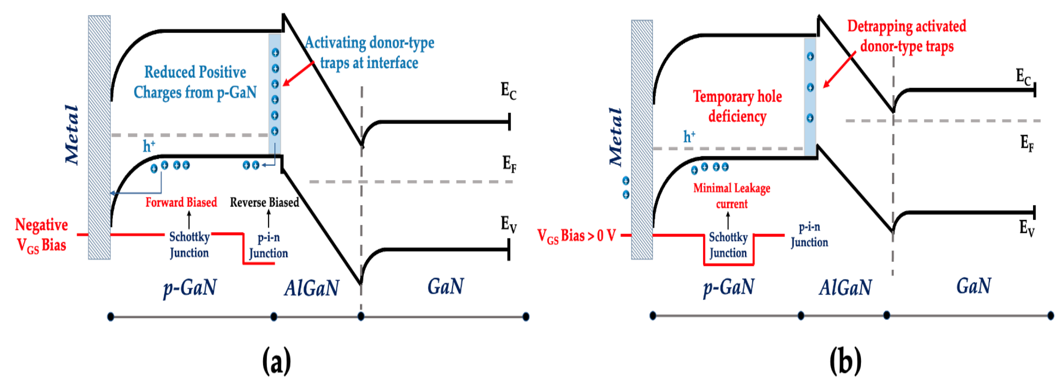

Figure 9. Band diagram of the p-GaN gate HEMT (**a**) device under negative gate bias stress condition and the (**b**) device after stress condition under turn-on state.

4. Conclusions

In summary, we have investigated the static electrical performances of E-mode GaN HEMTs with p-GaN gate under negative V_{GS} bias stresses as well as the physics-based mechanism behind the device degradation. The existence holes trapping at the gate region can play a role in the positive shift of the V_{TH}, increase of the $R_{DS\text{-}ON}$, decrease of the $G_{m,\,max}$, and the increase of the $I_{GS\text{-}Leakage}$. Under prolonged negative V_{GS} bias stress, the ionization of donor-type holes occurs at the p-GaN/AlGaN interface trap state, which results in a saturation of the degree of V_{TH} positive shift over the stress time evolution. Meanwhile, the on-state resistance under prolonged stress simultaneously increases with evolution of both the magnitude of the stress voltage and stress time. The extracted values for both pulsed and prolonged stress experiments show great agreement with the dominant degradation mechanisms. To achieve long-term system stability and reliability, more attention needs to be paid to the importance of electrical degradation, which is affected by a negative gate bias stress condition. This paper gives an understanding of the E-mode GaN HEMT with p-GaN gate devices, static reliability, and dynamic instability issues for system designers to avoid unsuitable negative bias conditions.

Author Contributions: Conceptualization, methodology, formal analysis, investigation, data curation, and writing—original draft preparation, S.E.; writing—review and editing, validation, super-

vision, funding acquisition, and project administration, S.C.; visualization and resources E.Y.C. All authors have read and agreed to the published version manuscript.

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