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Analytic Model of Threshold Voltage (V_{TH}) Recovery in Fully Recessed Gate MOS-Channel HEMT (High Electron Mobility Transistor) after OFF-State Drain Stress

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Abstract: Today, wide bandgap (WBG) GaN semiconductors are considered the future, allowing the improvement of power transistors. The main advantage of GaN is the presence of two-dimensional electron gas (2Deg) typically used as a conduction layer in normally-on and normally-off transistors. Concerning the normally-off family, several solutions are proposed. Among these, one of the most promising is the MIS-Gate technology that features a gate recess architecture allowing the semiconductor to physically cut off the 2Deg and drastically decrease gate–source leakage currents. The Vth relaxation characteristic, after voltage stress, has been investigated. It has been shown that the main impact is due to charges close to the gate dielectric/GaN interface, precisely dwelling within the dielectric or the GaN epitaxy. This work provides an analytical model of the Vth evolution of these MIS-GATE (metal insulator semiconductor gate) transistors fabricated on GaN-silicon substrate. This model allows the extraction of different trap energy levels from a temporary threshold voltage (Vth) shift after 650 V stress. Based on this method, it is possible to identify up to four different trap energy levels. By comparing state of the art methods, we show that these obtained energy levels are well correlated with either magnesium and carbon impurity or Ga and/or N vacancy sites in the GaN epitaxy.

Keywords: gallium nitride; MIS-Gate; charges; alumina; traps; threshold voltage; recovery; normally-off

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1. Introduction

The new generation of WBG HEMTs (high electron mobility transistor) featuring a recessed gate are very attractive in terms of the Vth/Ron trade-off. Nevertheless, during their fabrication, the critical gate etching step can create local degradation of the underlying GaN epitaxy. The defects can be in the form of dangling bonds that generate traps at the interface between the gate insulator and GaN material. To avoid the presence of contamination, the gate etching process is followed by several cleaning steps such as NH_4OH+HF at 65 °C preceding the gate insulator deposition. Theoretical device modeling shows that transistor threshold voltage should be greater than 1.3 V, but experimental results show a value of 0.8 V (Vth is extracted at Id = 10 µA/mm for Vds = 0.5 V (Note: This extraction method will be used throughout the remainder of the text). This difference could be explained by the presence of charges in the material and/or in the interfaces. Several authors have justified it with the presence of trap and interface states at the different interfaces of the MIS Gate stack (Al_2O_3/AlN/GaN [1,2] and Al_2O_3/AlGaN/GaN [3]), but

the link between these charges and the Vth evolution in time has never been explained by a simple analytic model. Therefore, a new method of energy level extraction based on the study of Vth recovery after blocking voltage stress is proposed here. The model supposes that the existence of kinetic phenomena is related to the positive and negative charges that interact with traps featuring different time constants or equally different energy levels in the E_{gap}. The present study links the kinetics with trap energy levels already reported in the literature. Furthermore, the physical origin of charge trapping was proposed; finally, the combination of positive and negative charge storage at the interface between Al_2O_3/GaN as well as in the GaN Bulk can explain the Vth shift and recovery in the time.

2. Materials and Methods

The fabricated MIS Gate transistor used in this work features an AlGaN/GaN heterostructure grown on a 200 mm Silicon (111) substrate by metal–organic chemical vapor deposition (MOCVD). The gallium and nitrogen precursors are TriMethylGallium (TMG) and ammonia (NH_3), respectively. The epitaxial wafer consisted of, from bottom to top, a nucleation layer, a several µm-thick GaN buffer doped with Carbon and a channel layer, a spacer layer and an AlGaN barrier layer. A SiN isolation layer is deposited at the end by the reactor. No intentional N doping process is performed during the MOCVD growth. The Gate–Drain distance and the gate length are designed to sustain 650 V stress. The recessed gate architecture, obtained by ALE through AlGaN and within the GaN, allows the fabrication of a normally-off transistor. This recess step is immediately followed by surface cleaning and by a thin layer of insulator material and finally by an Al_2O_3 insulator deposition carried out by atomic layer deposition (ALD); detail of process gate recess is described in a paper by R. Kom Kammeugne [4].

At the end of the process, metallization is used for the gate metal formation. Low-temperature Ti/Al fully recessed ohmic contact are formed at the source/drain electrodes. Device processing is finalized by a single interconnect metallization layer encapsulated by a thick passivation layer (Figures 1 and 2).

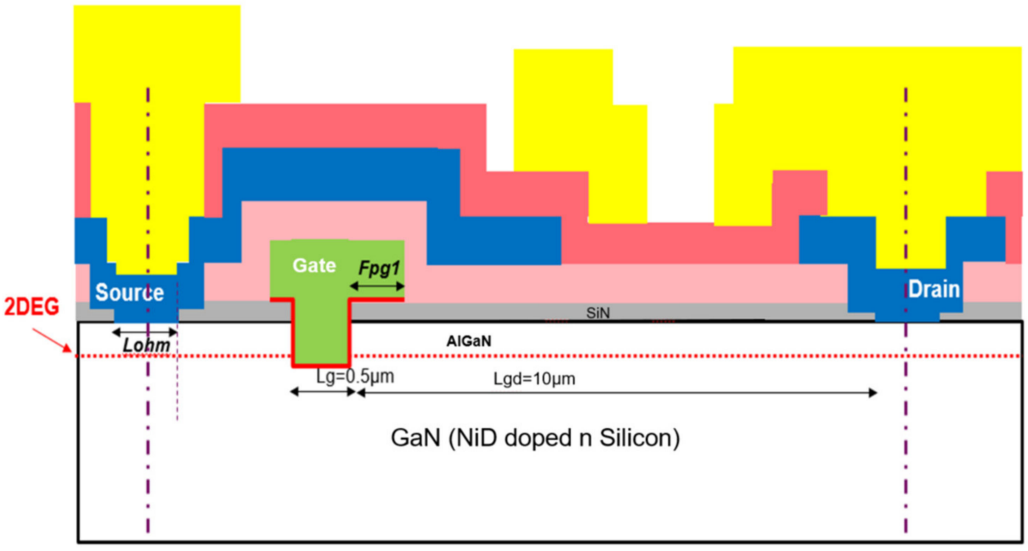

Figure 1. Cross-section of device study.

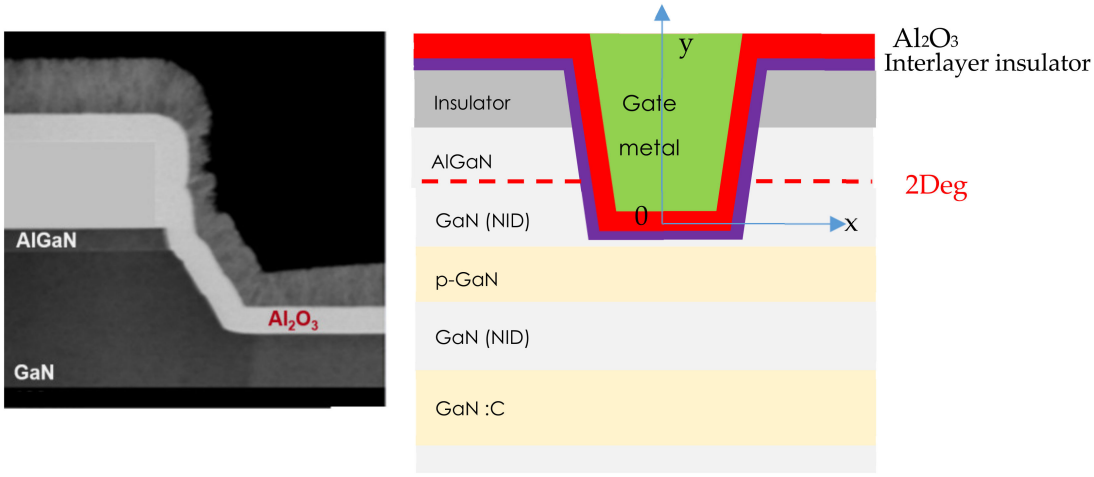

Figure 2. Detailed cross-section of metal insulated semiconductor gate (MISGate). TEM image and layers stack description.

3. Theory and Results

This work proposes an analytical approach of Vth evolution as a function of time induced by charge kinetics around the gate dielectric. The parameters of the model are extracted by fitting experimental measurements at 25, 75 and 150 °C, respectively, after blocking stress voltage. After stress, and therefore during relaxation, the Vth value is extracted at regular time intervals at a constant current value Id = 1×10^{-5} A/mm from the on-state measurement of the Id(Vgs) characteristics at Vds = 0.5 V. We observe a shift (positive or negative) of the Vth value in the time. These variations are due to charges de-trapping phenomena allowing the device to return to its original state (i.e., before stress).

3.1. Theory of Vth Computation

Based on Tapajna's model [1], the electrostatic effect of charges on the threshold voltage can be simplified and written as a sum of the following terms (1).

$$V_{th} = \varnothing_b - \Delta E_C - \varnothing_F - q \cdot \sum t_{mat}/\varepsilon_{mat}(N_{pos\_charges} - N_{neg\_charges}) \quad (1)$$

With $\varnothing_b$ the gate metal work function, ΔE_c the conduction band discontinuity for Al_2O_3/GaN interface, $\varnothing_F$ the energy difference between the conduction band and Fermi level of the semiconductor material, t_{mat} and ε_{mat} the thickness and permittivity of dielectric material, respectively, $N_{pos\_charges} - N_{neg\_charges}$ the net charge density at the edge of the material. The first part of the equation ($\varnothing_b - \Delta E_C - \varnothing_F$) is approximately equal to 1.34 eV considering a metal work function of 5.6 eV [5]. Note that this value is generally not obtained directly from the experimental results due to the presence of the other terms of the equation. The second part of the equation, the trapping charge dependency, is extracted using the information from the Vth characteristic measured during relaxation. It is clear that these charges (traps) are close to the gate stack in order to influence the Vth value. Three distinct areas can dwell on the charges (Figure 3).

The first ones are in the gate oxide, and it is known that in Al_2O_3 oxide, deposited by ALD, negative charges are present in the volume [1,6–8]. The second type of charges are localized at the interface of the dielectric and GaN semiconductor. They are fully dependent on recess quality, cleaning chemistry, and the method and materials used for dielectric deposition. The third kind of charges are present in the GaN bulk close to Al_2O_3/GaN interface. We suppose that charges in Al_2O_3 are trapped at the interface with GaN. They can be either positive or negative.

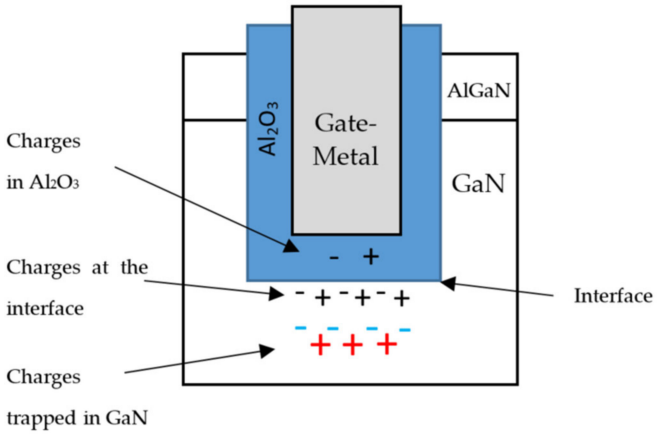

Figure 3. Location of charges around the gate.

To summarize, the positive charges are coming from GaN bulk, and negative charges have several origins and are mainly present in Al_2O_3, but also at the Al_2O_3/GaN interface as well as in GaN bulk.

Based on the Shockley–Read–Hall recombination equation and assuming a uniform traps distribution, we can write the kinetics of charge de-trapping for a single trap level as [3].

$$dn = -K.n.dt \tag{2}$$

where

$$K = Cte\ (constant) \tag{3}$$

Assuming N_t is the trap density with a trap effective cross-section of σ_t, n being the trapped charge density and by taking into account the de-trapping processes from Equation (2), we can write:

$$dn = \left(\frac{J(E)\sigma_t}{q}(N_t - n) - K.n\right)dt \tag{4}$$

Considering that $J(E)$ (density of leakage current) is constant in the time of stress:

$$A = \frac{J(E)\sigma_t}{q}.(N_t - n) \tag{5}$$

The solution of Equation (5) is:

$$n(t) = B.[1 - \exp(-(A + K)t)] \tag{6}$$

with

$$\mathrm{B} = \frac{A.N_t}{A + K} \tag{7}$$

Equation (6) is generalizable for positive and negative charges, whatever their localization. In addition, to take into account the presence of several energy levels, we must consider at least two levels of donor traps and two levels of acceptor traps.

$$n_i(t) = \sum_{i=1}^{i=4} B_i.[1 - \exp(-A_i.t)] \tag{8}$$

as

$$V_{th}(t) = Cte\ .\ n(t) \tag{9}$$

To summarize, the global Vth evolution during recovery can be approximated with the sum of four equations similar to Equation (6).

$$V_{th}(t) = Cte \,.\sum_{i=1}^{i=4} n_i(t) \tag{10}$$

$$V_{th}(t) = Cte.\{\sum_{i=1}^{i=4} B_i.[1 - \exp(-A_i.t)]\} \tag{11}$$

$$V_{th}(t) = Cte - \sum_{i=1}^{i=4} [B_i.\exp(-A_i.t)] \tag{12}$$

where B_i are the initially trapped charge densities (just after high voltage (Vds) stress) and 1/Ai are characteristic trapping time constants for each energy level.

Several methods can be used to extract the interface charge between an insulator and semiconductor [6–11], and it has been shown that the trap density Nt, between Al_2O_3 (ALD)/Interlayer/GaN, is in the range of 1×10^{11} to 1×10^{12} cm^{-2}/eV with Ec-Etrap energy between 0.3 eV and 0.52 eV [2,12].

3.2. Traps Location around the Gate

Positive and negative interface charges are dependent on the applied Vds voltage, time stress and temperature [13,14]. These charges are successively trapped and de-trapped during and after the stress. The trapping phenomena are dependent on the current injection, J(E), density and effective section of traps and traps density still empty (Nt–n).

Positive charges in the GaN are, for example, due to Carbon doping (p-doped) usually introduced during the epitaxy process to compensate for unintentional Silicon doping (n-doped). Another hypothesis is linked to the Ga Vacancy in the GaN bulk. The dynamic of the hole follows the de-trapping law for one level of energy which is given by:

$$\text{Nhole(t)} = \text{Nhole}_{\text{initial}} \times \exp(-\text{t}/\text{tau\_hole}) \tag{13}$$

$$\text{Nelec(t)} = \text{Nelec}_{\text{initial}} \times \exp(-\text{t}/\text{tau\_elec}) \tag{14}$$

where:

tau_hole (s), tau_elec (s) are the de-trapping characteristic times constant for positive and negative charges, respectively.
$\text{Nhole}_{\text{initial}}$ (cm^{-3}) and $\text{Nelec}_{\text{initial}}$ (cm^{-3}) are the densities of positive and negative charges initially trapped at a given level after Vds stress.
Nhole(t) (cm^{-3}) and Nelec(t) (cm^{-3}) are the densities of positive and negative charges at a given level after recovery time t.
t (s) is the recovery time after stress.

The goal of the measurement is to extract (from Vth recovery characteristics) the values of tau_elec and tau_hole for each energy level.

By replacing "Bi" in Equation (12) with N_(hole1_t) and N_(elec1_t) and by replacing "Ai" $(\text{tau1\_hole})^{-1}$ and $(\text{tau1\_elec})^{-1}$ and using Equations (13) and (14), we obtain Equation (15) which gives the Vth shift in the function of charges recovery.

$$\Delta\text{Vth} = \text{Cte} - \sum_{i=1}^{i=2} \left[\left(Nhole_i - Nhole_{initial_i}\right) - \left(Nelec_i - Nelec_{initial_i}\right)\right] \tag{15}$$

This model is based on the Vth shift (ΔVth), so it takes into account charges trapped and de-trapped during the test protocol and ignores charge fixes already present before and after a sequence of tests.

3.3. Test Protocol

We have measured the Vth to set parameters after Vds stress from 0 to 650 V. The devices studied are MISHEMT transistors designed for Vdsmax > 650 V and Id = 30 A. To take into account the de-trapping phenomena as a function of temperature shown in

relation (2) we have carried out measurements at room temperatures of 75 °C and 150 °C, respectively.

The test protocol consists of four main steps:

a. Id(Vgs) at Vds = 0.5 V with Vgs varying from −2 to 6 V and a Vth extraction at 10 µA/mm (Figure 4).
b. Id(Vds) at Vgs = −2 V and Vds varying from 0 to 650 V corresponding to a stress in blocking mode during 10 s.
c. Id(Vgs) at Vds = 0.5 V with Vgs varying from −2 to 6 V with Vth extraction carried out at 10 µA/mm. Allows us to measure the Vth in the GaN material after the Vds stress.
d. Step c/ is repeated for several hours to follow the recovery time of the transistor due to the de-trapping of electrons and holes.

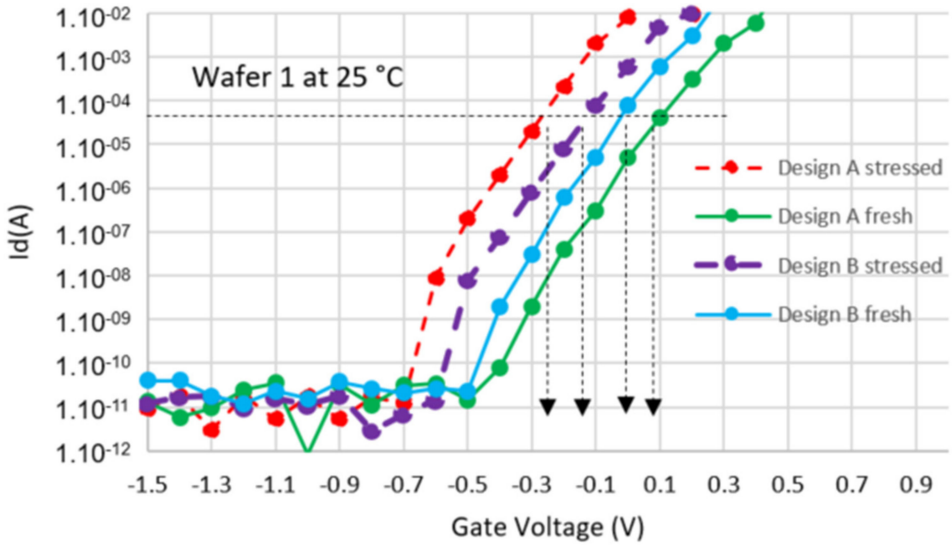

Figure 4. Example of Vth shift for two different devices named design A and design B before and after 650 V stress during 10 s.

These measurements are performed at room temperatures of 75 °C and 150 °C to take into account de-trapping speed as a function of temperature.

For confidential reasons, we define an arbitrary length of gate Lg_ref and a distance between gate and drain named Lgd_ref.

Two designs have been studied (Table 1): Design A features a gate length of 2 × Lg_ref and a gate to drain distance of 1.5 × Lgd_ref, and Design B features a Lg_ref and Lgd_ref. Moreover, for both designs, two different interlayer thicknesses are considered, which corresponds to wafers 1 and 2, respectively.

Table 1. Split wafer description.

Wafer and Design Name	Lg (µm)	Lgd (µm)	Interlayer (nm)	Al_2O_3 (nm)
wafer 1, design A	2 Lg_ref	1.5 Lgd_ref	3 Thick_ref	~30
wafer 1, design B	Lg_ref	Lgd_ref	3 Thick_ref	~30
wafer 2, design A	2 Lg_ref	1.5 Lgd_ref	Thick_ref	~30
wafer 2, design B	Lg_ref	Lgd_ref	Thick_ref	~30

3.4. Experimental Results

As reported in Figure 5, the analytical model, based on the sum of exponentials, allows us to reproduce the experimental characteristic.

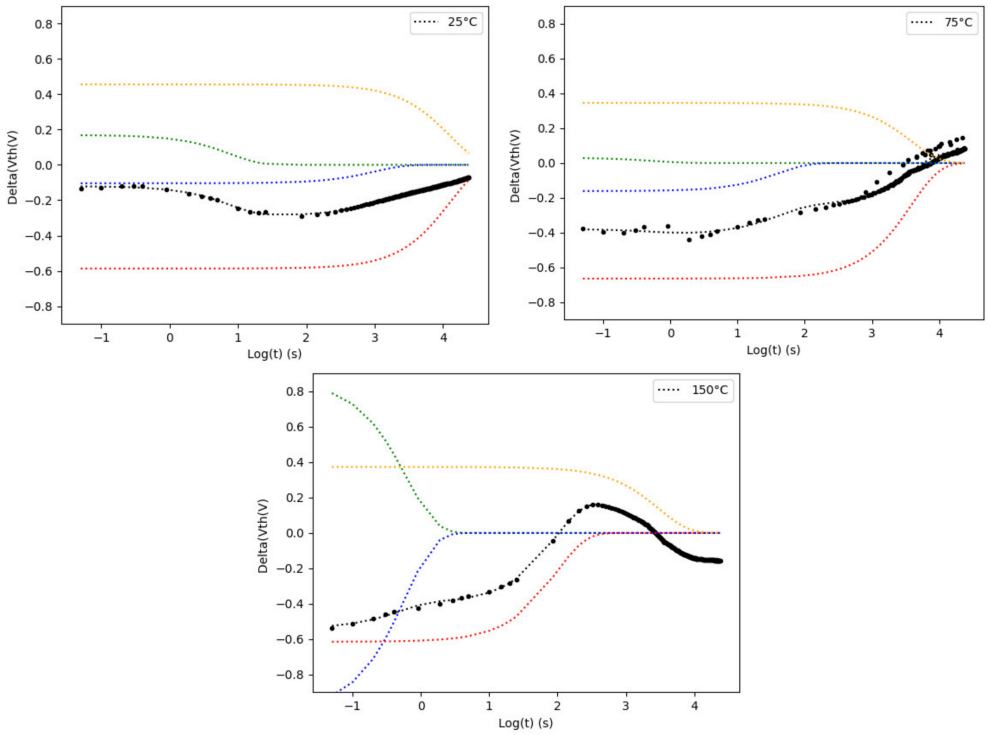

Figure 5. Example of experimental Vth shift at 25 °C, 75 °C and 150 °C (black point) and its recovery in the time after stress (Design A wafer 2). Color curves are used to rebuild experimental Vth recovery.

It is clear, especially in Figure 5 at 75 °C, that the four different slopes of the DeltaVth curve in the function of time (black dash) can be modelized by a sum of a minimum of four decreasing exponentials (color dash). Each exponential characteristic represents a trap energy level. Therefore, it is possible to reproduce the experimental curve (black curve) using two levels of initial positive charges (yellow and green curve) combined with two initial negative charges (blue and red curves).

By fitting the analytical model to the experimental curve, we can extract the values of the constant Cte and the coefficients Ai and Bi (see Equation (12)). The theoretical equation of V(t) evolution in the time after 650 V stress at 75 °C is therefore given by:

$$V(t) = -0.07109 + 0.000099\, e^{-\frac{t}{0.644}} - 0.1275\, e^{-\frac{t}{833}} - 0.62778\, e^{-\frac{t}{12671}} + 0.4656\, e^{-\frac{t}{12670}} \quad (16)$$

The constant Cte and each coefficient Ai are a function of the number of traps charged during the blocking voltage stress. These values are linked to the stress voltage, the duration of stress and the temperature, as mentioned previously.

From the experimental characteristics in Figures 6a, 7a, 8a and 9a, a nonlinear interpolation based on the generic sum of four exponentials allowed us to rebuild the experimental curves of the Vth recovery for three different temperatures (25, 75 and 150 °C). For example, concerning the negative charges, we can see their de-trapping phenomena trend, which is dependent on the temperature as reported in Figures 6–9, graphs (d). Initially trapped during the blocking voltage stress, we can observe that the charges are de-trapped more quickly when the temperature increases. For this example, the characteristic time of de-trapping could be estimated with the intercept of the slope with the X-axis. At 25, 75 and 150 °C, the characteristic times (tau) are: 1000 s, 300 s and 6 s, respectively. Using the extracted values of "tau" (in Arrhenius graph (f)), it is easy to extract associated trap energy levels. Based on the sign of the charge, we can tell whether the traps energy levels are linked to electrons or holes.

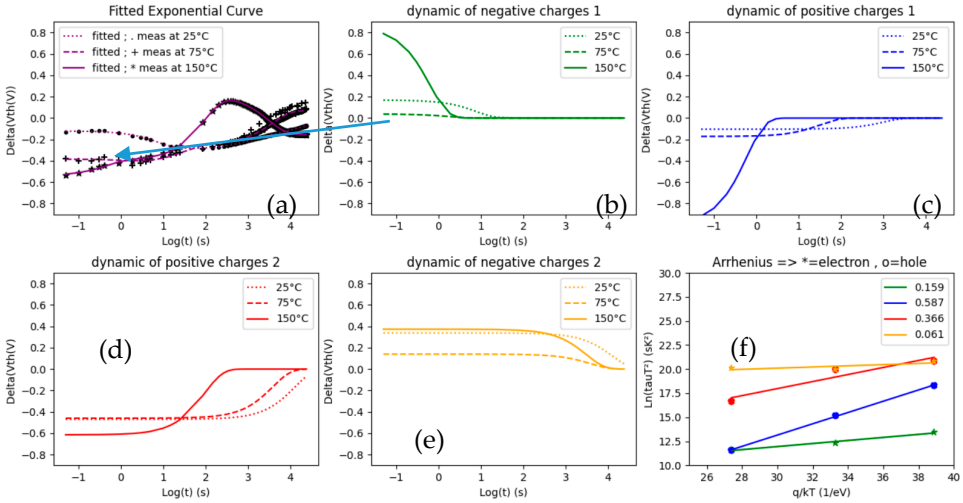

Figure 6. Design A wafer 1; (**a**) measurement at 25, 75 and 150 °C; (**b**) extraction of dynamic first level of negative charges; (**c**) extraction of dynamic first level of positive charges; (**d**) extraction of dynamic second level of negative charges; (**e**) extraction of dynamic second level of positive charges; (**f**) report of the four levels of charge in an Arrhenius graph (extraction of energy levels). Subfigures (**a**–**e**), show the Vth shift due to one trap level in function of time measured at 25, 75 and 150 °C. Subfigure (**f**), is the extraction of traps energies levels for each trap level.

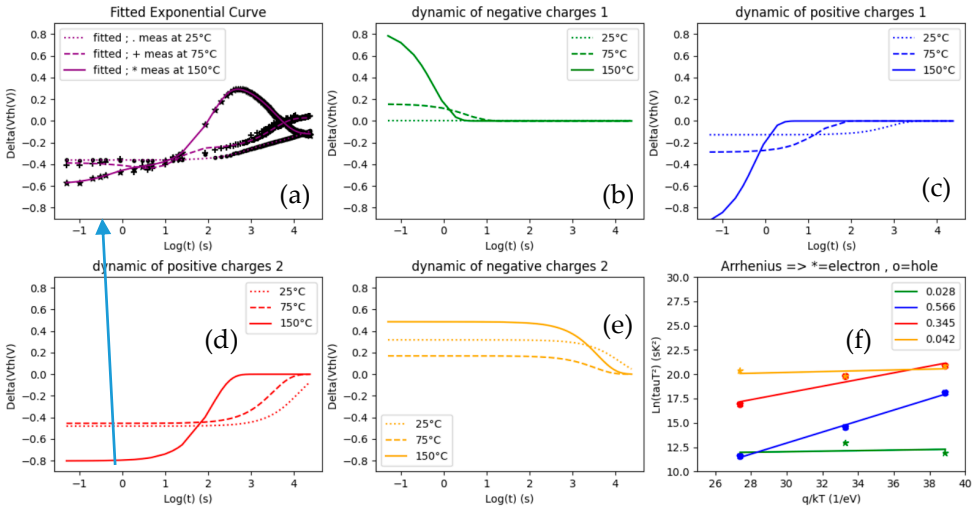

Figure 7. Design A wafer 2; (**a**) measurement at 25, 75 and 150 °C; (**b**) extraction of dynamic first level of negative charges; (**c**) extraction of dynamic first level of positive charges; (**d**) extraction of dynamic second level of negative charges; (**e**) extraction of dynamic second level of positive charges; (**f**) report of the four levels of charge in an Arrhenius graph (extraction of energy levels). Subfigures (**a**–**e**), show the Vth shift due to one trap level in function of time measured at 25, 75 and 150 °C. Subfigure (**f**) is the extraction of traps energies levels for each trap level.

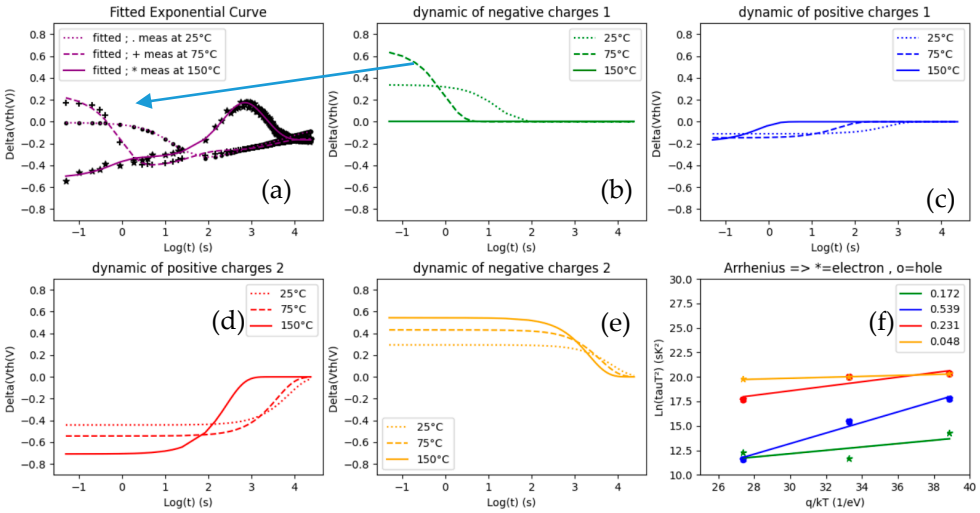

Figure 8. Design B wafer 1; (**a**) measurement at 25, 75 and 150 °C; (**b**) extraction of dynamic first level of negative charges; (**c**) extraction of dynamic first level of positive charges; (**d**) extraction of dynamic second level of negative charges; (**e**) extraction of dynamic second level of positive charges; (**f**) report of the four levels of charge in an Arrhenius graph (extraction of energy levels). Subfigures (**a**–**e**), show the Vth shift due to one trap level in function of time measured at 25, 75 and 150 °C. Subfigure (**f**) is the extraction of traps energies levels for each trap level.

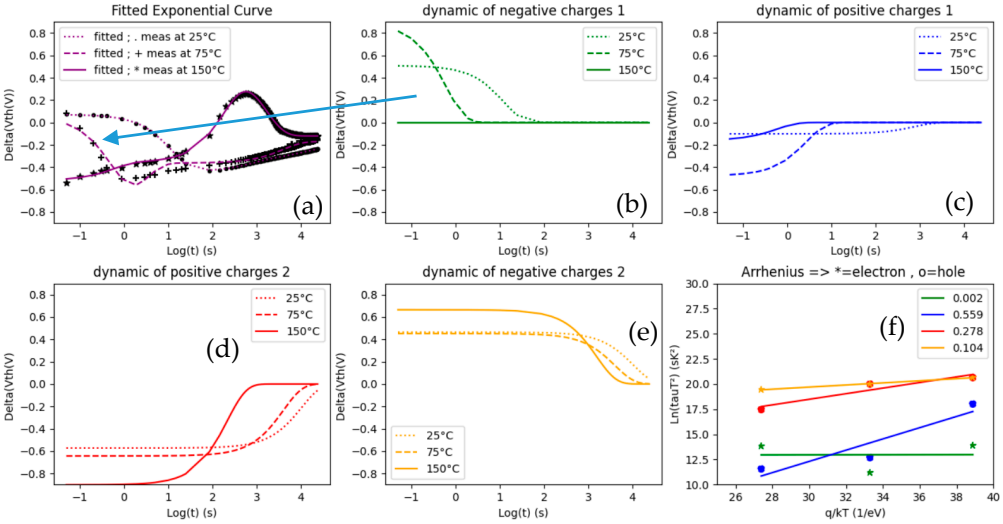

Figure 9. Design B wafer 2; (**a**) measurement at 25, 75 and 150 °C; (**b**) extraction of dynamic first level of negative charges; (**c**) extraction of dynamic first level of positive charges; (**d**) extraction of dynamic second level of negative charges; (**e**) extraction of dynamic second level of positive charges; (**f**) report of the four levels of charge in an Arrhenius graph (extraction of energy levels). Subfigures (**a**–**e**), show the Vth shift due to one trap level in function of time measured at 25, 75 and 150 °C. Subfigure (**f**) is the extraction of traps energies levels for each trap level.

A common dynamic behavior is observed for the four studied designs and is reported in Figures 6–9, graphs (c) and (d). The initial level of trapped charge is different, but the decreasing trend on time is the same and is associated with a hole de-trapping phenomenon. Another common behavior is observed in Figures 6–9, graphs (e), linked to electron de-trapping phenomena. In summary, the main difference between devices is only observed on the characteristics reported in Figures 6–9, graphs (b). Based on the Arrhenius plot, we observe that the extracted energy level corresponding to the curves (b), are in the range of 0.002 to 0.06 eV. This means that de-trapping is relatively fast with a characteristic time

constant of around 0.1 s. Another important aspect is the maximum Vth shift extracted for each energy level. The maximum shift reaches 0.8 V, which is generally compensated by a combination of positive and negative charges. At the end of the measurement, the Vth shift was between −0.6 V and +0.2 V (see curves (a)).

In the case of a negative charge localized close to the gate, the Vth shifts to a more positive value. In the case of a positive charge close to the gate, Vth shifts toward more negative values. Based on the methodology presented above, the energy levels extracted from the two wafers and the two different designs are reported in Table 2. Energy levels found after using this methodology are summarized in this table. For each device, four levels of energy are extracted, two for negative charges (E1 and E2) and two for positive charges (H1 and H2).

Table 2. Table of the results after traps energy levels extraction.

	Design A Wafer 1	**Design A Wafer 2**	**Design B Wafer 1**	**Design B Wafer 2**
E1	0.06	0.03	0.05	0.002
E2	0.16	0.04	0.17	0.10
H1 (Carbon/Mg/(N vacancy))	0.37	0.34	0.23	0.28
H2 (Ga vacancy/(Nvacancy))	0.59	0.57	0.54	0.56

4. Discussion

The extracted energy levels in this study are reported in Figure 10 (red circles) and are due to a combination of traps present by default in GaN and/or traps present due to impurities such as Magnesium and Carbon (red circles in Figure 11).

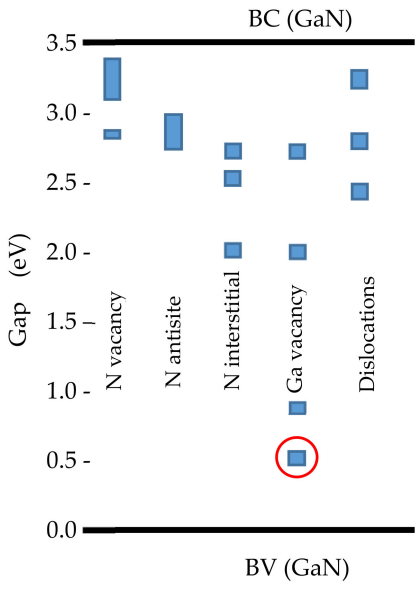

Figure 10. Traps levels due to defaults in GaN material: Allowed energy levels inside the forbidden GaN gap caused by intrinsic defects, dislocations. Zero energy correspond to the upper border of the valence band (own elaboration based on [15]).

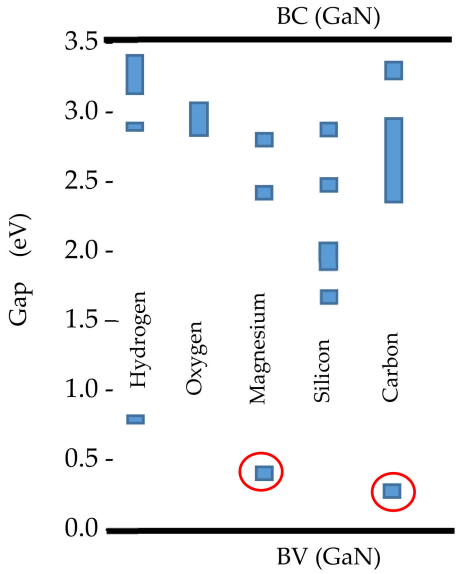

Figure 11. Traps levels due to impurities in GaN material: Allowed energy levels inside the forbidden GaN gap caused by impurities. Zero energy correspond to the upper border of the valence band (own elaboration based on [15]).

The first row of Table 1 show levels of electron traps localized at less than 0.05 eV from the conduction band (CB). Several studies have shown that N vacancy defects have a level in the conduction band (CB) which, when occupied, self-ionize into a hydrogenic configuration, i.e., with an energy of approximately 0.03 to 0.04 eV below the CB edge. However, it has also been proven that in the range of 0.025 to 0.035 eV, the donor is only associated with substitutional impurities [2]. To summarize, these trap energies are due to impurities and/or N vacancies.

The second row of Table 1 is also associated with electron traps. Nitrogen vacancies are one of the most common defects and are reported to behave as mid-shallow donors, covering almost the entire range from Ec − 0.089 eV to Ec − 0.26 eV. However, energies of 0.18 eV can also be associated with N-doped elements during GaN growth by MOCVD [6]. These traps can also be correlated to acceptor levels with activation energy varying with Mg doping levels between 0.13 and 0.17 eV [16]. In these studied devices, the Mg layer is localized close enough to the bottom of gate recess to justify the presence of Mg concentration residual at the Al_2O_3/Interlayer/GaN interface.

The third row shows holes traps energy levels between 0.23 and 0.37 eV [17]. The result can also be interpreted as electron trapping in a trap with an initial positive charge (as Ec-3.1 eV carbon-related or Mg-related deep acceptor). They are associated with charges corresponding to the electrons localized in the interface with more than 0.25 eV [2,11–13]. Hogyoung et al. [14] studied the AlN passivation mechanism in GaN with a Al_2O_3/AlN dielectric stack showing a trap energy level around 0.25 eV. They suggested that border traps were present in the AlN layer. Other studies [3] associated this border trap with V_N-related defects near the AlN/GaN interface. Our results do not show a dependence on the interlayer thickness but seem linked to the design of the transistor (this could be due to the different gate lengths). For this reason, we obtained a different interpretation than Hogyoung et al. [14].

The last energy level (reported in Table 1, last row) concerns deep hole trap energy levesl localized between 0.54 and 0.59 eV, known as the Ga vacancy effect (corresponding to Ec-2.85 eV associated with gallium vacancies [12,18]). An alternative interpretation correlates these levels to electron trapping by localized positive traps (in this case, the traps level is due to N vacancy). After electron trapping, the trap becomes neutral again.

It is known that MISGATE HEMT, in spite of the gate recess through 2-DEG (2-Dimensional Electron Gas), always has a Vth close to 0 V and sometimes negative (in the

function of the process used). It has been shown that even in the case of a process without Mg and with a Carbon layer far from gate recess bottom, the Vth stays close to 0 V. Graphs (c) and (d) in Figures 6–9 show the cause of negative Vth after stress. As mentioned in the literature [19], the large amount of holes trapped during stress is mainly due to Ga vacancy and, to a lesser extent, Mg and C impurities. As mentioned before, the second interpretation considers electron de-trapping during stress and re-trapping after stress (traps become neutral). In this case, the cause is due to N vacancy. When suppressing a negative Vth value after stress at 25, 75 and 150 °C, it is mandatory to improve the quality of epitaxy around the gate recess. However, it is known that the gate recess (even ALE (atomic layer etching)) creates surface states and must be followed by a cleaning phase [20]. This study showed that impurities which could remain after cleaning are not solely responsible for the Vth shift toward a negative value and that rebuilding the network phase is mandatory to suppress positive charges traps. The goal is to rebuild a perfect GaN crystal before Al_2O_3 deposition to suppress recovering time between 10 to 10,000 s. Fast traps occur due to electrons trapped very close to the conduction band and could be suppressed by eliminating N vacancies around the gate.

5. Conclusions

This study concludes that a model based on the Vth measurement at three temperatures combined with a simple sum of exponential equations applied during the recovery time allows the reproduction of the Vth shift after Vds stress. From a combination of exponential functions, four levels of traps are extracted: two for electron traps and two for hole traps in the Dielectric/GaN interface, which are Ec-Et~0.05 eV and Ec-Et~0.15 eV for electrons and equal at 0.3 eV and 0.55 eV upper valence band for holes. The energy levels compared to the literature show a correlation with the magnesium and carbon impurities present in the transistor but can also be due to Ga and/or N vacancy sites in the GaN. It has been shown that defects in the GaN crystal network can explain the Vth evolution during recovery time. One solution to avoid Ga/N vacancies is to perform a re-epitaxy after gate recess. This simple method of traps energy level extraction can be performed directly on a transistor by Vth extraction from Id(Vgs) measurements.

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