

Article

A Transformerless Enhanced-Boost Quasi-Z-Source Inverter with Low Input Current Ripple for Stand-Alone RES-Based Systems

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Abstract: The main drawback of DC-source-based renewable energy sources (RESs), such as photovoltaic (PV) panels or fuel cells (FCs), is that the voltage generated by a panel or cell is less than the required voltage for connection to a DC–AC inverter for grid applications. In this paper, a single-switched DC–DC boost converter equipped with a quasi-impedance source inverter (QZSI) with a modified switching model is proposed to increase the output voltage of these RESs and convert it to a fixed AC grid voltage for loads. By changing the position of the inductor in a classic step-up converter and using a switched-inductor block, the input current ripple is significantly decreased, and the reliability and long-life of the input sources are increased, which is the main contribution of this work. The quality of the generated AC voltage and the low amount of total harmonic distortion (THD) in the projected topology are significant, and no overshoot and undershoot have been reported for both output voltages and currents under different operating conditions with variable loads. Theoretical analysis, simulation results, and comparison with similar topologies are examined and a prototype with a power of 200 to 400 watts is presented. Experimental results confirm the theoretical studies.

Keywords: photovoltaic (PV) cell; DC–DC boost converter; quasi Z-source; switched-inductor cell; inverter; grid connection



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1. Introduction

By considering the increasing need for electricity, researchers are looking to generate electricity in different ways using existing energy sources. Given the limited sources of fossil fuels and the dangers and limitations of nuclear fuels, the interest in using renewable energy sources (RESs) is growing day by day.

Solar cells, batteries, and hydrogen energy-based fuel cells are devices that use different types of energy and convert these energies directly into electrical current or voltage. Today, these RESs are used in various applications, such as battery charging, electric vehicles (EVs), electric charging stations, water pumping, home and grid power supply applications, and off-grid and satellite energy systems [1,2]. In order to use these sources, a series of intermediate equipment and electronics converters are needed to prepare acceptable electrical energy to the electrical loads. One of the most important components of this equipment is power electronic converters that are used to increase or decrease the input voltage level, enhance the power quality control, reduce the harmonics, and convert DC to AC voltage or vice versa in these systems [3–5]. DC–DC and DC–AC converters are among the most widely used power converters in this field. Some environmental factors can change the voltages and

currents produced by these DC sources. For example, temperature, radiation, a combination of electrolyte and chemical components, and contamination and proportions of oxygen and hydrogen particles can instantly change voltages and currents [6–8].

Generally, the generated voltage of these sources is limited, and these low-voltage RESs are equipped with DC–DC converters before connecting to the power grid. The gain of DC–DC boost converters is theoretically infinite when the duty cycle is equal to one, but in practice, as the duty cycle increases, the voltage gain and efficiency of the converter decrease sharply. The reason for this is that through longer duty ratios, the dynamic losses due to the high number of current peaks in the components increase, and the voltage stress across the switch and diode which is equal to the output voltage of the converter in a conventional boost converter increases. Since an internal resistor is modeled for the switch and diode, larger currents lead to more power losses across these resistors with larger voltage drop values.

To solve these problems, various types of DC–DC converters have been proposed [9–13]. Basically, these converters offer techniques, such as voltage multiplier cells, coupled-inductor blocks, fly-back converters with transformer blocks, and a combination of these methods, to obtain higher voltage gain values. One of the disadvantages of these converters is the hard switching operating mode, which reduces the efficiency of the converter. In addition, their bulky and heavy components directly increase the volume and price of the circuit. In addition, the current ripple in these converters is usually high, which reduces the lifespan of the RES connected to these circuits. In these converters, a large filter must be used on the input side to eliminate the input current ripple.

On the other hand, in single-phase operations, the power density and efficiency of the converter are reduced. To improve the efficiency of the converter in the high-power ranges, researchers have proposed two-phase and three-phase interleaved methods in which the power is divided between the phases and the input current ripple is reduced, resulting in reduced losses and higher efficiency. Concerns and drawbacks about these structures are the high numbers of components used in the converter topology, which cause problems, such as bulky and heavy structures with expensive topologies and complexity in control processes [14,15]. In this study, different boost topologies were considered and their features, advantages, and disadvantages were investigated [16–20].

After obtaining an appropriate level of DC voltage, a DC–AC inverter block is applied to generate a sinusoidal voltage waveform at the grid voltage level for loads. Half-bridge (HBI) [21], full-bridge (FBI) [22], voltage source (VSI) [23], current source (CSI) [24], H5 [25], H6 [26], and HERIC [27] inverters are among the most used and considered topologies. Grid connection conditions and the necessity to apply a filter to the output side of the inverters, which requires precise and sometimes complex controller and switching topologies; high THD values for the output current and voltage; and the low-gain range of these inverters are the main drawbacks of these converters.

Meanwhile, impedance source inverters (ZSIs) are relatively efficient converters, and the application of these inverters is increasing day by day [28–30]. These inverters in the simplest design consist of two capacitors and two inductors. Conventional ZSI consists of an X-shaped impedance network. The shoot through (ST) feature is used to enhance the voltage in these converters.

Different topologies for these types of inverters have been presented by researchers for better performance and higher efficiency and reliability.

ZSI converters can also be used as step-up converters [31,32] or as a half-bridge-ZSI [33]. Different indicators are considered to evaluate these converters according to their type and application under different duty ratios, such as the number of components, voltage and current stresses across the semiconductor devices and inductors, the ripple of the input current, and the ripple for the output voltage. In this regard, one of the most important features of ZSIs is the voltage gain, which has led to the provision of different structures for these converters. Various structures for the quasi-ZSI (Q-ZSI) have been proposed in the studies. For example, the series-ZSI (SZSI) is proposed to decrease the

voltage stress across the capacitors [34,35]. Despite the low voltage value of the capacitors in SZSI, the main part of the current of the impedance network flows through these capacitors which directly enhances their nominal capacitance value. These structures have fewer passive components than a conventional ZSI and often have the advantages of ZSI, but their voltage gain is still low. For obtaining more voltage gain for the ZSI, a new converter was proposed in reference [36] for switching boost inverters.

In some other studies, in order to achieve higher voltage gains, improved structures, such as cascaded converters or topologies with transformers, are presented. In reference [36], the impedance source inverter with a switched-inductor cell (LZSI) is presented, which increases the voltage by removing the capacitors of the ZSI using the switched-inductor cell. A quasi-ZSI is presented in [37] in which the voltage gain is increased by the addition of the capacitor and inductor blocks. Ref. [38] provides an impedance source inverter equipped with a switched capacitor configuration and a bridge inverter with an output filter. In [39], the transformer circuit was removed, and an inductor network with a bridge inverter cell was used. In [40], a ZSI block based on the quadratic converter is presented. The advantage of the proposed topology is no need for high voltage gains, and the quality of the generated power is good. However, every Z-network should be equipped with a full bridge inverter which causes lower efficiency for this topology. Due to the fact that in RESs the generated voltage is usually in the low range, this shortage should be compensated in some way. For example, in solar systems, it is necessary to generate electricity in a wide range of voltages by using a large number of modules in series, which increases the cost of electricity production. Some of the details regarding electromagnetic interference calculations are presented in [41]. Different inverter topologies and switching and control methods are analyzed in [42–50].

To solve these problems, in this paper, a novel switched-inductor-based single-switch DC–DC boost converter is presented, and then a QZS inverter converts the DC output voltage of the boost converter to AC through an improved sinusoidal pulse width modulation (SPWM) technique. Different levels of the input voltage source are examined, and the stability of the boost converter for generating a fixed voltage at the input side of the QZSI block is tested. A wide range of resistive and resistive-inductive loads are connected to the QZSI output nodes, and the quality of the proposed switching model is presented. The low-ripple current waveform at the input side of the converter and pure sinusoidal voltage at the output side are among the advantages of the proposed topology and controllers. In addition, the value of the THD is very low, and the reaction of the converter by changing the loads is significant, where no overshoot or undershoot has been reported at the load changing time for the voltage and current waveforms. Mathematical investigations are presented, and finally, a 200 to 400 W prototype converter confirms the correctness of the theoretical analysis.

The proposed converter can be used in micro-grid applications and locations where the electricity grid cannot be reached and the energy of the location is generated by renewable energy sources (RESs), such as PV panels, off-grid home and green energy applications, or converting the energy of electric vehicles (EVs) to the requested AC voltages in off-grid locations through vehicle-to-grid (V2G) charging stations. Uninterruptible power supplies (UPSs) and DC power source usages are other possible applications of the proposed converter.

2. The Proposed Configuration and Switching Method

Figure 1 presents the general DC voltage-based configuration with DC–DC converter block and inverter structure. Since the generated voltages of conventional DC sources are not enough to be connected directly to the DC–AC inverter, a DC–DC boost converter is normally applied. Meanwhile, the output of the boost converter also needs to stay at the constant level of the voltage by changing the input voltage of the converter and also the different amounts of the loads at the output side of the converter. Therefore, a feedback mechanism is applied to measure the output voltage, compare it with the desired output DC voltage, and change the duty ratio of the power switch if an error signal is formed.

Then, the inverter block is activated to change the DC voltage to the AC in order to supply the necessary voltage and current for the grid or AC load. The general configuration for integration of the DC sources with the grid is shown in Figure 1.

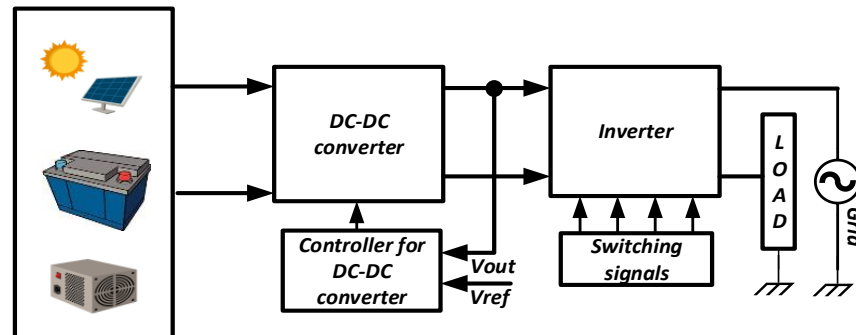


Figure 1. General configuration of the PV-based inverters for AC loads or grid applications.

Figure 2 shows the proposed converter. As can be seen, both the DC–DC boost converter and the proposed ZSI and the full-bridge-based inverter are presented by the DC–DC converter and inverter boxes, respectively. The details for these topologies will be presented in Sections 2 and 3. The internal topology of the DC–DC step-up converter is formed by using the conventional boost converter by replacing the location of the elements innovatively and by using a switched-inductor cell instead of the conventional inductor. To analyze the projected step-up converter, Figure 3 presents and investigates the state of the semiconductor devices and charging or discharging states of the inductors and capacitors in two different operational modes. These states can be seen in Figure 3a,b. These figures present the topology of the converter for time durations that the power switch is in on and off modes, respectively.

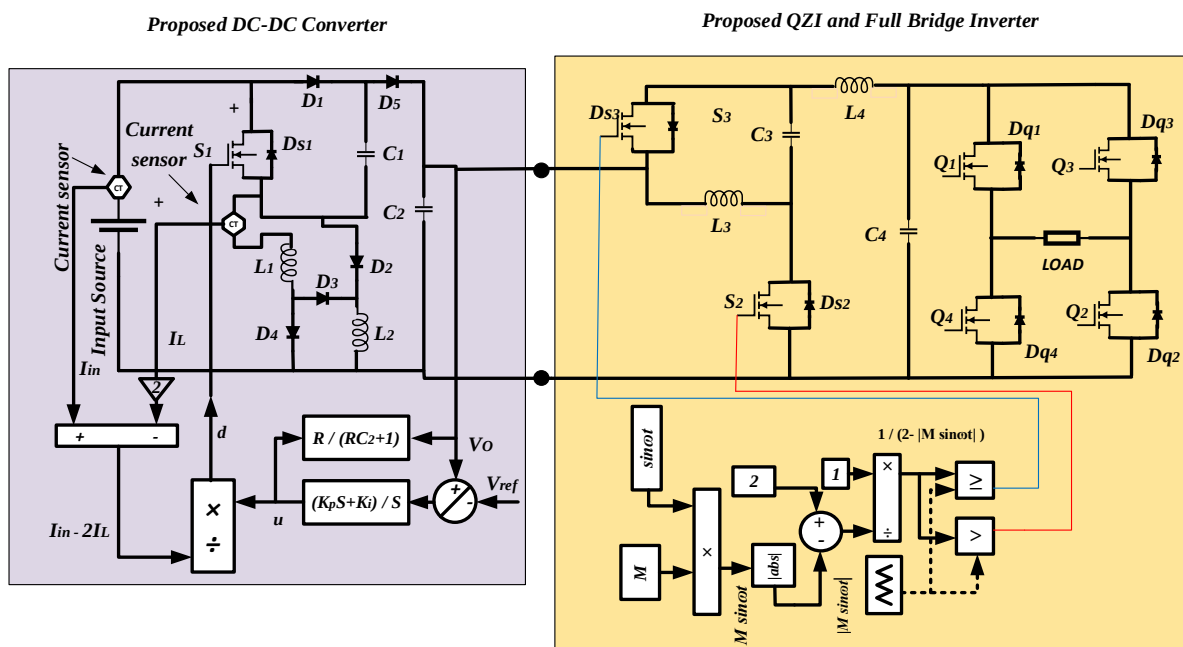


Figure 2. The proposed converter and its controller.

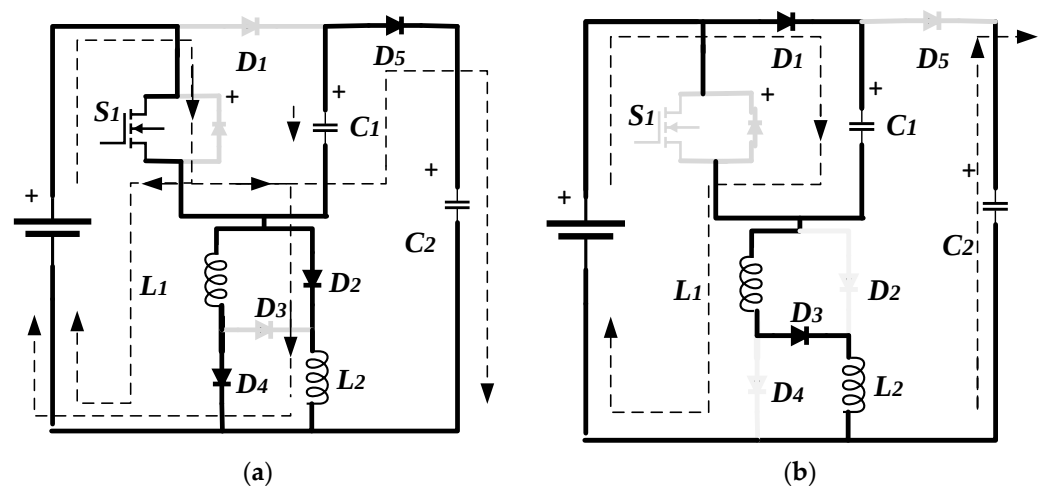


Figure 3. The proposed DC–DC boost converter for the time durations that the switch is in (a) on and (b) off-states.

The proposed inverter circuit is formed by the QZS inverter with integration with the full-bridge inverter (FBI). The proposed QZSI circuit is formed by using two power switches, two inductors, and two capacitors. The reaction of the elements on this side is complementary, and MOSFET transistors can simply be switched. This converter prepares a full-waved sinusoidal voltage and current waves for the FBI block, and finally, the FBI converts these waveforms to the sinusoidal voltage and current signals. The inverter section, separately, will be investigated in Section 2.4.

2.1. The Gain of the Proposed Boost Converter

The proposed DC–DC converter can be seen in Figure 2 with the light purple color. Switched-inductor cells prepare DC–DC converter circuits to operate at higher power ratings. The main reason for this is that in the on-state of the switch in the circuit, the inductors become parallel and can pull a higher current from the input power supply. When the switch is opened, the inductors become in series. In this way, they can transfer higher values of the power to the load. However, since they are discharged in series, a more ripple-free state of the current drawn from the input source can be achieved since a larger inductor value is obtained. This state prepares the converter for high-power and low-ripple applications. However, for a conventional boost converter, no possibility exists for charging in parallel and discharging in series for inductors. Furthermore, the second end of an inductor in a classical boost converter is connected to the switch and diode, and the current is changed by the on- and off-states of these semiconductor devices. However, by changing the location of the switch with the inductor, since the input source is connected to the inductor via the switch, the discharging process of the inductors will be slower. For obtaining the gain of the proposed DC–DC boost converter, the state of the converter should be analyzed separately for the time duration the power MOSFET is in on and off modes, respectively. Below, these two different modes are presented:

State 1: The configuration of the proposed topology for this operational mode is illustrated in Figure 3a. As can be seen, in this state the switch is activated. Both inductors $L1$ and $L2$ will be parallel with the input voltage source and start to be charged through the power diodes $D2$ and $D4$. Diode $D3$ is reversed biased and could not activate. The negative pole of capacitor $C1$ is connected to the positive pole of the input voltage, and this forces the capacitor to discharge across capacitor $C2$ through diode $D5$. The capacitor $C2$ is responsible for the ZSI input voltage side and will be ready to energize this block.

For a simple mathematical analysis, the power components are considered to work ideally, and the internal resistance of the switch and diodes are ignored. Therefore, the voltage across inductors L1 and L2 can be shown by:

$$V_{L1, \text{ and } L2} = V_{in} = L \frac{di_L(t)}{dt} \quad (1)$$

In this equation, V_{in} indicates the input voltage source. For the symmetrical conditions of the inductors, it is considered that inductors L1 and L2 are the same and can be represented by L.

State 2: The configuration of the proposed converter can be seen in Figure 3b for this working mode. Since the switch is in the off-state, diode D1 starts to handle the input current and charge capacitor C1. By charging this capacitor, both inductors begin to be discharged, and a serial connection is formed between them. Since this topology presents a voltage greater than the input voltage, diode D5 is deactivated, and the voltage across capacitor C2 starts to discharge across the ZSI block.

For this state, one can simply write:

$$V_{in} = 2V_L + V_{C1} \quad (2)$$

Therefore, the voltage across the inductors can be calculated by (3):

$$V_{in} = 2L \frac{di_L(t)}{dt} + V_{C1} \rightarrow V_L = L \frac{di_L(t)}{dt} = \frac{V_{in} - V_{C1}}{2} \quad (3)$$

Since for a time period the average voltage value across an inductor is zero for a switching circuit, Equation (4) can be written:

$$V_{L, ON} + V_{L, OFF} = 0 \rightarrow V_{in}D + \left(\frac{V_{in} - V_{C1}}{2} \right) (1 - D) = 0 \quad (4)$$

where D and (1 – D) indicate the ON and OFF-states of the power switch. In fact, D is the duty ratio of the switch and indicates the time duration that the switch is activated in a time period. The voltage across capacitor C1 can be written:

$$V_{C1} = V_{in} \left(\frac{1 + D}{1 - D} \right) \quad (5)$$

Since the average voltage across the inductor is zero, the voltage across capacitor C2 can be calculated the same as capacitor C1, and the DC gain of the boost converter can be found as:

$$V_{C2} = V_{in} \left(\frac{1 + D}{1 - D} \right) \rightarrow M = \frac{V_{C2}}{V_{in}} = \frac{1 + D}{1 - D} \quad (6)$$

2.2. Inductors and the Current Ripples

Input current ripple is one of the most important features for a DC–DC converter, and topologies with the least ripple values are preferred. The reliability of the converter and the long life of the components in the circuit, especially power semiconductors, are the reason for the minimum ripple for the input current. When the input source is a PV array, this feature will be more important since the large variations for the current directly decrease the useful long life of the module. In order to find the current ripple, the magnitude of the currents for two on- and off-states of the switch should be considered. For the time duration that the switch is in the on-state, the current for the inductors can be calculated through (7) and (8). In addition, for the next time duration that the switch is in the off-mode, the current magnitude can be presented by Equations (9) and (10).

$$V_{L1, \text{ and } L2} = V_{in} = L \frac{di_L(t)}{dt} \rightarrow \frac{di_L(t)}{dt} = \frac{\Delta i_L}{DT} = \frac{V_{in}}{L} \quad (7)$$

$$(\Delta i_L)_{closed} = \frac{V_{in}}{L} DT \quad (8)$$

$$V_L = L \frac{di_L(t)}{dt} = \frac{V_{in} - V_{C1}}{2} \rightarrow \frac{di_L(t)}{dt} = \frac{\Delta i_L}{(1-D)T} = \frac{V_{in} - V_{C1}}{2L} \quad (9)$$

$$(\Delta i_L)_{open} = \frac{V_{in} - V_{C1}}{2L} (1-D)T \quad (10)$$

where $(\Delta i_L)_{closed}$ and $(\Delta i_L)_{open}$, respectively, present the current magnitude for the inductors for the time durations that the power switch is in the on- and off-states. Since the V_{C1} is the same with V_O , they can be replaced in equations. Since for the steady-state operation, the change of the current should be zero for the inductor, from (8) and (10) one can write:

$$(\Delta i_L)_{closed} + (\Delta i_L)_{open} = 0 \rightarrow \frac{V_{in}}{L} DT + \frac{V_{in} - V_O}{2L} (1-D)T = 0 \quad (11)$$

By considering the P_{in} and P_{out} as the input and output powers for the converter and R_O as the load:

$$P_{out} = \frac{V_O^2}{R_O} = V_O I_O, \quad P_{in} = V_{in} I_{in} = V_{in} I_L (1-D)T \quad (12)$$

$$V_{in} I_L (1-D)T = \frac{V_O^2}{R_O} = \frac{\left(V_{in} \left(\frac{1+D}{1-D}\right)\right)^2}{R_O} = \frac{(V_{in}(1+D))^2}{(1-D)^2 R_O} \quad (13)$$

This equation can present the average current value for the inductor current:

$$I_L = \frac{V_{in}(1+D)}{(1-D)^2} \quad (14)$$

Since this current is the average value for the inductor current, the pick currents (minimum and maximum amplitudes) can be presented by:

$$I_{L, max} = I_L + \frac{\Delta i_L}{2} = \frac{V_{in}(1+D)}{(1-D)^2 R_O} + \frac{V_{in}}{2L} DT \quad (15)$$

$$I_{L, min} = I_L - \frac{\Delta i_L}{2} = \frac{V_{in}(1+D)}{(1-D)^2 R_O} - \frac{V_{in}}{2L} DT \quad (16)$$

Continuous conduction mode (CCM) indicates that the current of the inductor is always positive. Therefore, the minimum current of the inductor should be greater than zero. This current can be shown by $I_{L, min}$. When $I_{L, min} = 0$, the inductor value has been selected for the boundary condition (BCM) between CCM and discontinuous conduction mode (DCM). It means for the CCM operational mode; the value of the inductor should be selected at least 25 percent greater than the calculated value for BCM.

$$I_{L, min} = \frac{V_{in}(1+D)}{(1-D)^2 R_O} - \frac{V_{in}}{2L} DT = 0 \rightarrow \frac{V_{in}(1+D)}{(1-D)^2 R_O} = \frac{V_{in}}{2Lf} \quad (17)$$

where f indicates the switching frequency. From (17), a relation between f and L_{min} can be obtained:

$$(Lf)_{min} = \frac{D(1-D)^2 R_O}{2(1+D)}, \quad L_{min} = \frac{D(1-D)^2 R_O}{2(1+D)f} \quad (18)$$

2.3. Capacitor and the Voltage Ripples

Another important feature for a proper power converter circuit is its ability to present a fixed voltage at the load side and across the output voltage. It is preferred to have a

maximum 1 percent ripple for this voltage. To obtain this voltage ripple value, Equation (19) can be used:

$$|\Delta Q| = \left(\frac{V_O}{R_O} \right) DT = C_2 \Delta V_O \quad (19)$$

In this equation, Q presents the electrical charge of the capacitor for the time duration that the capacitor is charged. Voltage fluctuation ΔV_O can be calculated simply:

$$\Delta V_O = \left(\frac{V_O}{R_O C_2} \right) DT = \frac{V_O D}{R_O C_2 f} \quad (20)$$

$$\frac{\Delta V_O}{V_O} = \frac{D}{R_O C_2 f} \quad (21)$$

The recent equation shows that the value of this capacitor is directly in a relationship with the voltage fluctuation magnitude:

$$C_2 = \frac{D}{R_O (\Delta V_O / V_O) f} \quad (22)$$

Figure 4 shows the switching voltage for the power switch, voltage across the diodes, current for the capacitors, and voltage and current for the inductors to present the state of the components in a switching time period.

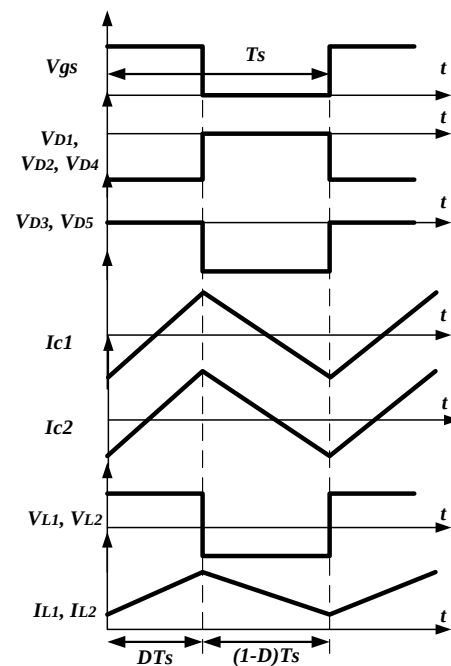


Figure 4. Switching voltage for the power switch, voltage across the diodes, current for the capacitors, and voltage and current for the inductors in a switching time period.

2.4. Controller Design

For the proposed converter, when the switch is in the on-state, Equation (23) can be written:

$$C_2 \frac{dV_2}{dt} + \frac{1}{R} V_2 = d(i_{in} - 2i_L) = u \quad (23)$$

R presents the amount of the output load and can be considered as the input impedance for the next block, ZSI. Here, i_{in} , i_L , and u present the input current of the converter, the current of the inductors, and the output signal for the controller as can be found for a PI controller in the literature.

By using the Laplace transform, we can obtain:

$$C_2 s V_2 + \frac{1}{R} V_2 = V_2 \left(C_2 s + \frac{1}{R} \right) = d(i_{in} - 2i_L) = u \quad (24)$$

Therefore, the duty cycle can be related with the u , i_{in} , and i_L :

$$d = \frac{u}{(i_{in} - 2i_L)} \quad (25)$$

To obtain the control signal, Figure 5 is presented and simply shows the relation between these parameters. Since the classic PI or PID controller is considered to be designed, the general transfer function of the PID controller, $G(s)$, is written, and the coefficients can be calculated:

$$G(s) = k_p + \frac{k_i}{s} = \frac{k_p s + k_i}{s} \quad (26)$$

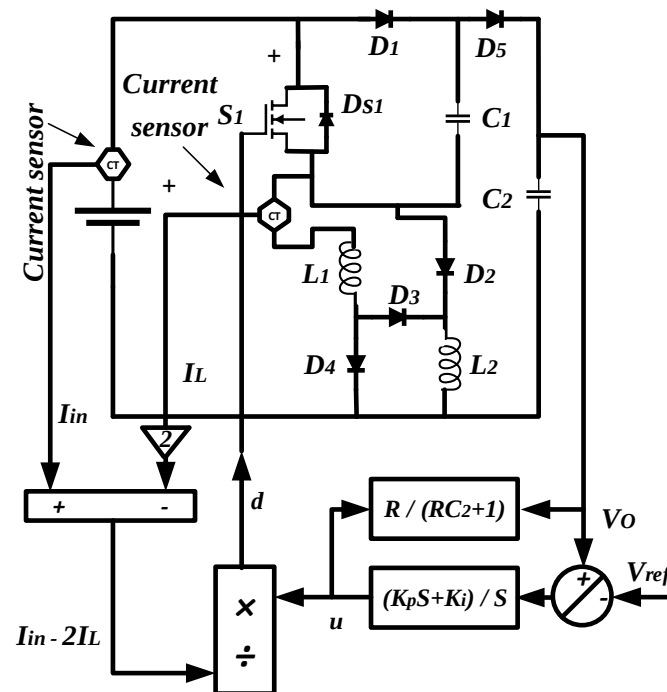


Figure 5. The proposed DC-DC converter circuit and controller.

The closed-loop form of the controller can then be written as:

$$G_F = \frac{G_o}{1 + G_o} = \frac{\frac{1}{C_2}(k_p + k_i)}{s^2 + \left(\frac{1+Rk_p}{RC_2}\right) + \frac{k_i}{C_2}} \Rightarrow G_F = \frac{\frac{1}{C_2}(k_p s + k_i)}{s^2 + 2\xi\omega_0 s + \omega_0^2} \quad (27)$$

The k_p and k_i coefficients can be calculated as below:

$$\begin{cases} \frac{1+Rk_p}{RC_2} = 2\xi\omega_0 \\ \frac{k_i}{C_2} = \omega_0^2 \end{cases} \Rightarrow \begin{cases} k_p = 2\xi\omega_0 C_2 - \frac{1}{R} \\ k_i = \omega_0^2 C_2 \end{cases} \quad (28)$$

2.5. Operation of the Quasi Z-Source Inverter

Figure 6 illustrates the state of the QZSI when the switches S2 and S3 are activated and deactivated. The working principle of this converter makes the power switches activate complementarily, and in the per time interval, only one of the switches will be in the on-mode. This is a useful feature of this converter since it simplifies the switching and

controller structure design. In addition, a unilateral sine wave can be generated at the output side of this inverter that can improve the THD of the converter without the need for the filter designs.

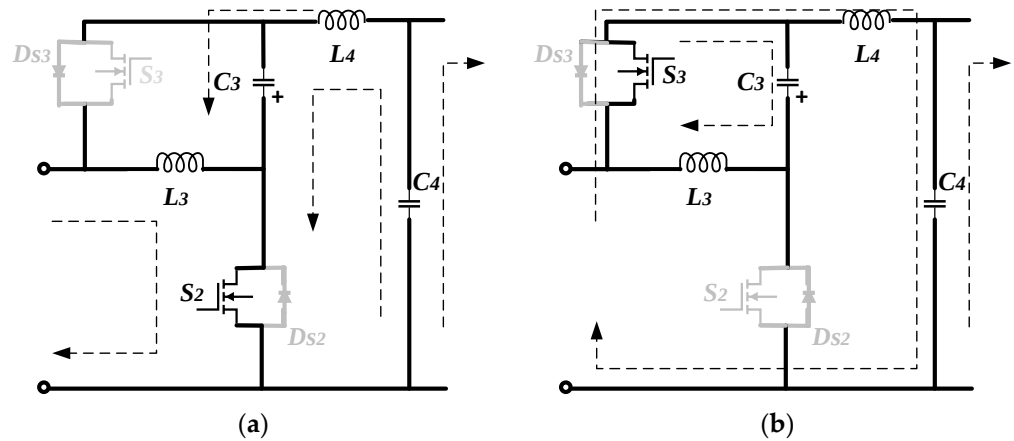


Figure 6. The state of the QZSI when the power switch (a) S_2 or (b) S_3 is activated.

A comprehensive explanation of the operating conditions of this converter is presented in [2]. This converter can be used in both CCM and DCM with different values of the duty ratios (d), and modulation indexes (M).

The state of the voltages and currents of the various components in this converter is depicted in Figure 7. As can be seen, for the time intervals that S_2 is activated, S_3 is deactivated and vice versa. When S_2 is in the on-mode, inductor L_3 is charged through this switch, and inductor L_4 is discharged by capacitors C_4 and C_3 . For the next time interval, S_3 is activated, the voltage across capacitor C_3 is discharged, and the current of inductor L_3 begins to decrease. Meanwhile, the input voltage starts to charge inductor L_2 and capacitor C_4 . These details can be followed in Figure 6a,b. In addition, the state of the voltage and currents for components of the QZSI block are shown in Figure 7. As can be seen in Figure 7, two opposed switching signals are considered to apply to the switches in the QZSI block. On this occasion, inductors L_3 and L_4 will be charged and discharged asynchronously and oppositely. The presence of positive voltage at both ends of an inductor ensures that the current through the inductor rises and charges. Conversely, at negative voltages, the current of the inductor starts to decrease, and the discharge process takes place. All these facts can be followed through Figure 7.

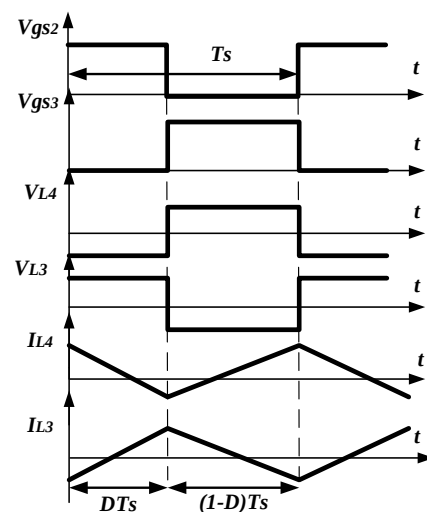


Figure 7. The state of the voltage and currents for the components of the QZSI block.

For the steady-state operational conditions, by considering the D_Z as the duty cycle of the power switch S2, the gain of the QZSI inverter G_{QZSI} , is obtained by (29):

$$G_{QZSI} = \frac{1 - 2D_Z}{1 - D_Z} \quad (29)$$

In addition, for this converter, the output voltage V_{O-QZSI} can be presented by (30):

$$V_{O-QZSI} = V_m \sin \omega t \quad (30)$$

By considering the V_m as the maximum magnitude of the generated voltage across capacitor C4, the modulation index M can be calculated by:

$$M = \frac{V_m}{V_{in-QZSI}} \quad (31)$$

where $V_{in-QZSI}$ indicates the input voltage for the QZSI block. By considering Equations (29)–(31), the duty ratio, D_Z , for the power switch S2 can be obtained as:

$$D_Z = \frac{1 - M \sin \omega t}{2 - M \sin \omega t} \quad (32)$$

Since the duty ratio, D'_Z , for the switch S3 is equal to $D'_Z = 1 - D_Z$, one can simply obtain:

$$D'_Z = \frac{1}{2 - M \sin \omega t} \quad (33)$$

Equations (32) and (33) show that for higher modulation indexes, the negative values for the duty ratios will be obtained; therefore, these equations can be rewritten for obtaining an AC voltage with peak values equal to the input DC voltage:

$$\begin{cases} D_Z = \frac{1 - |M \sin \omega t|}{2 - |M \sin \omega t|} \\ D'_Z = \frac{1}{2 - |M \sin \omega t|} \end{cases} \quad (34)$$

In practice, achieving this D'_Z seems to be easier for preventing the complexity of the controller. The results of the switching of the switches can be seen in Figure 8. The obtained voltage across capacitors C3 and C4 shows that a full-wave rectified voltage will appear across capacitors C3 and C4, and it will be suitable to convert to a sinusoidal voltage across the load by applying a full-bridge inverter (FBI) as can be seen in Figure 8.

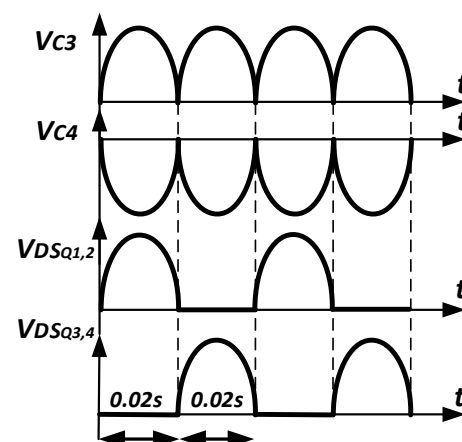


Figure 8. Voltage states across the capacitors of the QZSI and drain-source pins of the FBI switches.

Voltage across capacitors C3 and C4 can be obtained by:

$$\begin{cases} V_{C3} = \frac{D_Z}{1-D_Z} V_{in-QZSI} \\ V_{C4} = -\left(\frac{D_Z}{1-D_Z}\right) V_{in-QZSI} \end{cases} \quad (35)$$

Therefore, the voltage ripple across these capacitors can be presented by:

$$\begin{cases} \Delta V_{C3} = \frac{(1-D_Z)T_s I_{L3}}{C_3} \\ \Delta V_{C4} = \frac{(1-D_Z)T_s I_{L4}}{C_4} \end{cases} \quad (36)$$

In addition, the current ripple for the inductors can be calculated by (37):

$$\begin{cases} \Delta I_{L3} = \frac{V_{in-QZSI} T_s D_Z}{L_3} \\ \Delta V_{C4} = \frac{V_{in-QZSI} T_s (1-D_Z)}{L_4} \end{cases} \quad (37)$$

The improved switching model for the proposed QZSI can be presented by Figure 9 according to Equation (34).

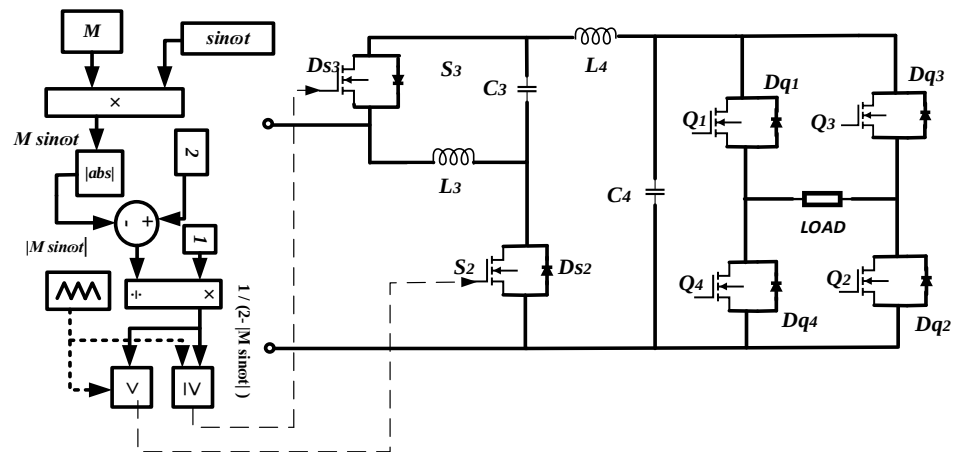


Figure 9. The proposed sinusoidal PWM model for the QZS inverter.

Figure 10 presents a conventional full-bridge inverter (FBI) that can easily convert the input voltage to a sinusoidal voltage. Since the voltage of capacitors C3 and C4 is connected to this block, as can be seen in Figure 8, a pure sine wave for voltage is obtained. The state of the FBI switches can be seen in Figure 10a,b. These power MOSFETs are switched simultaneously by a square wave-pulse with 50 Hz frequency suitable for grid applications. Switches Q1 and Q2 will be activated under conditions that switches Q3 and Q4 are deactivated and vice versa.

2.6. Losses Calculations for the Proposed Converter

The power losses for the DC–DC step-up converter circuit can be divided into dynamic and switching losses. Dynamic losses are in direct relation to the internal resistance of the inductors, capacitors, and semiconductor devices when the current is established. Switching losses can be calculated for power switches and diodes and will occur at the switching times when the voltage and current of the device form a cross point and generate a power loss under the real working conditions. Theoretically and in ideal operational modes, when a switch or diode is connected, the voltage across the device will sharply decrease and reach zero, but in practice the voltage of the mentioned element needs time to be zero. To overcome the switching losses, soft switching techniques including the zero voltage (ZVS) and zero current switching (ZCS) techniques should be considered. Basically,

in these techniques, a small and serial inductor is applied with the semiconductor devices, and a parallel capacitor is used across them.

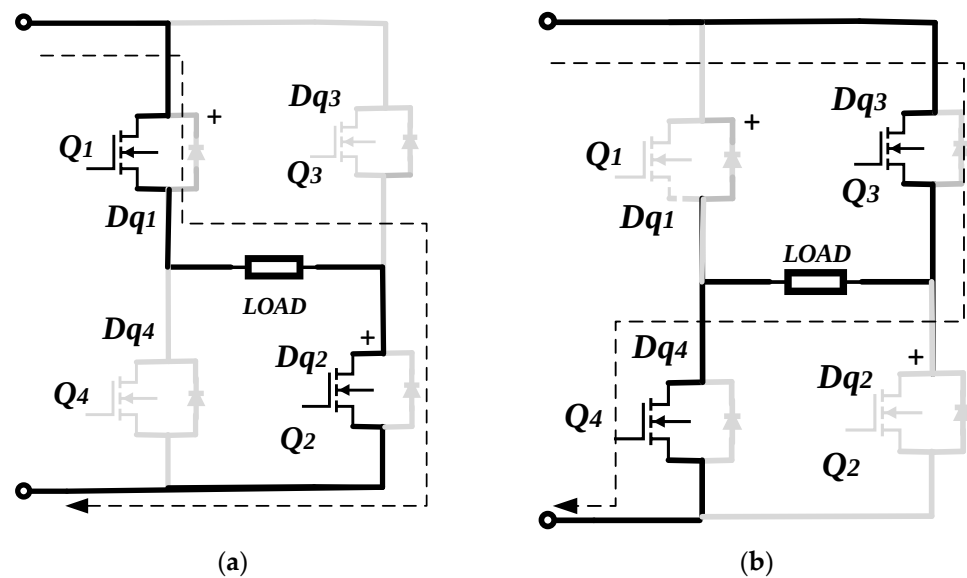


Figure 10. Full bridge inverter block and the state of the MOSFETs when (a) Q_1 and Q_2 and (b) Q_3 and Q_4 are switched.

Inductors:

Generally, two core and dynamic losses are considered for the inductors. The core losses normally are presented by the supplier and can be calculated through Equation (38):

$$P_{L, core} = K_x \cdot f \cdot y \cdot B_z \cdot V_w \quad (38)$$

In this equation, K_x , f , and y present a constant for the core material, switching frequency, and flux density, respectively. In addition, B_z , and V_w represent the flux density exponent and effective core volume. This type of loss is small and is discussed in mill-watts.

Dynamic or conduction loss for an inductor P_L can be calculated through Equation (39):

$$P_L = R_{DCL} I_L^2 \quad (39)$$

DC resistance of the inductor is indicated by R_{DCL} , and I_L presents the root mean square (RMS) value of the current. With an appropriate approximation, I_L can be considered as the average current of the inductor. The total dissipated conduction losses $P_{L-Total}$ for the inductors can be found by.

$$P_{L-Total} = P_{L1} + P_{L2} + P_{L3} + P_{L4} \quad (40)$$

Capacitors:

The general state of the loss P_C equation can be written by:

$$P_C = R_{DCC} I_C^2 \quad (41)$$

Simply, R_{DCC} and I_C indicate the equivalent serial resistance and RMS current of the capacitor. Since R_{DCC} is very small, normally the loss of the capacitor is ignorable. The total power loss for capacitors $P_{Total-C}$ is equal to:

$$P_{Total-C} = \sum_{i=1}^4 P_{Ci} \quad (42)$$

Mosfets:

The conduction power dissipated in a power MOSFET P_{Q-C} can be formulated by:

$$P_{Q-C} = R_{DCM-ON} I_Q^2 \quad (43)$$

As mentioned for the inductors, R_{DCM-ON} represents the internal resistance of the switch when it is activated, and I_Q is the RMS current for the switch. Since the switching losses also should be considered for the switches, the energy definition during the switching phase W_A and blocking phase W_B should also be considered. This loss value P_{Q-SS} can be found by:

$$P_{Q-SS} = (W_A + W_B) \cdot f \quad (44)$$

where f indicates the switching frequency. Generally, the power loss for a switch P_S is equal to:

$$P_S = P_{Q-C} + P_{Q-SS} \quad (45)$$

Therefore, the total power losses $P_{Total-S}$ can be formulated by:

$$P_{Total-S} = \sum_{i=1}^3 P_{Si} + \sum_{j=1}^4 P_{Sj} \quad (46)$$

Diodes:

Power diodes like the switches have both conduction and switching losses. The conduction loss P_{Q-D} can be presented by:

$$P_{Q-D} = R_{DCD-ON} I_D^2 \quad (47)$$

where R_{DCD-ON} and I_D are the DC resistance of the anode to cathode when the diode is in the on-state and average current of the diode, respectively.

The similar switching losses for diodes P_{Q-SD} can be reported by:

$$P_{Q-SD} = (W_A + W_B) \cdot f \quad (48)$$

Therefore, the total power loss for a diode P_D is equal to:

$$P_D = P_{Q-D} + P_{Q-SD} \quad (49)$$

Total losses of the diodes can be written by:

$$P_{D-Total} = \sum_{i=1}^5 P_{Di} \quad (50)$$

The total losses of the converter include the loss for the inductors, capacitors, switches, and diodes:

$$P_{Total} = P_{L-Total} + P_{Total-C} + P_{Total-S} + P_{D-Total} \quad (51)$$

The efficiency of the converter is:

$$\eta = \frac{P_O}{P_O + P_{Total}} \quad (52)$$

where P_O is the output power that is transferred by the converter to the load.

2.7. Shoot-Through and Non-Shoot-Through State Working Modes

Figure 11 illustrates the state of the converter when all of the switches are connected and disconnected at the same time. These two working modes are known as the shoot-through (ST) and non-shoot-through (NST) working states and are shown in Figure 11a,b, respectively.

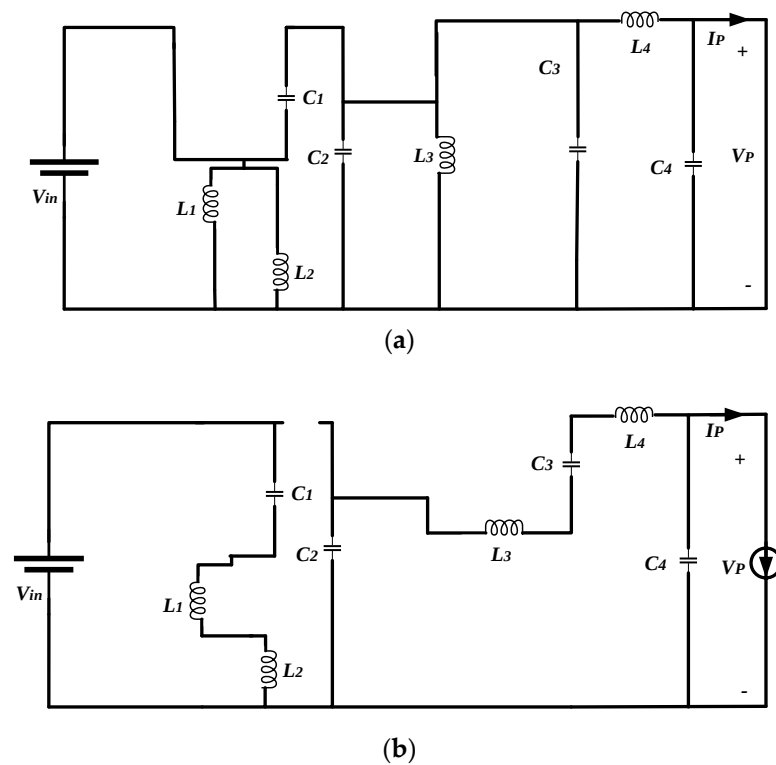


Figure 11. Equivalent circuits of the proposed inverter: (a) shoot-through state; (b) non-shoot-through state.

To analysis the converter in ST, since a positive charging current is established from the input voltage source to the ground, diode D3 is disconnected. In addition, since the voltage at the output in a boost converter is greater than the input voltage source, diode D1 is disconnected. In these working modes, inductors L_1 , L_2 and capacitor C_2 are charged, and C_1 is discharged. So, one can simply write:

$$\begin{cases} V_{L1} = V_{L2} = L_1 \frac{di_{L1}(t)}{dt} = L_2 \frac{di_{L2}(t)}{dt} = V_{in} \\ V_{C2} = V_{C3} = V_{L3} = L_3 \frac{di_{L3}(t)}{dt} = V_{L4} + V_{C4} = L_4 \frac{di_{L4}(t)}{dt} + V_P \end{cases} \quad (53)$$

In addition, since both switches S2 and S3 are connected, all the inductors and capacitors in the ZSI cell will be charged. This state can be followed by Figure 11a.

For the NST working mode (Figure 11b), diodes D1 and D3 are connected, D5 is disconnected, and a serial LCLC network is forming for the ZSI converter elements. For this mode, one can write:

$$V_{in} = 2L \frac{di_L(t)}{dt} + V_{C1} \rightarrow V_L = L \frac{di_L(t)}{dt} = \frac{V_{in} - V_{C1}}{2} \quad (54)$$

In recent equations, V_P and I_P are the short circuit and open circuit voltage and current for the output nodes of the inverter.

3. Comparison and Discussion

In this section, the different features of the proposed topology will be compared with some of the conventional and new structures that have been presented in recent years. For this purpose, the converter in two different sections will be discussed. Firstly, the proposed boost converter and then the inverter topologies will be considered. Table 1 presents different boost converters. Table 1 and Figure 12 compare the features of the similar boost converter circuits and the proposed converter. For a better analysis, Figure 12a–c are presented according to the equations in Table 1. For these figures, the duty cycles more than 0.5 are considered that normally are used in designing. In Figure 12a, the

gain of the converters is compared. As can be seen, the gain of the proposed converter is considerably high, especially when one compares the number of the components of the converters. The boost converters proposed in reference [17,20], and [18] use 14, 13, and 12 elements, respectively, and converters in [16,18,19] use 11 components, respectively, where the proposed converter and circuit in [51] use only 10 components. The converter in [52] has nine components. The number of the power switches is important since the high numbers of switches need more complex control circuits and strategies. The proposed converter has only one power switch, less than all other converters, [20], and the proposed converter has five diodes. The number of diodes for circuits in [16–18] is equal to four. In addition, since the inductor is one of the main sources of power losses based on the internal resistance, this parameter should be considered. The number of inductors is equal to the inductor numbers in [16,18,19] and less than the inductor numbers of the converters [17] and [51]. The gain of the proposed boost converter is comparable with most of these converters. The same results can be reported for the voltage stress across the output capacitor. These results can be followed through Figure 12b. Some of the references in Table 1 enhance the voltage by applying more than one block and one inductor.

Table 1. Comparison between the proposed and other boost converters.

	[16]	[17]	[18]	[19]	[20]	[51]	[52] Non-Isolated Converter	Proposed
Number of diodes	4	4	4	2	5	2	2	5
No of switches	2	2	2	4	2	2	4	1
No. of inductors	2	4	2	2	1	3	1 pair	2
No. of capacitors	3	4	4	3	5	2	3	2
Voltage Gain	$\frac{1+n}{1-D}$	$2 \frac{(1+n)}{1-D}$	$2 \frac{(1+n)}{1-D}$	$2 \frac{(1+n)}{1-D}$	$\frac{3+2n-D(3+n-D)}{(1-D)^2}$	$\frac{1+D}{1-D}$	$\frac{2n}{1-D}$	$\frac{1+D}{1-D}$
Voltage stress across the output capacitor	$\frac{1+n}{1-D} V_O$	$\frac{1}{(1+n)} V_O$	$2 \frac{(1+n)}{1-D}$	$2 \frac{(1+n)}{1-D} V_O$	—	$\frac{1+D}{1-D} V_O$	$\frac{2n}{1-D} V_O$	$\frac{1+D}{1-D} V_O$
Current stress across the main switch	$(\frac{1+n}{1-D} + \frac{2n}{D}) I_O$	$2(1+n) \frac{2-D}{D(1-D)} I_O$	—	—	—	$\frac{1}{1-D} I_O$	$\frac{2}{1-D} I_O$	$\frac{1+D}{1-D} I_O$
Voltage stress across the main switch	—	$\frac{V_O}{2(1+n)}$	$\frac{V_O}{2(1+n)}$	$\frac{V_O}{2(1+n)}$	$\frac{(1-D)V_O}{3+2n-D(3+n-D)}$	$\frac{V_O}{1+D}$	$\frac{(1-D)V_O}{4}$	$\frac{(1+D)V_O}{1-D}$

Therefore, for obtaining a result to present, the number of blocks is considered as $n = 1$ for all of these converters.

One of the main features of a converter is the current stress at the input inductors. This not only reduces the dynamic losses of the converter but also enhances the reliability and long life of the converter. Figure 12c shows this parameter. This figure illustrates that the current stress of the inductors is the least for the proposed converter. The topology of the inductors, especially when making a parallel configuration, is an effective parameter for achieving this specification that can be considered as one of the most important features of the proposed boost converter.

The same comparison is conducted for the proposed inverter block. A number of the new or well-known inverters are presented in Table 2, and Figure 13 analyses the features of the converters. Table 2 shows that the inverters in [36,37,39] have 13 elements, the inverter in [38] has 9, and the proposed inverter in [40] includes 11 components. The proposed converter has only six components in the QZS block and four power switches for FBI topology. Moreover, there is no power diode in the proposed inverter topology. The number of inductors in the proposed converter is less than the inductors in topologies [36,37,39], and the same is true for inverters in [40]. The inverter in [37] has the most, [39] has the least number of capacitors, and the proposed converter and the inverter presented in [36] include only two capacitors.

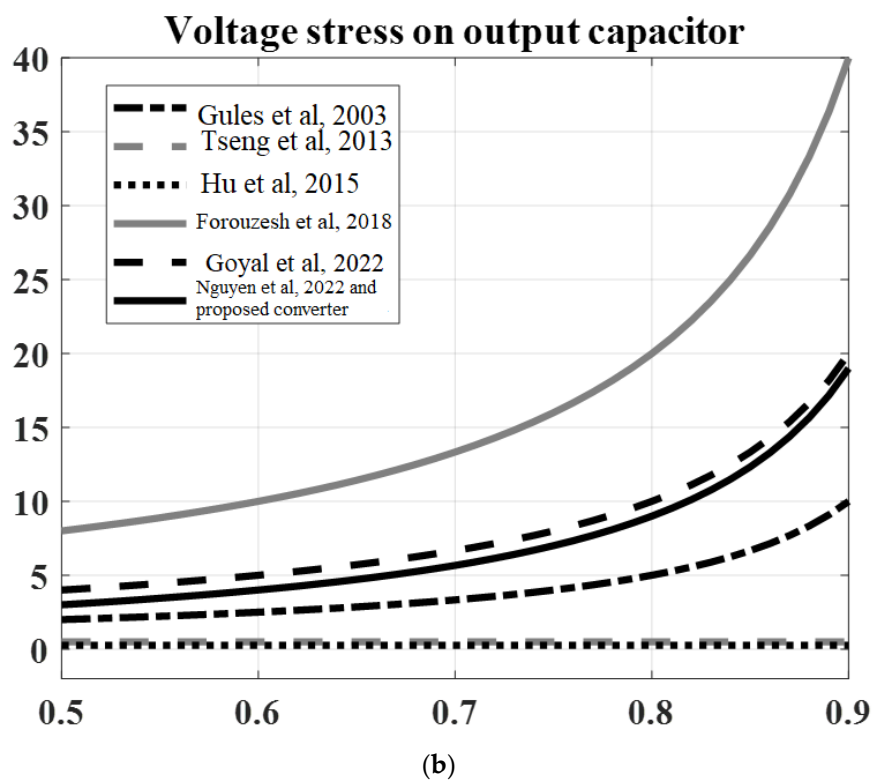
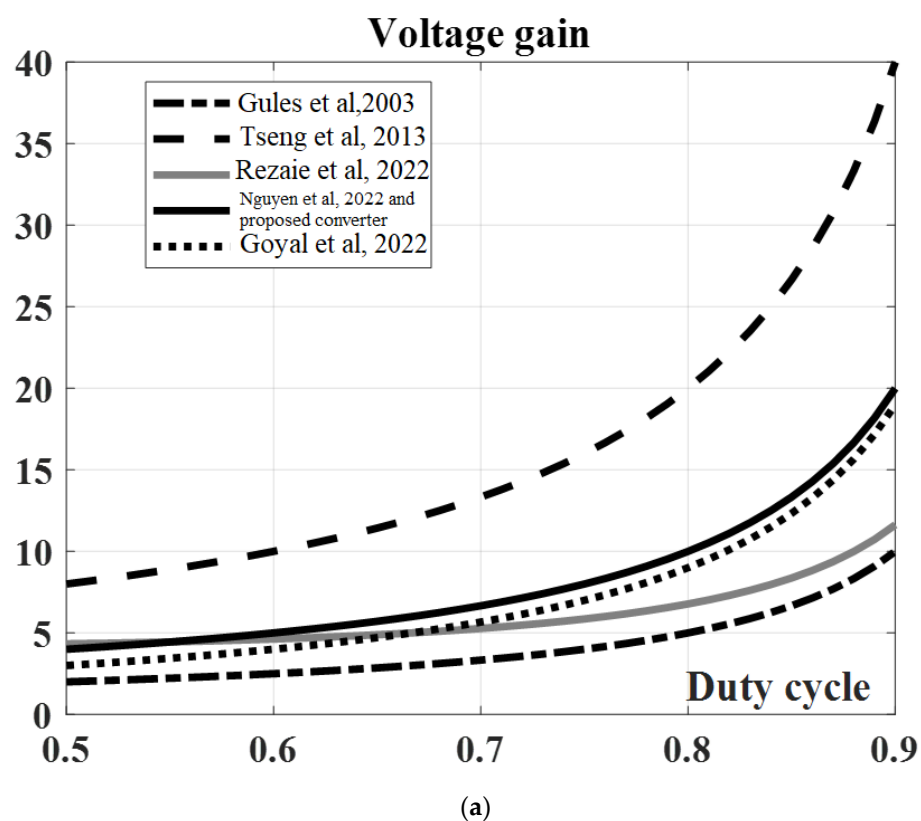


Figure 12. Cont.

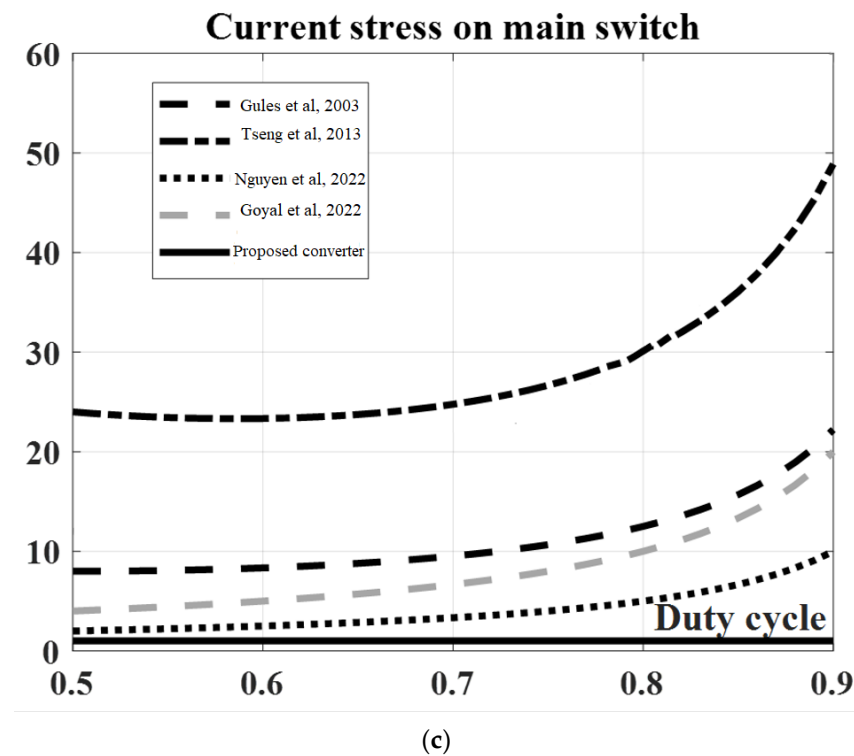
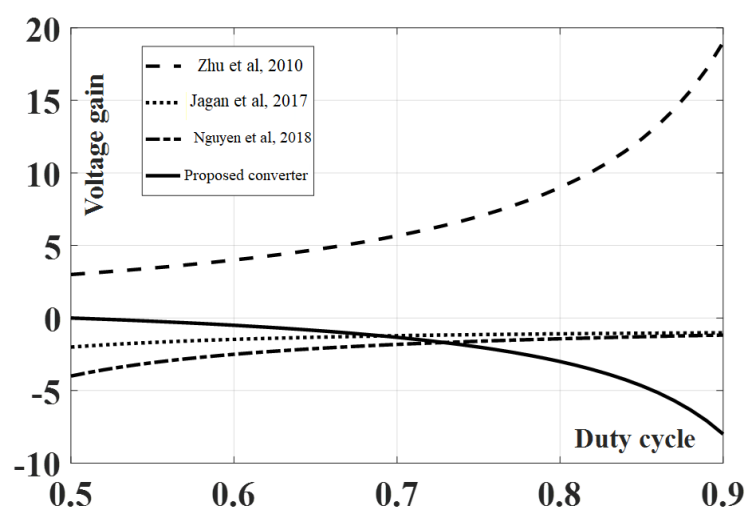


Figure 12. (a) Voltage gain: (b) voltage and (c) current stresses of the proposed boost converter in comparison with converters in [16–20] and [51,52].

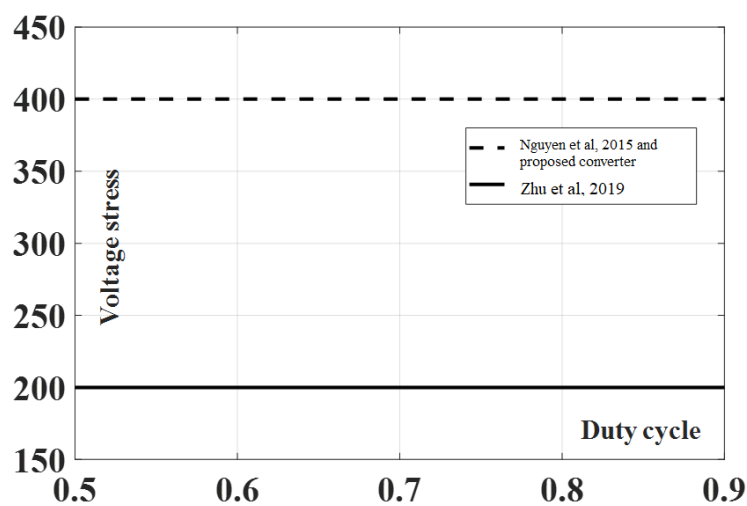
Table 2. Comparison between the selected and other Z-source converters.

	[36]	[37]	[38]	[39]	[40]	Proposed
Number of diodes	7	5	4	8	5	0
Number of switches	0	0	1	1	1	2
Number of inductors	4	4	1	3	2	2
Number of capacitors	2	4	3	1	3	2
Voltage Gain	$\frac{1+D}{1-3D}$	$\frac{1}{1-4D+2D^2}$	$\frac{2}{1-3D}$	$\frac{1+2D}{1-4D}$	$\frac{2}{1-4D+2D^2}$	$\frac{1-2D}{1-D}$
Voltage stress across the output capacitor	$\frac{1-D}{1+D} V_O$	$(1-D)^2 V_O$	$\frac{V_O}{2}$	V_O	$\frac{V_O}{2}$	V_O
Inductor current stress	$\frac{1-D}{1+D} I_O$	$(1-D) I_O$	$(1-D) I_O$	$\frac{1-D}{1+2D} I_O$	$(1-D) I_O$	$\frac{1-D}{1+D} I_O$
Voltage stress across the main switch	—	—	$\frac{V_O}{2}$	V_O	$\frac{V_O}{2}$	V_O

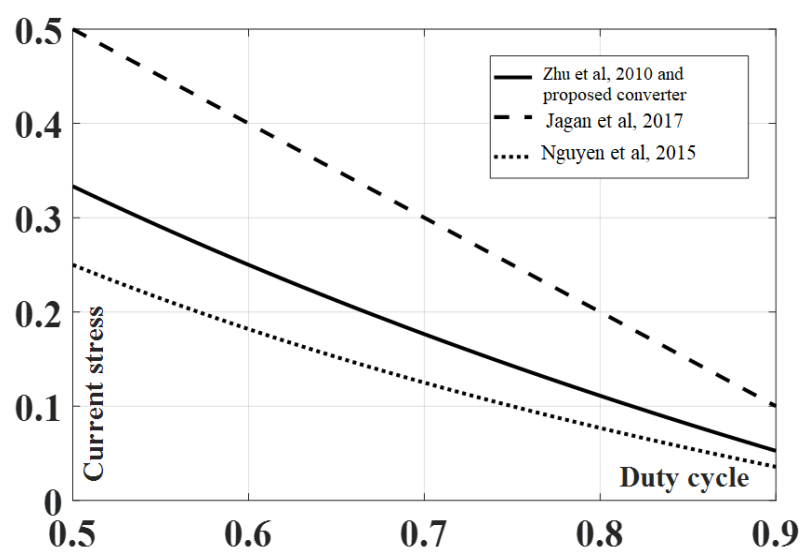
Figure 13a presents the gain of the inverter circuit in [36] as the most. After that, the proposed converter presents the next highest voltage gain. It is important to consider that a larger duty ratio for charging the inductors and the presence of current in the semiconductor elements that are the main sources of the dynamic losses generates currents with higher amplitudes and ripples that directly increase the power losses across the inductors, switches, and diodes. Therefore, longer duty cycles are not preferred, especially for high-power applications. The state of the gain curves for the inverters shows that the performance of the proposed QZS inverter circuit is appropriate in comparison with the other topologies by considering the number of elements and the ease of control and switching. Figure 13b shows the voltage stress across both power switches in the proposed topology and in comparison with other inverters. Half of the output voltage drops across switch S2, and the other half drops across switch S3. Totally, the output voltage is divided and drops across the switches that, with consideration of the other topologies, present an appropriate result.



(a)



(b)



(c)

Figure 13. (a) Voltage gain: (b) voltage and (c) current stresses of the proposed QZSI in comparison with inverters in [16–20] and [51,52].

The current stresses at the input side of the converters are presented in Figure 13c. This figure shows that the converter in [39] has the minimum current stresses for the input inductor, and this stress is a bit more for the proposed inverter and topology in [36]. Inverters in [37,38,40] have the most value of current stresses. All of these inverter circuits have important topologies and are the basis of new studies according to their advantages. By considering the features of these inverters, the number of used components, and the complexity of the control circuit and algorithm, the proposed inverter topology is comparable and presents many of the advantages.

The voltage and current stresses for the elements of the DC–DC boost converter are presented in Figure 14. Figure 14a,b show the current stresses for the switched-inductor block components including inductors L1 and L2 and diodes D2, D3, and D4. As presented theoretically, the current ripples of the inductors are the same, and the current ripples for the diodes are also equal. These figures show that the ripples of the current passing through the inductors are always smaller than the input. In addition the current ripples of the diodes when activated are always smaller than the input and inductor current ripples. The ripples magnitude for these diodes are considerable in comparison with the inductor current ripples.

Figure 14c is one of the most important figures that presents the current stresses of the switch and input diode D1 in comparison with the input current ripple. For all gain values, the current ripples for the main switch are more than the input ripples, and for higher DC gains, this value is increasing. In addition, the state of the ripples for diode D1 shows that the smaller gains cause this diode to pass currents with less ripples, and for higher DC gains, these ripples will increase.

As can be followed through the theoretical analysis and the configuration of the DC–DC converter, the voltage across capacitor C2 is the input voltage for the inverter side, and the stress for this capacitor is the same with output voltage. In addition, the voltage of capacitor C1 is smaller rather than the output voltage and follows the VC2. These states can be seen in Figure 14d.

The reversed biasing voltage across diodes D1 and D5 is reported in Figure 14e. As can be seen, the voltage stress for both of these diodes is the same, and with increasing the gain of the converter, the related reversed voltage also increases.

Finally, the voltage stress for the switch of the DC–DC converter in the proposed converter topology is illustrated in Figure 14f. This figure shows that the voltage stress across the switch is greater with higher DC gains in comparison with the input voltage, but the total voltage stress for the switch is acceptable by considering the amount of the output voltage.

For the ZSI cell, for the voltage equal to 96 VDC as the input voltage, a peak-to-peak voltage equal to 120 V drops across the inductors, and the same voltages are measured across capacitors C3 and C4. The maximum voltage across switches S2 and S3 is equal to the input voltage, and the same input current is reported for the switches. The currents following through the inductors are the same as the input current.

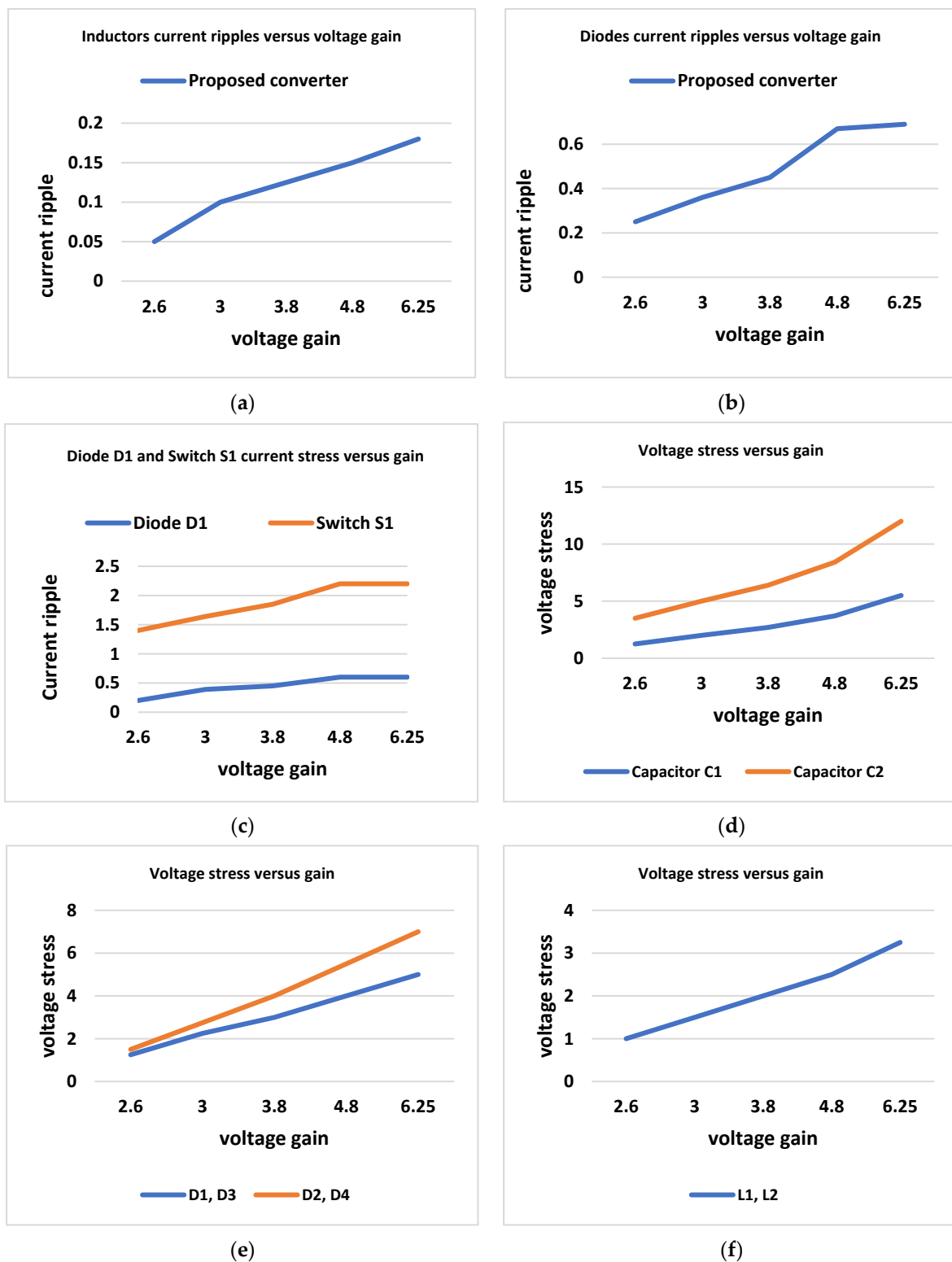


Figure 14. (a) $\frac{\Delta i_{L1}, \Delta i_{L2}}{\Delta i_{in}}$ versus gain; (b) $\frac{\Delta i_{D1}, \Delta i_{D2}, \Delta i_{D3}}{\Delta i_{in}}$ versus gain; (c) $\frac{\Delta i_{S1}}{\Delta i_{in}}$ versus gain; (d) $\frac{\Delta v_{C1}, \Delta v_{C2}}{\Delta v_{in}}$ versus gain; (e) $\frac{\Delta v_{D1}, \Delta v_{D2}}{\Delta v_{in}}$ voltage gain; (f) $\frac{\Delta v_{S1}}{\Delta v_{in}}$ according to gain of the converter.

4. Simulation Results

This section presents the simulation results for the proposed converter. Firstly, the main voltage and current signals of the proposed boost converter are presented, and then the results for the QSZI and FBI parts are illustrated. These results are presented for a prototype with 200 to 400 W and is in preparation for the comparison with the results

of the laboratory-scaled prototype circuit. To investigate fair theoretical and laboratory experimental studies and comparison, the same value of the elements are used. The component values based on the presented equations are reported in Table 3.

Table 3. Components values.

Component	Value of the Component for Both Theoretical and Experimental Studies
V_{in}	96 VDC
V_O , Boost converter	288 VDC
V_O , Inverter	220 Vac, RMS
RL Loads	200–400 W, 50 VAR
$L_1 = L_2$	440 μ H
C_1	220 μ F
C_2	680 μ F
$L_3 = L_4$	200 μ H
$C_3 = C_4$	10 μ F
Power Transistors	IXFH50N60P3
Power Diodes	DSEP30-06

Figure 15a presents the input source current, and Figure 15b,c show the switch and diode D1 currents, respectively. This figure indicates that the switch and diode D1 are working oppositely, and when one of these components is activated, the other one will be disconnected.

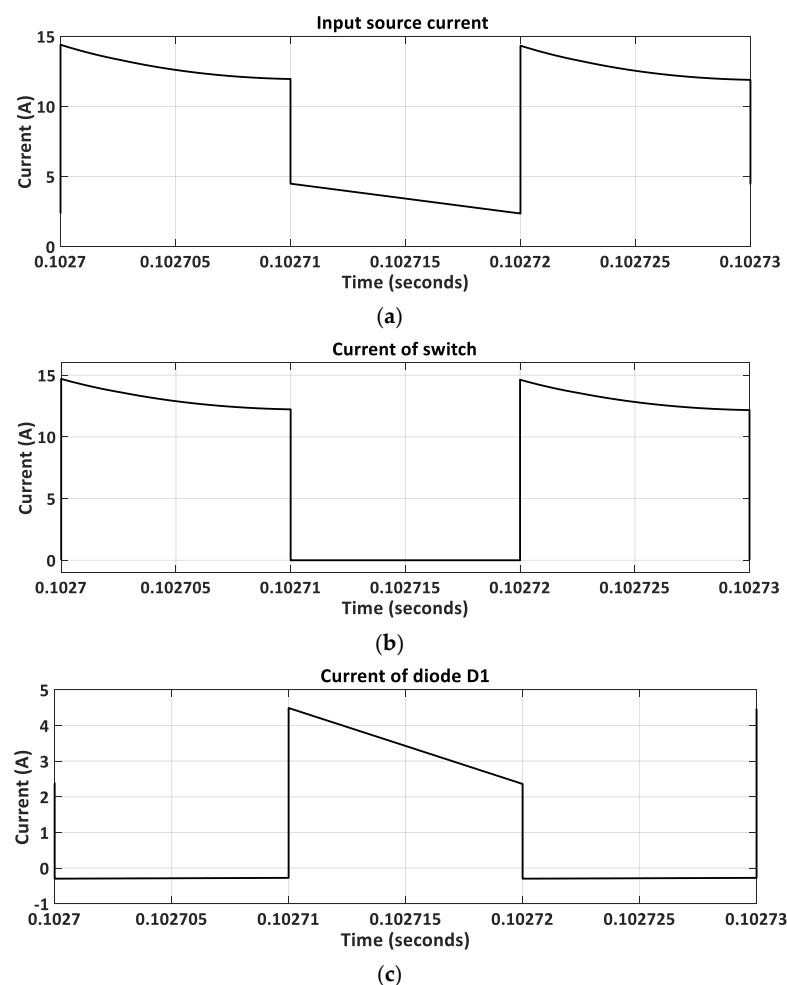


Figure 15. (a) Input source current and the current of the (b) switch and (c) diode D1 in the proposed boost converter.

In comparison with a conventional boost converter, the current wave at the input side changes at the switching times that causing electromagnetic interferences (EMIs). EMI is an undesired working state and appears in switching converters. EMI should be removed by using a CLC filter and is divided into conducted and radiated EMI. Figure 16 presents the general scheme of the EMI filter that should be located between the input source and the DC–DC converter. L_f is normally selected to be between 1 to 10 μH , most frequently close to 10 μH to support high current applications [41].

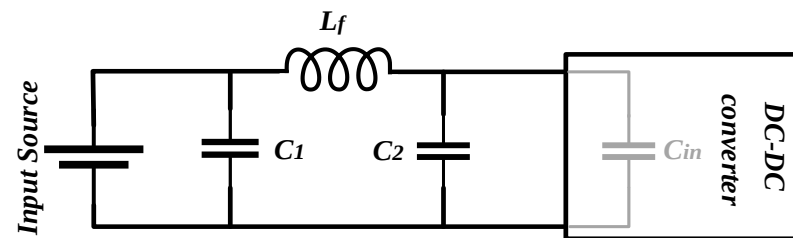


Figure 16. EMI filter design for the proposed boost converter.

The amount of capacitor C1 is defined by these two equations:

$$C_{1-1} = \frac{C_{in}}{C_{in}L_f(2\pi f_s/10)^2 - 1} \quad (55)$$

$$C_{1-2} = \frac{1}{L_f} \left(\frac{10^{|Att|_{dB}/40}}{2\pi f_s} \right)^2 \quad (56)$$

The value of C1 is selected as the higher value of C_{1-1} and C_{1-2} . In these equations, C_{in} is the input capacitor of the boost converter, and f_s indicates the switching frequency of the converter. $|Att|_{dB}$ is the requested debilitation according to the decibels and can be found through (57):

$$|Att|_{dB} = 20 \log \left(\frac{V_{in-ripple-p-p}}{1\mu V} \right) - V_{max} \quad (57)$$

where $V_{in-ripple-p-p}$ is the peak-to-peak input voltage ripple, and V_{max} represents the target maximum voltage in decibels. The amount of capacitor C2 is selected between 100 and 150 μF normally and is part of the input capacitors.

Figure 17a,b present the current and voltage waveforms of switch S_1 . These figures show that for the time intervals that the switch is activated, a voltage equal to zero drops across the drain-source pins, and for the time durations that the switch is deactivated, the current reaches zero amperes, and the voltage close to the voltage of capacitors C_1 and C_2 drops across the drain-source pins of this switch. An average current close to 2A is established in drain-source pins of the switch in a switching time period.

Figure 17c shows the voltages across the power diodes $D_1 - D_4$ in the boost converter. This figure confirms the results that were theoretically presented and shows that diodes $D_1 - D_3$ are activated at the same time intervals. In addition, the state of diodes $D_2 - D_4$ shows that these diodes are activated and deactivated simultaneously. The voltage across diodes D_2, D_3 , and D_4 is close to the input voltage, and the voltage of D_1 is close to the output voltage of the proposed boost converter since is connected to the output capacitors.

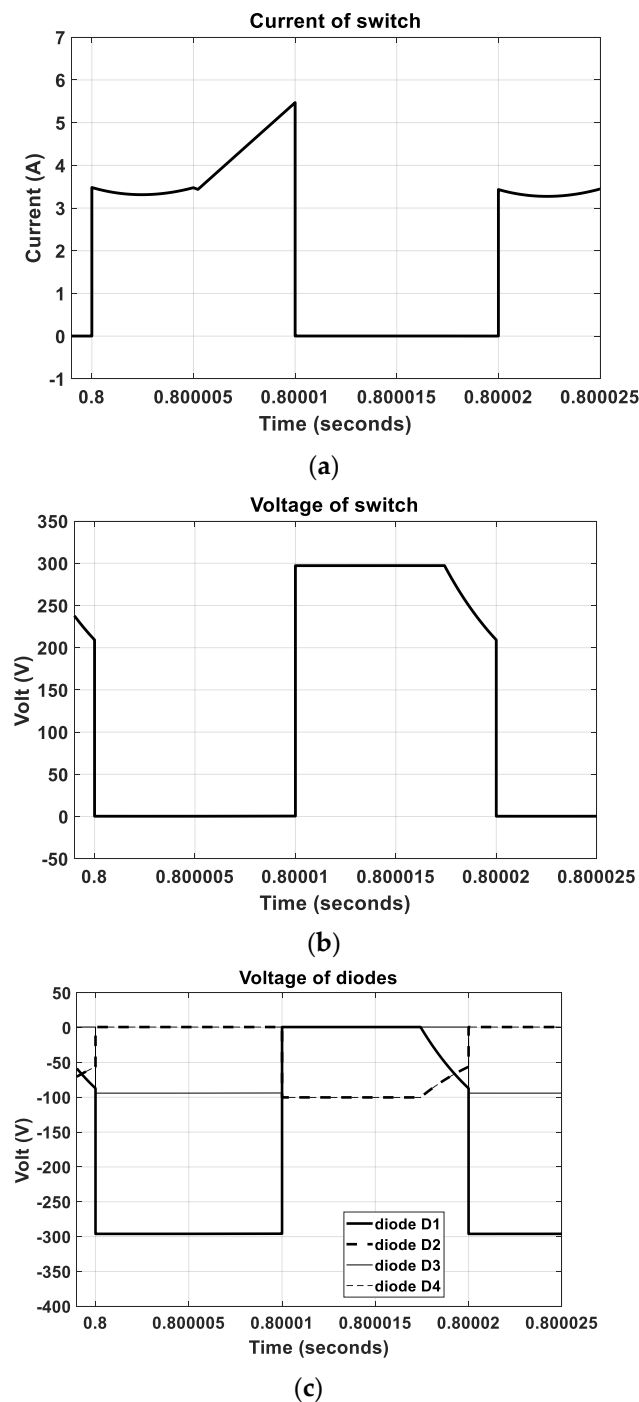


Figure 17. (a) Current and (b) voltage stresses of switch S1; (c) voltage waveforms across diodes $D_1 - D_4$ in the proposed boost converter.

The voltage across inductors L_1 and L_2 is shown in Figure 18a. This figure confirms that these inductors are charged and discharged simultaneously and proves that the presented theorem around the switched-inductor topology in the presented boost converter is correct. The maximum and minimum magnitudes of the voltage across these inductors are close to the input voltage, and the figure shows that the average voltage of the inductors is zero. Figure 18b illustrates the voltage across capacitors $C_1 - C_2$. This figure directly guarantees the correctness of Equations (5) and (6) and shows that the voltage of the capacitors are approximately the same. In addition, a voltage close to the 288VDC was predicted to be obtained across these capacitors theoretically, and voltages close to 282 and 280 VDC are obtained for the C_1 and C_2 capacitors in simulation. All internal resistances and non-ideal

working conditions are important parameters for this ignorable difference that is considered in the simulation steps.

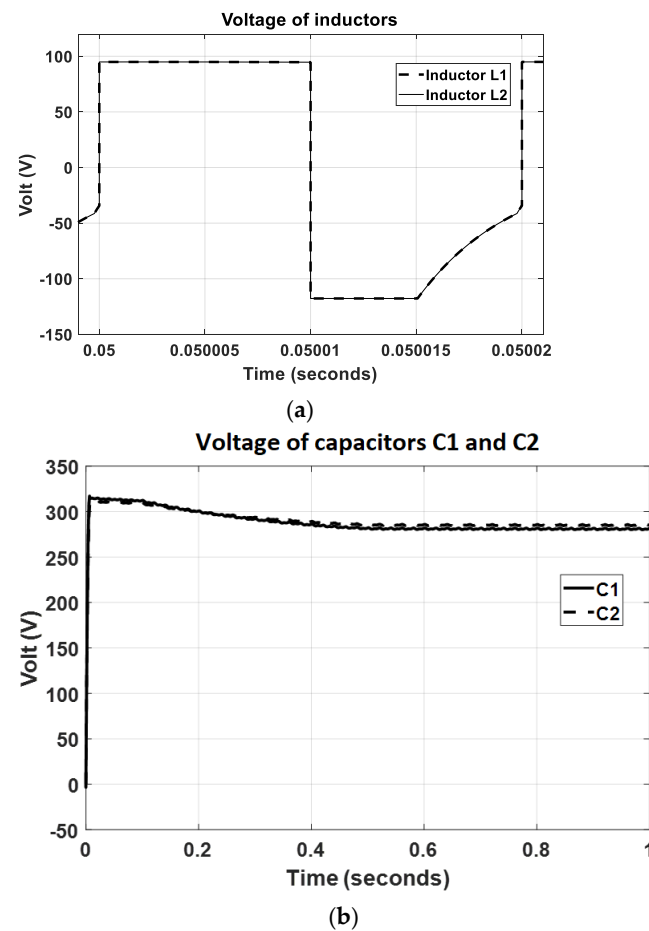


Figure 18. Voltage waveforms across inductors $L_1 - L_2$ (a) and capacitors $C_1 - C_2$ (b) in the proposed boost converter.

According to Equation (5), the voltage across capacitor C_1 by considering $V_{in} = 96$ VDC and $D = 0.5$ is predicted to be close to 288 VDC in the ideal working state and without considering the voltage drops and power losses across the components. Since the average voltage drop across inductors L_1 and L_2 is zero in a switching time period, a similar voltage is obtained across capacitor C_2 .

The state of the currents for the inductors in the QZSI circuit is shown in Figure 19a. This figure shows that for the power values between 200 and 400 W, a maximum value of 20 A and a minimum value of 10 A is established through these inductors. Currents with fewer amplitudes can be obtained by the application of larger inductors. Figure 19b,c present the state of the current for the same inductors L_3 and L_4 with 300 and 400 μ H inductivity, respectively. In addition, the voltage across capacitors C_3 and C_4 is presented in Figure 19b. The same form of the current waveforms with the same amplitude is obtained for these capacitors. The voltages across switches S_2 and S_3 are shown in Figure 20. The state of the switches guarantees that in any time interval only one of these transistors is activated. In addition, the amplitude of the voltage across the drain and source pins of these transistors is related to the input voltage, output voltage, and modulation index that is more than $M > 0.7$. The reason for this value for the M is the desired voltage amplitude at the load side that should be around 311VAC and 220 volt root-mean-square (RMS).

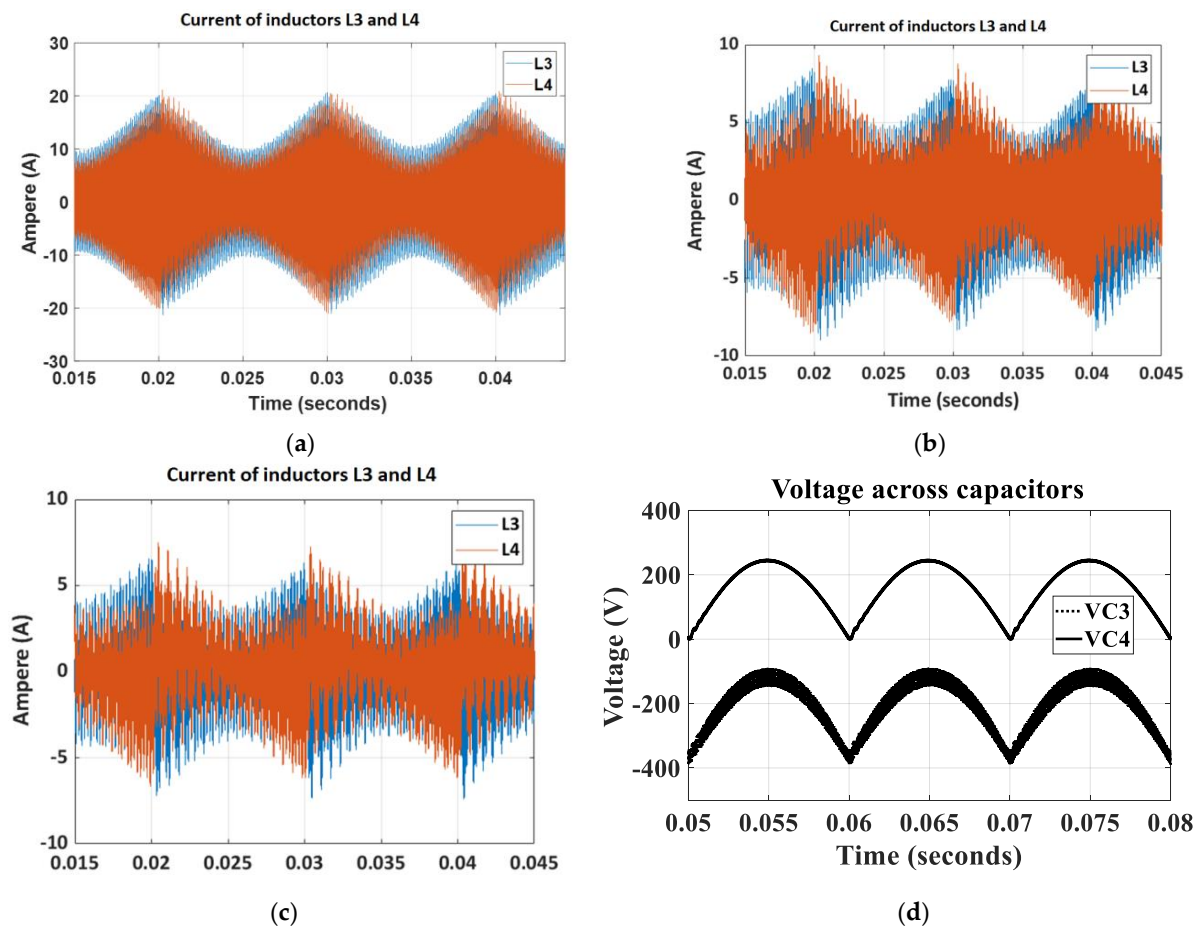


Figure 19. (a–c) Currents of inductors L_3 and L_4 ; (d) voltage waveforms across capacitors $C_3 - C_2$ in the proposed QZS converter.

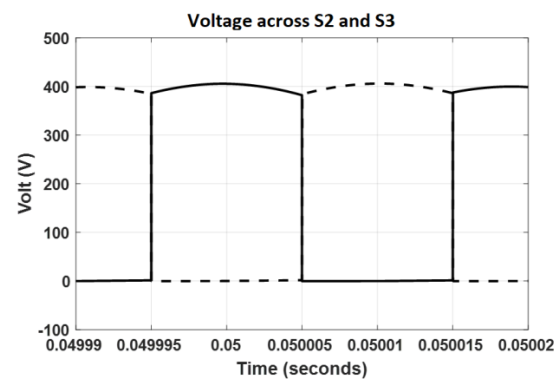


Figure 20. Voltage waveforms across the switches S_2 and S_3 in the proposed QZS converter.

The voltage waveforms for the transistors in the FBI circuit are shown in Figure 21a,b. One of the most important results is shown in these two figures. The maximum side of the output voltage is supplied by the $Q_1 - Q_2$ pair, and the minimum and negative side of the output voltage is prepared by the $Q_3 - Q_4$ transistor pair. It is important to carefully observe the sequence of the generated voltages by these pairs and see that for the time intervals that the $Q_1 - Q_2$ pair is generated, the positive side of the sinusoidal voltage of the generated voltage by the $Q_3 - Q_4$ is zero. When the $Q_3 - Q_4$ pair generates the negative side of the output sinusoidal voltage, no voltage is generated by the $Q_1 - Q_2$ pair. The final state of the output voltage with the present sinusoidal state is shown in Figure 21c, and the current waveform is presented in Figure 21d. The quality of the generated voltage and

currents is considerable. The RL type of the loads is selected to behave as the real state of the loads, and in order to be comparable with the laboratory test results, the amount of the R and L are selected as 200–400 W and 50 VAR, respectively. Figure 21e,f show the output voltage and current waveforms for a heavier load. For that, a similar RL load is connected across the first load at $t = 0.1$ s, and the behavior of the voltage and current waveforms are investigated. As can be seen, no change including any type of undershoots or overshoots is obtained for the voltage, and current is doubled at $t = 0.1$ s. To show the reaction of the proposed topology under resistive load, Figure 21g,h are presented. These two figures show the output current waves for the single and doubled resistive loads, respectively. Firstly, only one resistive load is considered, and then the second load equal to the first resistive load is added at $t = 0.045$ s. These waves show that the current is simply doubled.

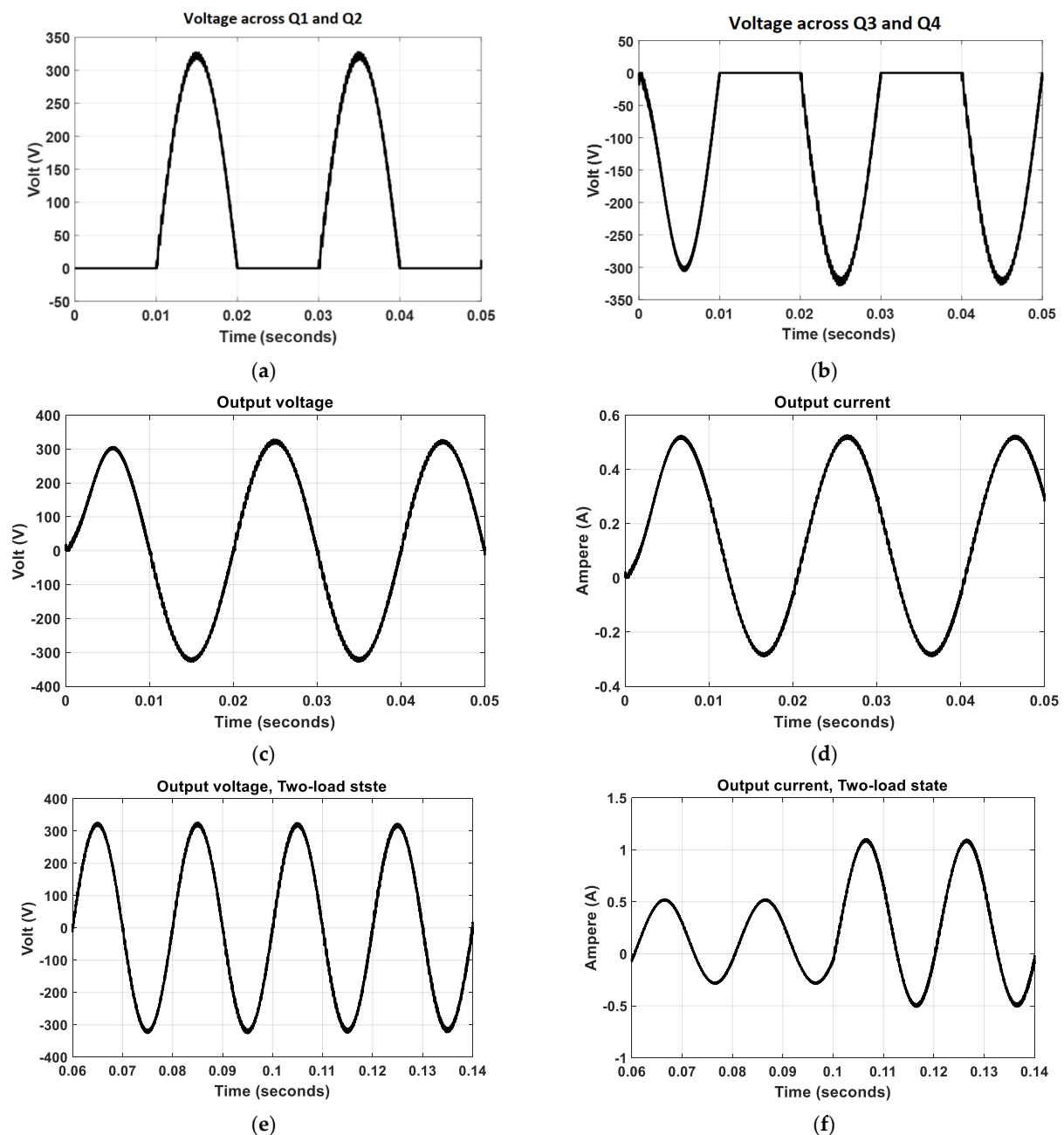


Figure 21. Cont.

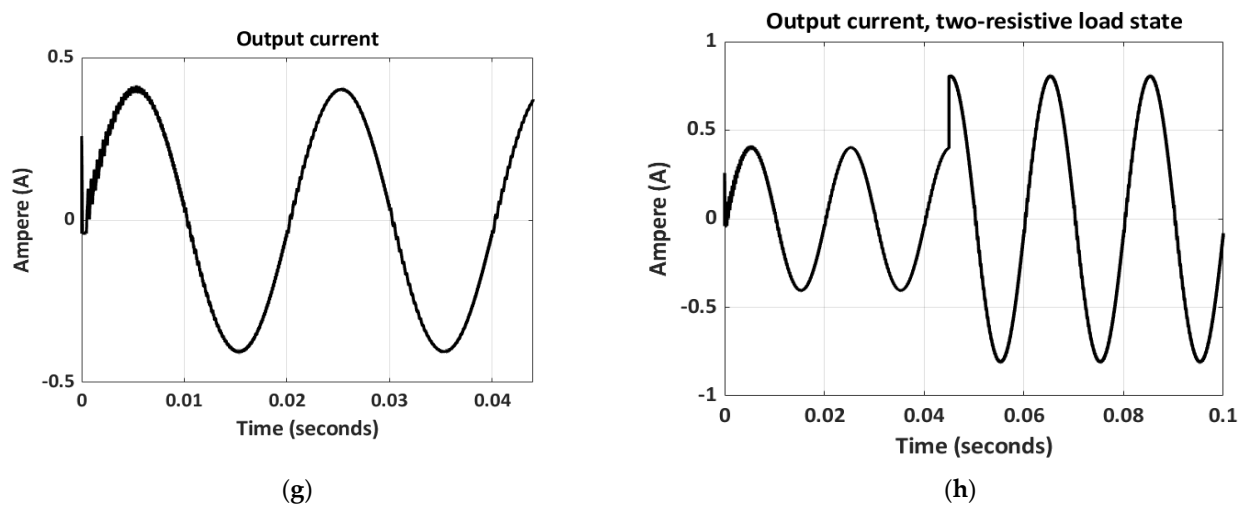


Figure 21. Voltage waveform across the transistors: (a) $Q_1 - Q_2$; (b) $Q_3 - Q_4$; (c) output voltage; (d) output current in one-load (RL); (e) output voltage in two-load (RL) states; (f) output current in two-load (RL) states, (g) output current in one-load (R); (h) output current in two-load (R) states.

5. Experimental Results

A prototype circuit with all details presented in Table 3 was established in the laboratory, and some of the results are reported in this section. A 96 DV voltage at the input side of the step-up converter was established, and finally a sinusoidal output voltage was obtained across the load nodes with 50 Hz frequency and around 220 RMS. The amount of the inductors and capacitors and the power semiconductor devices are the same with the considered devices in the simulation. Figure 22 presents the test results.

Figure 22a presents the voltage across inductors L1 and L2 at the boost converter side. According to the simulation results, a peak-to-peak voltage around 240 V should be obtained for these inductors. Test results confirm the correctness of the simulation results. The switching frequency at the boost converter side is equal to 50 kHz. Another result is that both inductors are charged and discharged simultaneously according to the theoretical results. Figure 22b shows the voltage across two D1 and D2 diodes. This figure easily proves that these diodes are activated in two different time intervals and work in reverse. Adjustable probes are used, and the volume on the probes are set to show the real measured voltages; -300 and -100 volts are obtained across these diodes.

Two interesting results are obtained in Figure 22c,d, and the voltage across the switches Q_1 - Q_2 and Q_3 - Q_4 are reported. As expected, rectified voltage waves with maximum and minimum amplitude of the output voltage and 50 Hz frequency are obtained for these pairs of transistors. These voltages are considered as the input voltage for the full bridge inverter block, and finally a fully sinusoidal voltage is obtained for the load. These voltage waves are presented in Figure 22e,f for RL and R loads, respectively. As mentioned, the volumes on the probes are adjusted to show the actual measured values. This sine wave is obtained for a 200 W and 50 VAR RL load. In addition, the same working condition is tested for the 200 W resistive load. A pure sinusoidal voltage waveform is reported for this operational state.

Figure 22g presents the input and output voltages of the boost converter. The output voltage of the quasi Z-source inverter across capacitor C4 is shown in Figure 22h. A full rectified voltage with about 310 V amplitude is reported across this capacitor with 50 Hz of frequency. After hardware tests in the laboratory for a group of load with a power maximum to 400 W, the efficiency diagram of the converter is obtained and reported in Figure 23. To evaluate the performance of the proposed boost converter-based QZS inverter, the similar converter topologies are considered and reported. As a result of examining the efficiency performance of the proposed converter circuit, it was noted that the highest efficiency of the circuit is obtained for powers above 350 watts. Compared with

other inverter circuits, the proposed inverter circuit performed above the average. These converter circuits are taken from articles published in the last 3 years.

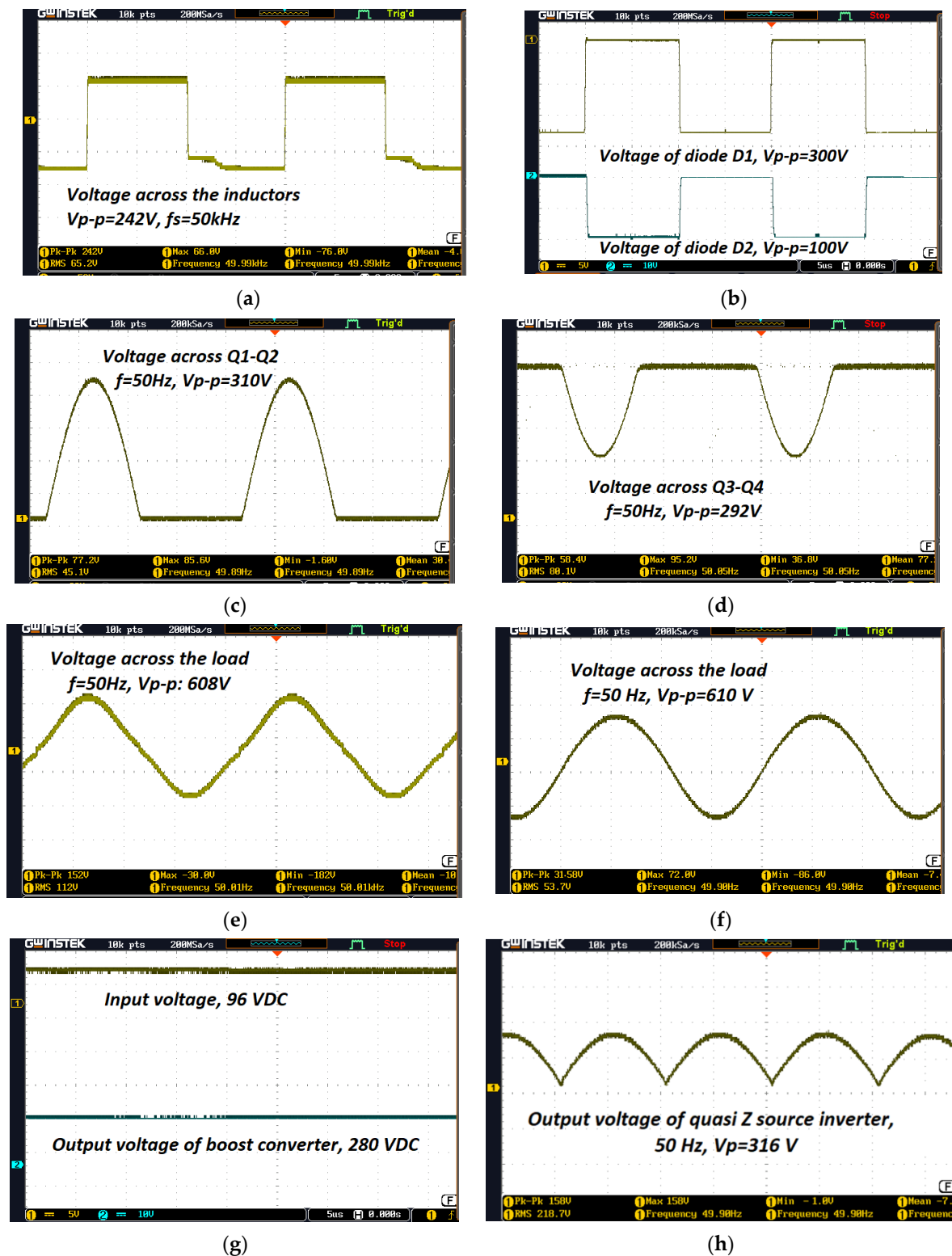


Figure 22. Test results: (a) voltage of inductors L1 and L2; (b) voltages of diodes D1 and D2; (c) voltages across the transistors Q1–Q2; (d) Q3–Q4, output voltage under (e) resistive–inductive; (f) resistive loads; (g) input–output voltages of boost converter; (h) output voltage of quasi Z-source inverter.

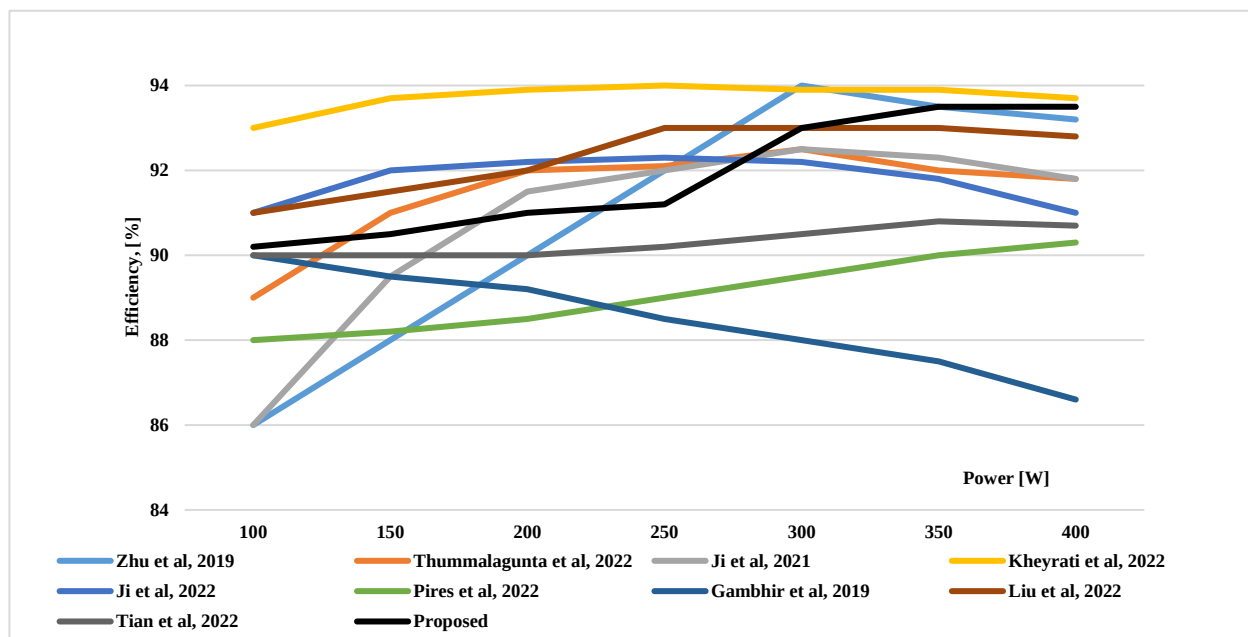


Figure 23. Measured efficiency and comparison with similar topologies [42–50].

According to the results, for input power equal to 100 W, 200 W, 300 W, and 400 W, respectively, 9.8 W, 18 W, 21 W, and 26 W, were reported as the power losses. Theoretical analysis shows that the main sources of the power losses are the semiconductor devices, and the test results confirm the theory. The test results in Figure 24 show the distribution of the power losses for the devices at different powers.

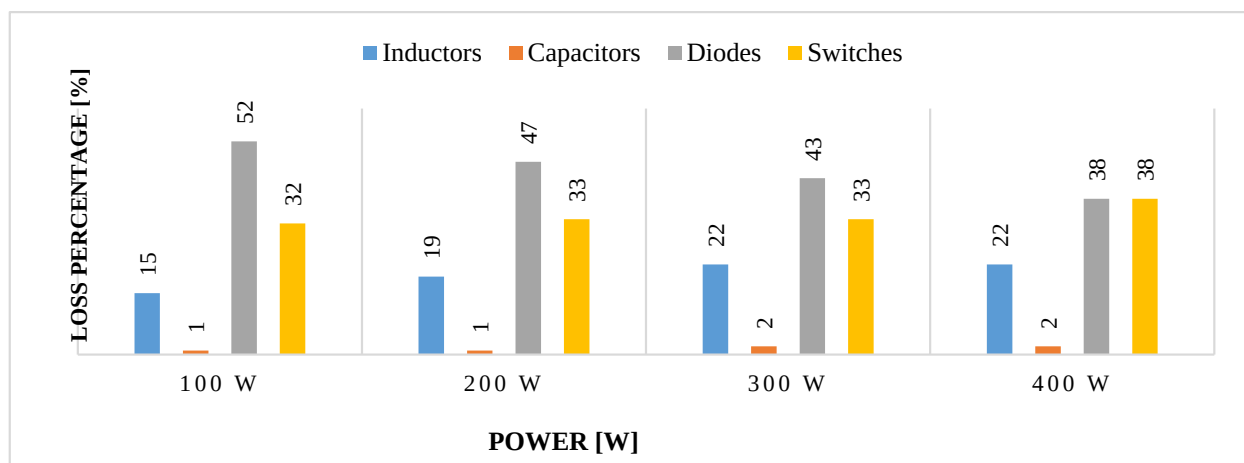


Figure 24. Power loss distribution for elements of a converter.

According to this figure, the main source of the power loss is the power diodes, and the minimum loss is for capacitors. The power losses for the diodes for the higher current values in the circuit are smaller, while the losses for the inductors are greater. Results show that the power losses for the switches are more in accordance with increasing current values in the circuit.

6. Conclusions

A DC to AC power converter topology is presented in this study. The configuration of the proposed converter is preparing the circuit for low input voltage applications, such as the photovoltaic approaches. For that, at the first stage, this limited DC input voltage is

enhanced through an optimized boost converter and then by the application of a modified quasi-impedance source inverter. A pair of positive and negative rectified AC voltage is obtained. At the final stage, these voltages are mixed in a full bridge inverter, and fully sinusoidal voltage is obtained for the load. For the boost converter, a switched-inductor block is used instead of the inductor, and the location of this component and power diode is changed. In comparison with a conventional step-up converter, not only is the gain of the converter increased, but also the ripples of the input current of the converter are decreased, which will obtain a more reliable converter topology with a longer lifetime of the input voltage source. On the quasi Z-source side, a pair of power transistors are used in the converter. Since the conventional Z-source inverters do not have any power semiconductor in their topology, the modified converter will have some advantages, such as the adjustable voltage gain on the output side of the converter in comparison with its input voltage. A modified sinusoidal PWM technique is used, and positive and negative voltages are formed at the output nodes of this block. Finally, a full bridge inverter simply mixed these voltages, and fully sinusoidal voltages are obtained at the load nodes. The presented topology can be used in different power classes and values.

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