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Perspective

Recent Developments and Prospects of Fully Recessed MIS Gate Structures for GaN on Si Power Transistors

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Abstract: For high electron mobility transistors (HEMTs) power transistors based on AlGaN/GaN heterojunction, p-GaN gate has been the gate topology commonly used to deplete the two dimensional electron gas (2-DEG) and achieve a normally-OFF behavior. But fully recessed MIS gate GaN power transistors or MOSc-HEMTs have gained interest as normally-OFF HEMTs thanks to the wider voltage swing and reduced gate leakage current when compared to p-GaN gate HEMTs. However the mandatory AlGaN barrier etching to deplete the 2-DEG combined with the nature of the dielectric/GaN interface generates etching-related defects, traps, and roughness. As a consequence, the threshold voltage (V_{TH}) can be unstable, and the electron mobility is reduced, which presents a challenge for the integration of a fully recessed MIS gate. Recent developments have been studied to solve this challenge. In this paper, we discuss developments in gate recess with low impact etching and atomic layer etching (ALE) alongside surface treatments such as wet cleaning, thermal or plasma treatment, all in the scope of having a surface close to pristine. Finally, different interfacial layers, such as AlN, and alternative dielectrics investigated to optimize the dielectric/GaN interface are presented.

Keywords: MOSc-HEMT; GaN; MOS; Etching; surface preparation; insulator; interface

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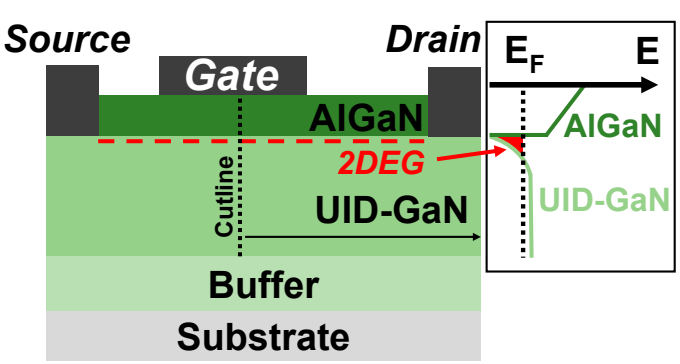
1. Introduction

The major challenge of power electronics today is dealing with the need for high conversion efficiency and reliability, and at the same time, the constant pursuit of cost and size reductions, with low environmental impacts. Replacing power devices made of silicon semiconductor material by power devices made of wide bandgap semiconductor materials such as gallium nitride (GaN) allows for smaller size, cost reduction, and higher switching speed at the power system level, thanks to better GaN intrinsic physical parameters. Noticeably, the AlGaN/GaN heterojunction allows to get a high mobile electron layer and to design GaN FETs such as HEMTs which offers high power density and high switching frequency.

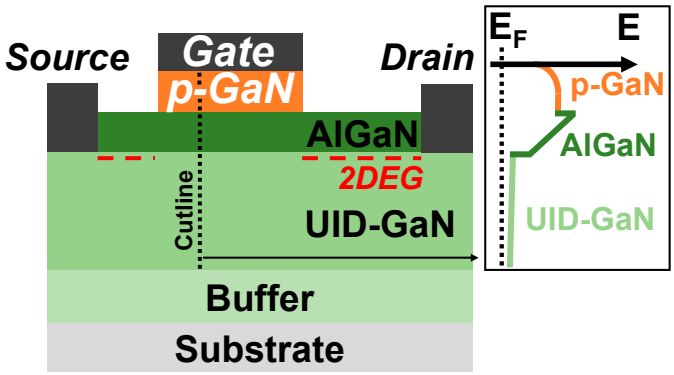
GaN transistors are faster and smaller than silicon MOSFETs thus leading to increased power density in chargers and adapters as well as high efficiency due to reduced conduction and switching losses. At the moment, the market of GaN power transistors with a positive threshold voltage (V_{TH}), or normally-OFF, is completely dominated by p-GaN gate architecture (proposed by EPC, GaN Systems, Panasonic for instance). Typical Mg concentrations used in p-type GaN layer are around 1×10^{19} cm^{-3} [1], the Mg saturation being as high as 8.9×10^{19} cm^{-3} [2]. However, since acceptor levels from Mg are in the range of 150–200 mV from the valence band, ionization of Mg is limited to a fraction of its concentration. However, the p-GaN gate architecture has intrinsic limits with respect to its

silicon power MOSFET counterparts. Because of the p-GaN gate topology, V_{TH} is generally limited to 1.5 V and the typical recommended gate drive is in the range of 0 V to 6 V or −3 V to 6 V for high current hard switching applications. Metal–insulator–semiconductor gate (MIS Gate) GaN transistors could give greater freedom in terms of gate driving voltage as a result of both increased threshold voltage and larger range in gate voltage swing. Alongside power applications, MIS Gate GaN transistors can be implemented for RF [3], gas sensing [4], and LiDAR [5]. Considering the benefits of a MIS Gate, the fully recessed MIS (metal insulator semiconductor) gate stack has gained increasing interest during the last few years for the development of normally-OFF lateral [6], pseudo-vertical [7], and vertical GaN on Si [8] power transistors. This structure is described in the literature by different names such as MOS-HEMT and MIS-FET which are also used to describe partially recessed MIS gates that allow us to obtain a normally-OFF transistor as well. In order to specifically describe the fully recessed MIS gate GaN HEMT, we chose to name it by MOS-channel-HEMT or MOSc-HEMT. Combining the benefits of a MIS gate, its interest comes from the fact that it allows to have a device with a positive threshold voltage by cutting the 2-DEG, low gate leakage current and high gate voltage swing. The MOSc-HEMT also enables a more stable V_{TH} than partially recessed MIS gate since the latter suffers from etching thickness variability affecting the V_{TH} [9]. The mentioned topologies as well such as the fluorine implanted gate and the cascode configuration are represented in Figure 1.

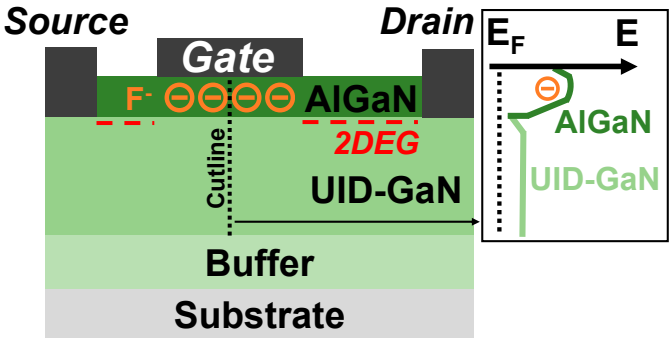
To get the full benefits of the fully recessed MIS gate, it is required to optimize the insulator–semiconductor interface in order to achieve good mobility and low interface trapping states. It is equally essential to tune the insulator properties in view of limiting or controlling its charge. For this reason, several process steps have been studied showing both the impact of AlGaN/GaN recess, cleaning, and dielectric deposition. The different defects at the MIS gate are represented in Figure 2.



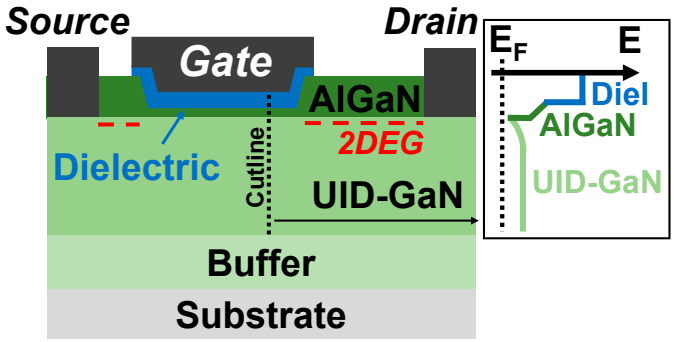
(**a**) Normally-ON GaN HEMT



(**b**) Normally-OFF p-GaN gate GaN HEMT

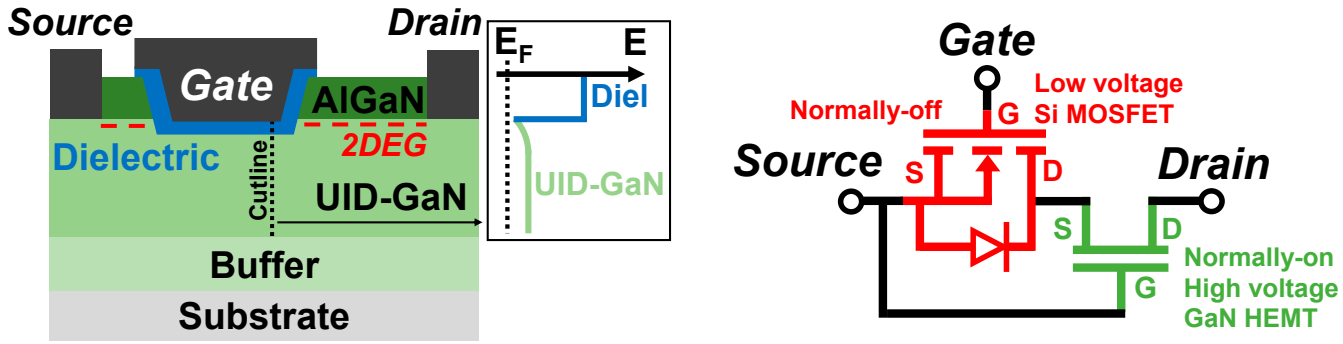


(**c**) Normally-OFF Fluorine implanted gate GaN HEMT



(**d**) Normally-OFF Partially recessed MIS gate GaN HEMT

Figure 1. *Cont.*



(**e**) Normally-OFF Fully recessed MIS gate GaN HEMT or MOSc-HEMT (**f**) Cascode configuration

Figure 1. Structure for (**a**) normally-ON GaN HEMT and different topologies of normally-ON GaN HEMTs: (**b**) p-GaN gate; (**c**) Fluorine implanted gate; (**d**) Partially recessed MIS gate; (**e**) Fully recessed MIS gate or MOSc-HEMT; (**f**) Cascode configuration (schematic inspired by [10]). Energy band diagrams are represented alongside the structures.

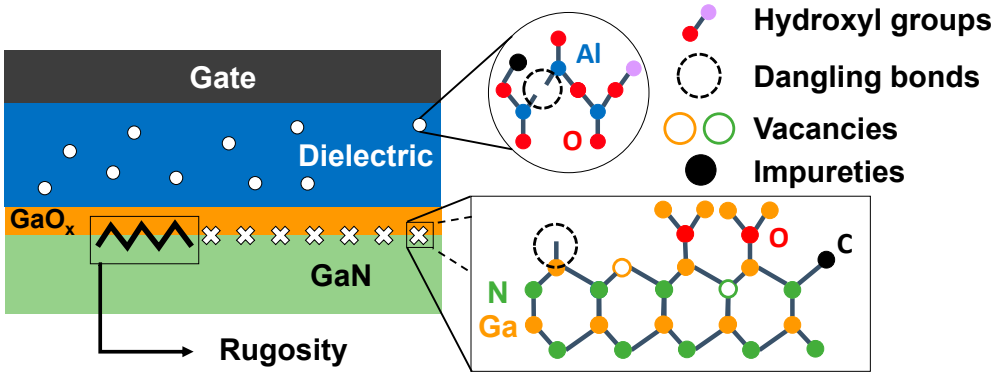


Figure 2. Different types of defects and impurities effectively or hypothetically encountered with fully recessed MIS gate.

Overall, these studies have been carried on either transistors or simple planar capacitors. In the case of transistors, parameters such as V_{TH}, its hysteresis (ΔV_{TH}), and channel mobility can be measured. But for simple planar capacitors, flat band voltage (V_{FB}), its hysteresis (ΔV_{FB}), and density of interface states (D_{it}) are usually studied to evaluate the properties of the dielectric/GaN interface. If the correspondence between results from transistors and planar capacitors can be established, with deeper recess depth, the impact of sidewalls is no longer negligible and needs to be taken into account. Moreover, planar capacitors will have an intentional n-doping in order to provide free carriers for positive voltage swing of C–V measurements, whereas transistors will have an unintentional doped (UID) GaN layer. Alongside electrical characterization, physical parameters such as roughness, presence of impurities and defects, and oxidation have been measured using different characterization techniques as AFM, XPS/HAXPES, and ToF-SIMS. Studying the physical parameters allows us to better understand the critical dielectric/GaN interface. Hence, combining both electrical and physical characterization has been proven important to better investigate the MIS gate and improve it.

2. Manufacturing Processes from Gate Recess to Surface Preparation

2.1. Gate Recess by Dry Plasma Etching

Etching is necessary to achieve a fully recessed gate structure in order to remove the passivation layers, the AlGaN barrier layer and a part of the GaN channel.

2.1.1. Reactive Ion Etching ICP-RIE

Reactive ion etching (RIE) is a form of dry plasma etching involving a mixture of different elements:

- Reactive and nonreactive ions;
- Reactive neutral species;
- Passivating species;
- Electrons;
- Photons.

The positively charged ions are guided towards the wafer surface through an applied negative bias on the wafer, and their acceleration is normal to the wafer surface. Alongside the neutral species present in the plasma, the positive ions work in unison to etch the wafer surface.

For wide bandgap semiconductors, the application of high-density plasma in etching processes such as electron cyclotron resonance (ECR), inductively coupled plasma (ICP), and magnetron RIE was proven to achieve better etching characteristics than simple RIE. The reason for this enhancement can be explained by the higher plasma density, which is typically two orders of magnitude higher than RIE (10^{11}–10^{12} cm^{-3} against 10^{9}–10^{10} cm^{-3}). This increased plasma density leads to a higher efficiency in breaking bonds for these strongly bonded semiconductors and facilitates the removal by sputtering of etching byproducts formed on the surface [11].

The use of inductively coupled plasma (ICP) reactors allows the separate control of the plasma density (chemical part of the etching, controlled with inductance power) and the bombardment energy (physical part of the etching, controlled with bias voltage); unlike capacitance coupled plasma (CCP) reactors where the plasma density and bombardment energy are controlled together.

GaN is usually etched using fluorine-based or chlorine-based plasmas. ICP-RIE etching of GaN using these plasmas cannot be purely chemical at room temperature because of the formation of nonvolatile etching byproducts such as GaF_x (T_{eb} = 1000 °C) with fluorine-based chemistries (e.g., SF_6) or $AlCl_3$ (T_{eb} = 183 °C) and $GaCl_3$ (T_{eb} = 201 °C) with chlorine-based chemistries (e.g., Cl_2) [11]. Therefore, the physical bombardment should be sufficiently strong to remove these byproducts and to expose the surfaces for further etching, for instance using Ar or N_2 in combination with SF_6 [12] or Ar in combination with Cl_2 [13]. Addition of noble gases and energetic-ion sputtering in ICP also improves the etching both by initially breaking the stable Ga–N bond and by preferentially sputtering the nitrogen atoms, which results in a Ga-rich GaN surface [14]. XPS measurements of the GaN surfaces etched by SF_6 and Cl_2 indicate, respectively, the presence of F and Cl on the etched GaN surface [15]. Worse on-state characteristics were observed with SF_6 etching, assumed to be due to deterioration of the negative V_{TH} with F [15]. Moreover, since Cl-based byproducts are more volatile, the etching process is faster. Therefore, etching of GaN using chlorine-based plasma is preferred to fluorine-based plasma.

Gallium oxide can be present at the GaN surface or may form during the etching process since the etching chamber can contain small amounts of oxygen (chamber walls, mask layers on the wafer). BCl_3 is helpful for gallium oxide removal as BCl_2^+ ions dissociated from BCl_3 are good Lewis acids with strong oxide affinity, leading to the formation of BCl_xO_y (g) [16]. Therefore, etching of GaN is usually performed using Cl_2 and BCl_3 chlorine-based plasma. By increasing the bias power, the physical component of the etch process is enhanced, as confirmed by linear correlation between ICP bias power variation and AlGaN, GaN, and AlN etch rate [17].

The use of other chemicals such as $SiCl_4$ have been reported to tune the profile shape, for instance $SiCl_4$ passivates the sidewalls by formation of SiO_x and SiN_x, leading to a more vertical profile [18].

Continuous dry etching on GaN has fast etch rates, but the surface damage as shown in Figure 3 (composition/roughness), the high variability and the non-uniformities at wafer and die level are, at present, the three main shortcomings [19,20].

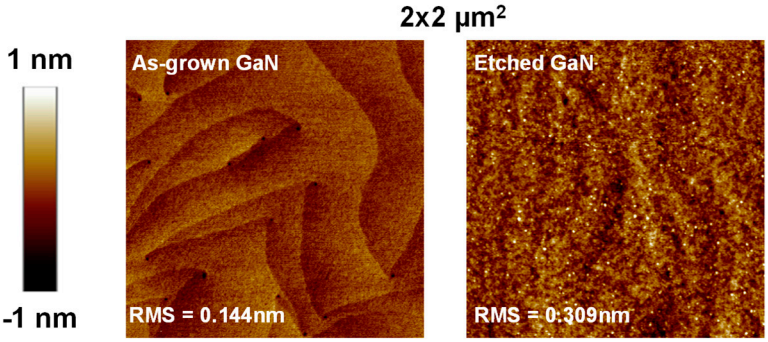


Figure 3. GaN surface before and after etching observed by AFM. The etching process is similar to the process used in [21].

2.1.2. Plasma Induced Damage

The device's performance can be seriously degraded due to the creation of plasma-induced damage, which occurs as a result of ion bombardment and exposure to ultraviolet (UV) photons during plasma assisted etching. Plasma-induced damage includes the following defects:

1. Lattice defects generated from energetic ions. These defects typically exhibit deep level states behavior and thus produce compensation, trapping, or recombination in the material. Due to channeling of the low energy ions that strike the sample, and rapid diffusion of the defects created, the effects can be measured as deep as 1000 Å from the surface, even though the projected range of the ions is only <10 Å [22];
2. Atomic hydrogen unintentional passivation of dopants. The hydrogen may be a specific component of the plasma chemistry, or may be unintentionally present from residual water vapor in the chamber or from sources such as photoresist mask erosion. The effect of the hydrogen deactivation of the dopants is a strong function of substrate temperature, but may occur to depths of several thousand angstroms [22];
3. Polymeric film deposition through plasma chemistries involving CH_x species, or through reaction of photoresist masks with Cl_2-based plasma [22];
4. Nonstoichiometric induced surfaces by selective removal of specific lattice elements. This can occur because of strong differences in the volatility of the respective etch products, leading to enrichment of the less volatile species, or by preferential sputtering of the lighter lattice element if there is a strong physical component to the etch mechanism. Typical depths of this nonstoichiometry are <100 Å [22].

In the case of AlGaN/GaN etching, various studies have shown that higher ICP bias power create ions with higher energy, ultimately leading to stronger ion bombardment damage [23], several GaN material damage or degradation of the devices performance [20,23–29]. The characterizations methods for dry plasma induced damage in AlGaN/GaN materials and devices are reported in Table 1.

Table 1. Characterizations methods for dry plasma induced damage in AlGaN/GaN materials or degradation of devices performances.

Characterization Technique	Material Damage or Degradation of the Device Performance	Ref.
AFM	Roughness of AlGaN surface	[30,31]
Photoluminescence	Increase of photoluminescence intensity ratio of YL/BE	[24]
Cathodoluminescence	Degradation of the AlGaN Near Band Edge signal intensity	[31]

Table 1. *Cont.*

Characterization Technique	Material Damage or Degradation of the Device Performance	Ref.
Depth Resolved Cathodoluminescence Spectroscopy (DRCLS)	V_N (@ E_C −0.9 eV) and C defects in the p-GaN layer	[32]
Electrochemical Impedance Spectroscopy	Decrease in built-in potential (V_{bi}) at the nGaN/electrolyte Interface	[25,33]
Sheet resistance measurement (R_{sheet}) with 4-probe equipment on GaN/AlN/AlGaN/GaN samples	Increase of 2DEG sheet resistance	[20,24,34–36]
Schottky diodes	Decrease of Schottky barrier height Φ_B	[25]
MOS capacitors or transistors	Increase of interface state density (Dit) Lower electron mobility Increase of leakage current Lower threshold voltage	[26–28,30,37] [27,37] [26] [23,37]

Reported electrical damage depth ranges from >10–20 nm [20,25] to 40 nm [38] or 50–60 nm [22,25]. From the AES electron spectrum of oxygen profile, surface damage was limited to the top few hundred angstroms [39].

One proposed explanation for the degradation of device performance is the introduction of donor levels, such as V_N, caused by dry-etching. These donor levels results in a n-GaN surface [32], which may contribute to the low V_{TH} since applying negative gate voltages is necessary to deplete the n-GaN surface donor layer and cut off the channel. As a matter of fact, under threshold conditions, some of these n-type defects become ionized and depleted, resulting the generation of positive ionized space charges. Therefore, the key factor for achieving normally-OFF operation in a fully dry-recessed MIS gate HEMT is the removal or recovery of the damaged layer (i.e., providing sufficient nitrogen to eliminate the V_N) [29].

Among the different approaches proposed to overcome the plasma induced damage issues are:

1. Reduction or elimination of the source of damage through use of etching methods without plasma or with low ICP bias power;
2. Recovery of the damaged layer;
3. Removal of the damaged layer.

The use of etching methods without plasma is a way to avoid damage. Photo-electrochemical (PEC) etching through photo-assisted anodic oxidation is interesting for nitride semiconductors since the high thermal and chemical stability hinders the use of typical wet chemical etching. The necessary amount of photo-induced holes is regulated by choosing the relevant wavelength λ and anodic bias [40]. The holes are generated at the anode present at the GaN/electrolyte interface, specifically where electrons are given off to the outside circuit. These holes then break down GaN into Ga^{3+} ions. The latter reacts with the electrolyte and results in the formation of Ga_2O_3 which dissolves in acid or base (H_3PO_4 and KOH [41] or H_2SO_4/H_3PO_4 mixture [42]). Finally, the etching depth is proportional to the total etching current [43].

The use of etching methods with low bias plasma is another way to reduce the damage.

In that matter, atomic layer etching (ALE) is an interesting solution to reduce the dry-etching surface damage, which mitigates device performance and electron mobility, and to accurately control the etching depth. ALE, with low etching rates, can be used directly to remove the AlGaN/GaN layers (full ALE) or after conventional ICP-RIE etching with higher etching rate. The combination of ICP-RIE with ALE was reported to reduce etching damage, evaluated by the reduction of the sheet resistance R_{sheet} in Figure 4.

However, it has also been reported that UV photon damage in ALE was larger than in RIE owing to the longer plasma irradiation time [31]. It has been found that the ALE photon-induced damage can be mitigated by a post etch anneal process at temperatures

which are compatible with the overall thermal budget of a GaN power transistor process flow [44].

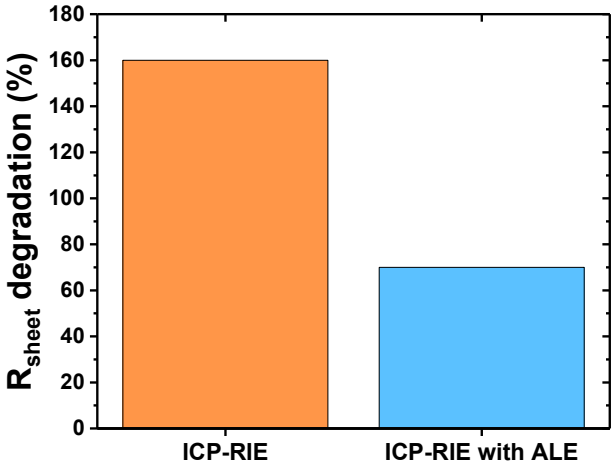


Figure 4. R_{sheet} measurements of the 2DEG after ICP-RIE etching or ICP-RIE with ALE etching [35].

In a similar approach and more recently, multistep etching with decreasing bias and post-etching anneal has been proposed to reduce the damage [18,45].

Also, a neutral beam etching (NBE) system using the neutralization of negative ions has been proposed by Lin and co-workers in order to eliminate UV photon irradiation [46].

2.1.3. GaN Atomic Layer Etching (ALE) or Digital Etching

The ALE mechanism consists of two sequential steps: surface modification (reaction A) and the removal of the modified surface (reaction B). The modification step creates a thin modified layer on surface with a specific thickness, which is easier to remove than the unmodified material. This modified layer has a distinct change in physical structure and/or in composition with a defined gradient.

The surface modification (reaction A) can occur through:

1. Chemisorption of species on the surface, which weakens the material bonds underneath (e.g., chlorination of GaN by Cl_2);
2. Deposition of a reactive layer on the surface;
3. Conversion of first layers into another material (e.g., oxidation of GaN);
4. Selective extraction of a specific species.

During the removal step (reaction B), the modified layer is removed while maintaining the integrity of the underlying substrate. This step allows the surface to be "reset" to a pristine or almost pristine state for the subsequent ALE cycle [20]. The ALE mechanism is represented in Figure 5:

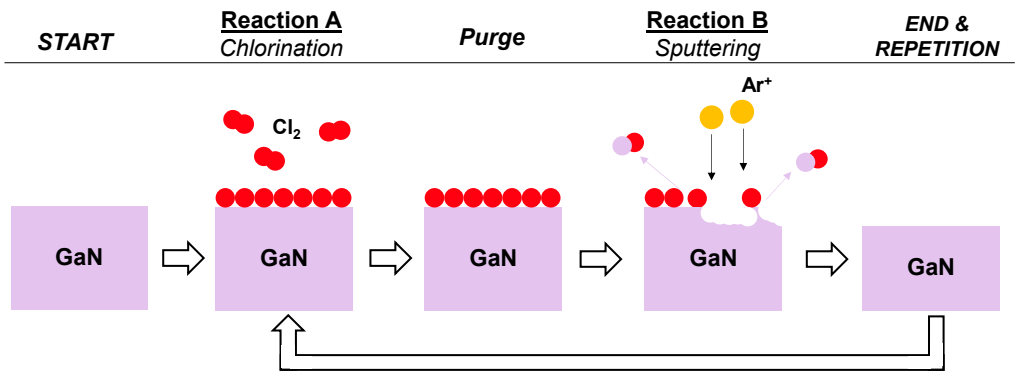


Figure 5. General concept of ALE with reaction A (chlorination of the GaN surface) and reaction B (removal of the modified surface with Ar plasma).

III-V and III-N materials are usually etched by directional ALE using a combination of chlorination and particle bombardment [20]. Chlorine mostly reacts with the surface and metallic Ga atoms to form Ga chlorides [14]. The removal of the chlorinated layer has been investigated by the bombardment of Ar or He ions [35,36]. Several teams have reported on Cl_2/Ar based ALE for GaN etching, achieving etch rates from 0.13 to 0.50 nm/cycle [35,36,44,47–50] and surfaces as smooth as the as-grown sample. The presumed etching by-products are $GaCl_3$(g) and N_2(g) [49].

Cl_2/Ar ALE parameters such as DC bias voltage during the Ar step, duration of each step, pressure during each step and gas ratio can be optimized in order to etch in the "ALE window" where there is no background etching during reaction A and only the modified layer by reaction A is removed by reaction B (no additional sputtering) [44,48,49]. A 2D fluid model is useful to determine the flux of reactive species, radicals and ions included, which arrive at the wafer surface. This flux can be calculated as a function of chlorine content, gas pressure, and RF power, showing a strong correlation between the chemical nature of the etching process and the rise in atomic chlorine flux [51]. Ar bombardment leaves Ga atoms with dangling bonds, leading for a low energy bombardment of 100 eV to a ~25Å amorphous layer enriched in Ga [52], for 400 eV to a Ga-rich surface layer [53,54], for 1 keV to Ga nanodroplets [55], for a high-energy bombardment of 2.5 keV to a metallic Ga layer [53,54]. Simultaneously, a portion of nitrogen is moved to interstitial position, forming split-interstitial defects [54]. This Ga-rich surface was associated with lower Ga 3d binding energy [55], increase in the downward band bending (nitrogen vacancies act as donors), and pinning of the surface Fermi level closer to the conduction band [56].

An alternative to chlorination for the surface modification step is the use of a bromine-based chemistry (HBr) that allows reduced Ar plasma power during the bombardment step [44].

An alternative to particle bombardment for the removal step is the thermal desorption of Ga chlorides at temperatures higher than 223 K [14].

Another ALE of III-V and III-N materials is a combination of oxidation of AlGaN/GaN by oxygen-based plasmas or by wet chemistries followed by removal of oxide by chlorine based plasma etching or wet etching, also called digital etching. This technique can also be used to remove unwanted native oxide/contamination and disordered gallium oxide/aluminum oxide residue. The oxidation step can be achieved by exposure to a low power O_2 plasma [19,57–63], to N_2O plasma [64], or to wet solutions such as H_2SO_4/H_2O_2 [65]. Increased GaN surface roughness has been reported, attributed to the locally improved oxidation around the dislocations. The pinholes, which are likely caused by dislocations, were significantly enlarged as the recess depth increases [66]. Removal of the oxide layer can be achieved using a low-power BCl_3 oxide etch step [67–69], which resembles a self-limiting process, due to the fact that BCl_3 etches the oxidized GaN layer much faster than unoxidized regions. This difference in etch rate is explained by B_xCl_y deposited layer on unoxidized GaN. After etching, this deposited layer can be easily removed by a stripping process [69]. Removal of the oxide layer can also be achieved by submerging the wafer into a wet HCl acid bath [19,20,57–59,61,64,65,70]. Thanks to the high oxidation selectivity ratio of GaN and AlGaN [71–74], TMAH and KOH are reported for selective etching of oxidized AlGaN and AlN, whereas GaN plays the role of etch stop layer [73–75]. GaN cap layer can be used as a recess mask [71].

In conclusion, etching of AlGaN/GaN is mandatory in order to obtain a recessed gate architecture. However, traditional ICP-RIE processes creates damage, which can alter the electrical performance. The following challenges arise:

1. Proper characterization of the damage, correlation with electrical damage (which depends on the target device);
2. Developments of damage-free or reduced damage etching processes, compatible with an industrial process (wafer size, throughput);
3. Process integration and choice of mask that enable the use of damage-free or reduced damage etching processes;

4. Adapted stripping that removes masks and etching residues.

Cyclic processes such as ALE show good repeatability and etch depth control with lower electrical degradation than ICP-RIE processes, reducing the damage. Other approaches include recovery or removal of the damaged layer, which can be performed by various GaN surface treatments.

2.2. Cleaning or Surface Preparation by Wet, Thermal or Plasma Treatments

The surfaces to clean are the GaN gate bottom, which is a polar (0001) Ga-face c-plane and the gate cavity AlGaN and GaN sidewalls. If the gate cavity had 90° sidewall angles, they could be non-polar m-planes and a-planes, depending on the orientation, due to the Wurtzite GaN crystal structure (hexagonal symmetry), as shown in Figure 6.

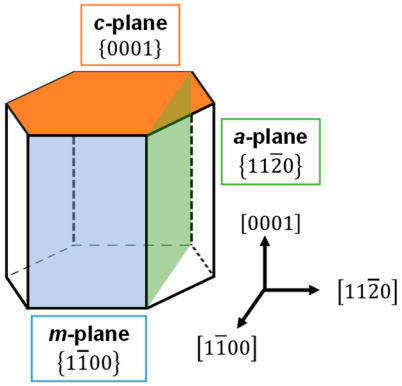


Figure 6. Different planes from the Wurtzite GaN crystal structure (hexagonal symmetry).

The contamination layer of air-exposed GaN is usually ~2–5 nm thick. About half of this contamination consists of transparent inorganic and organic species. The rest is presumed to be native oxide [76]. Wurtzite GaN surfaces are very active towards the adsorption of oxygen. The presence of dangling bonds at the GaN surface makes the surface reactive to a wide range of impurities, leading to higher impurity concentration on GaN than on Si [77].

GaN surface preparation aims at:

- Reducing the surface contamination (particulate, metallic, and chemical: native oxides, carbon and other);
- Not damaging the crystal structure nor introducing additional defect states;
- Removing the etch-induced damage;
- Smoothing the GaN surface;
- Improving the nucleation of the dielectric layer (for instance atomic layer deposited or ALD Al_2O_3).

Ex-situ cleaning includes solvents, various acid and bases, as well as UV/O_3. In situ cleaning includes room temperature or high temperature plasma, sputtering and vacuum or gas annealing [76]. A summary of all the treatments discussed in this paper can be found in Table 2.

Table 2. GaN surface treatments and their impact on contamination removal, etch-induced damage removal. The abbreviation "Y" and "N" are for "Yes" and "No", respectively.

Surface Treatment	Anisotropic Etching (Y/N)	Oxide Removal (Y/N)	Carbon Removal (Y/N)	Dry Etching Damage Removal (Y/N)	Impact on Roughness and Incorporation of Impurities	Impact on Device
TMAH	Y [78–80]			Y (sidewall [81]) N (planar [26])	Removal of F [82] Removal of plasma damage [83]	Positive V_{TH} shift [84] Improved mobility [83]
KOH	Y [85,86]					
NaOH				Y [37]		Positive V_{TH} shift [37]
NH_4OH		Y [21,87–91]	Y [90] N [87,88,92]	Y (100 °C [23])		Positive V_{TH} shift [23,91]
HCl		Y [21,89,93–95]	N [89,96,97]	Y (70 °C [98])	Incorporation of Cl [21,94,99] Detrimental impact on ALD nucleation [100]	Large hysteresis [100]
HF		Y [97,101]	Y [102] N [96,97]		Incorporation of F [97]	
H_2O_2:H_2SO_4		Y [97] N [96]	Y [96,97,102]		Smoothing [97,102]	Reduction of hysteresis [100,102]
H_3PO_4	Y [21,103]	Y [21]	Y [21]	Y [21]	Incorporation of P [21,103]	
$(NH_4)_2S$		Y [21]	N [97,102]		Incorporation of S [104]	Reduction of hysteresis [105]
UV/O_3		N [106]	Y [107]			
O_2 plasma			Y [99]		Removal of Cl [99]	
N_2 annealing				Y [38,45]	Removal of Cl [99]	
NH_3 annealing		Y [108,109]				
H_2S annealing					Incorporation of S [110]	Negative V_{TH} shift [110]
Ar plasma						Reduction of hysteresis [111,112]
NH_3 plasma		Y [87]	Y [87]			Reduction of hysteresis [113]
N_2 plasma			Y [88,114,115]	Y [23,24]	Incorporation of N [88,115]	
H_2 plasma		Y [116]	Y [116]		Formation of Ga droplets [116]	

Various wet cleaning sequences have been reported in the literature. After oxygen removing wet treatments, such as HF, the presence of a Ga–O bonds indicates the presence of a native oxide. It suggests a reoxidation (estimated to 0.5 Å) forming a GaO_x layer during surface exposure to ambient air prior to XPS measurement or during wet treatments (HF and/or DI water rinse) [101]. This further confirms the strong oxygen affinity of a clean GaN surface. The presence of a GaO_x layer is problematic, with increased hysteresis and

interface states [117–119]. In situ $NH_3/Ar/N_2$ plasma sequence has been reported for the removal of the surface native oxide [120] and formation of a nitridated inter-layer (NIL) prior to the gate dielectric deposition as seen in Figure 7. This treatment is sometimes labeled as remote plasma pretreatment (RPP). The NH_3-Ar plasma is used as a cleaning step to remove the native oxide. The subsequent N_2 plasma allows to nitride the surface (Ga dangling bonds passivated and possible V_N compensated), resulting in a NIL on the III-N surface [117,121,122]. Other plasma sequences such as H_2/NH_3 cycles [123], a sequence of NH_3 and N_2 [124] or N_2/H_2 [125] have been reported before ALD of AlN, SiN_x, or epitaxy, leading to a decrease in hysteresis, a reduction of the ON resistance, and also a decrease in V_{TH} [124].

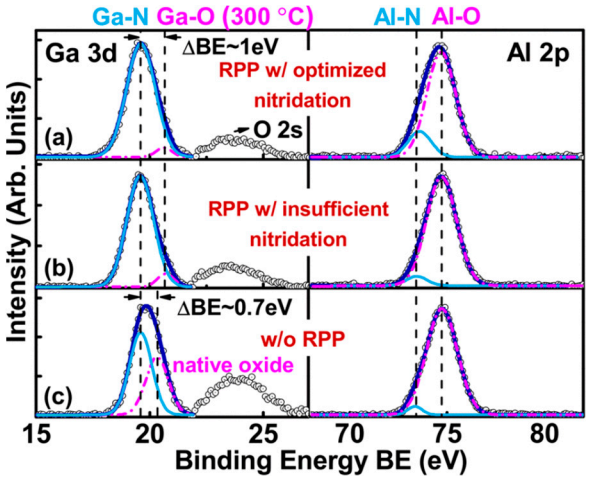


Figure 7. XPS measurements of Ga3d and Al2p spectra from Al2O3/GaN interfaces (**a**) with optimized RPP, (**b**) with RPP having insufficient nitridation, and (**c**) without RPP (© 2023 IEEE. Reprinted, with permission, from [116]).

Thus, it seems that a combination or a sequence of different treatments is the most suitable in order to achieve all the goals of the surface preparation [126]. Also, for a same surface preparation process, the surface states depend on previous processing, such as dry etching conditions, and therefore, the surface preparation should be adapted to the specificities of the material and overall process flow. For instance it was found that the Ga oxidation states at Al_2O_3/GaN interface were higher for etched samples than for non-etched samples [91] or that increased trapping occurred for etched GaN [127]. The higher oxidation state when reduced with the appropriate wet cleaning sequences was proven to increase V_{TH} (Figure 8)

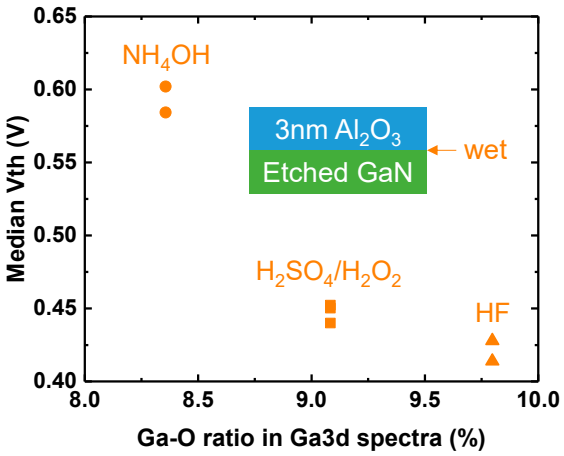


Figure 8. Trend of V_{TH} with gallium oxidation after different wet treatment on etched GaN (from [91]).

In addition, as stated in the Introduction, there is still a limited understanding of the impact of the gate cavity morphology, since most of the studies reported here focus on planar structures formed on the c-plane (corresponding to the bottom of the gate). We have seen that anisotropic GaN etchants such as tetramethylammonium hydroxide (TMAH), potassium hydroxide (KOH), or H_3PO_4 impact trench sidewall morphology [78,85,86,128]. For instance TMAH etches any plane of GaN, except for the (0001) c-plane, while it etches m-plane at a considerably lower rate than other semi-polar planes allowing, for instance, it to achieve rough a-plane oriented sidewall (composed of microscopic m-faces) and smooth m-plane oriented ones [78,79]. In the few studies carried out on different non-polar planes, it is clear that GaN crystallographic orientation impacts the effect of surface treatments on electrical characteristics [79,112,129–131] or that sidewall formation has a significant impact on device performance (in comparison with a planar etched structure) [127]. As a consequence, is it crucial to improve the understanding of how the GaN crystal orientation and 3D gate cavity with sidewalls formation impacts recessed gate devices' performance.

Finally, selective area regrowth faces some similar challenges with the deposition of a dielectric in a recessed GaN cavity (such as in MOSc-HEMTs): negative impact of the dry etching [98], exposure to air, difference between trench bottom and sidewalls, and incorporation and activation of the Mg dopant. Therefore, similar characterization techniques can be applied to study these impacts [132]. But regrown GaN is still promising to recover dry etching plasma-induced damage [133,134], and it can be combined with in situ dielectric deposition which allows an increase in electron mobility (OG-FET device reported in [135]).

3. Interface and Dielectric Materials

3.1. Interface

Since the growth of a thick native gallium oxide, similar to SiO_2 from Si, is difficult [136], the deposition of a dielectric layer has been necessary to form a MIS gate. However, due to the defective interfacial GaO_x and the lattice mismatch at the dielectric/GaN interface, this interface needs to be controlled to have the desired device properties.

In the case of GaO_x, reducing the low-quality interfacial oxide was presented in the previous section with wet cleaning and plasma treatments, notably with the NIL plasma treatment. This technique is important since, as stated before, GaO_x is not reduced with HF [101] nor after dielectric deposition such as Al_2O_3 [137]. Another solution is to create a high-quality interfacial gallium oxide. Oxidation by exposing the surface to ozone was found beneficial for AlGaN/GaN devices with reduced hysteresis [138]. More specifically, oxidation by O_2 plasma combined with a high temperature anneal under N_2 and prior SiN_x deposition by low-pressure chemical vapor deposition (LPCVD) was studied [139–141]. The result is a GaON layer formed at the interface between SIN_x and the recessed GaN surface. With the GaON layer, a V_{TH} of 1.15 V and a reduced hysteresis of 0.2 V is reported [139]. Reduced hole injection under negative stress is also observed, the high valence band offset between GaON and GaN explaining this improvement [140,141]. GaON can also be formed with a N_2O plasma [142–144], reducing the damage from the LPCVD SiN_x deposition process [143] and increasing electron mobility [144]. With a non-recessed gate structure, an AlGaON layer formed by controlled oxidation with N_2O plasma through a thin Al_2O_3 layer was reported in [145,146]. An increased V_{TH} was observed with a small hysteresis correlated to the oxidation step [145].

A thin interfacial AlN can be directly deposited before the dielectric to improve the interface quality due to its lower lattice mismatch with GaN with respect to Al_2O_3 [147]. Moreover, AlN is known to form a passive oxide layer, when exposed to air. For this reason, AlN deposition is typically followed by in situ dielectric deposition without air exposure. When applied on both GaN's c-plane (polar surface) and m-plane (non-polar surface) before ALD Al_2O_3, AlN reduces the V_{FB} hysteresis and the interface states, especially at the non-polar surface [130]. Specifically for MOSc-HEMT, a reduction of V_{TH} hysteresis from 800 mV to 65 mV is obtained with a 2 nm PEALD AlN interfacial layer at the Al_2O_3/GaN

interface, as well as a lower density of interface states [148]. By combining the NIL process and the AlN deposition, the improvement in terms of hysteresis is similar but a lower density of interface states is observed and a greater separation between defects on Al_2O_3 and GaN is obtained [119,149]. With an AlSiO dielectric, AlN improves the electron mobility by confining the electrons at the interface [150] and allows reduced Ga diffusion into the dielectric after high temperature post-deposition annealing (PDA) at 950 °C [151].

In conclusion, two ways of treating the interfacial GaO_X are possible; either reducing it or improving/growing the interfacial oxide with fewer defects. Specific AlN interfacial layer deposition before thicker dielectric deposition leads to increased mobility, lower hysteresis, and lower density of states. Since the direct deposition of oxides on GaN maintains the interfacial GaO_x, combining its removal with an AlN layer represents a promising solution to keep a low oxidation state at the interface, improve electron mobility, and reduce V_{TH} hysteresis.

3.2. Dielectric

Another essential aspect of the MIS gate is its dielectric. The considered properties are [152]:

- Larger band gap than GaN in another to have a conduction offset higher than 1 eV;
- Layer without grain boundaries;
- High relative permittivity and high breakdown voltage.

A summary of dielectrics, their band lineup with GaN, and their dielectric constant are represented in Figure 9. As the high-κ dielectric band gap tends to decrease with the dielectric constant, there is a limitation in the choice of candidates. Frequently used dielectrics are SiO_2, SiN_x, and Al_2O_3. Annealing after deposition or after metallization is equally important to improve the dielectric/GaN stack.

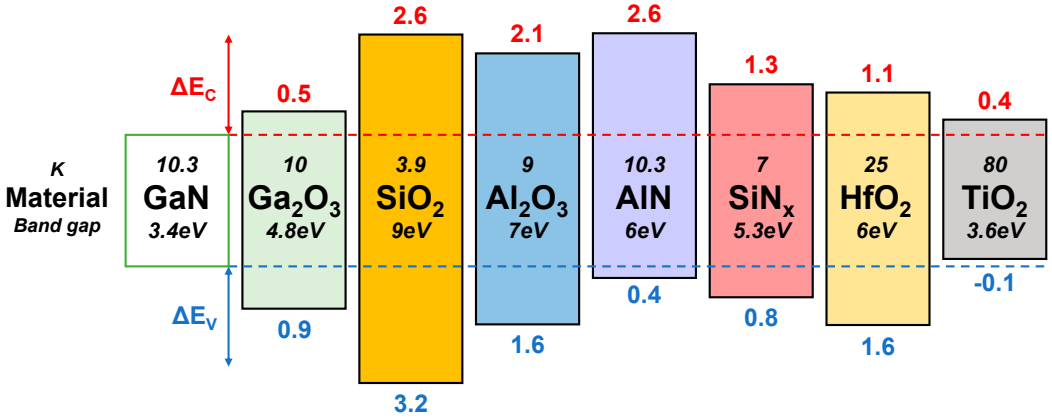


Figure 9. Band lineups of different dielectrics with GaN alongside their respective dielectric constant (Refs. [153–156]).

SiO_2 has a high gap (~9 eV) but a low relative permittivity (~3.9) [157,158]. Its large gap strongly reduces leakage current, and its thermal stability allows the use of high thermal budgets (>800 °C). However, Ga diffusion into SiO_2 can lead to increased leakage current as well as reduced breakdown voltage [132]. A negative shift of V_{FB} at high PDA temperature (800 °C) was also reported and attributed to the formation of V_O after hydrogen reduction with interfacial GaO_x [133].

SiN_x has a lower gap (~5.5 eV) and a higher relative permittivity (~7.5) [157,158]. The V_N passivation with SiN_x leads to a lower reported density of interface states [134,135]. However, because of its small gap, gate leakage may be, in certain cases, too high [136].

Al_2O_3 has a high gap (~7 eV) and relative permittivity (8~10) [157,158]. Regarding the interface, D_{it} values ranging from 10^{11} to 10^{13} $cm^{-2}{\cdot}eV^{-1}$ are found in the literature depending on the deposition and treatment before or after Al_2O_3 formation [159–161]. However,

amorphous Al_2O_3 has a lower thermal stability than SiN_x and SiO_2. Crystallization typically occurs at about 800 °C [160] on as-grown GaN and a beginning of crystallization can be observed at 600 °C on etched GaN [162]. When PDA is applied, usually between 400 °C and 800 °C, a general increase of V_{TH}/V_{FB} is reported [163–166], V_{TH} hysteresis is reduced [167] and electron mobility is increased [137,163,166]. These improvements can be related to the reduction of positive charges in both GaO_x [152,166] and Al_2O_3 [165], or to the reduction of interface states [164,167,168].

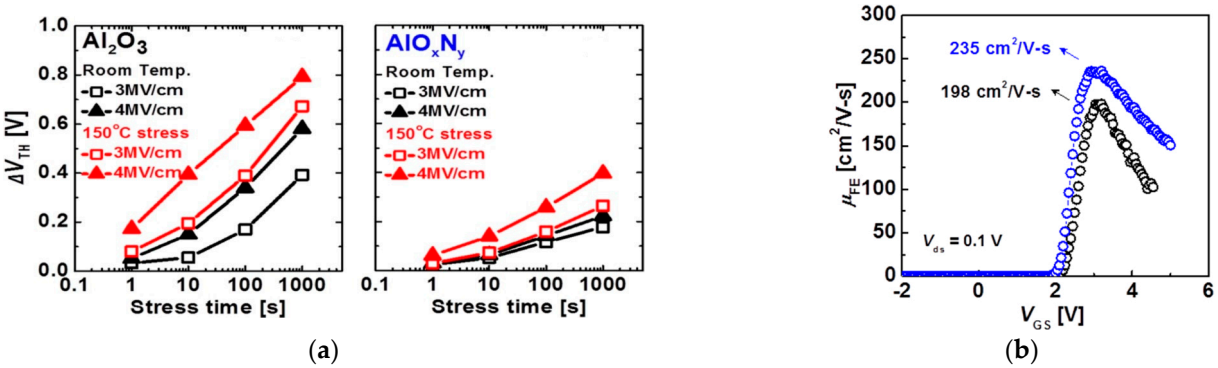
With the respective limitation of commonly used dielectrics, one approach is to develop ternary alloys to benefit from their specific properties.

3.2.1. Al_2O_3 and AlN Alloys for Improved Thermal Stability and Lower Electron Trapping: AlON

AlON is an example of such an alloy, consisting of a mixture between Al_2O_3 and AlN, and having many advantages compared to Al_2O_3 and AlN. It can be deposited by different techniques:

- Sputtering of an Al source with a flow of O_2 and N_2 [169];
- Nitriding ALD Al_2O_3 with N_2 plasma [170,171];
- ALD with trimethylaluminium (TMA) and N_2/O_2 precursors [172];
- ALD nanolaminates of Al_2O_3 and AlN [173,174];
- Oxidation of ALD AlN with O_3 [175,176].

In terms of advantages, the introduction of nitrogen into the Al_2O_3 matrix reduces current leakage by both passivating V_O defects [177] and increasing the electron barrier height between AlON and GaN [171], although AlON's band gap was reported to be smaller than Al_2O_3 [169,175]. The passivation of these defects could explain the reduction in hysteresis and electron injection reported for AlON in the literature [169,171,173,175,177,178]. Nozaki and co-workers indeed reported a reduction in electron injection with increasing nitrogen concentration, whereas Kang and co-workers reported a reduced V_{TH} instability under positive bias stress (Figure 10a). Furthermore, the presence of nitrogen induces the presence of negative fixed charges allowing V_{FB} to increase [170,173]. With a fully recessed MIS gate HEMT, a similar V_{TH} of ~2.25 V is found for AlON and Al_2O_3 [171]. According to an ab initio study by Choi and co-workers, the introduction of nitrogen into crystalline Al_2O_3 induces negative fixed charges for n-type doped GaN [179]. However, according to Guo and co-workers, these nitrogen defects are absent in the amorphous Al_2O_3 gap. Thus the negative charges introduced by these defects are also absent [180].



(**a**) (**b**)

Figure 10. For both Al_2O_3 and AlON deposited in a MOSc-HEMT: (**a**) V_{TH} shift with positive bias stress at room temperature and at 150 °C (**b**) field effect mobility extracted for a V_{DS} at 0.1 V [171] (© IOP Publishing. Reproduced with permission. All rights reserved).

Regarding the interface, AlON reduces interface states mostly for defect energy level from the conduction band or $E_C–E_T$ higher than 0.35 eV, possibly through the reduction of GaO_x at the interface [169,171,173,178]. With a better interface than Al_2O_3/GaN, field

effect mobility (μ_{FE}) for MOSc-HEMT with AlON increases by ~19% up to 235 $cm^2 \cdot V^{-1} \cdot s^{-1}$ (Figure 10b) [171].

However, while AlON has better immunity to electron injection, Hosoi and co-workers [181] reported a hole injection which could be problematic in the case of negative stress. These hole traps would be explained by the existence of defects in the N2p orbital near the AlON's valence band [182].

With the incorporation of nitrogen, AlON also benefits from a higher thermal stability up to 800 °C in PDA [169]. As such, the high temperature PDA or post-metallization annealing (PMA) allows increased V_{FB} and reducing its hysteresis [170,178]. However, few studies reported the impact of different PDA temperatures.

3.2.2. Al_2O_3 and SiO_2 Alloys for Improved Thermal Stability and Lower Electron Trapping: AlSiO

As well as AlON, AlSiO is a ternary alloy of Al_2O_3 and SiO_2, combining the higher relative permittivity of Al_2O_3 (~9) with the higher band gap of SiO_2 (~9 eV). It can be deposited by different techniques:

- Sputtering a silicon doped aluminum target [183,184];
- MOCVD [185–187];
- ALD nanolaminates of Al_2O_3 and SiO_2 [151,188–191].

By increasing the silicon concentration, the conduction band offset between AlSiO and GaN increases, reducing the leakage current [188,189]. The incorporation of silicon reduces the hysteresis [184–187] with Sayed and co-workers reporting a reduction in hysteresis for MOCVD AlSiO with increasing silicon percentage up to 46% [187]. However, they also describe a negative hysteresis for a percentage equal to 76%, possibly originating from mobile charges. Concerning V_{FB}, the impact of silicon content differs in the literature. Komatsu and co-workers reported an increase in V_{FB} for a silicon content of 29% [184], Gutpa and co-workers reported a reduction in V_{FB} [186], and Kikuta and co-workers reported a small correlation between V_{FB} and silicon content [188]. These differences could be due to the introduction of either positive or negative charges, or the different deposition methods used. More recently, Smith and co-workers reported an increase of V_{TH} with increasing Si content, this effect magnified with AlN interfacial layer [150]. Furthermore, by ab initio simulation, Chokawa and co-workers described a lower formation energy of V_O defects when the silicon concentration increases [192]. Unlike V_O defects that would be electrically active (V_O^{2+}) in Al_2O_3 [193], these vacancies surrounded by silicon are electrically inactive. However, the transition energy (2+/0) for V_O defects is approximately at 2.8~3.5 eV from the alumina's valence band (1.9~2.6 eV from GaN's valence band if the valence band off-set is considered to be 0.9 eV) [193,194]. In the case of n-doped and UID GaN, V_O defects would already have a neutral charge state. For p-doped GaN, this defect can be a source of hole leakage [194].

Finally, regarding the interface between AlSiO and GaN (0001) (or Ga-Face), the absence of dangling bonds is observed by ab initio simulation and explained by oxygen migration from the dielectric to the interface [195]. Thus, a low D_{it} is observed when compared to Al_2O_3/GaN (0001) interface [185,186]. In the case of p-MOSFET, the extracted μ_{FE} was found to be around 27.7–36.2 $cm^2 \cdot V^{-1} \cdot s^{-1}$ [191]. Similar to AlON, the incorporation of Si increases the thermal stability with respect to Al_2O_3 [185,190].

A study of PDA on AlSiO with Si content of 22% was carried out by Kikuta and co-workers by annealing from 650 °C to 1050 °C under N_2 for 10 min [190]. A reduction in hysteresis and in V_{FB} drift under positive stress for a PDA higher than 650 °C was observed (Figure 11). For a PDA above 850 °C, a plateau on the I–V characteristic related to electron trapping is reduced. Contrary to Al_2O_3, AlSiO presents no sign of crystallization for a PDA at 850 °C. However, the same group observed the onset of crystallization for AlSiO at the interface for a PDA at 950 °C. The proposed solution to reduce this crystallization was the deposition of a thin SiO_2 layer at the AlSiO/GaN interface. Moreover, the SiO_2 interfacial

layer improves μ_{FE} by 50% (i.e., 27.7–36.2 $cm^2 \cdot V^{-1} \cdot s^{-1}$), and it is explained by the possible reduction of border traps [191].

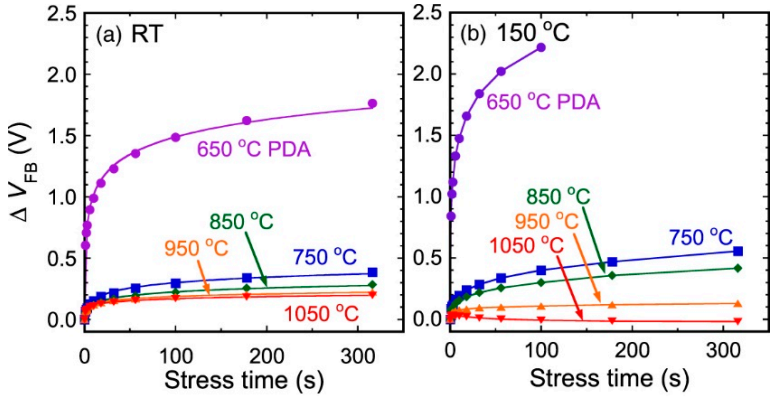


Figure 11. V_{FB} shift under positive bias stress at both (**a**) room temperature and (**b**) 150 °C for AlSiO (21%Si)/n-GaN MOSCAPs under different PDA temperatures (different symbols and colors per PDA temperature) [190] (© The Japan Society of Applied Physics. Reproduced by permission of IOP Publishing Ltd. All rights reserved).

3.2.3. HfO_2 and SiO_2 Alloys for Improved Mobility: $HfSiO_x$

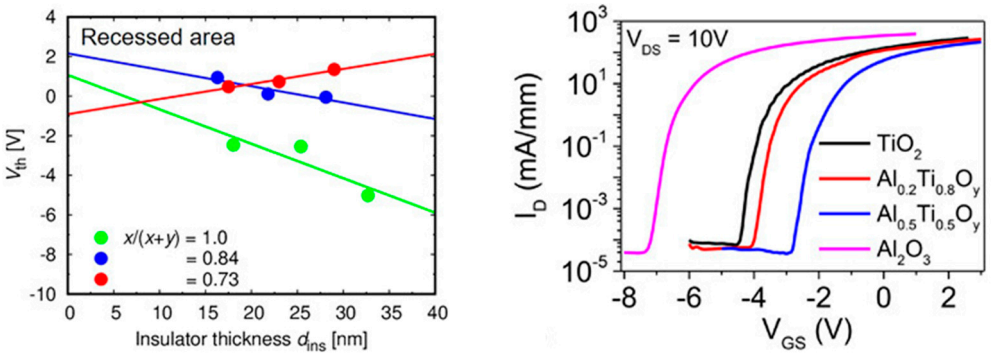
Another interesting approach is the use of $HfSiO_x$ by mixing HfO_2 and SiO_2 by ALD [69,196–199]. As AlSiO, $HfSiO_x$ is deposited by alternating ALD HfO_2 and ALD SiO_2. Hf and Si composition is controlled by adjusting the ratio of HfO_2 and SiO_2 ALD cycles [198,199]. HfO_2 has a higher relative permittivity but suffers from low thermal stability. In the same way with AlSiO, the introduction of Si increases the thermal stability. In that matter, non-crystallized film after a PDA at 900 °C for 5 min is reported with a silicon content of 43% [199]. Reported values of relative permittivity are on the order of 13~18 with a high band gap around 6.5 eV, close to reported ALD Al_2O_3 band gap of 6.8 eV [196,199,200]. Compared to HfO_2, $HfSiO_x$ leads to lower hysteresis possibly associated to fewer electron traps, but a lower V_{FB}/V_{TH} induced by possible positive charges is also reported [197,198]. For an ALE fully recessed MIS gate HEMT, a positive V_{TH} of 2.1 V was reported [196].

In terms of interface quality with GaN or AlGaN, $HfSiO_x$ has lower D_{it} than HfO_2 and Al_2O_3 (around 5×10^{11} $cm^{-2} \cdot eV^{-1}$ at E_C–$E_T \approx 0.3$ eV), possibly because of the high temperature PDA applied (i.e., 800 °C). This highlights the higher interface quality of GaN with $HfSiO_x$ than with HfO_2 and Al_2O_3 [196,198,199]. Combined with the high relative permittivity, transconductance is increased compared to Al_2O_3 in AlGaN/GaN HEMTs [199]. With an ALE fully recessed MIS gate HEMT, a μ_{FE} of around 406 $cm^2 \cdot V^{-1} \cdot s^{-1}$ is obtained [196].

3.2.4. Al_2O_3 and TiO_2 alloy for V_{TH} Engineering: AlTiO

Finally, the use of AlTiO, a ternary alloy of Al_2O_3 and TiO_2 obtained through the deposition of ALD Al_2O_3 and TiO_2 nanolaminates offers an interesting solution to increase V_{TH} [201,202]. Combining Al_2O_3 with TiO_2 lead to finding a trade-off between TiO_2 high relative permittivity but small band gap (60 and 3.5 eV, respectively) with Al_2O_3 lower relative permittivity and higher band gap (~9 and ~7 eV, respectively) [157,158]. The obtained band gap and relative permittivity are in the order of 5–6 eV and ~22, respectively [201,202]. However, the major gain with AlTiO consists in the increase of V_{FB}/V_{TH}. Indeed, on the one hand, Nguyen and Suzuki reported that with a decreasing Al content from 100% to 35%, a reduction of positives charges at the AlTiO/AlGaN interface is observed and explained by the reduction of O-Ga and O-Al at the surface by Ti [202]. Combined with partially recessed AlGaN barrier, further reduction of interfacial charges is obtained as shown in Figure 12a, leading to a V_{TH} of 1.7 V with an Al content of 73% and

a remaining AlGaN barrier of 4 nm [203]. Nonetheless, gate voltage of −6 V is reported to induce a V_{TH} negative shift of −0.5 V [203]. On the other hand, Gupta and co-workers reported a normally-OFF HEMT with a partially recessed AlGaN barrier (8 nm) and an AlTiO layer after PDA [201]. With increasing Al content from 10% to 52%, an increase in V_{TH} is observed, allowing a V_{TH} of 0.5 V. Compared to Al_2O_3 and TiO_2 on HEMTs, higher V_{TH} is obtained with a Ti content of 50% as represented in Figure 12b. The increase of V_{TH} with Al content is explained and confirmed by the formation of p-type doping with deep acceptors states close to AlTiO's valence band [204]. These states are formed by Al replacing Ti in TiO_2. Hence with higher Al content up to 52%, more p-doping is obtained. Concerning hysteresis, a low hysteresis of 40 mV for V_{DS} of 15 V was reported. Finally, by combining both results, it seems that an intermediate Al content is the optimal content to have the highest V_{TH}.



(**a**) (**b**)

Figure 12. (**a**) V_{TH} in function of Al_xTi_yO thickness in partially recessed MIS Gate for different Al content. Increasing Ti content up to 27% combined with partial AlGaN recess reduce positive charges at the interface (Reprinted from [203], with the permission of AIP Publishing); (**b**) I_D–V_{Gs} transfer characteristic for Al_2O_3, TiO_2, $Al_{0.2}Ti_{0.8}O_y$, and $Al_{0.5}Ti_{0.5}O_y$ on HEMTs. Decreasing Ti content up to 52% increase V_{TH} in comparison to Al_2O_3, TiO_2, and $Al_{0.2}Ti_{0.8}O_y$ (Reprinted from [204], with the permission of AIP Publishing).

3.2.5. Summary

In conclusion, many dielectric candidates exist for MOSc-HEMT, from standard Al_2O_3 to alternative solution such as ternary alloys. Their implementation is beneficial for both electrical (i.e., hysteresis and V_{TH}) and material properties (i.e., crystallization temperature). For high thermal stability, AlON, AlSiO, and $HfSiO_x$ are interesting, allowing higher thermal budget in the fabrication process. Better interface and less defects are also commonly reported for those dielectrics. Finally, AlTiO offers an interesting approach to increase the threshold voltage. Since AlTiO in a fully recessed gate is not yet reported, it would be reasonable to verify the possible V_{TH} obtained from this gate stack. A summary of the MOSCAPs discussed in this section is represented in Table 3.

Table 3. Summary of mentioned MOSCAPs.

Dielectric	Substrate Wet Cleaning	Deposition Technique	Annealing	V_{FB} (V)	ΔV_{FB} (mV)	D_{it} ($cm^{-2}\cdot eV^{-1}$)	Ref.
6 nm Al_2O_3 5 nm AlON (6.2% N)	n-GaN (Si:5 × 10^{18} cm^{-3}) NH_4OH	ALD PEALD	PMA 400 °C N_2/H_2 15 min	~1.1 ~1.4	0 40	10^{12} ($E_C - E_T$ = 0.5 eV) 10^{13} ($E_C - E_T$ = 0.5 eV)	[170]
11.5 nm AlON	AlGaN/GaN Acetone cleaning	PEALD nanolaminates	PDA 600 °C N_2 30 s PMA 400 °C N_2/H_2 3 min	+1.5 compared to Al_2O_3	/	10^{13}–10^{11} ($E_C - E_T$ = 0.42–0.54 eV)	[173]
10.5 nm AlON (~8% N)	AlGaN/GaN 5 min of 5% HCl	ALD	PDA 800 °C N_2 3 min PMA 600 °C N_2 3 min	/	/	/	[175]

Table 3. *Cont.*

Dielectric	Substrate Wet Cleaning	Deposition Technique	Annealing	V_{FB} (V)	ΔV_{FB} (mV)	D_{it} ($cm^{-2} \cdot eV^{-1}$)	Ref.
25 nm Al_2O_3	n-GaN (2×10^{17} cm^{-3})	MOCVD	/	−1.2	10(after 10 min at +4 V)	4.9×10^{12} ($E_C - E_T$ = 0.15 to 2 eV)	[185]
25 nm AlSiO (~44% Si)				−2.4	3 (after 10 min at +4 V)	6.4×10^{11} ($E_C - E_T$ = 0.15 to 2 eV)	
25 nm Al_2O_3	n-GaN (2×10^{17} cm^{-3})	MOCVD	/	0.28	/	5.3×10^{12} ($E_C - E_T$ = 0.15 eV)	[186]
25 nm AlSiO (28% Si)				−4.3	/	1.9×10^{12} ($E_C - E_T$ = 0.15 eV)	
24 nm AlSiO (~46% Si)	N-face n-GaN (2.5×10^{17} cm^{-3})	MOCVD	/	/	45	/	[187]
20 nm Al_2O_3	n-GaN (Si:1 $\times 10^{17}$ cm^{-3}) 1% HF	PEALD	PDA 650 °C N_2 1 hr PMA 400 °C N_2 5 min	−0.5	/	5.8×10^{11} ($E_C - E_T$ = 0.7 eV)	[188]
20 nm AlSiO (21% Si)		PEALD nanolaminates		−0.3	/	7.8×10^{11} ($E_C - E_T$ = 0.7 eV)	
40 nm AlSiO (22% Si)	n-GaN (Si:1 $\times 10^{17}$ cm^{-3}) 1% HF	PEALD nanolaminates	PDA 950 °C N_2 10 min	Negative shift compared to ideal curve	/	/	[190]
20 nm HfO_2	Etched GaN HCl	ALD	/	/	200	2.5×10^{13} ($E_C - E_T$ = 0.37 eV)	[197]
20 nm $HfSiO_X$	Etched GaN HCl	ALD nanolaminates		/	150	1.6×10^{12} (E_C -E_T = 0.37 eV)	
25.7 nm HfO_2	n-GaN (1.3×10^{18} cm^{-3}) Piranha + buffered HF	PEALD	PDA 800 °C N_2 5 min	2.05	600	6×10^{13}–4×10^{11} ($E_C - E_T$ = 0.12–0.58 eV)	[198]
23 nm $HfSiO_x$ (43% Si)		PEALD nanolaminates		0.63	70	8×10^{11}–2×10^{11} (E_C -E_T = 0.15–0.6 eV)	

4. Conclusions

The fully recessed MIS gate GaN HEMT (or MOSc-HEMT) is a promising solution for normally-OFF GaN-based power devices thanks to its positive threshold voltage, reduced leakage current, and higher allowed gate-voltage swing. Its development can be challenging due to the impact of different process steps of the transistor. The main effect is the low and unstable V_{TH}, and the reduced mobility at the gate channel. In addition, the necessary etching of the AlGaN barrier introduces a GaN surface far from pristine.

The main challenges are a proper characterization of the induced damage and a process integration compatible with industrial requirements. Among the current developments, ALE represents a useful tool to mitigate the damage caused by ICP-RIE. Its controlled etching process associated to the removal of the damaged layer can reduce the roughness and increase the electron mobility. In similar fashion, recent work on selective area growth shows promising results but shares the same issues related to the dry etching step.

In addition to the etched surface, the GaN surface has a tendency to both contain more impurities than semiconductors such as silicon and has difficulty removing native gallium oxide (i.e., GaO_x). This surface condition presents a challenge, specifically during air-break transitions. A recovery towards a more pristine GaN surface is possible through optimized etching (low impact etching and ALE) combined with specific surface treatments, from wet cleanings (e.g., HF or NH_4OH) to plasma treatment (e.g., remote plasma pretreatment).

Interface layer, such as AlN, seems mandatory to increase the electron mobility as well as to protect the recessed surface from oxidation during dielectric deposition. The choice of the dielectric is also important, both to optimize the dielectric/GaN interface and be suitable with the integration process of the fully recessed MIS gate transistors. Al_2O_3 is frequently used thanks to its high band gap and high relative permittivity. However, instable V_{TH}, low electron mobility and low thermal stability can limit its integration. Ternary alloys such as AlON, AlSiO, and $HfSiO_x$ could improve the above mentioned electrical properties as well as the thermal stability. As such, for AlON and AlSiO associated with high temperature annealing, immunity to electron trapping increases, hence, opening a path to lower V_{TH} instability. Moreover, the possible introduction of negative charges in AlON could increase V_{TH}. Another alternative is $HfSiO_x$ which allows an increase in the electron mobility thanks to both its good interface quality with GaN and its high relative permittivity. Combining

$HfSiO_x$ with AlN interfacial layer could possibly further increase the electron mobility. Specifically for V_{TH} engineering, the implementation of an AlTiO gate dielectric with an intermediary Ti content in fully recessed MIS Gate should further increase the V_{TH} thanks to its apparent p-type behavior. However, from the reviewed literature on MOSc-HEMT, the process having the highest V_{TH} is still in [166] with ICP-RIE and digital etching using Al_2O_3 with a PDA at 400 °C.

To summarize, the combination of different process steps from etching to dielectric deposition need to be well controlled in order to fit the desired final device properties. Such developments are also important in the case of vertical GaN MOS trench-gate transistors. A summary of the mentioned MOSc-HEMTs is reported in Table 4. Finally, a better understanding of gate–trench sidewall quality is needed in order to fully quantify their impact on device properties.

Table 4. Summary of mentioned fully recessed MIS gate HEMTs.

Substrate	Etching	Surface Preparation	Interfacial Layer	Dielectric	Annealing After Deposition	V_{TH} (V)	ΔV_{TH} (mV)	Mobility μ_{FE} ($cm^2 \cdot V^{-1} \cdot s^{-1}$)	D_{it} ($cm^{-2} \cdot eV^{-1}$)	Ref.
Si/GaN/AlN/AlGaN	ICP-RIE: Cl based	NH_4OH 0.6% 75 °C	/	Al_2O_3	/	0.6 [a]	/	/	/	[91]
Sapphire/GaN/ $Al_{0.26}Ga_{0.74}N$	ICP-RIE	TMAH 5% 90 °C 1 hr	/	Al_2O_3	Ohmic contact: 30 s 800 °C N_2	3.5 [b]	/	/	/	[83]
Si/Al(Ga)N/GaN/ AlN/$Al_{0.2}Ga_{0.8}N$/GaN/ AlN/$Al_{0.26}Ga_{0.74}$/GaN	ALE: Oxidation + KOH	/	/	Al_2O_3	PDA: 10 min 400 °C O_2	0.4 [a]	200	396	/	[74]
Si/AlN/AlGaN/GaN/ $Al_{0.2}Ga_{0.8}N$	Selective Area Growth	UV treatment + acid solution	/	Al_2O_3	PDA under N_2	~0.5 [c]	~0	/	/	[133]
Si/GaN/AlN/AlGaN	Selective Area Growth	$HF/H_2SO_4/HCl$	/	Al_2O_3	Ohmic contact: 30 s 850 °C N_2	2.6 [b]	/	80	Lowest = 9×10^{12} Highest = 1×10^{13}	[134]
Sapphire/GaN/AlN/ $Al_{0.25}Ga_{0.75}N$/GaN	ICP-RIE: BCl_3/Cl_2	NH_3:H_2O + Oxidation through thin Al_2O_3 + HCl wet etch	/	Al_2O_3	PMA: 5 min 450 °C O_2	2.8 [a]	300	48	/	[63]
Si/GaN/AlN/ $Al_{0.25}Ga_{0.75}N$/GaN	ICP-RIE + digital etching	/	ICP/RF 5/10W + O_2 plasma + NH_3 annealing: GaON	SiN_x	Ohmic contact: 30 s 850 °C N_2	1.15 [a]	200	150	Lowest = 3×10^{12} Highest = 1×10^{13}	[139]
Sapphire/GaN/ $Al_{0.23}Ga_{0.77}N$/GaN	Wet etching	/	PECVD RF 200W N_2O: GaON	SiN_x	Ohmic contact: 30 s 870 °C N_2	1.2 [a]	/	/	Lowest = ~3×10^{12} Highest = 1×10^{13}	[143]
SiC/GaN/AlN/ $Al_{0.25}Ga_{0.75}N$	ICP-RIE: BCl_3/Cl_2	/	PECVD 300W: N_2O	Al_2O_3	Ohmic contact: 30 s 840 °C	1.5 [b]	/	658	Lowest = 1.5×10^{11} Highest = 8×10^{12}	[144]
Si/GaN/AlN/ $Al_{0.25}Ga_{0.75}N$	Digital etching: O_2 plasma + HCl	RPP	AlN	Al_2O_3	PDA: 500 °C O_2	0.3 [a]	900	165	10^{11} ~ 10^{12}	[149]
Si/GaN/ALN/AlGaN	ICP-RIE: BCl_3/Cl_2 Digital etching: O_2 plasma + HCl	/	/	Al_2O_3	PDA: 10 min 400 °C N_2	5.2 [a]	400	70	/	[166]
Si/GaN/AlN/AlGaN	ICP-RIE: BCl_3/Cl_2	/	/	AlON	PDA: 10 min 500 °C N_2 PMA: 10 min 400 °C N_2/H_2	2.25 [c]	180	235	Lowest = 3.5×10^{11} Highest = 1×10^{13}	[171]
Si/GaN/$Al_{0.25}Ga_{0.75}N$	ICP-RIE: SF_6 BCl_3/Cl_2	/	AlN	$Al_{0.23}Si_{0.77}O$	PDA	~0.5 [c]	/	1000 (μ_{eff})	/	[150]

Table 4. *Cont.*

Substrate	Etching	Surface Preparation	Interfacial Layer	Dielectric	Annealing After Deposition	V_{TH} (V)	ΔV_{TH} (mV)	Mobility μ_{FE} ($cm^2 \cdot V^{-1} \cdot s^{-1}$)	D_{it} ($cm^{-2} \cdot eV^{-1}$)	Ref.
Si/GaN/AlN/ $Al_{0.25}Ga_{0.75}N$	ALE: O_2 + BCl_3 plasma	/	/	$HfSiO_x$	/	2.1 [b]	/	426	Lowest = 3×10^{11} Highest = 6×10^{12}	[196]

V_{TH} extracted by: [a] normalized fixed I_{DS} current; [b] linear extrapolation; [c] extraction technique not mentioned.

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