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Modeling Control and Robustness Assessment of Multilevel Flying-Capacitor Converters

Roberto Zanasi and Davide Tebaldi *

"Enzo Ferrari" Department of Engineering, University of Modena and Reggio Emilia,Via Pietro Vivarelli 10 Int. 1, 41125 Modena, Italy; roberto.zanasi@unimore.it

* Correspondence: davide.tebaldi@unimore.it

Abstract: When performing AC/DC-DC/AC power conversions, multilevel converters provide several advantages as compared to classical two-level converters. This paper deals with the dynamic modeling, control, and robustness assessment of multilevel flying-capacitor converters. The dynamic model is derived using the Power-Oriented Graphs modeling technique, which provides the user with block schemes that are directly implementable in the Matlab/Simulink environment by employing standard Simulink libraries. The performed robustness assessment has led to the proposal of a divergence index, which allows for evaluating the voltage balancing capability of the converter using different voltage vector configurations for the extended operation of the converter, namely when the number of output voltage levels is increased for a given number of capacitors. A new variable-step control algorithm is then proposed. The variable-step control algorithm safely enables the converter extended operation, which prevents voltage balancing issues, even under particularly unfavorable conditions, such as a constant desired output voltage or a sudden load change. The simulation results showing the good performances of the proposed variable-step control as compared to a classical minimum distance approach are finally provided and commented in detail.

Keywords: multilevel flying-capacitor converter; dynamic modeling; robustness assessment; control; voltage balancing capability

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1. Introduction

The need of performing power conversion is present in a large variety of engineering fields. When focusing on electrical power conversions, the cases of DC/DC [1–3], AC/DC-DC/AC [4–6] power conversions can be distinguished. These types of power conversion find application in many areas, including smart grids [1,4,5], hybrid electric vehicles [7], and many others. The physical modeling of the employed power converter topology is of great importance, as it represents the starting point for understanding its dynamic behavior and developing an effective control strategy. This paper deals with the modeling, control and robustness assessment of multilevel flying-capacitor converters.

Multilevel topologies bring several advantages when compared to classical two-level converters, such as a significant distortion reduction in the output voltage waveform and in the drawn input current, a reduction of the dv/dt effect in the output voltage waveform, and the generation of a lower common-mode voltage [8,9]. Furthermore, transformerless grid-connected multilevel converters are largely used in applications, such as motor drives, solid-state power transformers, and photovoltaic systems, as they provide advantages, such as increased power, voltage ratings, and lower harmonic distortion [10,11]. In this latter type of converters, the development of suitable ground potentials models is important, as high ground potentials represents an issue that may affect the converter operation. This matter is addressed in [10,11], together with the creation of local grounding points limiting ground potentials and blocking ground leakage currents from flowing through the host grid grounding, and together with the testing of grounding circuits for the considered

application. A vast array of different multilevel converter topologies have been proposed over the years [8,10–12], including diode-clamped converters, flying-capacitors converters, cascaded H-bridge converters, etc. Together with the advantages and potentialities that are brought by multilevel converters comes the difficulty of having more power electronics devices to control. This has led to the development of different modulation algorithms and techniques having different trade-offs between the pros and cons [13,14].

When dealing with the modeling and control of multilevel converters, the choice of the employed modeling approach represents the first step. In [15], the modeling of the Modular Multilevel Matrix Converter (M^3C) is addressed in a matrix form defining voltage-current model and a power-capacitor voltage model, whereas, in [16], the modeling of a Modular Multilevel Converter is performed using a state-space model, which is next discretized using a forward Euler approximation. In this paper, we address the dynamic modeling of multilevel flying-capacitor converters using the Power-Oriented Graphs (POG) modeling technique [17], extending the modeling approach that was proposed in [12]. The POG technique is one of the main graphical formalisms for modeling physical systems, together with Bond Graphs [18] and Energetic Macroscopic Representation [18]. The POG technique is deemed effective, as it allows for building block diagrams that can be directly implemented in the Matlab/Simulink environment using blocks that are available in basic libraries, and to effectively control the power flows within the system [18]. The proposed approach provides a very compact continuous-time model of the considered multilevel converter which can be applied to other converter topologies as well, and establishes a straightforward way of computing the capacitor voltages and currents starting from the Insulated Gate Bipolar Transistors (IGBTs) switching states. The Readers are referred to [19] for applications of the POG technique to physical systems modeling in different energetic domains, where a web POG modeling program is presented, together with some examples.

Once the modeling is performed, the next step is represented by the control of the considered multilevel converter topology. The subject of multilevel converters control has been largely treated in the literature, by focusing on different converter topologies and aiming at different objectives, depending on the converter topology. In [20], the authors propose an interesting space-vector based approach for modeling modular multilevel converters for battery electric vehicles, showing that the traditional approach for achieving cell balancing can be seen as a special case of the proposed model. In [21], the control of modular multilevel converters is approached using model predictive control that is aided by disturbance observers with the objective of controlling the AC current and suppressing the circulating current in the converter. An asymmetric cascade H-bridge multilevel converter topology that is equipped with a predictive control strategy is instead proposed in [22]. The purpose of the latter is to minimize the converter commutations, while also exploiting the redundant states to equally distribute the load among the switches, thus equalizing their lifetime expectation. Focusing on multilevel topologies having floating capacitors involved in their operation, an important aspect is represented by the capacitors voltages balancing. If not properly controlled, the floating capacitors voltages may suffer from ripple [23], which would cause output voltage and current distortion, or even voltages trajectory divergence, thus further compromising the converter operation. An important distinction needs to be made between those multilevel converters having full floating capacitors voltage balancing capability and those not having it, due to topology limitations or lack of redundancy. This latter case is addressed in [23], where a new PWM method was proposed to improve the floating capacitors voltage balancing capability. Multilevel flying-capacitor converters have full floating capacitors voltage balancing capability if properly controlled and if the number of output voltage levels m equals the number of capacitors n plus one (i.e., the number of floating capacitors plus two). An analytical investigation of the voltage balancing characteristics of the flying capacitor converter while using the phase disposition PWM (PDPWM) modulation technique is presented in [24]. An interesting approach to ensure floating capacitors voltage balancing capability is presented in [25], where a modification of the carrier-redistribution PWM (CRPWM) is

proposed in order to ensure a low output voltage harmonic content and low voltage ripple, thanks to the symmetric disposition of carriers in every fundamental period. However, the main drawback that is associated with open-loop methods is that they aim at keeping the floating capacitors voltages as close to the desired value as possible, but do not consider the case of a voltage unbalance occurring because of some unfavorable conditions, such as a fault, for example. In this latter case, a closed-loop control solution is required, in order to drive the capacitors voltages trajectory back to the desired operating point, thus ensuring the correct operation of the converter. The multilevel flying-capacitor converter having a generic number n of capacitors can actually generate all the way up to 2^n output voltage levels, giving rise to what is called "extended operation" [26,27]. However, if the number of voltage levels m is greater than $n+1$, then the multilevel flying-capacitor converter loses the property of full floating capacitors voltage balancing capability, and a suitable closed-loop control technique becomes paramount. An example of closed-loop control technique for the multilevel flying-capacitor converter in such operating condition using a "minimum distance" approach is proposed in [27]. However, to the best of our knowledge, there is no proposal in the literature of a metric allowing for performing the robustness assessment of multilevel flying-capacitor converters against the divergence of the flying capacitors voltage trajectory. This becomes especially crucial with the converter working in extended operation, namely with a number m of output voltage levels greater than $n+1$ all the way up to 2^n. In this paper, we address: (a) the dynamic modeling of multilevel flying-capacitor converters; (b) the analysis of all the possible configurations of the converter in terms of capacitors voltage ratio allowing for the converter to work in extended operation; (c) the robustness assessment of multilevel flying-capacitor converters when working in extended operation and controlled using a classical minimum distance approach; (d) the proposal of a divergence index determining the degradation of the converter operation using a minimum distance control as the number of output voltage levels is increased for all of the possible capacitors voltages configurations; (e) the proposal of a new variable-step closed-loop control strategy for guaranteeing the best flying capacitors voltage balance in any extended operating condition; and, (f) the comparison of the proposed variable-step control strategy for multilevel flying-capacitor converters with a classical minimum distance control approach.

The remainder of the paper is organized as follows. Section 2 introduces the characteristics and basic properties of the POG modeling technique. Section 3, and the included subsections, address the dynamic modeling of the multilevel flying-capacitor converter. The main matrices and vectors of the model are introduced and described, together with some interesting properties that they exhibit. The model verification against the PLECS simulator is addressed in Section 3.4. Section 4 deals with the control of the multilevel flying-capacitor converter. In particular, Section 4.1 addresses the minimum distance algorithm, whereas Section 4.2 defines the basic configuration of the multilevel flying-capacitor converter. Section 4.3 describes the robustness assessment of the considered converter in extended mode using a minimum distance algorithm, whereas Section 4.4 proposes the new variable-step control algorithm. The converter simulation in extended mode with different dynamic loads is addressed in Section 5. Section 6 finally provides the conclusions of this work.

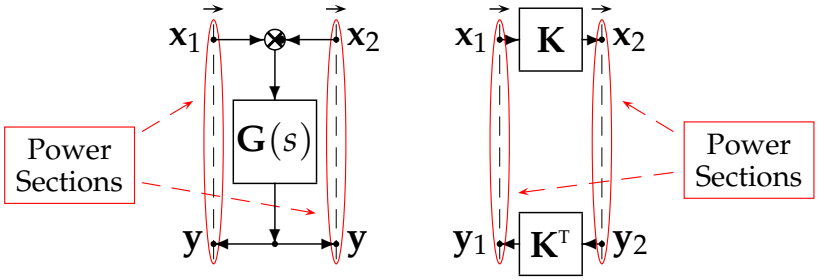
2. The POG Modeling Technique

The Power-Oriented Graphs (POG) technique [17,18] is a graphical modeling formalism that is based on the same energetic approach employed by the Bond Graph (BG) technique [18] using a different graphical notation. Power-Oriented Graphs are created using two elementary blocks, namely the elaboration block and the connection block, which are shown in Figure 1. The first block is employed for the modeling of all the physical elements storing and/or dissipating energy, whereas the second one is used for the modeling of all the physical elements performing energy conversion. The elaboration block describes static or dynamic physical elements, and is characterized by the transfer

function (or matrix) $G(s)$ of the considered element. If the transfer function $G(s) = R$ is constant, then the considered physical element is static, being characterized by the static relation between the input variable v_f and the output variable v_e or viceversa. The dynamic elements can be classified into two types:

- *across elements* D_e, having a flow variable v_f as input and an across variable v_e as output;
- *flow elements* D_f, having an across variable v_e as input and a flow variable v_f as output.

A flow power variable v_f is always defined in each point of the space, whereas an across power variable v_e is defined between two points. Table 1 provides a compact description of the dynamic and static elements, together with the across and flow variables, in the four typically considered energetic domains. The crossed circle in the upper part of the elaboration block in Figure 1 is a *summation node*, where the black spot on the right denotes that the power variable entering the summation node from that side has to be subtracted. The connection block is characterized by a coefficient (or matrix) K, which completely describes the energy conversion between the energetic domains.



a) *Elaboration block* b) *Connection block*

Figure 1. POG elementary blocks: *elaboration block* and *connection block*.

Table 1. Physical elements and power variables in the different energetic domains.

	Electrical	**Mechanical Translational**	**Mechanical Rotational**	**Hydraulic**
D_e	Capacitor C	Mass M	Inertia J	Hydraulic Capacitor C_I
v_e	Voltage V	Velocity $\dot{x}$	Angular Velocity ω	Pressure P
D_f	Inductor L	Spring E	Rotational Spring E	Hydraulic Inductor L_I
v_f	Current I	Force F	Torque τ	Volume Flow Rate Q
R	Resistor R	Friction b	Angular Friction b	Hydraulic Resistor R_I

One of the main characteristics of the POG modeling technique is the maintained direct correspondence between the power sections in the POG model, as highlighted by the red ellipses in Figure 1, and the power sections of the actual physical system. The scalar product $\mathbf{x}^T\mathbf{y}$ of the two power variables $\mathbf{x}$ and $\mathbf{y}$ in the considered power section has the physical meaning of *power flowing through the considered section*. The black oriented arrows placed at the top of each power section in the scheme of Figure 1 highlight the positive direction of the power flow through the considered section.

Any physical system that is modeled by means of the POG technique is characterized by the following POG state-space representation:

$$\begin{cases} \mathbf{L}\,\dot{\mathbf{x}} = \mathbf{A}\,\mathbf{x} + \mathbf{B}\,\mathbf{u} \\ \mathbf{y} = \mathbf{C}\,\mathbf{x} + \mathbf{D}\,\mathbf{u} \end{cases},$$

where **L** is the energy matrix, **A** is the power matrix, **B** is the input matrix, **C** is the output matrix, and **D** is the input-output matrix. The energy matrix **L** and power matrix **A** describe the instantaneous energy E_s stored in the system and the instantaneous power P_d dissipated in the system, respectively:

$$E_s = \frac{1}{2}\,\mathbf{x}^{\mathrm{T}}\,\mathbf{L}\,\mathbf{x}, \qquad P_d = \mathbf{x}^{\mathrm{T}}\,\mathbf{A}_s\,\mathbf{x},$$

where $\mathbf{A}_s$ is the symmetric part of matrix **A**.

3. Modeling of the *n*-Dimensional Multilevel Flying-Capacitor Converter

3.1. Physical System and Configuration Vectors

Let us consider the electric scheme of an *n*-dimensional Multilevel Flying-Capacitor Converter that is shown in Figure 2. The output voltage V_{out} is a function of the IGBTs activation signals $T_i \in \{0,\ 1\}$, for $i \in \{1\ ,2\ ,\dots\ ,n\}$. Let $\mathbf{V}_c$ and $\mathbf{T}_j$ denote the capacitors voltage column vector and the IGBTs signal row vectors, defined as follows:

$$\mathbf{V}_c = \begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ \vdots \\ V_n \end{bmatrix}, \qquad \begin{bmatrix} \mathbf{T}_0 \\ \mathbf{T}_1 \\ \mathbf{T}_2 \\ \mathbf{T}_3 \\ \vdots \\ \mathbf{T}_{m_c-2} \\ \mathbf{T}_{m_c-1} \end{bmatrix} = \begin{bmatrix} 0 & \dots & 0 & 0 & 0 \\ 0 & \dots & 0 & 0 & 1 \\ 0 & \dots & 0 & 1 & 0 \\ 0 & \dots & 0 & 1 & 1 \\ \vdots & \ddots & \vdots & \vdots & \vdots \\ 1 & \dots & 1 & 1 & 0 \\ 1 & \dots & 1 & 1 & 1 \end{bmatrix} \quad \begin{matrix} n=3 \\ \Rightarrow \end{matrix} \quad \begin{bmatrix} \mathbf{T}_0 \\ \mathbf{T}_1 \\ \mathbf{T}_2 \\ \mathbf{T}_3 \\ \mathbf{T}_4 \\ \mathbf{T}_5 \\ \mathbf{T}_6 \\ \mathbf{T}_7 \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 1 \\ 0 & 1 & 0 \\ 0 & 1 & 1 \\ 1 & 0 & 0 \\ 1 & 0 & 1 \\ 1 & 1 & 0 \\ 1 & 1 & 1 \end{bmatrix}, \tag{1}$$

where $j \in \{0\ ,1\ ,\dots\ ,m_c-1\}$, $m_c = 2^n$, and V_i are the voltages across the capacitors C_i. The electrical schemes that are reported in Figure 3 show how, for the case $n = 3$, the output voltage V_{out} is a function of the IGBTs signal vectors $\mathbf{T}_j$ in the two cases $\mathbf{T}_j = \mathbf{T}_2 = [\ 0\ 1\ 0\ ]$ and $\mathbf{T}_j = \mathbf{T}_6 = [\ 1\ 1\ 0\ ]$.

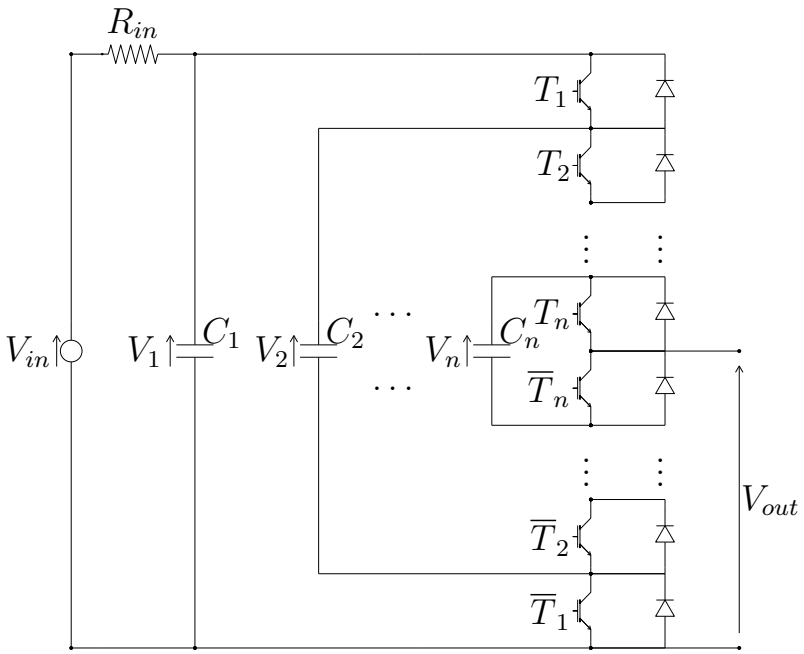


Figure 2. Electrical scheme of the *n*-dimensional Multilevel Flying-Capacitor Converter.

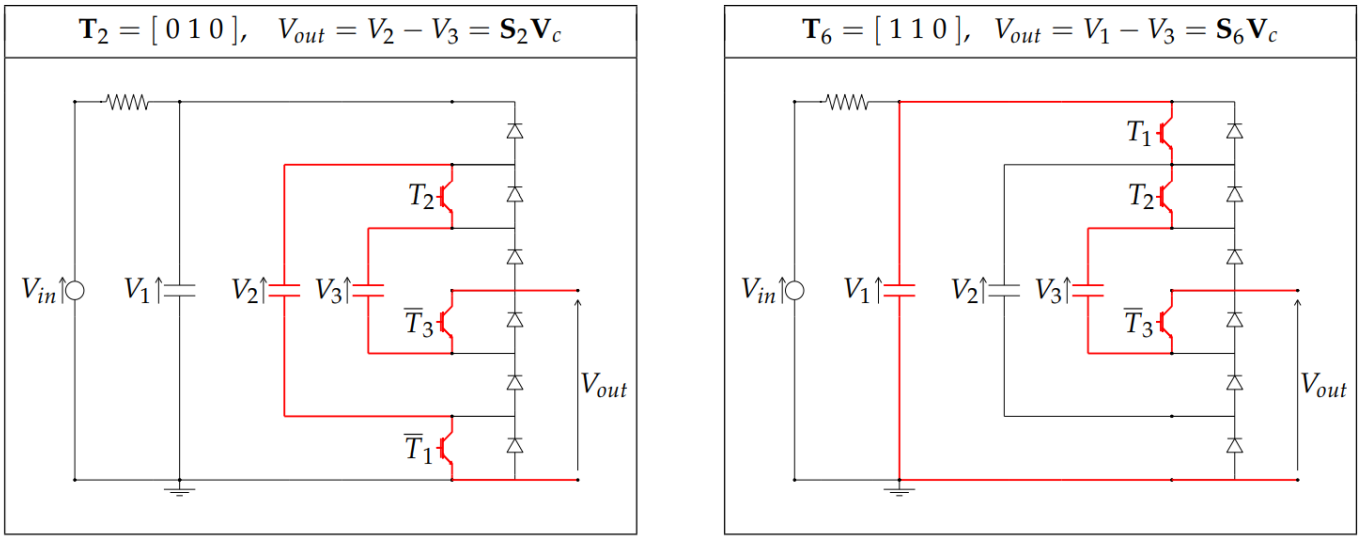


Figure 3. Electrical schemes showing how the output voltage V_{out} is obtained as a function of the Insulated Gate Bipolar Transistors (IGBTs) signal vectors $\mathbf{T}_i$ in the two cases $\mathbf{T}_j = \mathbf{T}_2 = [\,0\;1\;0\,]$ and $\mathbf{T}_j = \mathbf{T}_6 = [\,1\;1\;0\,]$.

One can easily verify that the output voltage V_{out} can always be expressed as follows:

$$V_{out} = \mathbf{S}_j\,\mathbf{V}_c, \tag{2}$$

where $\mathbf{S}_j = [s_1\; s_2\; \cdots\; s_n]$, for $j \in \{0\,, 1\,, \ldots\,, m_c - 1\}$, are proper configuration vectors. In the two cases of Figure 3, for example, the output voltage V_{out} can be expressed as in (2) by using the following two configuration vectors: $\mathbf{S}_2 = [\,0\;\;1\;\;-1\,]$ and $\mathbf{S}_6 = [\,1\;\;0\;\;-1\,]$. Table 2 shows the relations between the IGBTs signal vectors $\mathbf{T}_j$, the output voltage V_{out} and the configuration vectors $\mathbf{S}_j$ for the case $n = 3$, highlighting the connection between vectors $\mathbf{T}_j$ and $\mathbf{S}_j$. One can verify that the following property holds.

Table 2. Relations between the IGBTs signal vectors $\mathbf{T}_j$, the output voltage V_{out} and the configuration vectors $\mathbf{S}_j$ when $n = 3$.

$\mathbf{T}_j$	$[\,T_1\;T_2\;T_3\,]$	V_{out}	$[\,s_1\;\;s_2\;\;s_3\,]$	$\mathbf{S}_j$	V_{out} (5)	α_i
$\mathbf{T}_0$	$[\;0\;\;0\;\;0\,]$	$\mathbf{S}_0\mathbf{V}_c = 0$	$[\;0\;\;\;0\;\;\;0\,]$	$\mathbf{S}_0$	0	0
$\mathbf{T}_1$	$[\;0\;\;0\;\;1\,]$	$\mathbf{S}_1\mathbf{V}_c = V_3$	$[\;0\;\;\;0\;\;\;1\,]$	$\mathbf{S}_1$	$V_{in}/3$	1
$\mathbf{T}_2$	$[\;0\;\;1\;\;0\,]$	$\mathbf{S}_2\mathbf{V}_c = V_2 - V_3$	$[\;0\;\;\;1\;-1\,]$	$\mathbf{S}_2$	$V_{in}/3$	1
$\mathbf{T}_3$	$[\;0\;\;1\;\;1\,]$	$\mathbf{S}_3\mathbf{V}_c = V_2$	$[\;0\;\;\;1\;\;\;0\,]$	$\mathbf{S}_3$	$2V_{in}/3$	2
$\mathbf{T}_4$	$[\;1\;\;0\;\;0\,]$	$\mathbf{S}_4\mathbf{V}_c = V_1 - V_2$	$[\;1\;-1\;\;\;0\,]$	$\mathbf{S}_4$	$V_{in}/3$	1
$\mathbf{T}_5$	$[\;1\;\;0\;\;1\,]$	$\mathbf{S}_5\mathbf{V}_c = V_1 - V_2 + V_3$	$[\;1\;-1\;\;\;1\,]$	$\mathbf{S}_5$	$2V_{in}/3$	2
$\mathbf{T}_6$	$[\;1\;\;1\;\;0\,]$	$\mathbf{S}_6\mathbf{V}_c = V_1 - V_3$	$[\;1\;\;\;0\;-1\,]$	$\mathbf{S}_6$	$2V_{in}/3$	2
$\mathbf{T}_7$	$[\;1\;\;1\;\;1\,]$	$\mathbf{S}_7\mathbf{V}_c = V_1$	$[\;1\;\;\;0\;\;\;0\,]$	$\mathbf{S}_7$	V_{in}	3

Property 1. *For $j \in \{0\,, 1\,, \ldots\,, m_c - 1\}$, the components $s_i \in \{-1,\ 0,\ 1\}$ of the configuration vectors $\mathbf{S}_j = [s_1\; s_2\; \cdots\; s_n]$ can be obtained from the components $T_i \in \{0,\ 1\}$ of the IGBTs signal vectors $\mathbf{T}_j = [T_1\; T_2\; \cdots\; T_n]$, as follows:*

$$s_i = \begin{cases} T_1 & \text{if} \quad i = 1, \\ \overline{T}_{i-1}\,T_i - T_{i-1}\,\overline{T}_i & \text{if} \quad i \in \{2, \cdots, n\}, \end{cases} \tag{3}$$

or, equivalently, as follows:

$$s_i = \begin{cases} 1 & \text{if} \quad T_i > T_{i-1}, \\ 0 & \text{if} \quad T_i = T_{i-1}, \\ -1 & \text{if} \quad T_i < T_{i-1}, \end{cases} \tag{4}$$

for $i \in \{1, 2, \cdots, n\}$ *and* $T_0 = 0$.

As an example, the Reader can verify that Property 1 holds for all of the configuration vectors $\mathbf{S}_j$ that are reported in Table 2 for the case $n = 3$. The second last column of Table 2 shows the values of the output voltage V_{out} corresponding to the following capacitors voltages V_i:

$$V_1 = V_{in}, \qquad V_2 = \frac{2V_{in}}{3}, \qquad V_3 = \frac{V_{in}}{3} \qquad \Rightarrow \qquad \mathbf{V}_c = \begin{bmatrix} V_{in} \\ \frac{2V_{in}}{3} \\ \frac{V_{in}}{3} \end{bmatrix}. \tag{5}$$

The last column of Table 2 shows the normalized values α_i, as defined in Section 3.3, used for representing the equally spaced values of the output voltage V_{out} in the case of $n = 3$ capacitors and $m = 4$ output voltage levels.

Let $\mathbf{S}_M$ denote the matrix containing all of the possible configuration vectors $\mathbf{S}_j$, for $j \in \{0, 1, \ldots, m_c - 1\}$:

$$\mathbf{S}_M = \begin{bmatrix} \mathbf{S}_0 \\ \mathbf{S}_1 \\ \vdots \\ \mathbf{S}_{m_c-1} \end{bmatrix}, \qquad \begin{matrix} \text{if } n = 3 \\ \rightarrow \end{matrix} \qquad \mathbf{S}_M = \begin{bmatrix} \mathbf{S}_0 \\ \mathbf{S}_1 \\ \mathbf{S}_2 \\ \mathbf{S}_3 \\ \mathbf{S}_4 \\ \mathbf{S}_5 \\ \mathbf{S}_6 \\ \mathbf{S}_7 \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 1 \\ 0 & 1 & -1 \\ 0 & 1 & 0 \\ 1 & -1 & 0 \\ 1 & -1 & 1 \\ 1 & 0 & -1 \\ 1 & 0 & 0 \end{bmatrix}. \tag{6}$$

Matrix $\mathbf{S}_M$ can always be rewritten in block matrix form as follows:

$$\mathbf{S}_M = \left[\begin{array}{c|cc} \mathbf{0} & \multicolumn{2}{c}{\mathbf{S}_{M0}} \\ \hline \mathbf{1} & \multicolumn{2}{c}{\mathbf{S}_{M1}} \end{array}\right] \qquad \begin{matrix} \text{if } n = 3 \\ \rightarrow \end{matrix} \qquad \mathbf{S}_M = \left[\begin{array}{c|cc} 0 & 0 & 0 \\ 0 & 0 & 1 \\ 0 & 1 & -1 \\ 0 & 1 & 0 \\ \hline 1 & -1 & 0 \\ 1 & -1 & 1 \\ 1 & 0 & -1 \\ 1 & 0 & 0 \end{array}\right]. \tag{7}$$

One can verify that the block matrices $\mathbf{S}_{M0}$, $\mathbf{S}_{M1} \in \mathbf{R}^{2^{n-1} \times (n-1)}$ satisfy the following property.

Property 2. *Let* $\mathbf{S}^j_{M0}$ *and* $\mathbf{S}^j_{M1}$ *denote the j-th row of the block matrices* $\mathbf{S}_{M0}$, $\mathbf{S}_{M1} \in \mathbf{R}^{2^{n-1} \times (n-1)}$ *defined in* (7). *Matrix* $\mathbf{S}_{M1}$ *can be obtained from matrix* $\mathbf{S}_{M0}$, *as follows:*

$$\mathbf{S}^j_{M1} = -\mathbf{S}^{2^{n-1}+1-j}_{M0} \qquad \text{for} \qquad j \in \left\{1, 2, \cdots, 2^{n-1}\right\}. \tag{8}$$

Equation (8) *means that the rows of matrix* $\mathbf{S}_{M1}$ *are equal, with opposite sign, to the rows of matrix* $\mathbf{S}_{M0}$ *considered in reverse order.*

From Property (2) and Equations (2) and (7), one can verify that the following property holds.

Property 3. *If the output value* $V_{out1} = \mathbf{S}_j \, \mathbf{V}_c$ *is obtained using the configuration vector* $\mathbf{S}_j$*, then the following conjugate output value*

$$V_{out2} = V_{in} - V_{out1} = \mathbf{S}_{m_c - j} \, \mathbf{V}_c$$

is obtained by employing the configuration vector $\mathbf{S}_{m_c - j}$*, for* $j \in \{0, 1, \cdots, m_c - 1\}$ *and* $m_c = 2^n$.

3.2. Dynamic Model of the Multilevel Flying-Capacitor Converter

The dynamic model of the Multilevel Flying-Capacitor Converter shown in Figure 2 can be given by using the Power-Oriented Graphs (POG) scheme reported in Figure 4. The corresponding POG state-space equations are the following:

$$\begin{cases} \mathbf{C} \, \dot{\mathbf{V}}_c = \mathbf{A} \, \mathbf{V}_c - \mathbf{S}_j^{\mathrm{T}} \, I_{out} + \mathbf{B} \, V_{in}, \\ V_{out} = \mathbf{S}_j \, \mathbf{V}_c. \end{cases} \tag{9}$$

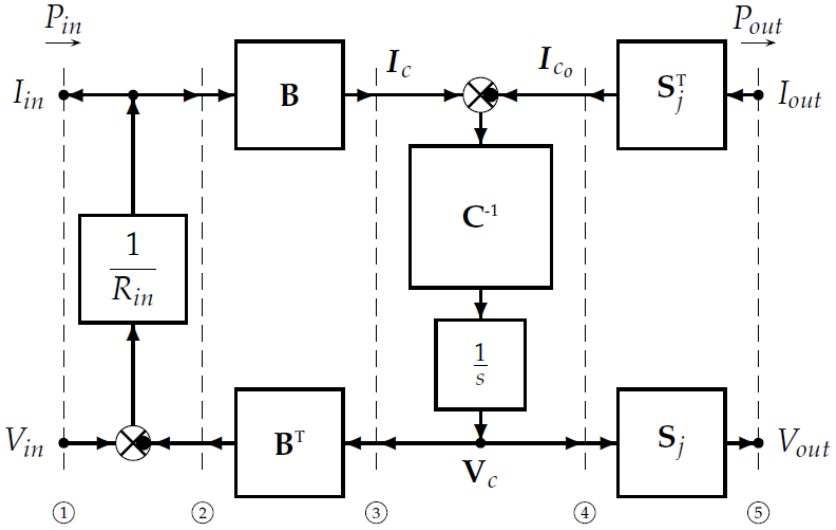


Figure 4. Power-Oriented Graphs (POG) model of the Multilevel Flying-Capacitor Converter.

Matrices $\mathbf{C}$, $\mathbf{A}$ and vectors $\mathbf{V}_c$, $\mathbf{S}_j^{\mathrm{T}}$ and $\mathbf{B}$ are defined, as follows:

$$\mathbf{C} = \left[\begin{array}{c|ccc} C_1 & 0 & \cdots & 0 \\ \hline 0 & C_2 & \cdots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \cdots & C_n \end{array}\right], \quad \mathbf{A} = \left[\begin{array}{c|ccc} \frac{-1}{R_{in}} & 0 & \cdots & 0 \\ \hline 0 & 0 & \cdots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \cdots & 0 \end{array}\right], \quad \mathbf{V}_c = \begin{bmatrix} V_1 \\ V_2 \\ \vdots \\ V_n \end{bmatrix}, \quad \mathbf{S}_j^{\mathrm{T}} = \begin{bmatrix} s_1 \\ s_2 \\ \vdots \\ s_n \end{bmatrix}, \quad \mathbf{B} = \begin{bmatrix} \frac{1}{R_{in}} \\ 0 \\ \vdots \\ 0 \end{bmatrix}. \tag{10}$$

A representation such as the one that is shown in (9) and (10) highlights the following interesting features of the system:

- The energy matrix $\mathbf{C}$ groups together the dynamic physical parameters C_i for $i \in \{1, 2, \ldots, n\}$, namely the system capacitors.
- The power matrix $\mathbf{A}$ and the input matrix $\mathbf{B}$ contain the static physical parameter R_{in}, which is the system input resistance.
- The *configuration vector* $\mathbf{S}_j$ contains the control signals that directly determine how the output current I_{out} is going to charge/discharge the capacitors through $\mathbf{I}_{c_0} = \mathbf{S}_j^{\mathrm{T}} I_{out}$ and, at the same time, how the output voltage V_{out} is going to be generated from the capacitors voltages through (2).

Therefore, the proposed POG state-space model allows for the parameters within the system matrices to maintain their physical meaning, and also allows to emphasize the presence of

the configuration vector $\mathbf{S}_j$, representing the output of the two control algorithms that are addressed in Section 4.1 and Section 4.4. The POG block scheme that is shown in Figure 4 presents a graphical representation of the dynamic model of the considered system. The vertical dashed lines ①, ②, . . ., and ⑤ present in the POG scheme describe the system power sections: the product of the two power variables characterizing the power section has the physical meaning of "power flowing through the considered power section". The input power $P_{in} = V_{in}\, I_{in}$ flows through power section ① and the output power $P_{out} = V_{out}\, I_{out}$ flows through power section ⑤. The block scheme in between sections ① and ② describes the static equation of the input resistance R_{in}, the block scheme in between sections ② and ③ describes the interaction between the input resistance R_{in} and the capacitors C_i, and the block scheme in between sections ③ and ④ describes the dynamic equations of the capacitors C_i. Finally, the block scheme in between sections ④ and ⑤, which is characterized by the configuration vector $\mathbf{S}_j$, describes the interaction between the capacitors C_i and the output power section ⑤.

Remark 1. *The first vectorial equation of system (9) can be rewritten as follows:*

$$\dot{\mathbf{V}}_c = \mathbf{C}^{-1}\mathbf{A}\mathbf{V}_c \underbrace{-\mathbf{C}^{-1}\mathbf{S}_j^T\, I_{out}}_{\dot{\mathbf{V}}_c^{out}} + \mathbf{C}^{-1}\mathbf{B}\, V_{in}.$$

Vector $\dot{\mathbf{V}}_c^{out} = -\mathbf{C}^{-1}\mathbf{S}_j^T\, I_{out}$ *is the component of the velocity vector* $\dot{\mathbf{V}}_c$ *which is due to the presence of the output current* I_{out}*. The direction of vector* $\dot{\mathbf{V}}_c^{out}$ *is completely defined by the configuration vector* $\mathbf{S}_j$ *and by the values of the capacitors* C_i*.*

Remark 2. *The first scalar equation of system (9) can be rewritten as follows:*

$$R_{in} C_1 \dot{V}_1 = V_{in} - V_1 - R_{in}\, s_1\, I_{out}. \tag{11}$$

Because the value of the input resistance R_{in} *is typically very low, from (11) it follows that* $V_1 \simeq V_{in}$*, that is the value of voltage* V_1 *tends to remain close to the input voltage value* V_{in}*. Hereinafter, the condition* $V_1 = V_{in}$ *will be assumed. This condition holds exactly if* $R_{in} \to 0$*, or if capacitor* C_1 *is replaced with a battery providing a constant voltage* V_{in}*.*

3.3. Calculation of All the Configuration Voltage Vectors

An m-level Multilevel Converter is characterized by m different equally spaced values V_{oi} of the output voltage V_{out}:

$$V_{oi} = \frac{i\, V_{in}}{m-1} \qquad \text{for} \qquad i = \{0,\ 1,\ \ldots,\ m-1\}. \tag{12}$$

In the following, the values V_{oi} in (12) will often be referred to by using the symbolic integer values α_i, defined as follows:

$$\alpha_i = \frac{V_{oi}}{K_m} = i \qquad \text{where} \qquad K_m = \frac{V_{in}}{m-1}, \tag{13}$$

for $i = \{0,\ 1,\ \ldots,\ m-1\}$. From (13), it follows that the product $\alpha_i\, K_m$ directly gives the values of the corresponding equally spaced values V_{oi} of the output voltage V_{out}. All of the possible values V_{oi} of the output voltage V_{out} that can be obtained using a particular voltage vector $\mathbf{V}_c$ can be expressed as follows:

$$\mathbf{V}_o = \mathbf{S}_M \mathbf{V}_c, \tag{14}$$

where $\mathbf{S}_M$ is the matrix defined in (6). The considered Flying-Capacitor system acts properly as a Multilevel Converter only if vector $\mathbf{V}_o = [\ V_{o1},\ V_{o2},\ \ldots,\ V_{om_c}]^{\mathrm{T}}$ contains, among its components V_{oj}, all of the m different equally spaced values V_{oi} given in (12):

$$\forall i \in \{0,\ 1,\ \ldots,\ m-1\},\ \ \exists\ V_{oj} \in \{V_{o1},\ V_{o2},\ \ldots,\ V_{om_c}\}\ \mid\ V_{oj} = \frac{i\,V_{in}}{m-1}. \tag{15}$$

Definition 1. *Any voltage vector* $\mathbf{V}_c$ *satisfying* (14) *and* (15) *will be called a " Configuration Voltage Vector of order m" for the Multilevel Flying-Capacitor Converter.*

The problem of finding all the Configuration Voltage Vectors $\mathbf{V}_c$ of order m for the considered Multilevel Flying-Capacitor Converter can be solved as follows. Dividing (14) by constant K_m, one obtains the following symbolic integer relation:

$$\mathbf{V}_L = \mathbf{S}_M \mathbf{V}_m \qquad \text{where} \qquad \mathbf{V}_L = \frac{\mathbf{V}_o}{K_m} \quad \text{and} \quad \mathbf{V}_m = \frac{\mathbf{V}_c}{K_m}. \tag{16}$$

A vector $\mathbf{V}_m$ in (16) is a Configuration Voltage Vector of order m only if all the components V_{Lj} of vector $\mathbf{V}_L = [V_{L1},\ V_{L2},\ \ldots,\ V_{Lm_c}]$, for $j \in \{1,\ 2,\ \ldots,\ m_c\}$, are integer values $V_{Lj} \in \{0,\ 1,\ \ldots,\ m-1\}$ that satisfy the following relation:

$$\text{unique}(\{V_{L1},\ V_{L2},\ \ldots,\ V_{Lm_c}\}) = \{0,\ 1,\ \ldots,\ m-1\}, \tag{17}$$

where "unique($\mathcal{S}$)" is a function providing a new set containing all the elements of set $\mathcal{S}$ which are different from each other.

Property 4. *In* (16)*, all of the components* β_i *of a Configuration Voltage Vector* $\mathbf{V}_m$*, for* $i \in \{1,\ \ldots,\ n\}$*, are integer values satisfying* $\beta_i \in \{0,\ 1,\ \ldots,\ m-1\}$*:*

$$\mathbf{V}_m = \begin{bmatrix} \beta_n \\ \beta_{n-1} \\ \vdots \\ \beta_1 \end{bmatrix} = \begin{bmatrix} m-1 \\ \beta_{n-1} \\ \vdots \\ \beta_1 \end{bmatrix}, \tag{18}$$

where $\beta_{i+1} \geq \beta_i$ *for* $i \in \{1,\ 2,\ \ldots,\ n-2\}$*. Furthermore, note that the top component* β_n *of vector* $\mathbf{V}_m$ *is always given by* $\beta_n = m-1$*.*

The first statement of Property 4 holds true, because: (1) all of the components V_{Lj} of vector $\mathbf{V}_L$ in (16) are integer values, see (17); and, (2) the configuration vectors $\mathbf{S}_1 = [0\ \ldots,\ 0,\ 0,\ 1]$, $\mathbf{S}_2 = [0\ \ldots,\ 0,\ 1,\ 0]$, $\mathbf{S}_3 = [0\ \ldots,\ 1,\ 0,\ 0]$, …, $\mathbf{S}_{m_c} = [1,\ 0\ \ldots,\ 0,\ 0]$ are always present among the rows of matrix $\mathbf{S}_M$. The second statement of Property 4 holds true, because the top component β_n of vector $\mathbf{V}_m$ is always equal to the first component V_1 of vector $\mathbf{V}_c$ expressed in symbolic integer form: $\beta_n = V_1/K_m = V_{in}/K_m = m-1$, see (13). This relation holds thanks to the assumption $V_1 = V_{in}$ made in Remark 2.

Thanks to Property 4, all of the Configuration Voltage Vectors $\mathbf{V}_m$ of order m for the considered Multilevel Flying-Capacitor Converter can be found by making an exhaustive research in (18) for $\beta_i \in \{0,\ 1,\ \ldots,\ m-1\}$, and keeping all of the solutions $\mathbf{V}_m$ that satisfy (16) and (18). Table 3 reports all of the Configuration Voltage Vectors $\mathbf{V}_m$ for the case $n = 3$ and for $m \in \{4,\ 5,\ \ldots,\ 8\}$. The total number N_c of Configuration Voltage Vectors for the case $n = 3$ is $N_c = 24$. Figure 5 shows a graphical representation of the normalized form

$\overline{\overline{\mathbf{V}}}_m$ of all the Configuration Voltage Vectors $\mathbf{V}_m$ for the case $n = 3$. The normalized form $\overline{\overline{\mathbf{V}}}_m$ of the Voltage Vectors $\mathbf{V}_m$ defined in (18) is obtained as follows:

$$\overline{\overline{\mathbf{V}}}_m = \frac{\mathbf{V}_m(2:\text{end})}{m-1} = \begin{bmatrix} \frac{\beta_{n-1}}{m-1} \\ \vdots \\ \frac{\beta_1}{m-1} \end{bmatrix} = \begin{bmatrix} \overline{\overline{V}}_2 \\ \vdots \\ \overline{\overline{V}}_n \end{bmatrix} \quad \begin{matrix} \text{if } n = 3 \\ \rightarrow \end{matrix} \quad \overline{\overline{\mathbf{V}}}_m = \begin{bmatrix} \overline{\overline{V}}_2 \\ \overline{\overline{V}}_3 \end{bmatrix}, \quad (19)$$

meaning that the last $n-1$ components of vector $\mathbf{V}_m$, from the second to the last one, are normalized by $m-1$. Figure 5 clearly shows a symmetry with respect to the red straight line $\overline{\overline{V}}_3 = 1 - \overline{\overline{V}}_2$. This symmetry is strictly connected to Property 5 and Property 6, introduced in the following.

Table 3. All of the Configuration Voltage Vectors $\mathbf{V}_m$ for the case $n = 3$ and $m \in \{4, 5, \ldots, 8\}$.

m	4	4	4	5	5	5	6	6	6	6	6	6	7	7	7	7	7	7	8	8	8	8	8	8
	3	3	3	4	4	4	5	5	5	5	5	5	6	6	6	6	6	6	7	7	7	7	7	7
$\mathbf{V}_m$	1	2	2	2	3	3	2	3	3	4	4	4	3	3	4	4	5	5	3	3	5	6	5	6
	1	1	2	1	1	2	1	1	2	1	2	3	1	2	1	3	2	3	1	2	1	2	4	4
N_β	2	3	4	3	4	5	3	4	5	5	6	7	4	5	5	7	7	8	4	5	6	8	9	10

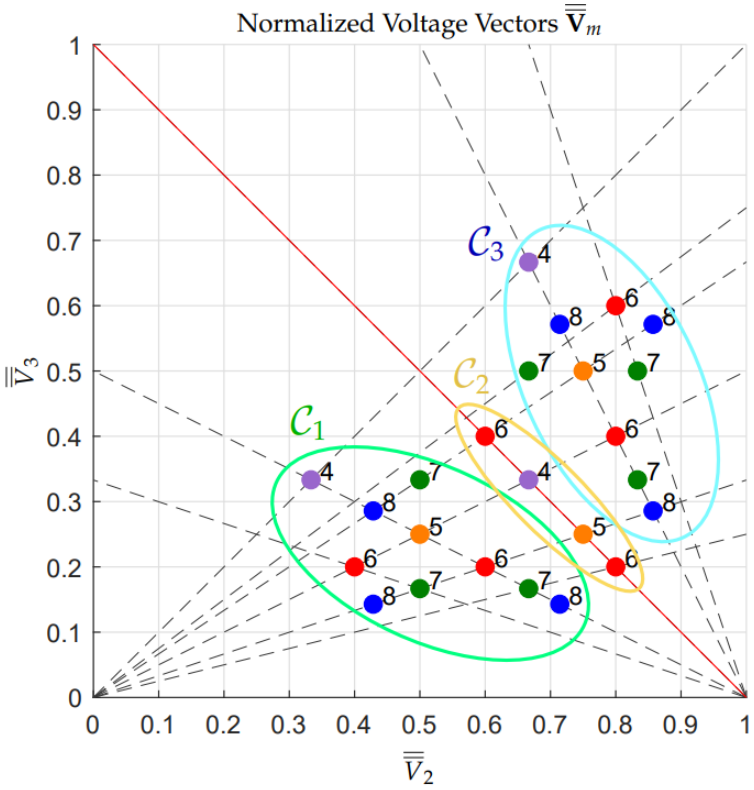


Figure 5. All the Configuration Voltage Vectors $\mathbf{V}_m$, in normalized form $\overline{\overline{\mathbf{V}}}_m$, for the case $n = 3$.

Property 5. *For every Configuration Voltage Vector* $\mathbf{V}_m$*, there exists a* Conjugate Configuration Voltage Vector $\mathbf{V}_m^\star$*, defined as follows:*

$$\mathbf{V}_m = \begin{bmatrix} m-1 \\ \beta_{n-1} \\ \vdots \\ \beta_2 \\ \beta_1 \end{bmatrix} \quad \Rightarrow \quad \mathbf{V}_m^\star = \begin{bmatrix} m-1 \\ m-1-\beta_1 \\ m-1-\beta_2 \\ \vdots \\ m-1-\beta_{n-1} \end{bmatrix}. \quad (20)$$

Furthermore, one can easily verify that $(\mathbf{V}_m^\star)^\star = \mathbf{V}_m$. *This property directly follows from Property 3.*

Property 6. *Every Configuration Voltage Vector* $\mathbf{V}_m$, *see* (20), *is characterized by a configuration number* N_β, *defined as follows:*

$$N_\beta = \sum_{i=1}^{n-1} \beta_i.$$

The set $\mathcal{C}$ *of all the Configuration Voltage Vectors* $\mathbf{V}_m$ *can be divided into three different subsets, which are denoted by* $\mathcal{C}_1$, $\mathcal{C}_2$, *and* $\mathcal{C}_3$, *defined as follows:*

$$\mathcal{C}_1 = \{\mathbf{V}_m \in \mathcal{C} | N_\beta < m-1\}, \quad \mathcal{C}_2 = \{\mathbf{V}_m \in \mathcal{C} | N_\beta = m-1\}, \quad \mathcal{C}_3 = \{\mathbf{V}_m \in \mathcal{C} | N_\beta > m-1\}. \quad (21)$$

The sets $\mathcal{C}_1$ *and* $\mathcal{C}_3$ *are conjugate to one another: if* $\mathbf{V}_m \in \mathcal{C}_1$, *then* $\mathbf{V}_m^\star \in \mathcal{C}_3$ *and vice versa. Furthermore, set* $\mathcal{C}_2$ *is conjugate to itself: if* $\mathbf{V}_m \in \mathcal{C}_2$, *then* $\mathbf{V}_m^\star = \mathbf{V}_m$.

Note: Table 3 has been given, for each number of output voltage levels m, in ascending order from left to right with respect to the configuration number N_β. Additionally, the colors that are present in Table 3 denote the subsets to which the Configuration Voltage Vectors $\mathbf{V}_m$ belong: green color if $\mathbf{V}_m \in \mathcal{C}_1$, yellow color if $\mathbf{V}_m \in \mathcal{C}_2$, and blue color if $\mathbf{V}_m \in \mathcal{C}_3$. The same color notation has been adopted in Figure 5 to identify the subsets to which the normalized forms $\overline{\overline{\mathbf{V}}}_m$ of the Configuration Voltage Vectors $\mathbf{V}_m$ belong, which are highlighted by the colored ellipses.

The number N_c of Configuration Voltage Vectors $\mathbf{V}_m$ for the case $n = 4$ is $N_c = 407$. Figure 6 shows a graphical representation of the normalized form $\overline{\overline{\mathbf{V}}}_m$ of all the Configuration Voltage Vectors $\mathbf{V}_m$ for the case $n = 4$. The considerations that are introduced in Property 5 and Property 6 also apply to the set of all the Configuration Voltage Vectors $\mathbf{V}_m$ for the cases $n = 4$, $n = 5$, etc.

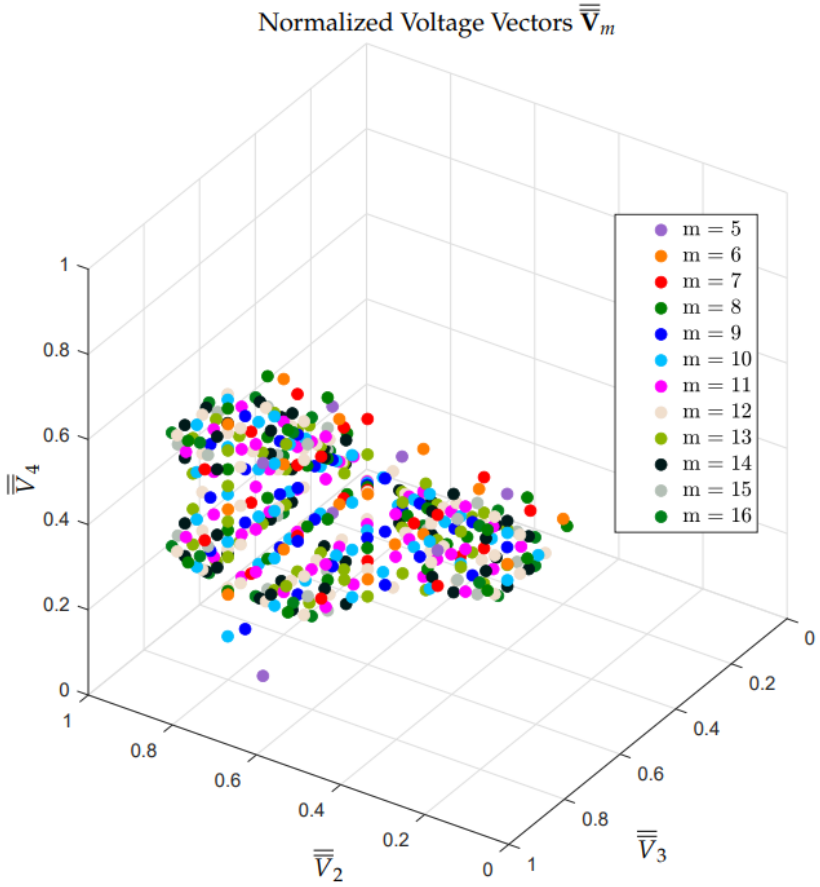
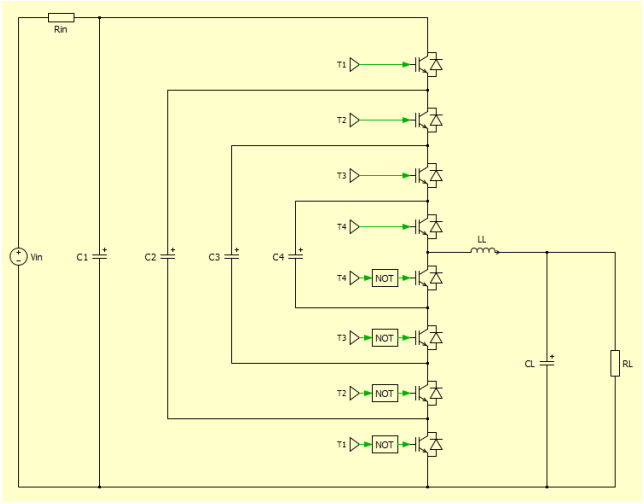


Figure 6. All of the Configuration Voltage Vectors $\mathbf{V}_m$, in normalized form $\overline{\overline{\mathbf{V}}}_m$, for the case $n = 4$.

The number N_c of the Configuration Voltage Vectors $\mathbf{V}_m$ increases very rapidly by increasing n, with a rate faster than exponential: $N_c = 24$ for $n = 3$, $N_c = 407$ for $n = 4$, $N_c = 14252$ for $n = 5$, $N_c = 1044305$ for $n = 6$, etc.

3.4. Model Verification

The model of the multilevel flying-capacitor converter proposed in Figure 4 has been tested in simulation against one of the most well-known platforms for the simulation of power electronics systems, namely PLECS, in order to perform a model verification. For this comparative simulations, the case $n = 4$ and $\mathbf{V}_m = [4\ 3\ 2\ 1]^{\mathrm{T}}$ has been considered to be a case study. Figure 7 reports the PLECS model and the system parameters. The initial and desired voltages for the multilevel converter capacitors can be determined by computing the voltage vector $\mathbf{V}_c$ starting from the configuration voltage vector $\mathbf{V}_m$ and using (13) and (16), namely $\mathbf{V}_c = [100\ 75\ 50\ 25]^{\mathrm{T}}$. The initial conditions of the RLC load are assumed to be equal to zero. The desired voltage V_d is assumed to be sinusoidal with an offset equal to $V_{in}/2$, a peak-to-peak amplitude equal to V_{in} and a frequency equal to 50 Hz. The simulation performed using the PLECS model in Figure 7 and the simulation performed using the Matlab/Simulink POG model in Figure 4 have both been performed applying the Minimum Distance Control described in Section 4.1.



V_{in}	100 [V]
R_{in}	0.1 [mΩ]
C_1	25 [mF]
C_2	33 [mF]
C_3	50 [mF]
C_4	100 [mF]
L_L	19 [mH]
C_L	50 [μF]
R_L	10 [Ω]

Figure 7. PLECS implementation and parameters of the $n = 4$ multilevel flying-capacitor converter.

The results that are given by the PLECS model are shown in Figure 8. The comparison of these results with those given by the Matlab/Simulink POG model is reported in Figure 9.

Figure 8. Simulation results given by the PLECS model: output voltage V_{out} (upper subplot) and filtered voltage across C_L (lower subplot).

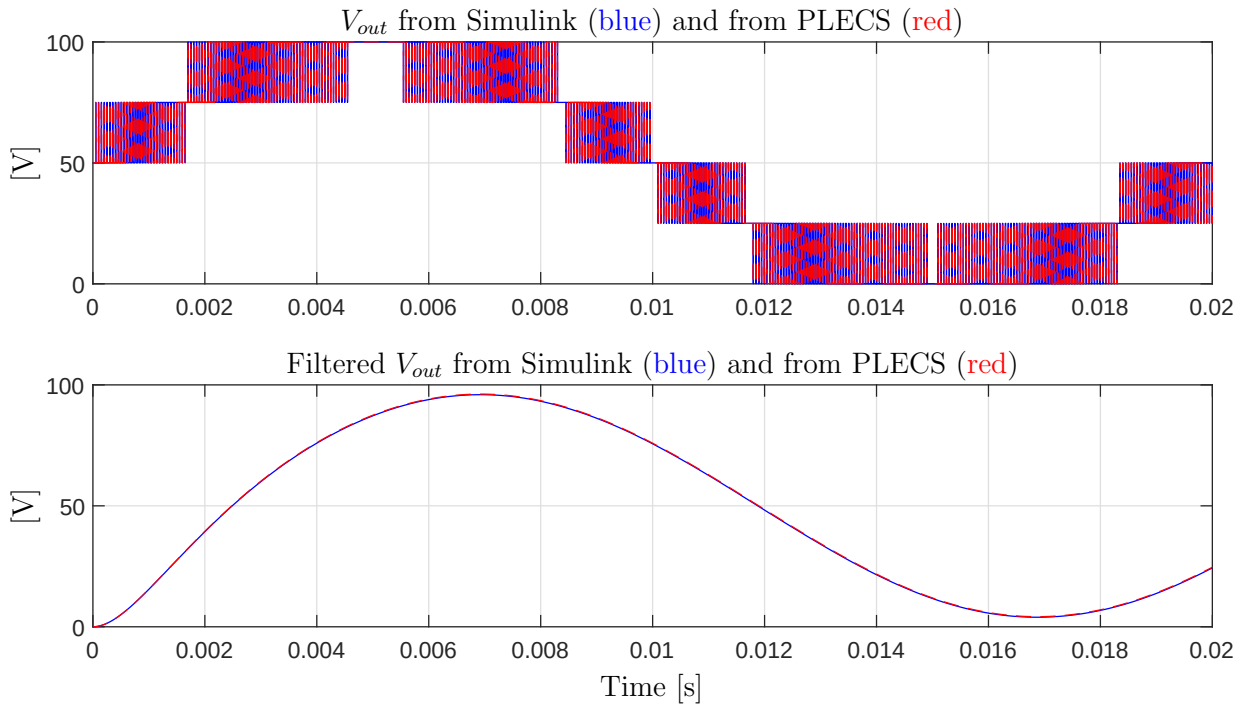


Figure 9. Comparison of the results given by PLECS and Matlab/Simulink: output voltage V_{out} (upper subplot) and filtered voltage across C_L (lower subplot).

The very good matching between the output voltage characteristics that are given by PLECS and by Matlab/Simulink in Figure 9 verifies the correctness of the proposed model of the multilevel flying-capacitor converter.

4. Control of the Multilevel Flying-Capacitor Converter

4.1. Minimum Distance Control

Figure 10 shows the typical scheme of a closed-loop Minimum Distance Control of a Multilevel Flying-Capacitor Converter. The first block of the scheme is the Output Level Generator. Let us consider the case of $m = 6$ output voltage levels, which will, therefore, be equally spaced between level "0" and level "$m - 1 = 5$". The black characteristic in Figure 11 shows the desired normalized voltage $\tilde{V}_d$ multiplied by $m - 1$, in order to see it superimposed to the blue characteristic, namely the *desired output voltage level* α.

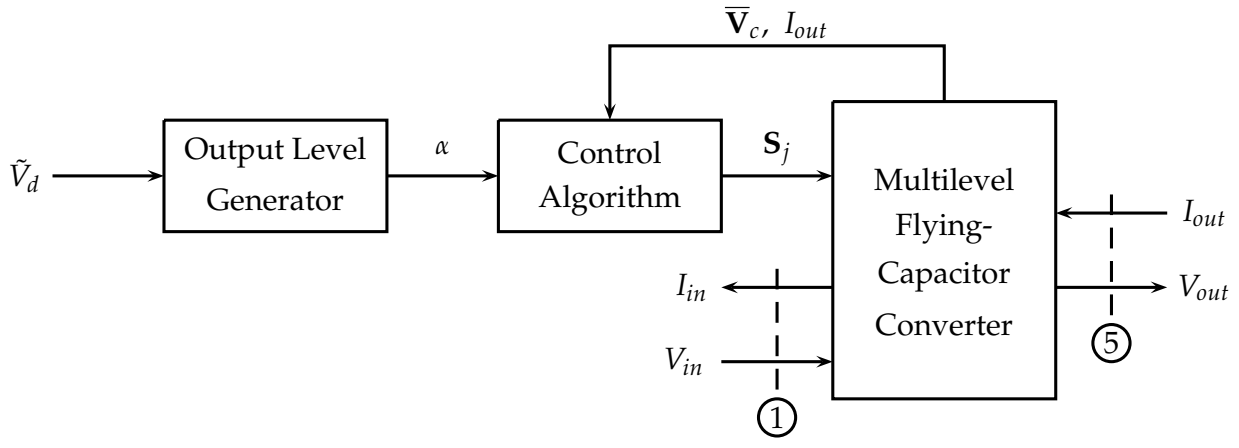


Figure 10. Typical scheme of a closed-loop Minimum Distance Control of a Multilevel Flying-Capacitor Converter.

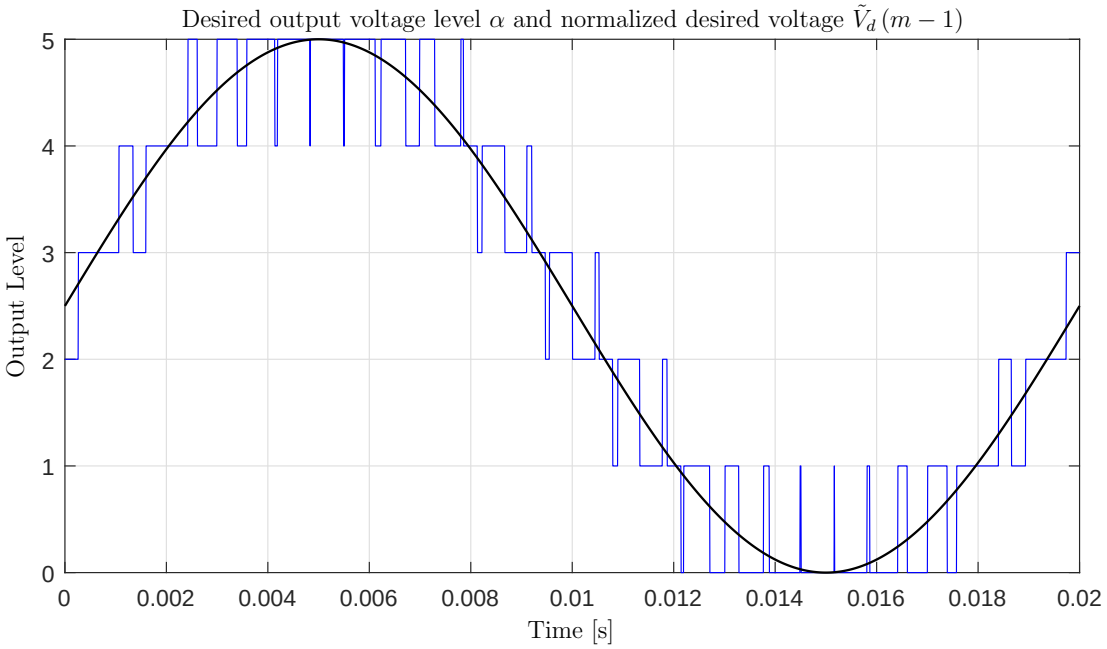


Figure 11. Desired output voltage level α superimposed to normalized desired voltage $\tilde{V}_d\,(m-1)$.

The Output Level Generator generates an integer value $\alpha \in \{0,\ 1,\ \ldots,\ m-1\}$, which defines the desired output level to be applied at a certain time instant t_k:

$$\alpha = \sum_{h=0}^{m-1} (V_d \geq V_{cr_h}),$$

where $(V_d \geq V_{cr_h}) = 1$ if $V_d \geq V_{cr_h}$ and $(V_d \geq V_{cr_h}) = 0$ if $V_d < V_{cr_h}$. The second and third blocks in the scheme of Figure 10 are the Control Algorithm and the Multilevel Flying-Capacitor Converter. The latter is modeled using the POG block scheme that is shown in Figure 4. Indeed, it is possible to notice the correspondence between the power sections ① and ⑤ in Figures 4 and 10. The purpose of the Control Algorithm is to properly generate the Configuration Voltage Vector $\mathbf{S}_j$, which has a one-to-one correspondence with the IGBTs signal vector $\mathbf{T}_j$ through Property 1, giving the desired output level α. This will be accomplished by exploiting the redundance of Configuration Voltage Vectors $\mathbf{S}_j$ generating the same desired output level α when available, as described in the remainder of this section. The Control Algorithm shown in Figure 10 is typically a "Minimum Distance Algorithm". Thanks to the assumption $V_1 = V_{in}$ made in Remark 2, the Minimum Distance algorithm only applies to the components V_2, V_3, ..., V_n of the capacitors voltage vector $\mathbf{V}_c$. Let us denote, as $\overline{\mathbf{V}}_c = \mathbf{V}_c(2:n)$, $\overline{\mathbf{V}}_{m0} = K_m \mathbf{V}_m(2:n) = V_{in}\overline{\overline{\mathbf{V}}}_m$ and $\overline{\mathbf{S}}_{Cj} = -\mathbf{S}_j(2:n)./\mathbf{C}(2:n)$, the following reduced vectors:

$$\overline{\mathbf{V}}_c = \begin{bmatrix} V_2 \\ V_3 \\ \vdots \\ V_n \end{bmatrix}, \qquad \overline{\mathbf{V}}_{m0} = \begin{bmatrix} \frac{V_{in}\beta_{n-1}}{m-1} \\ \frac{V_{in}\beta_{n-2}}{m-1} \\ \vdots \\ \frac{V_{in}\beta_1}{m-1} \end{bmatrix}, \qquad \overline{\mathbf{S}}_{Cj} = \begin{bmatrix} -\frac{s_{2j}}{C_2} \\ -\frac{s_{3j}}{C_3} \\ \vdots \\ -\frac{s_{nj}}{C_n} \end{bmatrix}, \tag{22}$$

where $\mathbf{V}_m$ is the considered Configuration Voltage Vector that is introduced in (16), and $\mathbf{S}_j$ is the j-th configuration vector defined in (10). The minimum distance algorithm tries to

keep the reduced voltage vector $\overline{\mathbf{V}}_c$ as close as possible to the desired reduced voltage vector $\overline{\mathbf{V}}_{m0}$. Let α be the desired output level to be applied at time t_k and let

$$\mathcal{S}_\alpha = \left\{ j \;\middle|\; j \in [0,\ 1,\ \ldots,\ m_c - 1] \wedge \mathbf{S}_j \mathbf{V}_c = \frac{\alpha V_{in}}{m-1} \right\} \tag{23}$$

be the set of the indexes j of all the configuration vectors $\mathbf{S}_j$, which, for the considered Configuration Voltage Vector $\mathbf{V}_m$, provide the output level α. The Minimum Distance algorithm acts as follows:

1. At instant t_k, read the value of the reduced voltage vector $\overline{\mathbf{V}}_c(t_k)$;
2. For any $j \in \mathcal{S}_\alpha$, compute the new position $\overline{\mathbf{V}}_{cj}(t_k + T_W)$ of the reduced voltage vector $\overline{\mathbf{V}}_c$ at instant $t_k + T_W$, which is due to the application of the configuration vector $\mathbf{S}_j$:

$$\overline{\mathbf{V}}_{cj}(t_k + T_W) = \overline{\mathbf{V}}_c(t_k) + \underbrace{\overline{\mathbf{S}}_{Cj}\, I_{out}\, T_W}_{\Delta\overline{\mathbf{S}}_{Cj}} = \overline{\mathbf{V}}_c(t_k) + \Delta\overline{\mathbf{S}}_{Cj}, \tag{24}$$

   where I_{out} is the value of the output current at instant t_k and T_W is the time for which the configuration vector $\mathbf{S}_j$ is applied.
3. For any $j \in \mathcal{S}_\alpha$, compute the following distance vectors:

$$\Delta\overline{\mathbf{V}}_{cj} = \overline{\mathbf{V}}_{cj}(t_k + T_W) - \overline{\mathbf{V}}_{m0} \tag{25}$$

   between points $\overline{\mathbf{V}}_{cj}(t_k + T_W)$ and the desired reduced Voltage Vector $\overline{\mathbf{V}}_{m0}$.
4. At instant t_k, apply the configuration vector $\mathbf{S}_{j^*}$, with $j^* \in \mathcal{S}_\alpha$, for which the norm of vectors $\Delta\overline{\mathbf{V}}_{cj}$ is minimized:

$$\mathbf{S}_{j^*} \quad \text{such that} \quad |\Delta\overline{\mathbf{V}}_{cj^*}| \leq |\Delta\overline{\mathbf{V}}_{cj}| \quad \text{for} \quad j \in \mathcal{S}_\alpha. \tag{26}$$

Figure 12 shows a graphical example of how the Minimum Distance algorithm works in the case of $n = 3$, $m = 4$, $\mathbf{V}_m = [\,3\ \ 2\ \ 1\,]^{\mathrm{T}}$ when the desired output level is $\alpha = 1$. In this case, the distance vector $\Delta\overline{\mathbf{V}}_{cj}$ in (25) having the minimum norm is $|\Delta\mathbf{V}_{c4}|$, highlighted in magenta in the figure.

4.2. Basic Configurations

For any n-dimensional multilevel flying-capacitor converter, let us denote, as *Basic Configuration Voltage Vector*, the following Configuration Voltage Vector:

$$\mathbf{V}_m^* = \left[\, m{-}1 \quad m{-}2 \quad \ldots \quad 2 \quad 1 \,\right]^{\mathrm{T}}, \tag{27}$$

occurring when $m = n + 1$.

Property 7. *For any given n, the basic configuration voltage vector $\mathbf{V}_m^*$ is the only configuration voltage vector for which the Minimum Distance algorithm is able to keep the reduced voltage vector $\overline{\mathbf{V}}_c$ in the neighborhood of the desired reduced voltage vector $\overline{\mathbf{V}}_{m0}^*$, for any value of the normalized desired voltage $\tilde{V}_d$ and the output current I_{out}.*

This property holds because the Basic Configuration Voltage Vector $\mathbf{V}_m^*$ is the only one for which the number of possible configurations $\mathbf{S}_j$ that are associated to the two adjacent levels of any desired voltage V_d are sufficient to guarantee that, at each PWM step, the distance between the reduced vector $\mathbf{V}_c$ and the desired reduced voltage vector $\mathbf{V}_{m0}^*$ is decreased for any value of the output current I_{out}. For any other Configuration Voltage Vector $\mathbf{V}_m$, it is always possible to find values for V_d and I_{out} causing the reduced vector $\mathbf{V}_c$ to indefinitely diverge from the desired reduced voltage vector $\mathbf{V}_{m0}$.

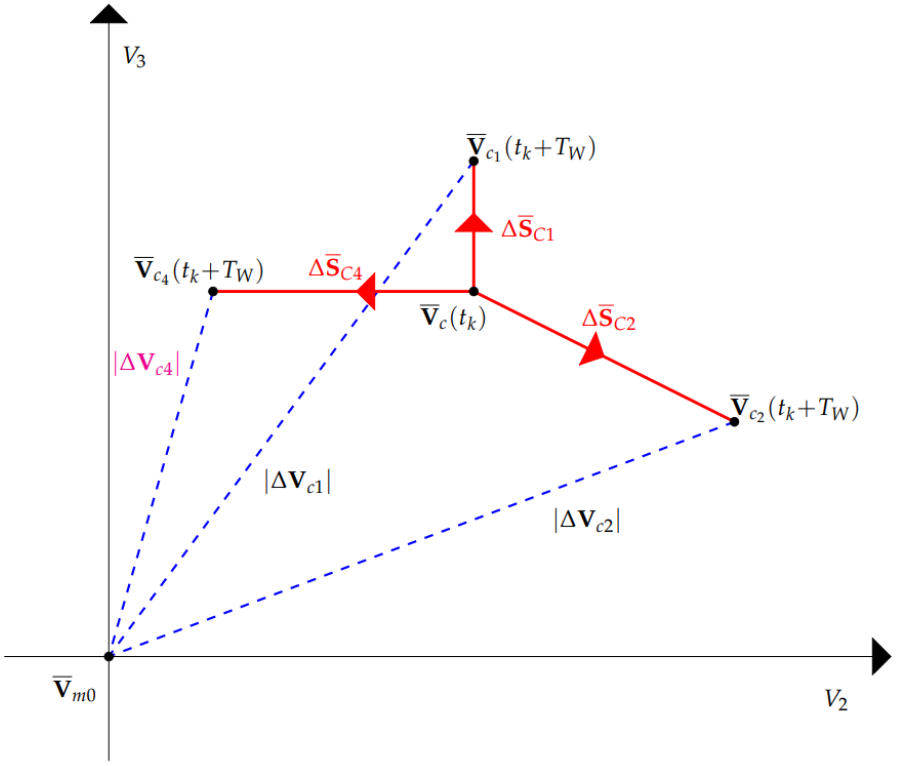


Figure 12. Calculations of the Minimum Distance algorithm in the case of $n = 3$, $m = 4$, $\mathbf{V}_m = [\,3\;\;2\;\;1\,]^{\mathrm{T}}$ when the desired output level is $\alpha = 1$.

Figure 13 shows a first example of the validity of Property 7, for the case $n = 3$ and $\mathbf{V}_m^* = [\,3\;\;2\;\;1\,]^{\mathrm{T}}$. In this figure, a certain number of trajectories in the space (V_2, V_3) starting from initial conditions that are distant from the desired reduced voltage vector $\overline{\mathbf{V}}_{m0}$ are shown. Red asterisks in the figure denote the considered initial conditions. The trajectories have been obtained using the Minimum Distance algorithm and using the following input signals:

$$V_d = \frac{V_{in}}{2} + \frac{V_{in}}{2}\sin(800\pi t), \qquad I_{out} = 10\,A, \qquad V_{in} = 1\,V. \tag{28}$$

The figure clearly shows that all of the trajectories asymptotically tend to the desired reduced voltage vector $\overline{\mathbf{V}}_{m0} = [\,0.66\;\;0.33\,]^{\mathrm{T}}$.

A second similar example is given in Figure 14 for the case $n = 4$ and $\mathbf{V}_m^* = [\,4\;\;3\;\;2\;\;1\,]^{\mathrm{T}}$. The three-dimensional trajectories in the space (V_2, V_3, V_4) have been obtained using the same input signals (28) that were used for the previous example. Even in this case, one can notice that all of the trajectories asymptotically tend to the desired reduced voltage vector $\overline{\mathbf{V}}_{m0} = [\,0.75\;\;0.5\;\;0.25\,]^{\mathrm{T}}$.

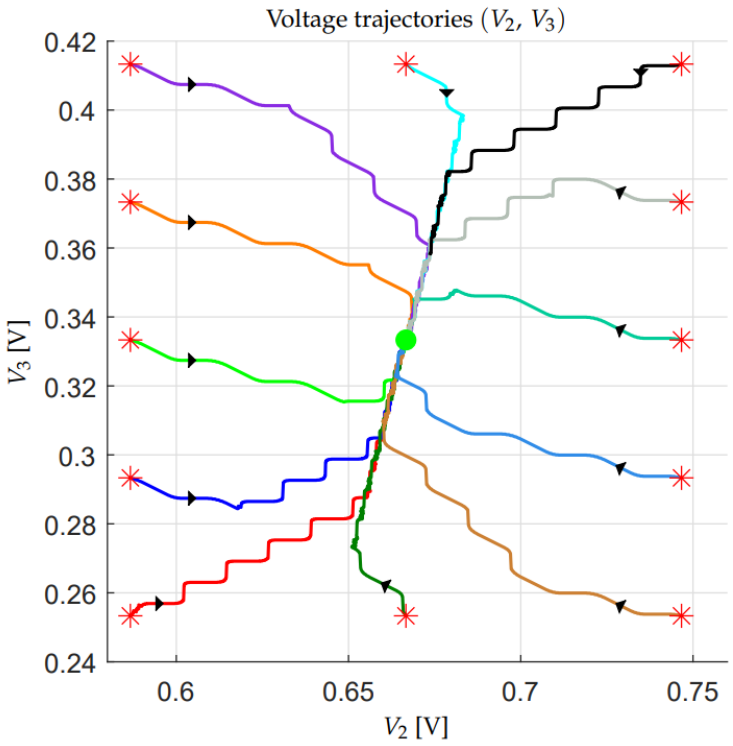


Figure 13. Stability of the Basic Configuration Voltage Vector $\mathbf{V}_m^* = [3\ \ 2\ \ 1]^{\mathrm{T}}$ for $n = 3$.

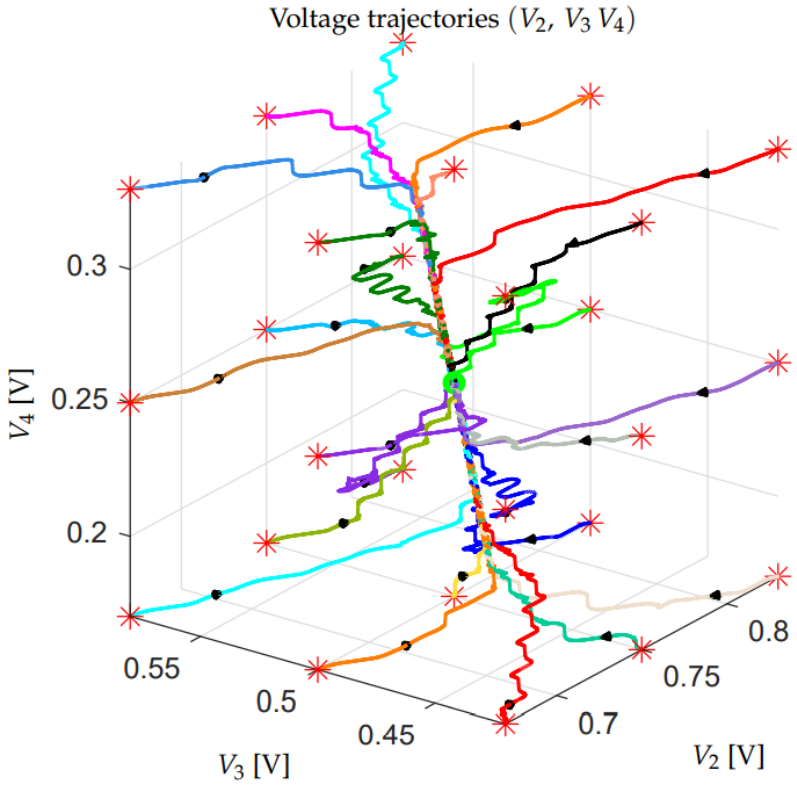


Figure 14. Stability of the Basic Configuration Voltage Vector $\mathbf{V}_m^* = [4\ \ 3\ \ 2\ \ 1]^{\mathrm{T}}$ for $n = 4$.

4.3. Robustness Assessment of the Configuration Voltage Vectors

All of the Configuration Voltage Vectors $\mathbf{V}_m$ different from the basic one $\mathbf{V}_m^*$ are characterized by divergent voltage trajectories under particularly unfavorable operating

conditions, as stated in Property 7. In Figures 15 and 16, for example, the voltage trajectories that are associated with two different Configuration Voltage Vectors $\mathbf{V}_m$ in the space (V_2, V_3) for the case $n = 3$ are reported, starting from different initial conditions that are distant from the desired reduced voltage vector $\overline{\mathbf{V}}_{m0}$. The considered initial conditions are denoted by red asterisks in the figures. The trajectories shown in Figure 15 have been obtained using $\mathbf{V}_m = [5\ 4\ 3]^{\mathrm{T}}$, $\overline{\mathbf{V}}_{m0} = [\ 0.8\ \ 0.6\ ]^{\mathrm{T}}$, $V_d = 0.3\,\mathrm{V}$ and $I_{out} = 10\,\mathrm{A}$. The trajectories in Figure 16 have been obtained using $\mathbf{V}_m = [5\ 3\ 2]^{\mathrm{T}}$, $\overline{\mathbf{V}}_{m0} = [\ 0.6\ \ 0.4\ ]^{\mathrm{T}}$, $V_d = 0.7\,\mathrm{V}$ and $I_{out} = 10\,\mathrm{A}$. In both cases, after a transient, all of the trajectories tend to diverge along a particular direction, which is characteristic of the considered Configuration Voltage Vectors $\mathbf{V}_m$. One can verify that the same qualitative behavior is obtained for any $\mathbf{V}_m$ different from the Basic Configuration Voltage Vector $\mathbf{V}_m^*$.

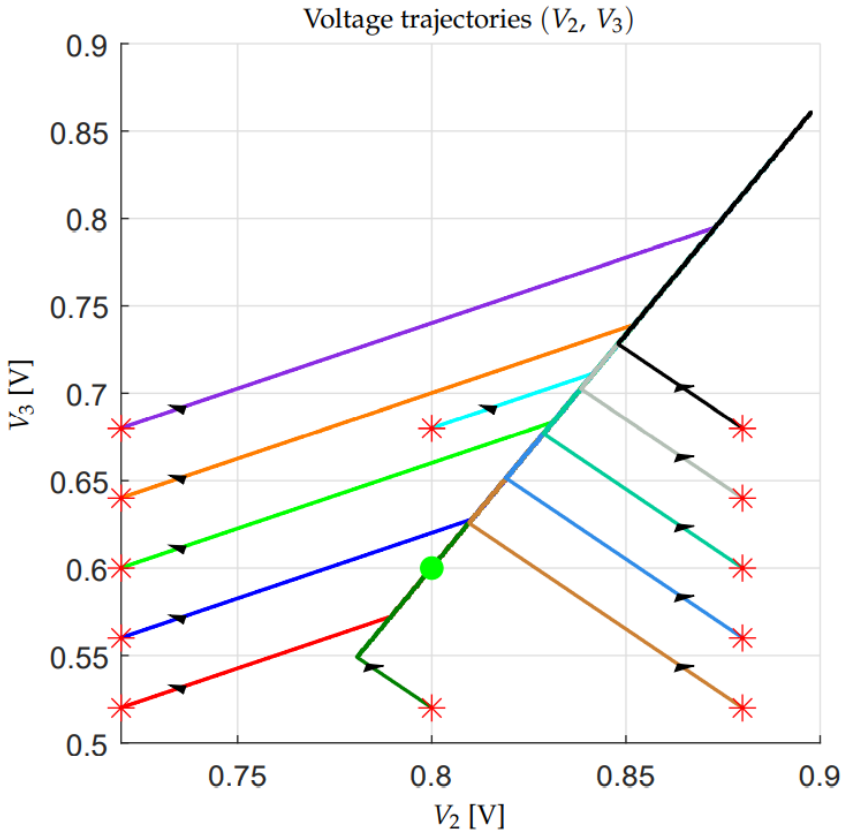


Figure 15. Instability of the Configuration Voltage Vector $\mathbf{V}_m = [5\ 4\ 3]^{\mathrm{T}}$ when $V_d = 0.3$ and $I_{out} = 10\,[\mathrm{A}]$.

From the previous considerations, the need to find a criterion to evaluate the degree of divergence of the different Configuration Voltage Vectors $\mathbf{V}_m$ arises. For this purpose, a *Vectorial Divergence Function* $\overrightarrow{\mathbf{V}}_m(\tilde{V}_d)$ can be defined for each $\mathbf{V}_m$. Before giving the definition of this function, the following preliminary material needs to be introduced.

- Given the Configuration Voltage Vectors $\mathbf{V}_m = [\ m-1\ \ \beta_{n-1}\ \ \ldots\ \ \beta_2\ \ \beta_1\ ]^{\mathrm{T}}$ and the value of the last n-th capacitor C_n, let us choose the values of the remaining $n-1$ capacitors $C_1, C_2, \ldots, C_{n-1}$, as follows:

$$C_1 = \frac{\beta_1 C_n}{m-1}, \qquad C_2 = \frac{\beta_1 C_n}{\beta_{n-1}}, \qquad \ldots, \qquad C_{n-2} = \frac{\beta_1 C_n}{\beta_3}, \qquad C_{n-1} = \frac{\beta_1 C_n}{\beta_2}, \tag{29}$$

namely, each capacitor C_i is chosen inversely proportional to the components of vector $\mathbf{V}_m$.

- The Minimum Distance Algorithm that is given in Section 4.1 can be rewritten in an equivalent form by using the following Matlab-like function "$[\mathbf{S}_j,\ \Delta\overline{\mathbf{V}}] = \mathbf{MDA}(\Delta\overline{\mathbf{V}}, \alpha, I_{out}, T_W)$", which must be called providing $\Delta\overline{\mathbf{V}} = \overline{\mathbf{V}}_c(t_k) - \overline{\mathbf{V}}_{m0}$:

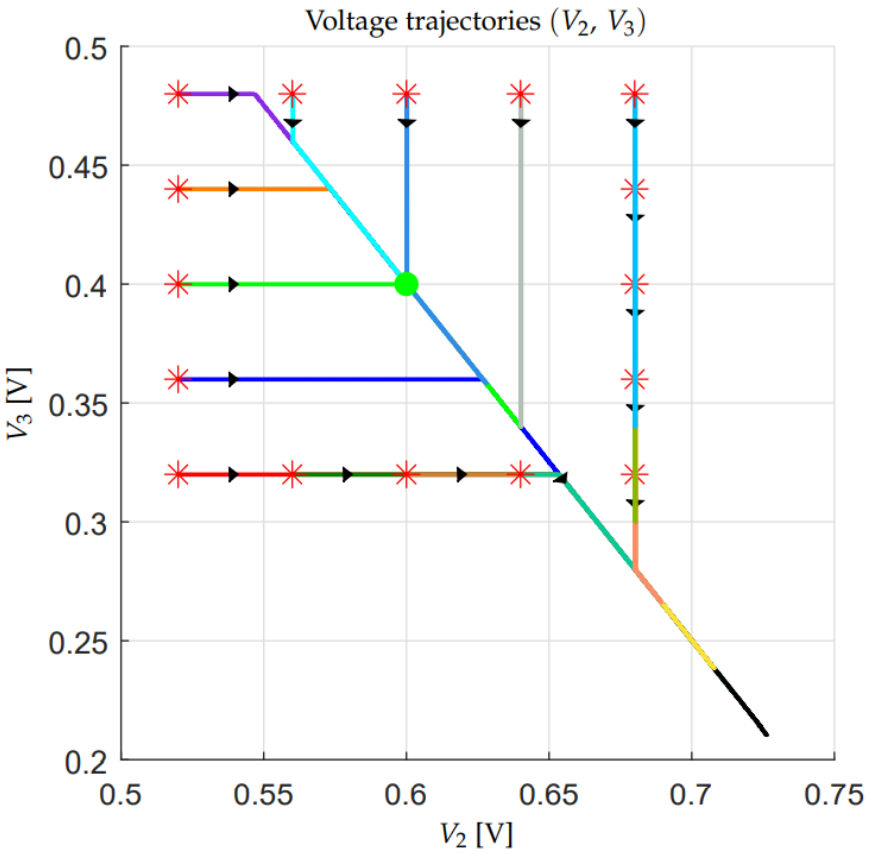


Figure 16. Instability of the Configuration Voltage Vector $\mathbf{V}_m = [5\ 3\ 2]^{\mathrm{T}}$ when $V_d = 0.7$ and $I_{out} = 10$ [A].

---

function $[\mathbf{S}_j,\ \Delta\overline{\mathbf{V}}] = \mathbf{MDA}(\Delta\overline{\mathbf{V}}, \alpha, I_{out}, T_W)$
Compute set $\mathcal{S}_\alpha$ defined in (23);
Compute vectors $\overline{\mathbf{S}}_{Cj}$ defined in (22) using (29);
for $j \in \mathcal{S}_\alpha$
    Compute $\Delta\overline{\mathbf{V}}_{cj}$ as follows, see (25):
    $\Delta\overline{\mathbf{V}}_{cj} = \Delta\overline{\mathbf{V}} + \overline{\mathbf{S}}_{Cj}\, I_{out}\, T_W$;
end
Find $j^* \in \mathcal{S}_\alpha$ for which the norm of vectors $\Delta\overline{\mathbf{V}}_{cj}$ is minimized, as in (26);
Set $\mathbf{S}_j = \mathbf{S}_j^*$;
Set $\Delta\overline{\mathbf{V}} = \Delta\overline{\mathbf{V}}_{cj}^*$;

Definition 2. *Given a Configuration Voltage Vector* $\mathbf{V}_m$*, the corresponding* Vectorial Divergence Function $\overrightarrow{\mathbf{V}}_m(\tilde{V}_d)$ *is defined, by employing a Matlab-like notation, as follows:*

```
I_out = 1;                                   % Function normalized with respect to I_out
T_PWM = 1;                                   % Function normalized with respect to time
C_n = 1;                                     % Function normalized with respect to C_n
for Ṽ_d = (0 : 1/N_Points : 1)               % N_Points of variable Ṽ_d ∈ [0, 1]
    V_D = Ṽ_d(m − 1);                        % N_Points of variable V_D ∈ [0, m − 1]
    α_H = ceil(V_D);                         % Upper adjacent level
    α_L = floor(V_D);                        % Lower adjacent level
    d_c = V_D − α_L;                         % Duty cycle of the upper level
    ΔV̄ = 0;                                  % Zero initial condition
    for h = 1 : N_Steps                      % Repeat N_Steps times
        T_W = d_c T_PWM                      % Time interval of the upper level
        [∼, ΔV̄] = MDA(ΔV̄, α_H, I_out, T_W);  % Upper level Minimum Distance Algorithm
        T_W = (1 − d_c)T_PWM                 % Time interval of the lower level
        [∼, ΔV̄] = MDA(ΔV̄, α_L, I_out, T_W);  % Lower level Minimum Distance Algorithm
    end
    V⃗_m(Ṽ_d) = ΔV̄/N_Steps;                   % Function V⃗_m is defined in point Ṽ_d
end
```

The precision of calculation of function $\overrightarrow{\mathbf{V}}_m(\tilde{V}_d)$ increases if the values of parameters N_{Points} and N_{Steps} increase. The Vectorial Divergence Function $\overrightarrow{\mathbf{V}}_m(\tilde{V}_d)$ satisfies the following properties.

Property 8. *The Vectorial Divergence Function* $\overrightarrow{\mathbf{V}}_m(\tilde{V}_d)$ *of all the Basic Configuration Voltage Vectors* $\mathbf{V}_m^*$ *is zero for any value of variable* $\tilde{V}_d = [0\ \ 1]$*:*

$$\overrightarrow{\mathbf{V}}_m(\tilde{V}_d) = 0 \qquad for \qquad \tilde{V}_d = [0,\ \ 1].$$

This property holds as a direct consequence of Property 7.

Property 9. *The Vectorial Divergence Function* $\overrightarrow{\mathbf{V}}_m(\tilde{V}_d)$ *satisfies the following symmetry with respect to the value* $\tilde{V}_d = 0.5$*:*

$$\overrightarrow{\mathbf{V}}_m(\tilde{V}_d) = -\overrightarrow{\mathbf{V}}_m(1 - \tilde{V}_d), \qquad for \qquad \tilde{V}_d \in [0,\ 0.5].$$

This property holds as a direct consequence of Property 3. Property 9 implies the symmetry of the Vectorial Divergence Function $\overrightarrow{\mathbf{V}}_m(\tilde{V}_d)$ with respect to the origin. Figure 17 gives an example showing two different graphical representations of the Vectorial Divergence Function $\overrightarrow{\mathbf{V}}_m(\tilde{V}_d)$ that is associated with all of the Configuration Voltage Vectors $\mathbf{V}_m$ for the case $n = 3$, $N_{Points} = 400$ and $N_{Steps} = 200$. The left subplot shows the norm $|\overrightarrow{\mathbf{V}}_m(\tilde{V}_d)|$ of the Vectorial Divergence Function versus $\tilde{V}_d \in [0,\ 0.5]$. The function $|\overrightarrow{\mathbf{V}}_m(\tilde{V}_d)|$ has not been plotted for $\tilde{V}_d \in [0.5,\ 1]$, because of the symmetry defined in Property 9. The right subplot of Figure 17 shows the Vectorial Divergence Function $\overrightarrow{\mathbf{V}}_m(\tilde{V}_d)$ on plane $(V_2,\ V_3)$. This subplot clearly shows the symmetry of function $\overrightarrow{\mathbf{V}}_m(\tilde{V}_d)$ with respect to the origin, as stated in Property 9. The two digit numbers "*m.i*", which are present for each characteristic in the two subplots of Figure 17, denote the number m of output levels and the order i of the Configuration Voltage Vector $\mathbf{V}_m$ of the nearby colored line, according to the order and the colors reported in Figure 18. The two subplots of Figure 17 clearly show that the norm $|\overrightarrow{\mathbf{V}}_m(\tilde{V}_d)|$ of the Vectorial Divergence Function $\overrightarrow{\mathbf{V}}_m(\tilde{V}_d)$ tends to increase with the number m of the output levels and, therefore, it can be used as a starting point to estimate the degree of divergence and, thus, the degradation of

the voltage balancing capability, associated to the corresponding Configuration Voltage Vector $\mathbf{V}_m$. For this purpose, let us define the following Divergence Index.

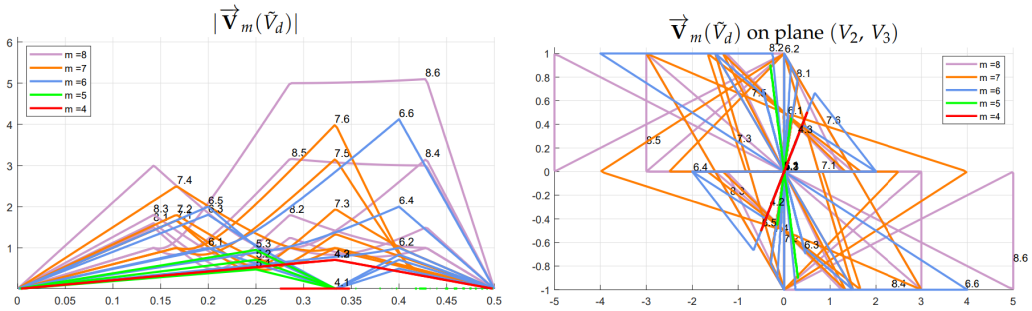


Figure 17. Left subplot: Norm $|\vec{\mathbf{V}}_m(\tilde{V}_d)|$ of the Vectorial Divergence Function vs $\tilde{V}_d \in [0, 0.5]$; **Right** subplot: Vectorial Divergence Function $\vec{\mathbf{V}}_m(\tilde{V}_d)$ on the plane (V_2, V_3) for all of the Configuration Voltage Vectors $\mathbf{V}_m$ in the case $n = 3$.

Definition 3. *The* Divergence Index I_M *of a Configuration Voltage Vector* $\mathbf{V}_m$ *is defined as follows:*

$$I_M = \max\left(|\vec{\mathbf{V}}_m(\tilde{V}_d)|\right),$$

namely as the maximum value of the norm $|\vec{\mathbf{V}}_m(\tilde{V}_d)|$ *of the Vectorial Divergence Function* $\vec{\mathbf{V}}_m(\tilde{V}_d)$.

The larger the Divergence Index I_M, the less robust is the corresponding Configuration Voltage Vector $\mathbf{V}_m$. *Therefore, the Divergence Index* I_M *is inversely proportional to the degree of robustness of the corresponding Configuration Voltage Vector* $\mathbf{V}_m$. For all of the Basic Configuration Voltage Vectors $\mathbf{V}_m^*$, the Divergence Index I_M is zero, according to Property 8. Index I_M can also be used to provide a new sorting for the Configuration Voltage Vectors $\mathbf{V}_m$ having the same number m of output levels. Figure 18 shows the new sorting, in ascending order of the Divergence Index I_M for each vector $\mathbf{V}_m$ having the same number m of output voltage levels. Therefore, the different Configuration Voltage Vectors $\mathbf{V}_m$ having the same number m of output levels are sorted in decreasing degree of robustness when moving from left to right in Figure 18. The magenta line that is reported in Figure 18 is the *Mean Index* I_m of the Configuration Voltage Vectors $\mathbf{V}_m$. The *Mean Index* I_m is defined as the mean value of the norm $|\vec{\mathbf{V}}_m(\tilde{V}_d)|$ of the Vectorial Divergence Function $\vec{\mathbf{V}}_m(\tilde{V}_d)$: $I_m = \text{mean}\left(|\vec{\mathbf{V}}_m(\tilde{V}_d)|\right)$. Figure 18 clearly shows a strong correlation between the *Divergence Index* I_M and *Mean Index* I_m.

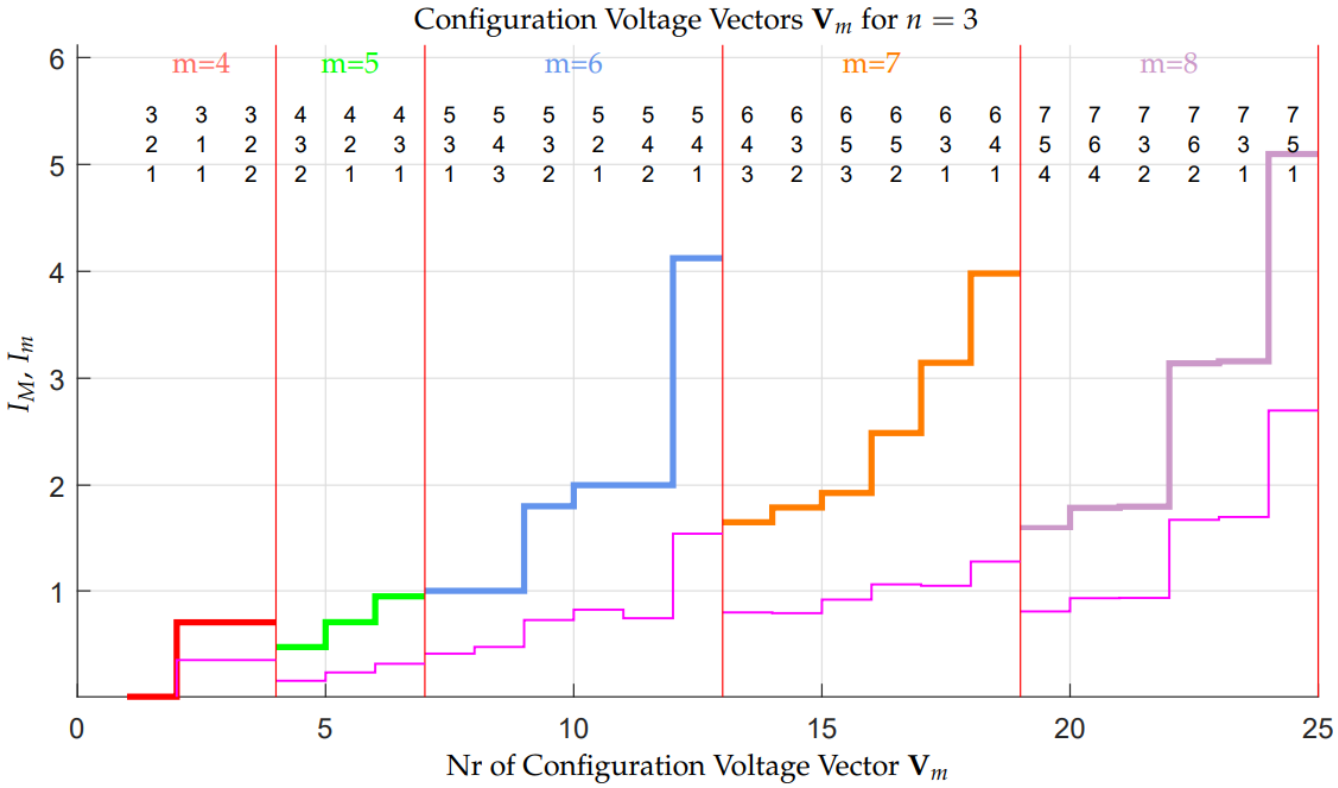


Figure 18. Configuration Voltage Vectors $\mathbf{V}_m$, for $n = 3$, sorted in ascending order with respect to the Divergence Index I_M.

In order to verify the correctness of the sorting proposed in Figure 18, all of the Configuration Voltage Vectors $\mathbf{V}_m$, for $n = 3$, have been tested in simulation using the three types of voltage signals V_d that are shown in Figure 19 (sinusoidal, triangular, and sawtooth) with $V_{in} = 1\,\mathrm{V}$, an offset equal to $V_{in}/2$, a peak-to-peak amplitude equal to V_{in}, a frequency equal to 50 Hz, an output current equal to $I_{out} = 1\,\mathrm{A}$, and capacitors C_i chosen as in (29) with $C_n = 1\,\mathrm{F}$. Figure 20 shows the results of these simulations, where the Divergence Index I_M (red characteristic, left vertical axis) is compared with the maximum norm $\max(|\Delta\overline{\mathbf{V}}|)$ of vectors $\Delta\overline{\mathbf{V}} = \overline{\mathbf{V}}_c(t) - \overline{\mathbf{V}}_{m0}$ obtained in simulation for the three types of the considered periodical signals (colored characteristics, right vertical axis). Two different reference axes have been used in Figure 20, because the Vectorial Divergence Function $\overrightarrow{\mathbf{V}}_m(\tilde{V}_d)$ and corresponding Divergence Index I_M have been computed using a constant normalized voltage $\tilde{V}_d \in [0, 1]$, whereas the maximum norms $\max(|\Delta\overline{\mathbf{V}}|)$ have been obtained in simulation using different signals, i.e., periodical normalized signals $\tilde{V}_d$ with a non-zero frequency of 50 Hz. It can be shown that the two quantities I_M and $\max(|\Delta\overline{\mathbf{V}}|)$ would tend to be comparable only if the frequency of the periodical normalized signals $\tilde{V}_d$ became equal to zero. Consequently, *the Divergence Index I_M represents an upper boundary for the maximum norm index* $\max(|\Delta\overline{\mathbf{V}}|)$*, for each Configuration Voltage Vector* $\mathbf{V}_m$. Furthermore, Figure 20 shows the good direct proportionality existing between the Divergence Index I_M and the maximum norm indices $\max(|\Delta\overline{\mathbf{V}}|)$ of the three considered signals. This good proportionality shows the effectiveness of using the Divergence Index I_M for evaluating the divergence characteristics of the different Configuration Voltage Vectors $\mathbf{V}_m$, which gives a direct measurement of their degree of robustness.

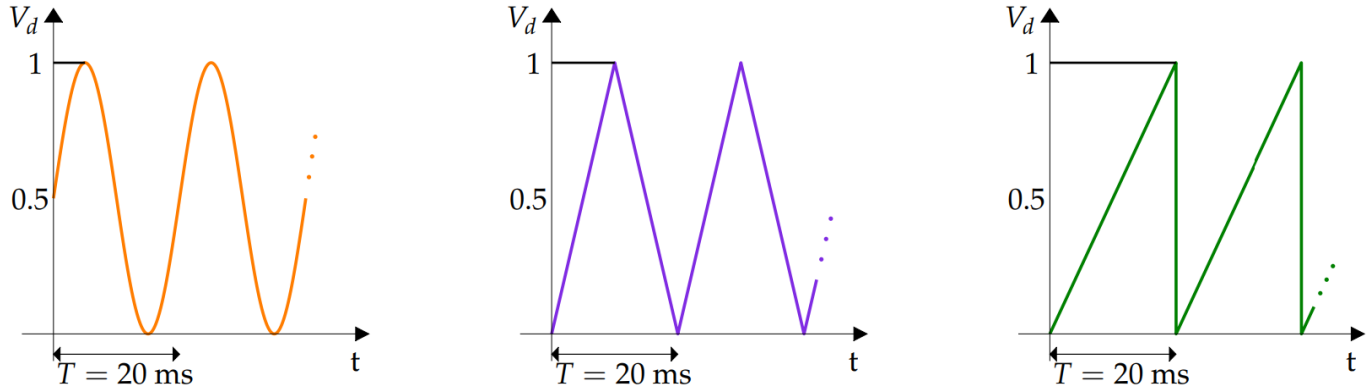


Figure 19. Desired voltage signals V_d for the comparisons in Figures 20 and 21.

Even for the case $n = 4$, all the Configuration Voltage Vectors $\mathbf{V}_m$ have been tested in simulation by employing the same normalized periodical signals $\tilde{V}_d$ used for the case $n = 3$, which are shown in Figure 19. Figure 21 reports the results of these simulations and the comparison between the Divergence Index I_M (red characteristic, left vertical axis) and the maximum norm indices $\max(|\Delta\overline{\mathbf{V}}|)$ (colored lines, right vertical axis). In this figure, the 407 Configuration Voltage Vectors $\mathbf{V}_m$ of case $n = 4$ have been sorted with respect to the Divergence Index I_M. The upper part of the figure shows, for each $m \in [5, 6, \ldots, 16]$, the Configuration Voltage Vector $\mathbf{V}_m$ having the minimum Divergence Index I_M. The simulation results that are reported in Figure 21 show the good direct proportionality existing between the Divergence Index I_M and the maximum norm indices $\max(|\Delta\overline{\mathbf{V}}|)$, even in the case $n = 4$, and, therefore, the effectiveness of using the Divergence Index I_M for evaluating the divergence characteristics, i.e., the degree of robustness, of the different Configuration Voltage Vectors $\mathbf{V}_m$.

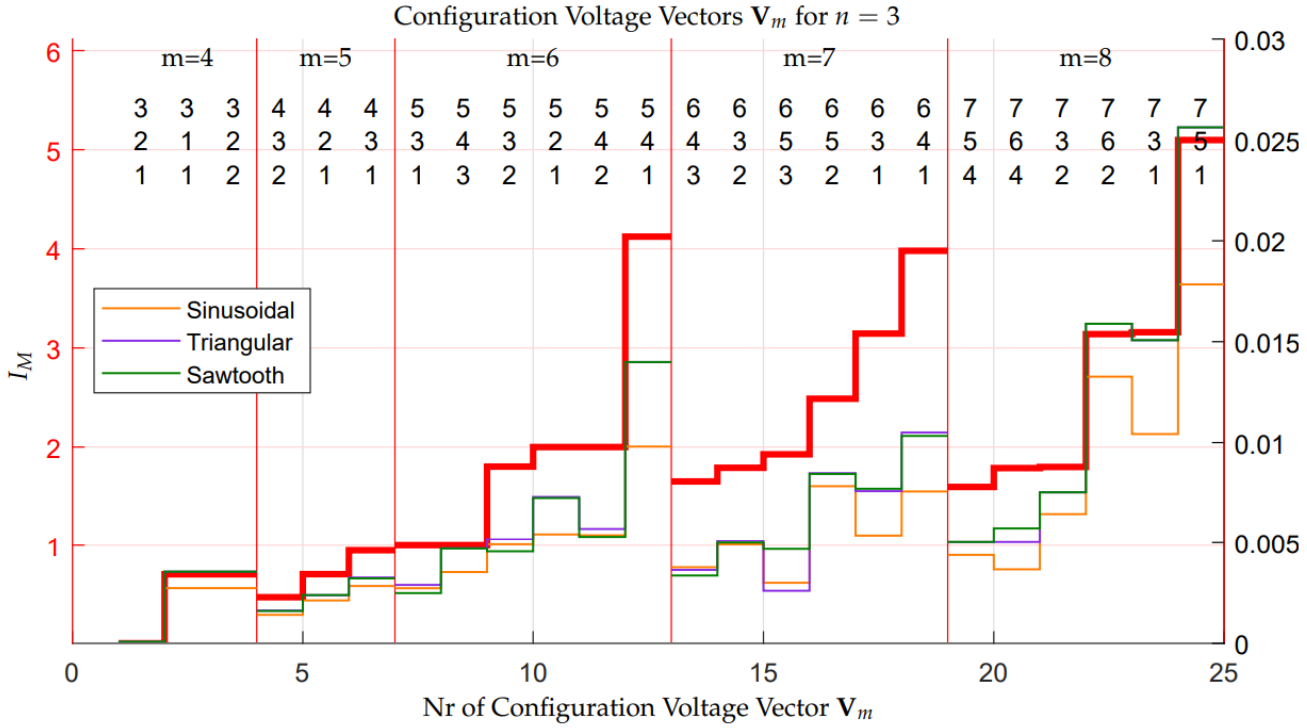


Figure 20. Comparison between the Divergence Index I_M and metric $\max(\Delta\overline{\mathbf{V}})$, computed from simulation using three different $\tilde{V}_d$ signals, for the Configuration Voltage Vectors $\mathbf{V}_m$ in the case $n = 3$.

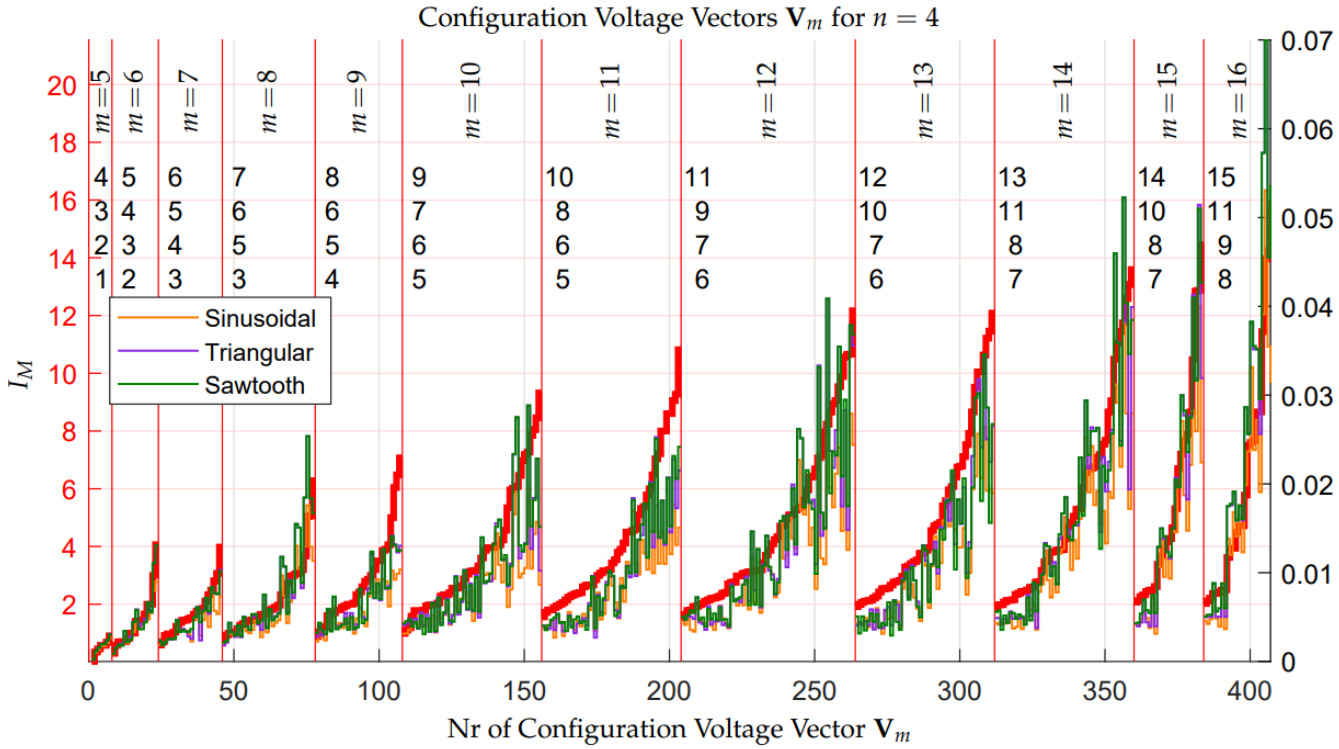


Figure 21. Comparison between the Divergence Index I_M and metric $\max(\Delta\overline{\mathbf{V}})$, computed from simulation using three different $\tilde{V}_d$ signals, for the Configuration Voltage Vectors $\mathbf{V}_m$ in the case $n = 4$.

4.3.1. Minimum Distance Control: Stability Issues in Extended Operation

The analysis performed on the basis of the Vectorial Divergence Function $\overrightarrow{\mathbf{V}}_m(\tilde{V}_d)$ has shown that all of the Configuration Voltage Vectors $\mathbf{V}_m$, other than the basic one $\mathbf{V}_m^*$, are unstable with different degrees of divergence in some unfavorable conditions, such as constant desired voltage $\tilde{V}_d$, while using the Minimum Distance algorithm. Moreover, Figures 20 and 21 have shown that, for some periodical desired signal $\tilde{V}_d$ with an average value equal to 0.5, the maximum distance $\max(\Delta\overline{\mathbf{V}})$ of the voltage vector $\overline{\mathbf{V}}_c$ from the desired voltage vector $\overline{\mathbf{V}}_{m0}$ remains bounded. The amplitude of the maximum distance $\max(\Delta\overline{\mathbf{V}})$ increases if the output current I_{out} increases, and it decreases if capacitor C_n or the frequency of the periodical signal $\tilde{V}_d$ increase.

If $\overline{\mathbf{V}}_c$ remains in the vicinity of the desired voltage vector $\overline{\mathbf{V}}_{m0}$, then the multilevel converter works properly, providing an output signal V_{out} switching between equally spaced voltage values. On the contrary, if the maximum distance $\max(\Delta\overline{\mathbf{V}})$ increases excessively, then the output values $\mathbf{S}_M\mathbf{V}_c$ of the multilevel converter will no longer be equally spaced and the average value of the output switching signal V_{out} will no longer be equal to the desired signal $V_{in}\tilde{V}_d$. If this situation occurs, the multilevel converter cannot work properly, because it provides output signals that are not equal to the desired ones. The output voltage error $V_{err} = V_{out} - V_{in}\tilde{V}_d$ remains low and, therefore, acceptable, only if the maximum distance $\max(\Delta\overline{\mathbf{V}})$ remains sufficiently low. Unfortunately, in practical applications, such as the electric motors control, it can happen that the desired voltage vector $\tilde{V}_d$ does not have an average value equal to 0.5. In this condition, vector $\overline{\mathbf{V}}_c$ diverges from the desired voltage vector $\overline{\mathbf{V}}_{m0}$, which means that the output voltage error V_{err} increases excessively and the multilevel converter can no longer work correctly. Another destabilizing condition can be identified in a sudden load change. These two scenarios are considered in the following two simulation case studies:

(A) Let us consider the case of a constant output current $I_{out} = 1.1$ A and a sinusoidal desired voltage with an average value that is equal to 0.5: $\tilde{V}_d = 0.5 + 0.5\sin(393\,t)$. Furthermore, the voltage signal is supposed to remain constant at the value $\tilde{V}_d = 0.43$ for a short time interval $t \in [t_1 \quad t_2]$, where $t_1 \simeq 32$ ms and $t_2 \simeq 72$ ms. Figure 22 shows the simulation results. The red characteristic in Figure 22 is the desired signal $\tilde{V}_d$, the gray characteristic is the output switching signal V_{out}, whereas the blue characteristic is the average value of the output signal V_{out}. From the figure, it is evident that: (1) in the first part of the simulation, i.e., $t < t_1$, the multilevel converter works correctly, since the output switching levels are equally spaced and, thus, the output voltage error V_{err} is very low; (2) during the second part of the simulation, i.e., $t \in [t_1 \quad t_2]$, the values of the output switching levels change considerably with respect to the desired ones, and they are no longer equally spaced. Therefore, the average value of the output signal V_{out} (blue characteristic) is no longer equal to the desired value $\tilde{V}_d$ (red characteristic); and, (3) in the third part of the simulation, i.e., $t > t_2$, the multilevel converter no longer works correctly, since the output signals (the gray and blue characteristics) are no longer equal to the desired one (the red characteristic). This is due to the fact that the trajectories of the reduced voltage vector $\overline{\mathbf{V}}_c$ have diverged from the desired value $\overline{\mathbf{V}}_{m0}$ because of the constant voltage $\tilde{V}_d$. Moreover, the Minimum Distance algorithm is not able to force the reduced voltage vector $\overline{\mathbf{V}}_c$ to move back towards the desired voltage vector $\overline{\mathbf{V}}_{m0}$ after divergence has occurred.

(B) Let us consider the case of a sinusoidal desired voltage with an average value that is equal to 0.5: $\tilde{V}_d = 0.5 + 0.5\sin(393\,t)$. The load current is supposed to be constant and equal to $I_{out} = 1$ A for $t < t_1 = 0.04$ s. Next, a sudden load change causing a current step is supposed to occur, causing I_{out} to jump from 1 A to 10.5 A for $t_1 \leq t < t_2 = 0.1$ s. The load operating condition giving $I_{out} = 1$ A is supposed to be reestablished for $t \geq t_2$. Figure 23 shows the simulation results. The characteristics color notation is the same as the one adopted in Figure 22. From Figure 23, it is evident that: (1) in the first part of the simulation, i.e., $t < t_1$, the multilevel converter works correctly, since the output switching levels are equally spaced, which means that the output voltage error V_{err} is very low; (2) for $t \in [t_1 \quad t_2)$, the values of the output switching levels change with respect to the desired ones, and they are no longer equally spaced; and, (3) for $t \geq t_2$, the output voltage levels remain unequally spaced, due to the divergence of the trajectories of the reduced voltage vector $\overline{\mathbf{V}}_c$ from the desired value $\overline{\mathbf{V}}_{m0}$ caused by the sudden load change. Moreover, the Minimum Distance algorithm is not able to force the reduced voltage vector $\overline{\mathbf{V}}_c$ to move back towards the desired voltage vector $\overline{\mathbf{V}}_{m0}$ after the divergence has occurred.

Unfortunately, situations such as those that are shown in Figures 22 and 23 can happen for all of the Configuration Voltage Vectors $\mathbf{V}_m$, except for the basic one $\mathbf{V}_m^*$. This poses quite a limitation on the operation of the converter in the so-called "Extended Operation", namely for $\mathbf{V}_m \neq \mathbf{V}_m^*$ allowing to generate a number of output voltage levels $m > n + 1$ for the given n, since unpredictable undesired conditions may compromise the correct functioning of the multilevel converter.

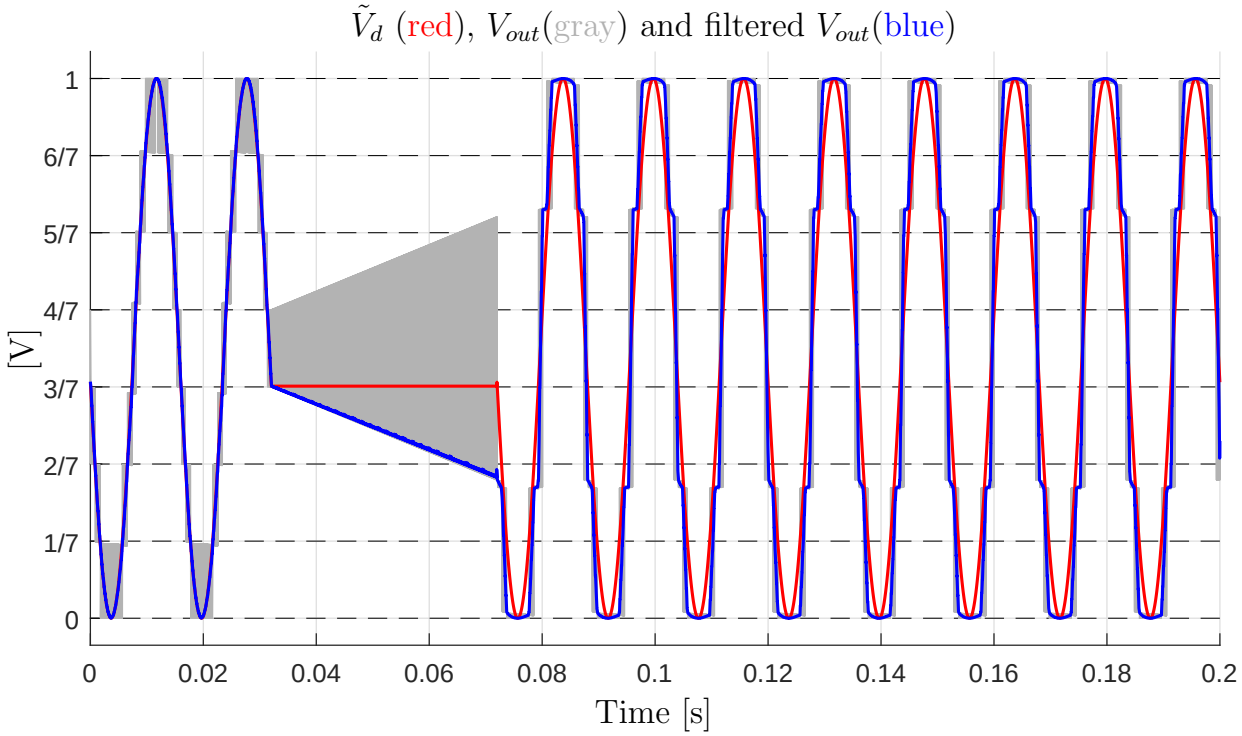


Figure 22. Deformation of the output voltage waveform in the extended operation of the converter with the Configuration Voltage Vector $\mathbf{V}_m = [7\ 6\ 2]^{\mathrm{T}}$ caused by the voltage trajectory divergence in presence of a constant output voltage.

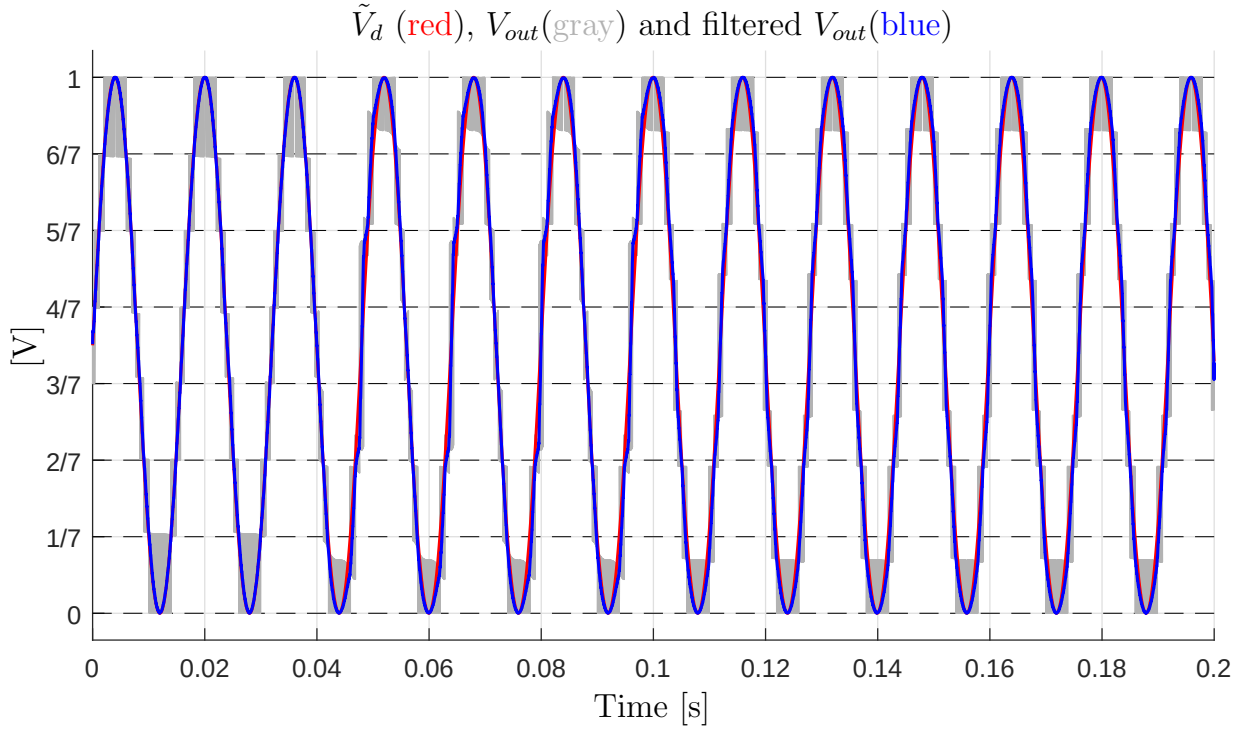


Figure 23. Deformation of the output voltage waveform in the extended operation of the converter with the Configuration Voltage Vector $\mathbf{V}_m = [7\ 6\ 2]^{\mathrm{T}}$ caused by the voltage trajectory divergence in presence of a sudden load change.

4.4. Variable-Step Control of the Multilevel Flying-Capacitor Converter

To cope with the divergence problem described in the previous section, the use of a new solution based on the PWM physical scheme that is shown in Figure 24 is proposed.

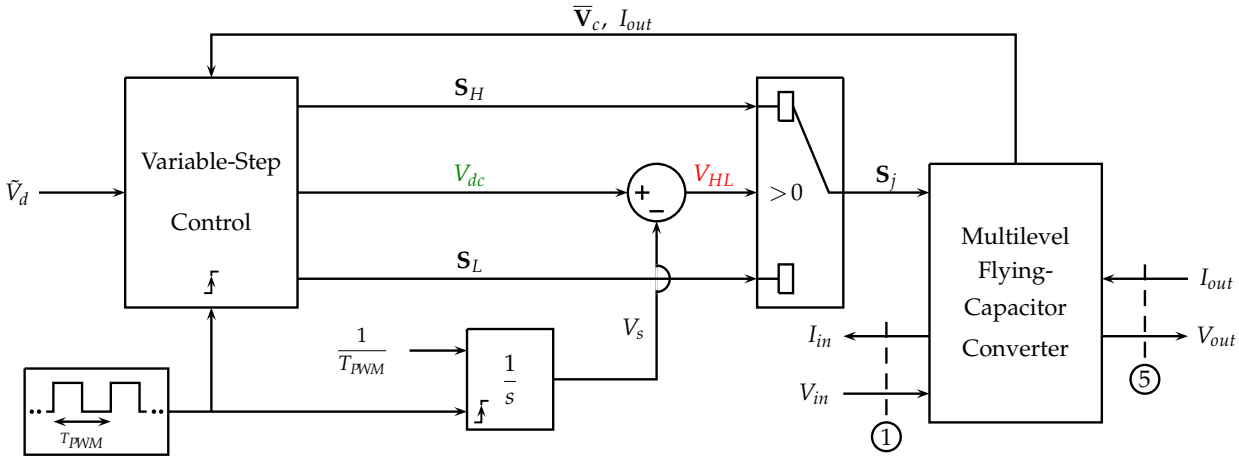


Figure 24. PWM physical scheme and Variable-Step Control of the Multilevel Flying-Capacitor Converter.

The basic elements of the new PWM scheme are the following:

(a) a square wave signal having period T_{PWM} acting as a clock, which activates the Variable-Step Control and resets the integrator to the zero initial condition when the rising edge occurs;

(b) an integrator with a constant input $\frac{1}{T_{PWM}}$ and a reset signal that is timed by the square clock. The output V_s of the integrator is a sawtooth signal which ranges from 0 to 1 within a time interval $t \in [t_r, t_r + T_{PWM}]$, where t_r is the reset time instant, see the black line in Figure 25;

(c) the voltage V_{dc} that is provided by the Variable-Step Control block, defining the duty cycle of the high level of the PWM signal, namely the time interval T_H, see the green line in Figure 25;

(d) the value of the signal $V_{HL} = V_{dc} - V_s$ determines the output of the selector and, thus, the configuration vector $\mathbf{S}_j$, which is going to be applied to the multilevel converter during the next time interval: $\mathbf{S}_j = \mathbf{S}_H$ for a time interval T_H if $V_{HL} > 0$ and $\mathbf{S}_j = \mathbf{S}_L$ for a time interval $T_{PWM} - T_H$ if $V_{HL} < 0$;

(e) at each activation time, the Variable-Step Control reads the input signal $\tilde{V}_d$ and generates three output signals: $\mathbf{S}_H$, V_{dc} and $\mathbf{S}_L$. Using these signals, the Variable-Step Algorithm can decide the duty cycle d_c and the two levels $\mathbf{S}_H\mathbf{V}_c$ and $\mathbf{S}_L\mathbf{V}_c$ of the next PWM period;

(f) let $V_H > V_d$ denote the voltage corresponding to configuration vector $\mathbf{S}_H$ and $V_L < V_d$ denote the voltage corresponding to configuration vector $\mathbf{S}_L$. The duty cycle $d_c = T_H / T_{PWM}$ of the next PWM period, that is the ratio between the duration T_H of the higher level and the duration of the PWM period T_{PWM}, can be computed, as follows:

$$V_d = V_H\, d_c + V_L(1 - d_c) \qquad \leftrightarrow \qquad d_c = \frac{V_d - V_L}{V_H - V_L}. \tag{30}$$

Using (30), the duty cycle d_c always guarantees that the average value of the PWM output voltage in the next period T_{PWM} is equal to the desired value V_d.

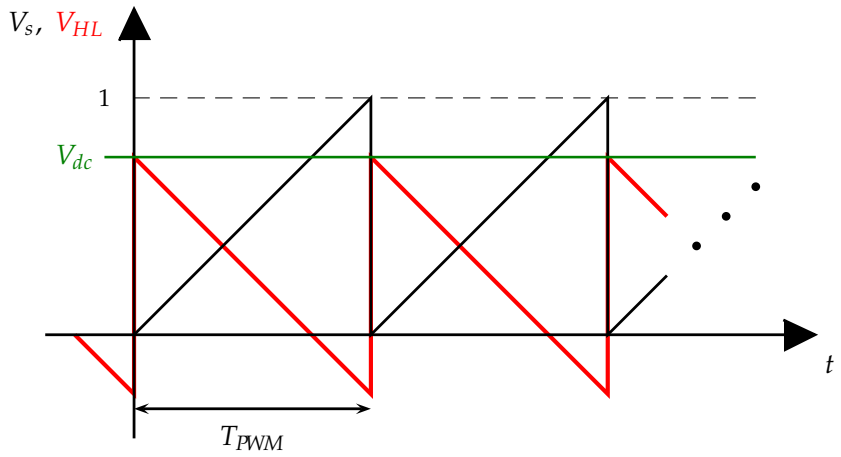


Figure 25. Scheme for the application of the configuration vectors $\mathbf{S}_{j_H}$ and $\mathbf{S}_{j_L}$ associated with the higher and lower level time intervals T_H and $T_{PWM} - T_H$.

Figure 26 provides the basic structure of the Variable-Step Control algorithm by means of a Matlab-like function called "**Multi_Step_Algorithm**$(\cdots)$". This function is called at each activation time providing the following input parameters: $\Delta\overline{\mathbf{V}}$, $\tilde{V}_d$, I_{out}, T_{PWM}, N_s, V_{r0}. The "Multi_Step_Algorithm" attempts to keep the reduced voltage vector $\overline{\mathbf{V}}_c$ as close as possible to the desired reduced voltage vector $\overline{\mathbf{V}}_{m0}$, see (22). The main features of the "Multi_Step_Algorithm" are the following:

function $[\mathbf{S}_H,\ V_{dc},\ \mathbf{S}_L] =$ **Multi_Step_Algorithm**$(\Delta\overline{\mathbf{V}},\ \tilde{V}_d,\ I_{out},\ T_{PWM},\ N_s,\ V_{r0})$

1. $V_D = \tilde{V}_d(m-1)$; % *Variable* $V_D \in [0,\ m-1]$
2. $\alpha_{H0} = \text{ceil}(V_D)$; % *Initial upper adjacent level*
3. $V_{dc} = V_D - \text{floor}(V_D)$; % *Voltage* V_{dc} *in Figure 24 and Figure 25*
4. $N_m = \infty$; % *Initialize minimum norm of* $\Delta\overline{\mathbf{V}}_{cij}$
5. **for** $N_{si} = 1 : N_s$ % N_{si} *is the amplitude of the Step*
6. **for** $k = 0 : N_{si} - 1$ % *k is the up and down Shift*
7. $\alpha_H = \alpha_{H0} + k; \quad \alpha_L = \alpha_H - N_{si}$; % *Current levels* α_H *and* α_L
8. Compute the new duty cycle d_c; % *As in (30)*
9. **if** $(\alpha_H < m)\&\&(\alpha_L \geq 0)$ % α_H, α_L *must not exceed boundaries*
10. Compute sets $\mathcal{S}_{\alpha_H}$ and $\mathcal{S}_{\alpha_L}$; % *Defined in (23)*
11. Compute vectors $\overline{\mathbf{S}}_{CHi}$ and $\overline{\mathbf{S}}_{CLj}$; % *Defined in (22)*
12. **for** $i \in \mathcal{S}_{\alpha_H}$ % *Cycle over indexes in* $\mathcal{S}_{\alpha_H}$
13. **for** $j \in \mathcal{S}_{\alpha_L}$ % *Cycle over indexes in* $\mathcal{S}_{\alpha_L}$
14. $\Delta\overline{\mathbf{V}}_{cij} = \Delta\overline{\mathbf{V}} + [\overline{\mathbf{S}}_{CHi}\, d_c + \overline{\mathbf{S}}_{CLj}(1-d_c)]\, I_{out}\, T_{PWM}$; % *Distance vector*
15. **if** $\text{norm}(\Delta\overline{\mathbf{V}}_{cij}) < N_m$ % *If* $|\Delta\overline{\mathbf{V}}_{cij}| <$ *current minimum*
16. $N_m = \text{norm}(\Delta\overline{\mathbf{V}}_{cij})$; % *Set* N_m *to the current one*
17. Set: $\mathbf{S}_H = \mathbf{S}_i; \quad \mathbf{S}_L = \mathbf{S}_j; \quad V_{dc} = d_c$; % *Set the outputs*
18. **end**
19. **end**
20. **end**
21. **end**
22. **end**
23. **if** $(N_m < \text{norm}(\Delta\overline{\mathbf{V}}))||(N_m < V_{r0}N_{si})$ % $N_m <$ *or* $|\Delta\overline{\mathbf{V}}| <$ *hypersphere radius*
24. **return** % *Exit from the algorithm*
25. **end**
26. **end**

Figure 26. Matlab-like form of the Variable-Step Control algorithm.

- At each activation time t_k, the "Multi_Step_Algorithm" computes the two configuration vectors $\mathbf{S}_H$, $\mathbf{S}_L$ and the duty cycle V_{dc} to be applied in the following PWM time interval $[t_k \quad t_k + T_{PWM}]$: configuration $\mathbf{S}_H$ will be applied in the first part of the PWM period when $V_{HL} = V_{dc} - V_s > 0$, while configuration $\mathbf{S}_L$ will be applied in the second part of the PWM period when $V_{HL} < 0$, see Figure 25.
- The input N_s defines the maximum amplitude of the Step to be used in the algorithm, which is the *maximum level-to-level distance*. The **for** cycle at line 5 in Figure 26 defines the current value $N_{si} \in [1,\ 2,\ \ldots,\ N_s]$ of the amplitude of the Step, i.e., the current level-to-level distance. The **for** cycle at line 6 defines the current value k of the up and down shift to be considered for the current amplitude N_{si} of the Step.
- At lines 7 and 8, the current values of the upper level α_H, the lower level α_L, and the duty cycle d_c are computed. If the current values of α_H and α_L are admissible, see condition at line 9, then the sets $\mathcal{S}_{\alpha_H}$ and $\mathcal{S}_{\alpha_L}$ of the admissible configuration vectors $\mathbf{S}_{Hi}$ and $\mathbf{S}_{Lj}$ and the corresponding vectors $\overline{\mathbf{S}}_{CHi}$ and $\overline{\mathbf{S}}_{CLj}$ are computed at lines 10 and 11.
- The two **for** cycles at lines 12 and 13 are used to compute the distance vector $\Delta\overline{\mathbf{V}}_{cij}$ for each possible combination of the configuration vectors $\mathbf{S}_i$ and $\mathbf{S}_j$ belonging to the two sets $\mathcal{S}_{\alpha_H}$ and $\mathcal{S}_{\alpha_L}$. At line 14, the distance vector $\Delta\overline{\mathbf{V}}_{cij}$ is computed starting from the initial condition $\Delta\overline{\mathbf{V}}$ and adding the two terms $\overline{\mathbf{S}}_{CHi}\, d_c I_{out} T_{PWM}$ and $\overline{\mathbf{S}}_{CLj}(1-d_c) I_{out} T_{PWM}$, due to the application of the configuration vectors $\mathbf{S}_{Hi}$ and $\mathbf{S}_{Li}$ in the first part $d_c T_{PWM}$ and in the second part $(1-d_c)T_{PWM}$ of the PWM period T_{PWM}, respectively.
- If the norm of the distance vector $\Delta\overline{\mathbf{V}}_{cij}$ is smaller than the current minimum norm N_m, see line 15, then the algorithm updates the value of parameter N_m, see line 16, and it sets the values of the output variables $\mathbf{S}_H$, $\mathbf{S}_L$ and V_{dc} equal to the values $\mathbf{S}_i$, $\mathbf{S}_j$ and d_c of the current solution, see line 17.
- The "Multi_Step_Algorithm" ends its minimum distance vector search, see line 24, when one of the conditions at line 23 is verified, or when the maximum level-to-level distance N_s has been achieved. At line 23, the algorithm exits the search if the current minimum distance N_m is lower than the initial one, or if N_m is lower than radius $V_{r0}\, N_{si}$, where V_{r0} is the input basic radius and N_{si} is the current level-to-level distance. Radius $V_{r0}\, N_{si}$ represents the varying radius of an hypersphere in the $(n-1)$-dimensional space. Figure 27 shows the resulting circumferences with varying radius $V_{r0}\, N_{si}$ for the case $n = 3$.
- The "Multi_Step_Algorithm" introduces and uses the new concept of "*variable level-to-level distance*". This concept means that the algorithm can choose a higher level α_H and a lower level α_L *that are not adjacent*, see line 7 of the algorithm. The current level-to-level distance is denoted by variable $N_{si} \in [1,\ N_s]$. The new duty cycle d_c associated with the two levels α_H and α_L, computed in line 8, guarantees that the average value of the PWM output voltage in the next PWM period T_{PWM} will be equal to the desired value V_d.
- The ability to change the level-to-level distance allows the "Multi_Step_Algorithm" to keep the reduced voltage vector $\overline{\mathbf{V}}_c$ in the vicinity of the desired voltage vector $\overline{\mathbf{V}}_{m0}$ even in extended operation and in presence of some particularly unfavorable operating conditions, such as normalized desired voltage $\tilde{V}_d$ having an average value different from 0.5.
- If the unfavorable conditions persist, the algorithm can enlarge the level-to-level distance N_{si} up to its upper boundary $N_s = m - 1$. This enlargement increases the number of the configuration vectors $\mathbf{S}_j$ that the algorithm can use to keep vector $\overline{\mathbf{V}}_c$ in the vicinity of the desired vector $\overline{\mathbf{V}}_{m0}$, and to maintain the correct functioning of the multilevel converter. Furthermore, when the unfavorable conditions no longer occur, the "Multi_Step_Algorithm" has the ability to force the converter to go back to work as a normal multilevel converter switching between adjacent levels only, i.e., with a current level-to-level distance N_{si} equal to one.

- The example reported in Figure 28 shows all the possible combinations of levels α_H and α_L that can be obtained when $m = 6$, $N_{si} \in \{1, 2, 3, 4, 5\}$ and the desired voltage $V_D = (m-1)\tilde{V}_d$ is in between levels "2" and "3".

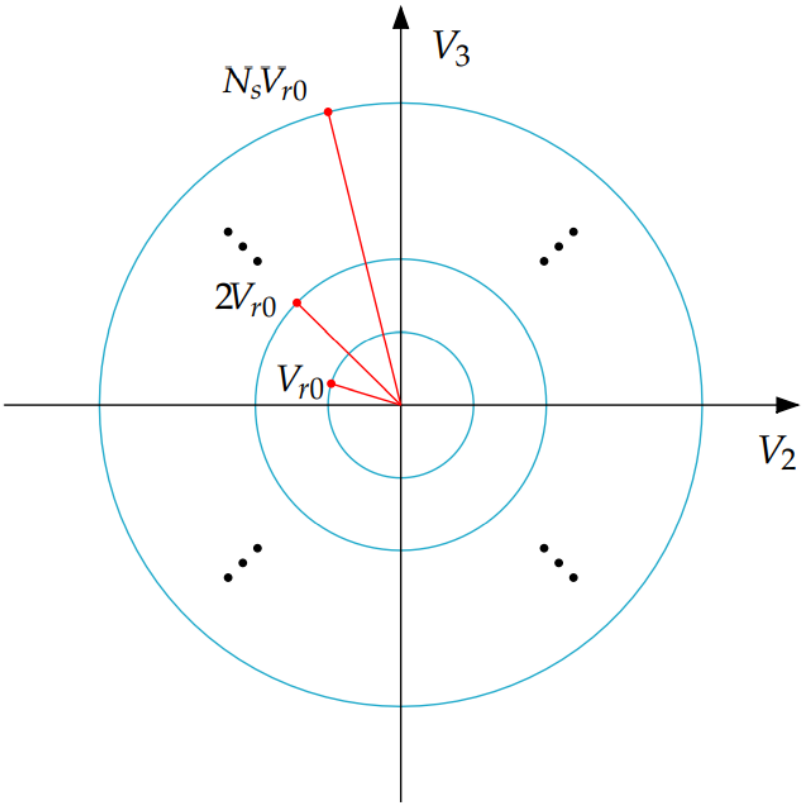


Figure 27. Circumference with varying radius $N_{si}\,V_{r0}$ in the two-dimensional space for the case $n = 3$.

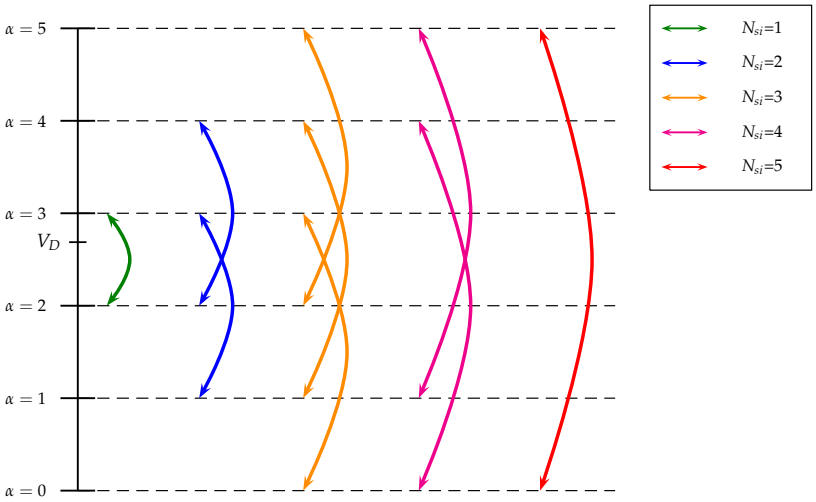


Figure 28. Possible combinations of higher and lower output voltage levels α_H and α_L as a function of the current level-to-level distance N_{si} for the case $m = 6$ and a desired voltage V_D in between "2" and "3".

4.4.1. Variable-Step Control: Solution of the Stability Issues in Extended Operation

Section 4.3.1 has shown that the Minimum Distance Control is not capable of ensuring the correct operation of the multilevel flying-capacitor converter, in extended mode, under particularly unfavorable operating conditions, such as a desired voltage $\tilde{V}_d$, with an average value that is different from 0.5 or a sudden load change. Examples of this type are shown in Figures 22 and 23, respectively. On the contrary, the Variable-Step Control that was presented in the previous section is able to ensure the correct functioning of the multilevel converter, even under unfavorable operating conditions. To give some examples, reference is made to Figures 29 and 30, showing the simulation results obtained using the Variable-Step Control under the same operating conditions as those of the simulations in Figures 22 and 23, respectively, when the Minimum Distance Control was used instead. In Figures 29 and 30, the red characteristic is the desired signal $\tilde{V}_d$, the gray characteristic is the switching output signal V_{out}, and the green characteristic is the average value of the output signal V_{out}.

With reference to Figure 29, it is evident that: (1) in the first part of the simulation, for $t < t_1$, the multilevel converter works correctly in extended operation using the minimum level-to-level distance $N_{si} = 1$ and the output voltage error $V_{err} = V_{out} - V_{in}\tilde{V}_d$ remains low; (2) during the second part of the simulation, for $t \in [t_1 \quad t_2]$, the current level-to-level distance N_{si} increases from 1 to 2, and the gray output variable V_{out} switches between levels $V_L = 2/7$ and $V_H = 4/7$. In this part of the simulation, the effectiveness of the Variable-Step Control comes into play, which prevents vector $\overline{\mathbf{V}}_c$ from diverging excessively from the desired reduced vector $\overline{\mathbf{V}}_{m0}$, even in the presence of the unfavorable condition of a signal $\tilde{V}_d$ constant and different from 0.5. On the other hand, in the simulation of Figure 22, the Minimum Distance Algorithm was not able to prevent the divergence of the vector $\overline{\mathbf{V}}_c$, therefore compromising the correct functioning of the converter; (3) in the third part of the simulation, for $t > t_2$, the operating condition $N_{si} = 2$ is maintained until the distance between vectors $\overline{\mathbf{V}}_c$ and $\overline{\mathbf{V}}_{m0}$ is sufficiently reduced, namely until time instant $t_3 \simeq 176$ ms; and, (4) in the fourth part of the simulation, for $t > t_3$, the converter starts operating as a classical multilevel flying-capacitor converter in extended mode once again, setting the current level-to-level distance N_{si} back to 1. On the other hand, in the simulation of Figure 22, the Minimum Distance Algorithm was not able to force the vector $\overline{\mathbf{V}}_c$ to move back towards the desired vector $\overline{\mathbf{V}}_{m0}$ after the divergence occurred.

With reference to Figure 30, it is evident that: (1) in the first part of the simulation, for $t < t_1$, the multilevel converter works correctly in extended operation using the minimum level-to-level distance $N_{si} = 1$ and the output voltage error $V_{err} = V_{out} - V_{in}\tilde{V}_d$ remains low; (2) for $t \in [t_1 \quad t_2)$, the current level-to-level distance N_{si} increases from 1 to 2, in order to prevent vector $\overline{\mathbf{V}}_c$ from diverging excessively from the desired reduced vector $\overline{\mathbf{V}}_{m0}$ as a consequence of the undesired sudden load change. On the other hand, in the simulation of Figure 23, the Minimum Distance Algorithm was not able to prevent the divergence of the vector $\overline{\mathbf{V}}_c$, therefore compromising the correct functioning of the converter; (3) for $t \geq t_2$, the operating condition $N_{si} = 2$ is maintained until $t = t_3 \simeq 0.1039$ s, namely for the very short time interval that it takes for the distance between vectors $\overline{\mathbf{V}}_c$ and $\overline{\mathbf{V}}_{m0}$ to be sufficiently reduced; and, (4) for $t \geq t_3$, the converter starts operating as a classical multilevel flying-capacitor converter in extended mode once again, setting the current level-to-level distance N_{si} back to 1. On the other hand, in the simulation of Figure 23, the Minimum Distance Algorithm was not able to force the vector $\overline{\mathbf{V}}_c$ to move back towards the desired vector $\overline{\mathbf{V}}_{m0}$ after the divergence occurred.

The simulation results that are reported in Figures 29 and 30 clearly highlight the effectiveness of the proposed Variable-Step Control as compared with the classical Minimum Distance Control. This especially holds in those applications, such as the electric motors control, where it can happen that the desired voltage vector $\tilde{V}_d$ does not have an average value equal to 0.5, or that an undesired sudden load change occurs. At the same time, it is desirable to have the converter operating in extended mode, because of all the advantages in the output voltage quality coming from a larger number of output voltage

levels without increasing the number of capacitors. The proposed Variable-Step Control aims at enabling the multilevel flying-capacitor converter operation in extended mode any time the operating conditions allow it, and it enlarges the level-to-level distance N_{si} only when strictly necessary to prevent the divergence of the flying capacitors voltages.

The Reader is invited to refer to the supplementary material in order to test and compare the Minimum Distance Control algorithm and the Variable-Step Control algorithm [28]. The Simulink model "Multilevel_Flying_Capacitor_Converter_mdl.slx" has been created with Matlab R2020b and it contains the dynamic model of the multilevel flying-capacitor converter with n capacitors given in Figure 4, as well as the implementation of both the Minimum Distance Control and the Variable-Step Control. The two algorithms are implemented in the Matlab functions "Distance_Control_0.m" and "Distance_Control_n.m", respectively. The main script that allows to control the simulations is named "Multilevel_Flying_Capacitor_Converter.m", where the system parameters that the user can set are reported and commented. Note that variables m and m_{ii} in the script "Multilevel_Flying_Capacitor_Converter.m" denote the number m of output levels and the order m_{ii} of the Configuration Voltage Vector $\mathbf{V}_m$, according to the orders that are reported in Figure 20 for the case $n = 3$ and in Figure 21 for the case $n = 4$.

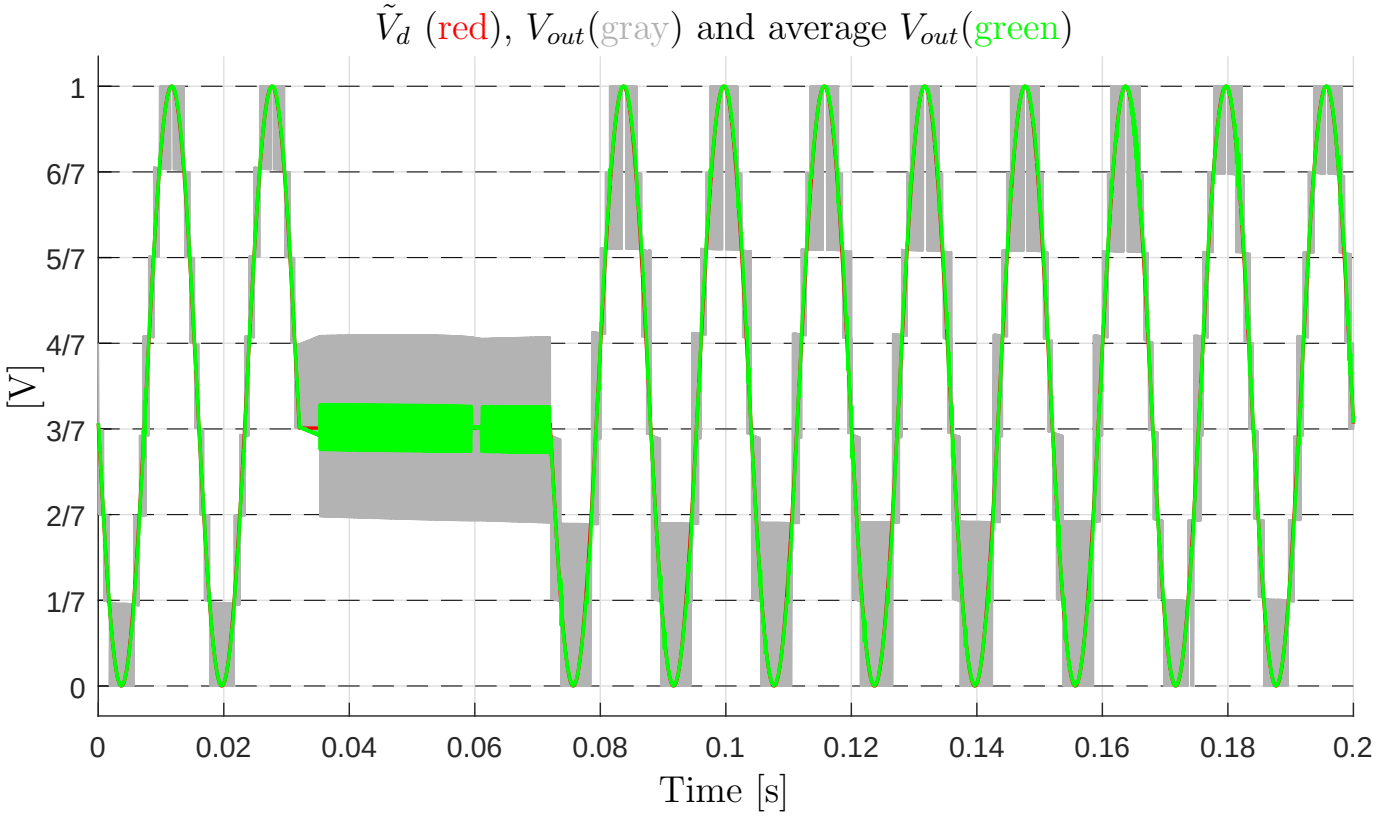


Figure 29. Non-Deformation of the output voltage waveform in the extended operation of the converter with the Configuration Voltage Vector $\mathbf{V}_m = [7\ 6\ 2]^{\mathrm{T}}$, in the presence of a constant output voltage, thanks to the Variable-Step Control.

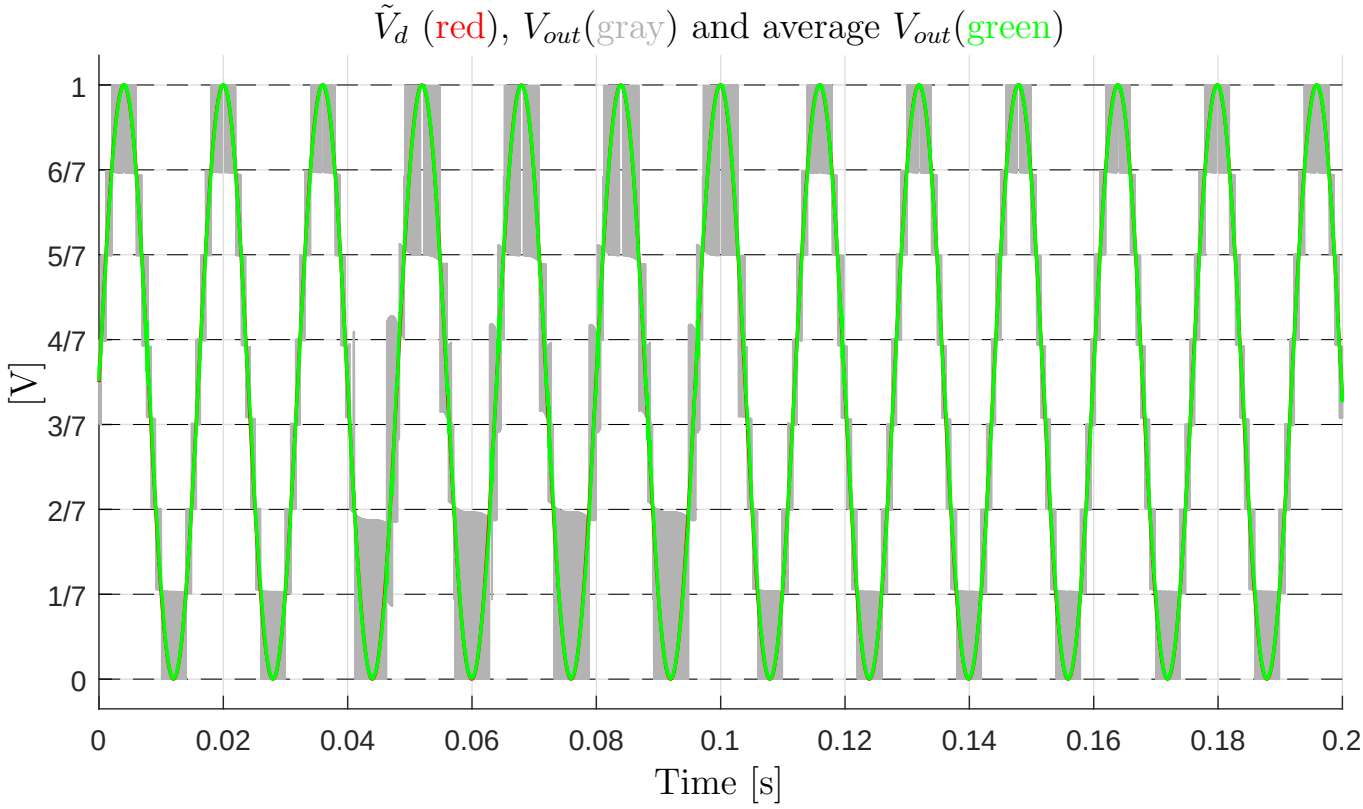


Figure 30. Non-Deformation of the output voltage waveform in the extended operation of the converter with the Configuration Voltage Vector $\mathbf{V}_m = [7\ 6\ 2]^{\mathrm{T}}$, in the presence of a sudden load change, thanks to the Variable-Step Control.

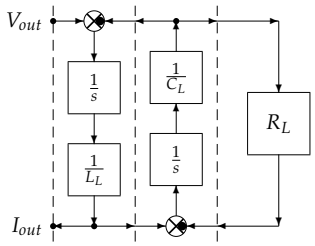
5. Converter Testing with Dynamic Loads

This section deals with the simulation of the multilevel flying-capacitor converter with $n = 3$ in extended operation, while using the Configuration Voltage Vector $\mathbf{V}_m = [5\ 4\ 1]^{\mathrm{T}}$, with several proposed load case studies. The considered load configuration is an RLC circuit, where a capacitor C_L and a resistor R_L are connected in parallel, and their parallel configuration is connected in series to an inductor L_L. The described load can be modeled using the POG block scheme that is shown in Figure 31 on the left. The transfer function $H(s)$ relating the output power variable I_{out} to the input power variable V_{out} is the following:

$$H(s) = \frac{I_{out}(s)}{V_{out}(s)} = \frac{sR_LC_L+1}{s^2R_LC_LL_L+sL_L+R_L}. \tag{31}$$

The parameters values for the considered load case studies are shown in Figure 31 on the right, together with the converter parameters. As far as loads 1, 2 and 3 are concerned, the desired voltage V_d is assumed to be sinusoidal with an offset that is equal to $V_{in}/2$, a peak-to-peak amplitude equal to V_{in} and a frequency equal to 50 Hz. As far as load 4 is concerned, the desired voltage V_d is assumed to be constant and equal to 4.5 V. By focusing on the loads 1, 2, and 3, and using the parameters L_L, C_L, and R_L given in Figure 31, one can notice that they represent the cases of voltage V_{out} delayed by $\pi/4$ with respect to current I_{out}, current I_{out} delayed by $\pi/4$ with respect to voltage V_{out}, and current I_{out} in phase with voltage V_{out}, respectively. The initial conditions of the RLC load are assumed to be equal to zero. Figure 32 shows the simulation results in terms of output voltages V_{out}. The first three rows of subplots show the simulation results after the transient when the loads 1, 2 and 3 are considered. From the first three rows of subplots on the left-hand side, obtained using the Minimum Distance Control, it is possible to see that the average V_{out} characteristic exhibits different degrees of deviation from the desired voltage V_d. This is due to the fact

that the distance between vectors $\overline{\mathbf{V}}_c$ and $\overline{\mathbf{V}}_{m0}$ tends to increase, even if the average value of $\tilde{V}_d$ is equal to 0.5, i.e., the average value of V_d is equal to $V_{in}/2$. This can be explained by recalling that the output current I_{out} *is not constant*, as the load is dynamic, which means that the *strength* of the control action applied by the Configuration Vector $\mathbf{S}_j$ in (24) *changes in time* through I_{out}, which is a function of V_{out}. Without a loss of generality, it is possible to state that this makes the Voltage Configuration Vectors $\mathbf{V}_m$ different from the basic one $\mathbf{V}_m^*$ loose the full flying capacitors voltage balancing capability, i.e., to become unstable, *even when the average value of the desired voltage* V_d *is equal to* $V_{in}/2$. It follows that the distance between vectors $\overline{\mathbf{V}}_c$ and $\overline{\mathbf{V}}_{m0}$ will keep increasing, thus causing the output voltage levels to be increasingly unequally spaced. On the other hand, the subplots on the right-hand side show the very good matching between the average V_{out} characteristic and the desired voltage V_d when the converter is controlled using the Variable-Step Control. It follows that the Variable-Step Control is capable of handling the cases of non-constant output current I_{out} in extended operation as well, by increasing the current level-to-level distance N_{si} when necessary in order to prevent the divergence of vector $\overline{\mathbf{V}}_c$ from vector $\overline{\mathbf{V}}_{m0}$. As an example of this, the voltage trajectories of the flying capacitors, namely the components of vector $\overline{\mathbf{V}}_c$, are shown in Figure 33 for the case "Load 2" when the two different controls are used. From the figure, it is clearly possible to see that the Minimum Distance Control causes the divergence of vector $\overline{\mathbf{V}}_c$ (blue characteristic) from the desired vector $\overline{\mathbf{V}}_{m0}$, which is highlighted by the red spot in the figure. Furthermore, the blue characteristic also shows that the strength of the control action applied by the Configuration Vector $\mathbf{S}_j$ in (24) is indeed not constant during the simulation, but it is a function of the output current I_{out}, since the length of the blue voltage trajectories in Figure 33 is not constant. On the other hand, the Variable-Step Control is indeed capable of ensuring the convergence of vector $\overline{\mathbf{V}}_c$ to the desired vector $\overline{\mathbf{V}}_{m0}$.



	Load 1	Load 2	Load 3	Load 4
L_L	84.06 [μH]	31.7 [mH]	316.8 [μH]	31.7 [mH]
C_L	320 [μF]	320 [μF]	320 [μF]	320 [μF]
R_L	10 [Ω]	10 [Ω]	1 [Ω]	10 [Ω]

V_{in}	10 [V]	10 [V]	10 [V]	10 [V]
R_{in}	0.1 [mΩ]	0.1 [mΩ]	0.1 [mΩ]	0.1 [mΩ]
C_1	2 [mF]	2 [mF]	2 [mF]	4 [mF]
C_2	2.5 [mF]	2.5 [mF]	2.5 [mF]	5 [mF]
C_3	10 [mF]	10 [mF]	10 [mF]	20 [mF]

Figure 31. On the left: RLC load POG scheme; On the right: RLC load and converter parameters.

The fourth row of subplots presented in Figure 32 shows the case of constant desired voltage V_d with the load parameters identified by "Load 4" in Figure 31 on the right. The bottom-left subplot shows that the case of constant desired voltage $V_d \neq V_{in}/2$, namely $\tilde{V}_d \neq 0.5$, is still the most severe one. This can be seen from the fact that the output voltage levels quickly become unequally spaced because of the divergence of vector $\overline{\mathbf{V}}_c$ from vector $\overline{\mathbf{V}}_{m0}$. Furthermore, note that the average output voltage in the bottom-left subplot of Figure 32 tends to decrease, as a consequence of the divergence of the vector $\overline{\mathbf{V}}_c$ trajectories. Consequently, the output current I_{out} will also tend to decrease. This situation gives rise to an unstable loop: the more V_{out} decreases with respect to the desired value V_d, the lower the output current I_{out}, the weaker the control action applied by the Configuration Vector $\mathbf{S}_j$ in (24), the more severe the divergence of the $\overline{\mathbf{V}}_c$ trajectories from $\overline{\mathbf{V}}_{m0}$. However, the bottom-right subplot of Figure 32 shows how the divergence of the $\overline{\mathbf{V}}_c$ trajectories from $\overline{\mathbf{V}}_{m0}$ is prevented by the Variable-Step Control, thanks to the increase of the current level-to-level distance N_{si} from 1 to 2, showing the effectiveness of the proposed Variable-Step Control.

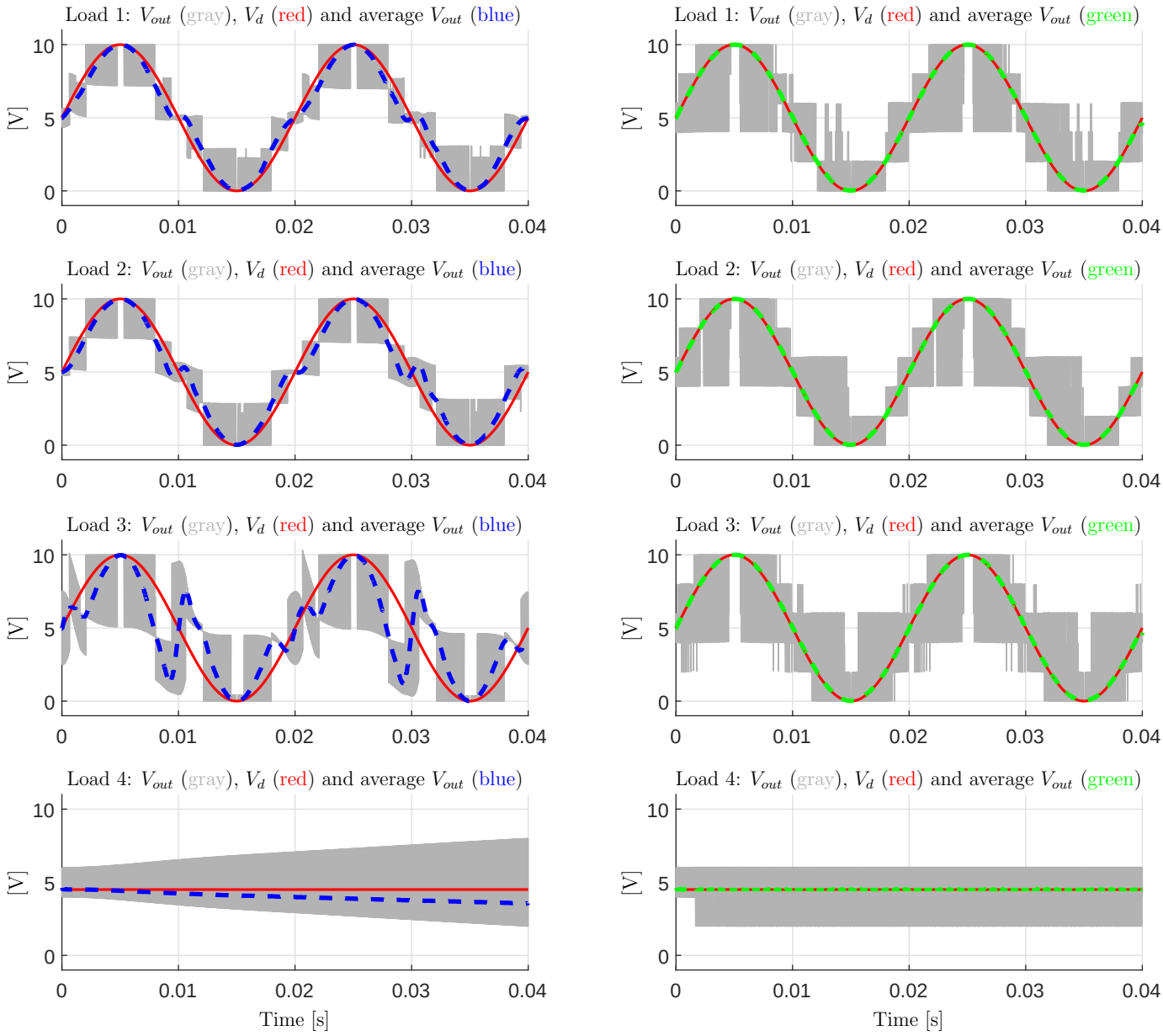


Figure 32. Left subplots: simulations using the Minimum Distance Control for $\mathbf{V}_m = [5\ 4\ 1]^{\mathrm{T}}$; Right subplot: simulations using the Variable-Step Control for $\mathbf{V}_m = [5\ 4\ 1]^{\mathrm{T}}$.

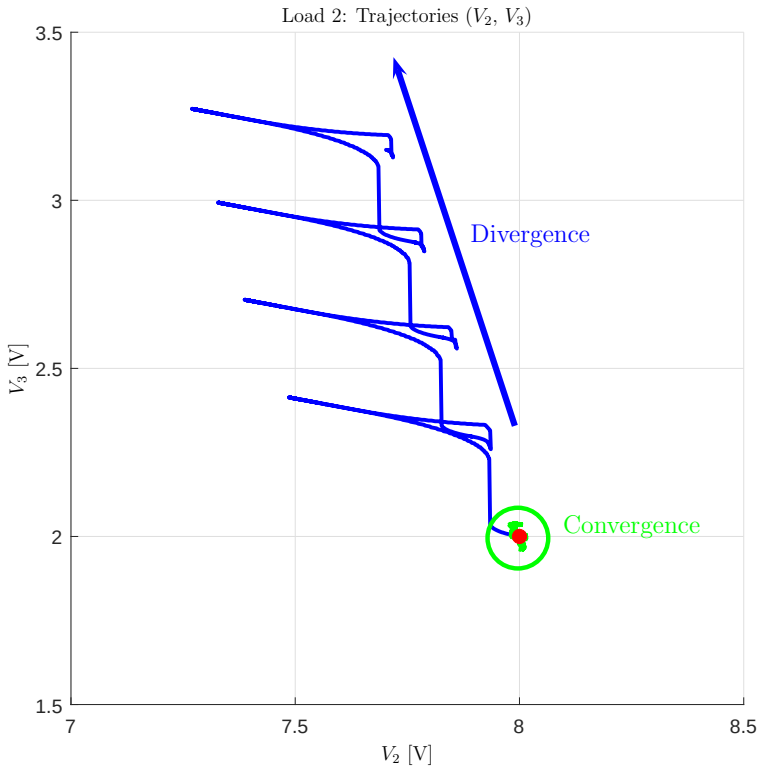


Figure 33. Voltage trajectories for the "Load 2" case using the Minimum Distance Control (blue) and the Variable-Step Control (green).

6. Conclusions

In this paper, the modeling, the control, and the robustness assessment of the multi-level flying-capacitor converter have been addressed. The main contributions of this paper are summarized in the following:

- the Power-Oriented Graphs modeling technique has been exploited to derive the system dynamic model of the n-dimensional converter, generating a POG model that can be directly implemented in Matlab/Simulink by employing standard Simulink libraries;
- a procedure for computing all the possible voltage vector configurations $\mathbf{V}_m$ providing equally spaced levels of the output voltage V_{out} has been given;
- the robustness assessment of the converter operating in extended mode when using a Minimum Distance Control has been performed;
- a Divergence Index I_M has been introduced, which can be used as a metric for properly ordering the different Configuration Voltage Vectors on the basis of their voltage balancing capability in extended operation;
- a new Variable-Step Control algorithm has been proposed, allowing for the safe extended operation of the converter even under particularly destabilizing operating conditions, such as a constant desired output voltage or a sudden load change.

The good performances of the proposed control algorithm have finally been tested in simulation and compared with the results that are given by the classical Minimum Distance Control.

The next steps of the research work presented in this paper include the code optimization of the Variable-Step Control, in order to study and address its real-time implementation, as well as the investigation of the other potential benefits that the Variable-Step Control can bring. Additionally, the closed-loop stability analysis through the load can provide important criteria that the load must satisfy in order to ensure closed-loop stability. As far as the modeling part is concerned, the presented modeling procedure can be extended in order to show that it can also be easily applied to other converter topologies, such as the

diode-clamped topology. Furthermore, we are planning to address the analysis and the modeling of other multilevel converters, in order to perform their stability analysis and investigate the properties they exhibit, following the outlines introduced in this paper for multilevel flying-capacitor converters.

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