energies

MDPI

Article

A PWM/PFM Dual-Mode DC-DC Buck Converter with Load-Dependent Efficiency-Controllable Scheme for Multi-Purpose IoT Applications

Myeong Woo Kim and Jae Joon Kim *

Department of Electrical Engineering, Ulsan National Institute of Science and Technology (UNIST), Ulsan 44919, Korea; mwkim5036@unist.ac.kr

* Correspondence: jaejoon@unist.ac.kr; Tel.: +82-52-217-2126

Abstract: This paper presents a dual-mode DC-DC buck converter including a load-dependent, efficiency-controllable scheme to support multi-purpose IoT applications. For light-load applications, a selectable adaptive on-time pulse frequency modulation (PFM) control is proposed to achieve optimum power efficiency by selecting the optimum switching frequency according to the load current, thereby reducing unnecessary switching losses. When the inductor peak current value or converter output voltage ripple are considered in some applications, its on-time can be adjusted further. In heavy-load applications, a conventional pulse width modulation (PWM) control scheme is adopted, and its gate driver is structured to reduce dynamic current, preventing the current from shooting through the power switch. A proposed dual-mode buck converter prototype is fabricated in a 180 nm CMOS process, achieving its measured maximum efficiency of 95.7% and power density of 0.83 W/mm^2.

Keywords: load-dependent efficiency control; selectable adaptive on-time; pulse frequency module; pulse width modulation; DC-DC buck converter

Citation: Kim, M.W.; Kim, J.J. A PWM/PFM Dual-Mode DC-DC Buck Converter with Load-Dependent Efficiency-Controllable Scheme for Multi-Purpose IoT Applications. *Energies* **2021**, *14*, 960. https://doi.org/10.3390/en14040960

Academic Editor: Anna Richelli

Received: 17 January 2021

Accepted: 8 February 2021

Published: 11 February 2021

1. Introduction

DC-DC converters for Internet of Things (IoT) or portable applications have provided energy-input interfaces from lithium-ion batteries, next-generation batteries, or various harvesting sources [1,2]. For supporting different kinds of load stages, their efficiency specifications over a wide load range are important, as various functional blocks can be individually turned on or off. Considering portability, their area and power density performance are also important in accordance with trends in miniaturization of IoT devices [3–6]. A variety of DC-DC converters, which are efficient over a wide range of load currents, have been developed to maximize the usage time of batteries with limited capacity [7–11].

Pulse frequency modulation (PFM) control has been widely studied to achieve high efficiency under light-load conditions [8,12,13], which are important in IoT environments. As the load current decreases, the switching period increases, and the output voltage ripple becomes bigger. It is also not easy to filter out electromagnetic interference (EMI) noises since its switching frequency varies. Higher efficiency is achieved by reducing switching losses that dominate overall losses in light-load conditions. PFM control under light-load conditions has been implemented in a variety of ways. Hysteretic voltage-mode control [14–17] requires only a few sub-circuits within a small area, whose implementation is relatively simple. The controller detects the output voltage ripple, and the switching regulation is performed depending on the time when the output voltage reaches the maximum or minimum set by the designer. Therefore, a stable regulator would lead to a large output voltage ripple. Hysteretic current mode control [18–20] has the advantage of being able to generate a smaller output voltage ripple. However, hysteretic control of both voltage-mode and current-mode has inherent problems of varying the switching frequency according to

input voltage, output voltage, and load current. Constant on-time control [21–23] can also be implemented in PFM within a small area under light-load conditions, but the problem of switching frequency variability still remains. Therefore, adaptive on-time control [24–28] has been utilized to improve EMI problems due to switching frequency variation. It alleviates the problem of switching frequency variability by using a simple sensing circuit, which requires additional area and power consumption.

The pulse width modulation (PWM) control method is still popular under heavy-load conditions, which gives better EMI performance than the PFM. A disadvantage of the voltage-mode PWM control method [12,29] is its complicated compensation circuit design, but it has a simple feedback loop structure that utilizes a single voltage control loop with high noise immunity. An advantage of the current-mode PWM control method [30,31] is its fast transient response speed, but it requires one more current control loop. Thus, it requires additional area and power consumption to support the current sensor and compensation ramp circuit.

A dual-mode control method to include both the PWM and the PFM has been previously reported [30,32]. It adopts the conventional PWM control method for heavy-load conditions. In light-load conditions, the PFM control method is adopted or modified to be suitable for application. In [33], a voltage-mode, ripple-based PFM control is introduced, where the voltage ripple for output regulation is relatively large. Its inductor peak current and converter output voltage ripple cannot be controlled for specific applications, and it is also difficult to control the EMI problem. Unnecessary switching leads to efficiency loss under a wide range of light-load conditions. In [34], the inductor peak current was limited to a certain value, and complex inductor current sensor circuits were burdensome together with additional current consumption. In these PFM controls where switching operations are dependent on the inductor peak current value, their converter efficiency cannot be optimized in a wide range of light-load conditions.

Therefore, this paper presents a PWM/PFM dual-mode DC-DC buck converter with a load-dependent, efficiency-controllable scheme that could be applied to various IoT applications. In light-load conditions, a selectable adaptive on-time control is proposed to improve the adaptive on-time control method. That is, it provides optimal power efficiency by selecting the optimal switching frequency depending on various light-load current conditions. When the inductor peak current or converter output voltage ripple are considered, it can be adjusted further. In heavy-load conditions, the converter operates as the voltage-mode PWM control with a fixed switching frequency of 1 MHz. Its gate driver includes a non-overlap pre-driving structure to reduce dynamic current losses. It not only prevents the current from shooting through the power switches, but it also reduces unnecessary dynamic power loss inside the driver. Section 2 describes the proposed dual-mode DC-DC converter structure and operation, and Section 3 shows its experimental results including functional verifications. Finally, the conclusions are drawn in Section 4.

2. Proposed Dual-Mode Buck Converter

2.1. Conventional Buck Converter Structures

Figure 1 presents two conventional DC-DC buck converter control methods for the adaptive on-time controlled PFM converter [24,35] and the voltage-mode PWM DC-DC buck converter [36–38]. In Figure 1a, the PFM buck converter operates with the adaptive on-time control scheme. When the converter output voltage (V_{OUT}) goes down, the output feedback voltage (V_{FB}) follows. When V_{FB} is lower than the reference voltage (V_{REF}), the comparator output increases, and the following adaptive on-time generator and control logic turn on the high-side switch with enough energy via a driver. After the controlled on-time by the adaptive generator has elapsed, the high-side switch is turned off. Then, after sufficient dead time to prevent current from shooting through the power switch, the low-side switch is turned on via the driver. Then, if the inductor current decreases and crosses zero, the zero-current detect (ZCD) detects this instance and turns off the low-side switch. In this case, it creates an intentional dead time condition where both the

high-side switch and the low-side switch are turned off. Then, as this cyclic operation is repeated continuously, the average converter output value approaches a desired converter output value. In this adaptive on-time controlled buck converter, the problem of switching frequency variability is alleviated, relaxing the EMI problem. The peak inductor current and the converter output ripple voltage can also be kept relatively constant compared to other PFM methods even under varying conditions of input voltage, output voltage, and load current. Since there is no need for complicated current sensing circuits, the power dissipation and the area are relatively small.

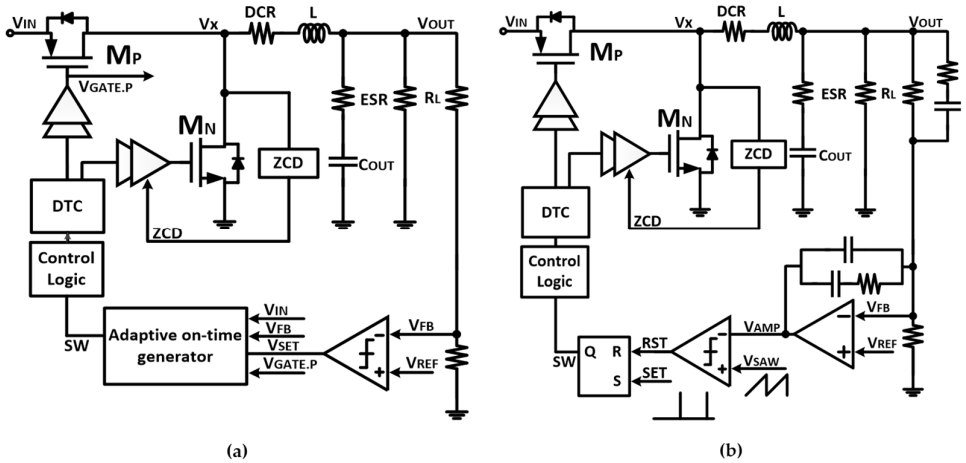


Figure 1. Conventional DC-DC buck converters: (**a**) adaptive on-time controlled pulse frequency modulation (PFM) converter and (**b**) voltage-mode pulse width modulation (PWM) converter.

Regarding the voltage-mode PWM converter in Figure 1b, V_{FB} is amplified by an error amplifier with respect to V_{REF}. Its amplified voltage is compared to a ramp generator output voltage in a compensating comparator. Pulse width information proportional to the comparison value is used as duty cycle information to turn on the high-side switch at a constant switching frequency. After the duty time, the high-side switch is turned off and the down-side switch is turned on with dead time components suitable for non-overlapping switching. If the current through the inductor during this down-side switching operation crosses zero, it creates the ZCD state where both the high-side switch and the low-side switch are turned off. Through this iterative loop operation, the average output value gets close to a desired value. Since the switching frequency is constant, the EMI problem is relaxed. The output voltage ripple is relatively small, and its transient response is fast. However, the lower the load current is, the lower the efficiency is.

2.2. Proposed Dual-Mode Buck Converter Structure

A PFM/PWM dual-mode buck converter was designed to obtain high efficiency under a wide range of load current conditions, as shown in Figure 2. It adopts a voltage-mode PWM (VPWM) control loop for the heavy-load condition and an adaptive on-time PFM control loop for the light-load condition. The adaptive on-time PFM control is improved to provide further adaptive optimization through a proposed selectable adaptive on-time scheme. The VPWM is designed to improve its efficiency through a proposed non-overlapping gate-driving circuit.

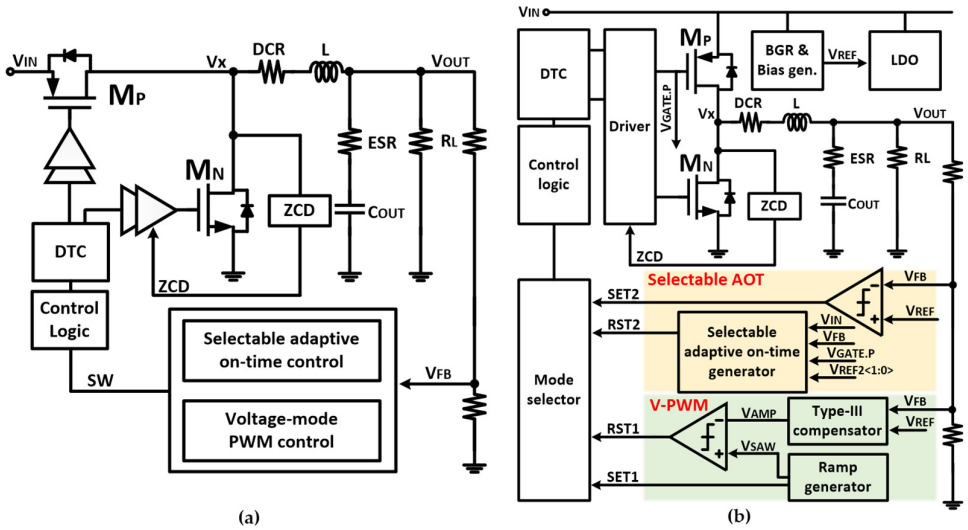


Figure 2. Proposed DC-DC buck converter with dual modes of PWM and selectable adaptive on-time controls: (**a**) simplified circuit diagram and (**b**) top block diagram.

2.3. Selectable Adaptive On-Time PFM Control

When the output load current becomes lower than a certain level, it is difficult for the VPWM buck converter operation to achieve high efficiency. Therefore, for efficient power delivery, better efficiency is achieved by using a PFM control rather than the VPWM. Conventional adaptive on-time controlled buck converters show high efficiency under light-load conditions. Their peak inductor current and output ripple voltage can be kept relatively constant, and less switching frequency variability relaxes the EMI. However, it is not easy to maintain optimal efficiency over a wide light-load range. Additionally, since its peak inductor current and converter output voltage ripple are fixed or predesigned, one designed converter may not be used in other applications that need to limit the maximum inductor current or output voltage ripple.

The proposed selectable adaptive on-time control scheme can adjust the on-time according to the required efficiency, peak inductor current, and output voltage ripple specification under light-load conditions. Figure 3a,b shows the buck converter with the proposed PFM control, and Figure 3c details the proposed selectable adaptive on-time generator. In Figure 3c, adaptive on-time control generates an adaptive current proportional to the difference between the input voltage and the output feedback voltage through the adaptive on-time generator. The adaptive current is generated by R1, C0, the amplifier, and M_{N1}. The generated adaptive current is used to generate a ramp waveform through a current mirror. When the high-side switch of the converter is turned on, the $V_{GATE\cdot P}$ signal is deactivated. The generated adaptive current charges the C1 capacitor through the current mirror, which increases its voltage over time. If it reaches a reference voltage of V_{REF2}, the high-side switch of the converter is turned off. Then, the $V_{GATE\cdot P}$ signal is activated and C1 is discharged. Through its iterative operation, the C1 voltage follows a ramp shape. The on-time corresponds to the time when the C1 voltage is charged, which is proportional to the V_{REF2}. The proposed selectable adaptive on-time controller controls the V_{REF2} and the high-side switch on-time (Ton) of the converter by adjusting the 2-bit digital-to-analog converter (DAC) inside the adaptive on-time generator. The adaptive on-time generator increases the on-time by increasing the V_{REF2}. The on-time is proportional to V_{REF2}.

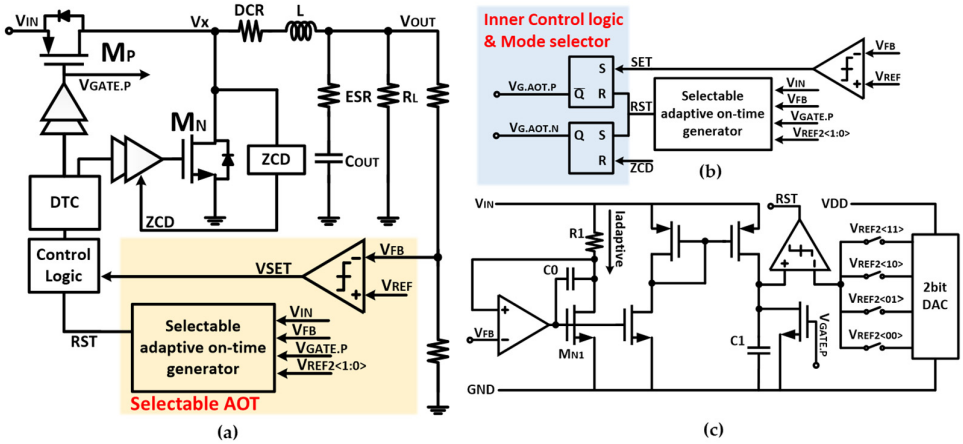


Figure 3. PFM buck converter with proposed selectable adaptive on-time control: (**a**) buck converter structure, (**b**) selectable adaptive on-time controller, and (**c**) selectable adaptive on-time generator.

The selectable adaptive on-time control is intended to operate at an on-time dependent switching frequency that derives optimum efficiency depending on the load current. The proposed adaptive on-time generator controls the on-time by adjusting the internal 2-bit DAC. As the on-time increases, the switching frequency decreases. The switching frequency is inversely proportional to the square of the on-time as shown in Figure 4a. Figure 5 illustrates that an optimal switching frequency to derive the optimum efficiency varies with the load current, where F_{PWM} is the PWM switching frequency under heavy-load conditions and F_{PFM} is the PFM switching frequency under light-load conditions. Under sufficient light-load conditions, the smaller the load current, the smaller the optimal switching frequency. The proposed selectable adaptive on-time control method increases the on-time value as the load current value decreases under light-load conditions. Then, the increased on-time reduces the switching frequency, and it reduces switching losses further, achieving the optimum efficiency.

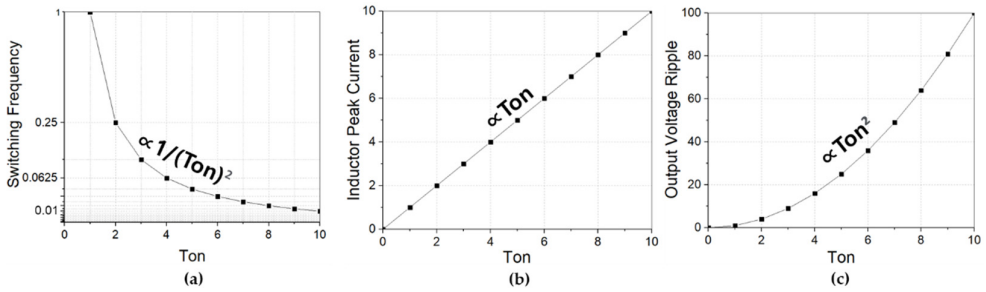


Figure 4. Selectable adaptive on-time characteristics: (**a**) relationship between on-time and switching frequency, (**b**) relationship between on-time and inductor peak current, and (**c**) relationship between on-time and output voltage ripple.

The selectable adaptive on-time control can control the inductor peak current or the output voltage ripple where the values are important in IoT applications. The proposed adaptive on-time generator adjusts the on-time by adjusting the internal 2-bit DAC. As the on-time increases, the inductor peak current increases. The inductor peak current is proportional to the on-time as shown in Figure 4b. Assuming a sufficiently low output current condition, the periodic operation of the converter takes a long time to discharge the energy charged in the capacitor (Cout) of the converter. The time used to discharge the energy becomes dominant in the switching cycle. In this case, as the on-time increases, the output voltage ripple increases. The output voltage ripple is proportional to the square of the on-time as shown in Figure 4c. Therefore, the selectable adaptive on-time control scheme can control the on-time. In Figure 4, the converter can adjust the light-load efficiency,

inductor peak current, and output voltage ripple to meet the needs of multi-purpose IoT applications through on-time adjustment.

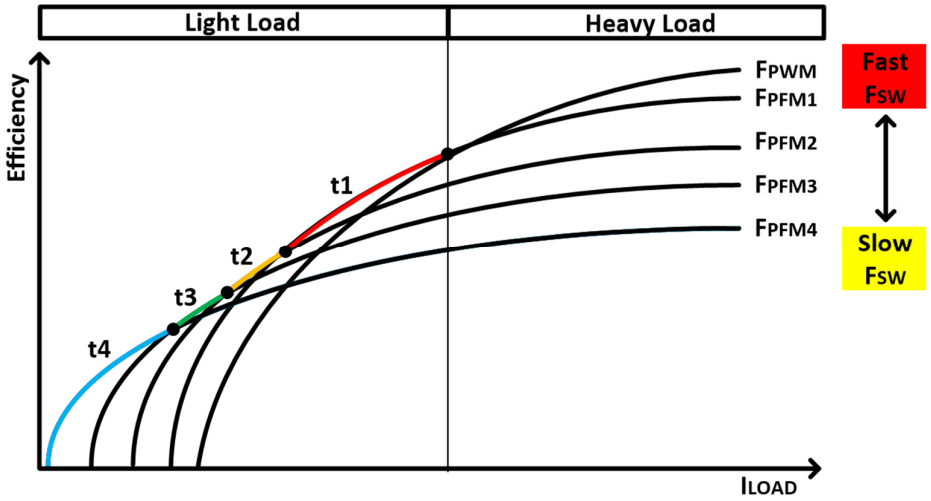


Figure 5. Switching frequency dependent efficiency difference in light-load conditions.

2.4. Voltage-Mode PWM Control with Non-Overlapping Gate Driving

VPWM control for heavy-load conditions is implemented by utilizing two improved sub-circuits. The first circuit is an enhanced gate driver. The proposed gate driver reduces dynamic current consumption at the end of the driver as well as prevents current from shooting through the power switch. The second circuit is an error amplifier structure that adopts the constant-transconductance rail-to-rail operational amplifier structure, which works reliably for the entire input voltage range. These improvements can increase operational stability in a start process and a load transient response under heavy-load current conditions. Figure 6 shows a schematic diagram of a conventional gate driver and the proposed gate driver. The conventional gate driver treats duty-modulated pulses from the PWM control circuit through the dead-time controller (DTC), and it generates two non-overlapping clock signals with dead time, which drive the high-side and low-side power switches through tapering-based drive buffers. It is also intended to prevent the current from shooting through the power switch.

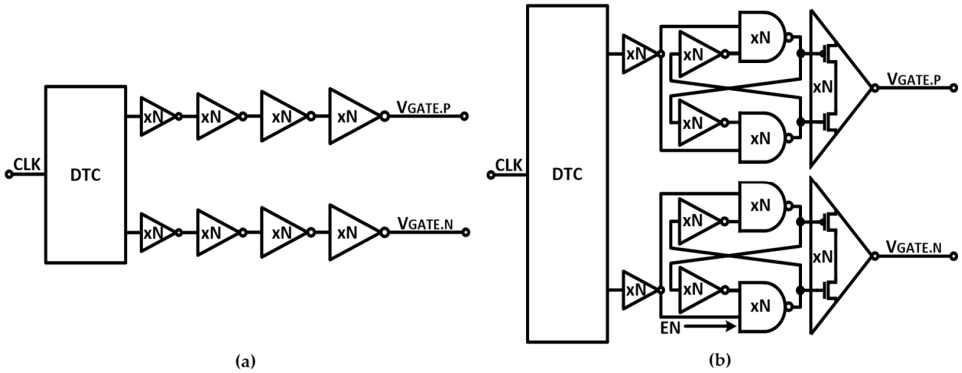


Figure 6. Simplified gate driver structures: (**a**) Conventional gate driver and (**b**) proposed non-overlapping gate driver.

Figure 7 presents the proposed nonoverlapping gate driver operations applied to the high-side switch and the low-side switch of the buck converter. It is used together with the DTC, but it has its own non-overlap feedback structure inside the driver. In the conventional tapered buffer-based gate driver, the dynamic current at the output stage increases as it passes through buffer stages. The buffer at the end of the switch driver has a large amount of dynamic current with enough energy to drive the power switch. The proposed gate driver not only prevents the current from shooting through the power switch, but it also reduces dynamic current loss at the driver's end stage. The proposed gate driver for the low-side switch has the same structure as that of the high-side driver. The difference is when the ZCD circuit detects the instance when the inductor current becomes zero, there is an auxiliary switch to momentarily open the low-side switch. At the moment the ZCD signal changes from low to high, the phase of the CLK2 signal coming into the gate driver's input is reversed. After a short delay time, the EN (enable) signal is activated, and the auxiliary switch is turned on in a short time to open the low-side switch.

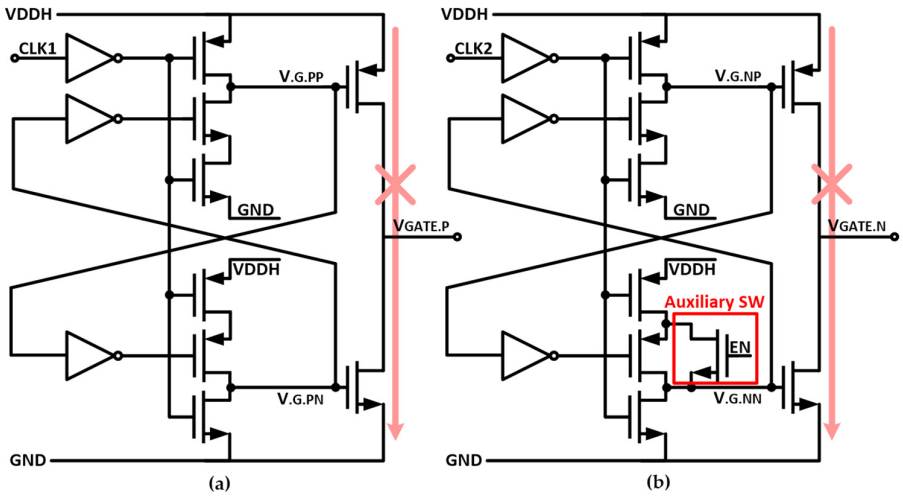
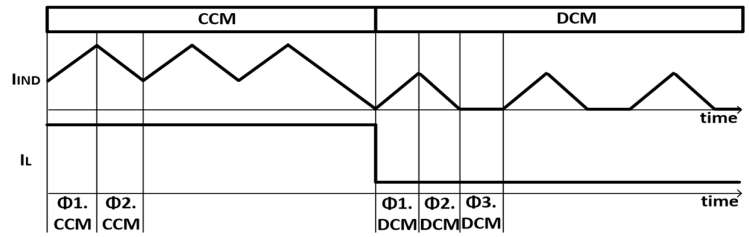


Figure 7. Circuit implementation of the proposed gate driver with reduced dynamic current: (**a**) gate driver for the high-side switch, (**b**) gate driver for the low-side switch.

Figure 8 shows the control signal state of the proposed gate drivers for the high-side switch and the low-side switch under continuous conduction mode (CCM) and discontinuous conduction mode (DCM) conditions. In the CCM condition where the load current is sufficiently high, periodic switching of the converter is performed by operation of phase 1 ($\Phi_{1.CCM}$) and phase 2 ($\Phi_{2.CCM}$). In phase 1, the high-side switch is turned on when each CLK signal is inputted to the gate driver, and the final output of the gate driver is low. If the low-side switch is turned on after a short dead time, the final output stage of the gate driver becomes high. In DCM conditions where the load current is close to zero, periodic switching of the converter is performed by operation of phase 1 ($\Phi_{1.DCM}$), phase 2 ($\Phi_{2.DCM}$), and phase 3 ($\Phi_{3.DCM}$). The operation of phase 1 and phase 2 is the same as under the CCM condition. During phase 2 operation, if the ZCD circuit detects that the inductor current crosses zero, both the high-side switch and the low-side switch open, which is phase 3.



	Phase	CLK1	CLK2	EN	V.G.PP	V.G.PN	VGATE.P	V.G.NP	V.G.NN	VGATE.N
CCM	Φ1.CCM	CLK	CLK	L	H	H	L	H	H	L
	Φ2.CCM	CLK	CLK	L	L	L	H	L	L	H
DCM	Φ1.DCM	CLK	CLK	L	H	H	L	H	H	L
	Φ2.DCM	CLK	CLK	L	L	L	H	L	L	H
	Φ3.DCM	CLK	$\overline{CLK}$	H	L	L	H	H	H	L

Figure 8. Operation of the proposed gate driver in continuous circuit mode (CCM) and discontinuous circuit mode (DCM) conditions.

Figure 9 shows the timing diagram of the proposed gate driver under CCM and DCM conditions. In the CCM condition, gate drivers for the high-side switch and low-side switch perform phase 1 and phase 2 periodic operation as illustrated in Figure 9a. Similar to the CLK signal for the DTC circuit, CLK1 for the high side and CLK2 for the low side are configured to have a non-overlapping characteristic. Non-overlapping delay times at the rising and falling edges of the CLK1 and CLK2 signals correspond to tdc1 and tdc2, respectively. In the driver for the high-side switch, the signal that controls the last-stage buffer through its own internal non-overlapping feedback structure in the gate driver corresponds to $V_{G \cdot PP}$ and $V_{G \cdot PN}$. Non-overlapping delay times at the falling and rising edges of $V_{G \cdot PP}$ and $V_{G \cdot PN}$ correspond to tdp1 and tdp2, respectively. Non-overlapping delay times at the falling and rising edges of $V_{G \cdot NP}$ and $V_{G \cdot NN}$ in the driver for the low-side switch correspond to tdn1 and tdn2, respectively. Non-overlapping delay times at the rising and falling edges of the final driver outputs ($V_{GATE \cdot P}$, $V_{GATE \cdot N}$) correspond to Td1 and Td2, respectively. The proposed gate driver prevents dynamic current loss by applying the optimal dead time to the final stage of the gate driver. In addition, it prevents current from shooting through the power switch.

In the DCM condition, each gate driver operates periodically in phase 1, phase 2, and phase 3 as described in Figure 9b. The operation in the transition from phase 1 to phase 2 is the same as that in the CCM condition. With the high-side switch off and the low-side switch on, the current amount flowing through the inductor gradually decreases. When the inductor current crosses zero (Tclk1), the phase of the signal path to CLK2 is reversed. After a short delay time, at the timing moment of Ten1, the EN signal changes from low to high, which turns on the auxiliary switch in a short time and then turns off the low-side switch (phase 3). In the process of switching from phase 3 to phase 1, if the $V_{GATE \cdot P}$ signal changes from low to high (Tclk2, Ten2), the output signal of the ZCD circuit changes from high to low. The phase of the signal path to CLK2 returns to its original state. At the same time, the EN signal changes from high to low, and the auxiliary switch is turned off.

Figure 10 shows the VPWM controller, which is composed of a comparator, a ramp generator, and a type-III compensator including an error amplifier (EA), R1, R2, R3, C1, C2, and C3. It also shows circuit implementation of the constant-transconductance rail-to-rail operational amplifier. In the normal state of the converter, the common-mode levels of two inputs in the error amplifier are equally biased to the reference voltage V_{REF}. In the soft start process, while the positive input voltage of the error amplifier increases smoothly from zero to V_{REF}, the negative input should be kept at the same common-mode. Under normal converter operation, the negative input of the error amplifier temporarily fluctuates in transient responses, and conventional amplifiers might go into undesired states in the

case of instantaneous rising or falling responses of the load current. Therefore, this work adopted the rail-to-rail amplifier structure to maintain constant transconductance over a wide input voltage, and its resulting operation became stable even in cases of overshooting or undershooting.

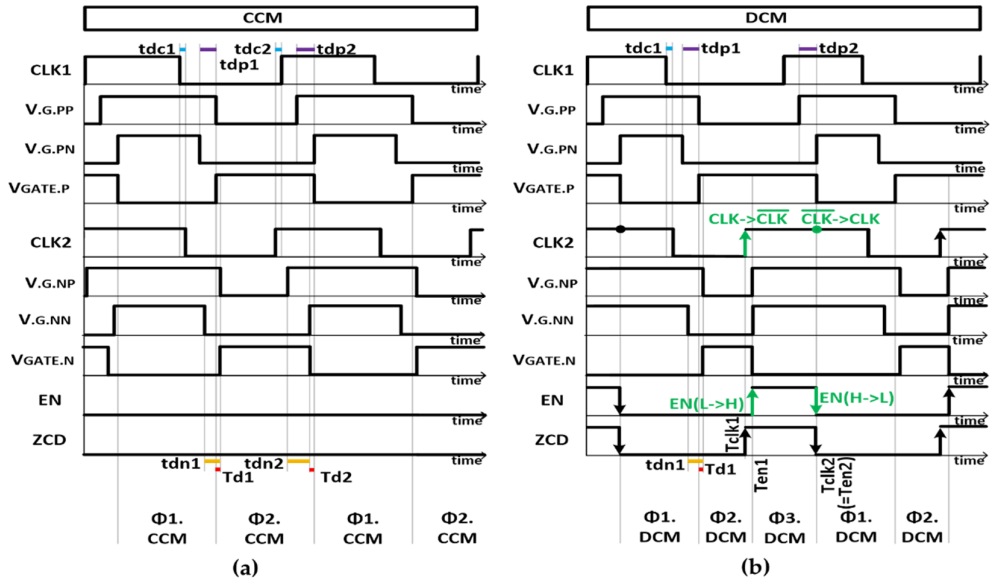


Figure 9. Timing diagrams of the proposed gate driver under (**a**) CCM condition and (**b**) DCM condition.

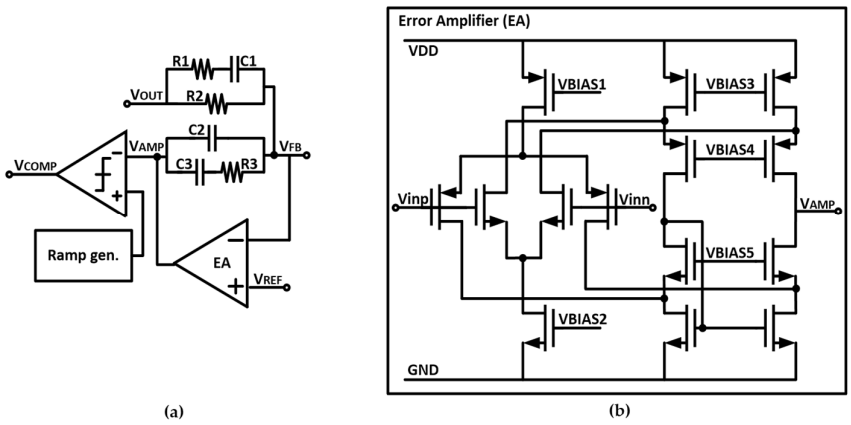


Figure 10. Voltage pulse width modulation (VPWM) controller implementation: (**a**) block diagram of the VPWM controller and (**b**) schematic of constant-transconductance rail-to-rail amplifier.

3. Experimental Results

A proposed dual-mode buck converter prototype was fabricated in a 180 nm CMOS process, and its proposed schemes were experimentally verified. Figure 11 shows its chip microphotograph whose core area was 0.47 mm × 0.85 mm. The buck converter utilized 4.7 µH inductor and 33 µF capacitor off-chip components. The proposed dual-mode DC-DC buck converter operation was functionally verified with an input voltage of 4.4 V as the load current was varied, and its measured waveforms including converter output voltage (V_{OUT}) and inductor current (I_{IND}) are given in Figure 12. As the load current was swept from 80 mA to 5 mA, PWM–PFM mode transition occurred from 20 mA to 10 mA. The PWM mode transitioned from CCM to DCM as the load current decreased. In the case of PFM with 10 mA and 5 mA load currents, the inductor peak current and

output voltage ripple remained constant, but the switching frequency decreased as the load current decreased.

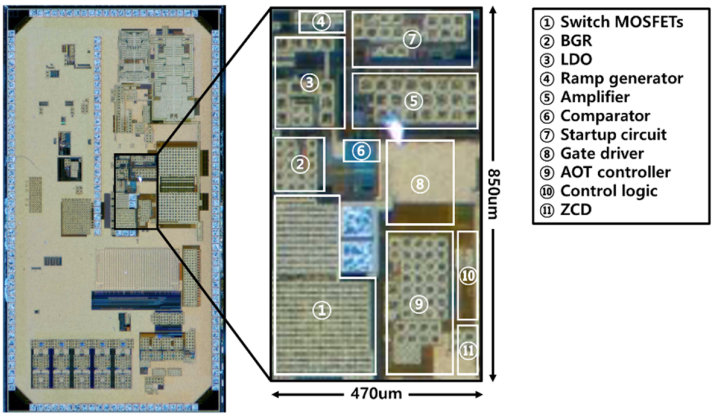


Figure 11. Microphotograph of proposed dual-mode DC-DC buck converter prototype.

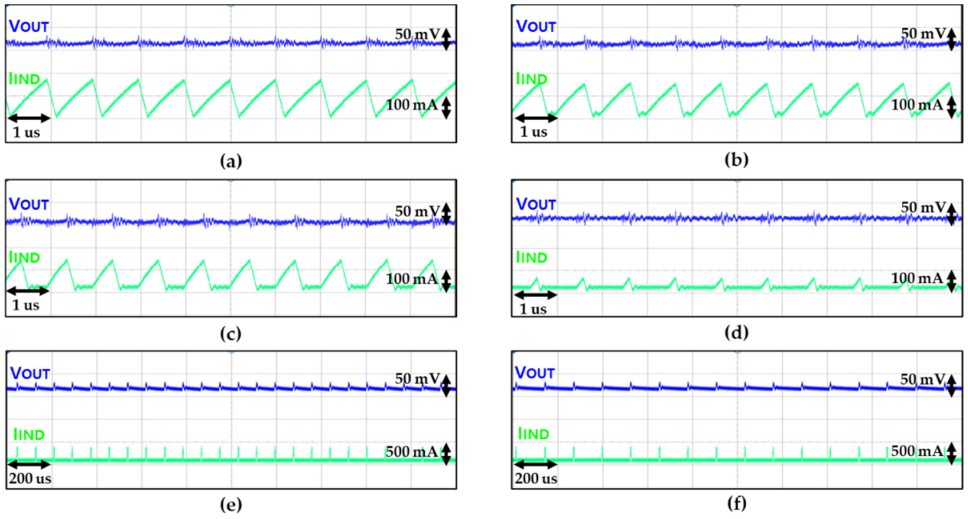


Figure 12. Measured steady-state DC-DC buck operations with respect to load currents of (**a**) PWM 80 mA, (**b**) PWM 60 mA, (**c**) PWM 40 mA, (**d**) PWM 20 mA, (**e**) PFM 10 mA, and (**f**) PFM 5 mA.

Figure 13a shows the measured line regulation characteristic of the proposed buck converter when the converter input voltage was swept from 3.6 V to 5.5 V by 0.1 V unit steps under 40 mA load current. The output voltage, whose nominal value was 3.3 V, changed from 3.282 V to 3.306 V, resulting in the output line regulation of 8.888 mV/V. Figure 13b shows the measured load regulation characteristic when the load current was swept from 0 to 100 mA by 10 mA unit steps under 4.4 V converter input. The output voltage, whose nominal value was also 3.3 V, changed from 3.321 V to 3.262 V, resulting in the output load regulation of 0.59 mV/mA. Figure 14 shows the comparison of dynamic current between the conventional gate driver and the proposed non-overlapping gate driver, which were applied to both the high-side switch (HSW) and the low-side switch (LSW) of the buck converter with variable input voltage. The measured amount of dynamic current in the proposed gate driver was smaller than that of the conventional gate driver. As the converter input voltage increased, the improvement became prominent, and the maximum reduction in dynamic current was 17.82% in the LSW with 4.8 V input.

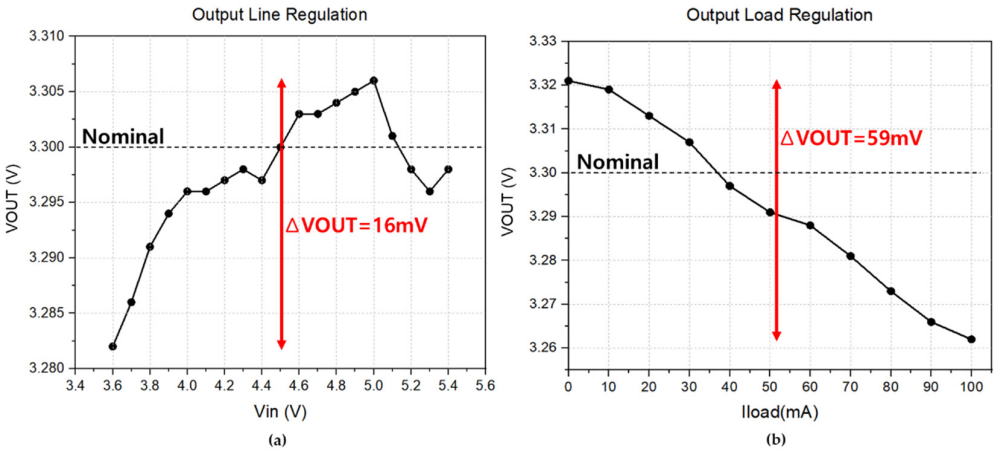


Figure 13. Measured regulation characteristics of proposed buck converter: (**a**) output line regulation and (**b**) output load regulation.

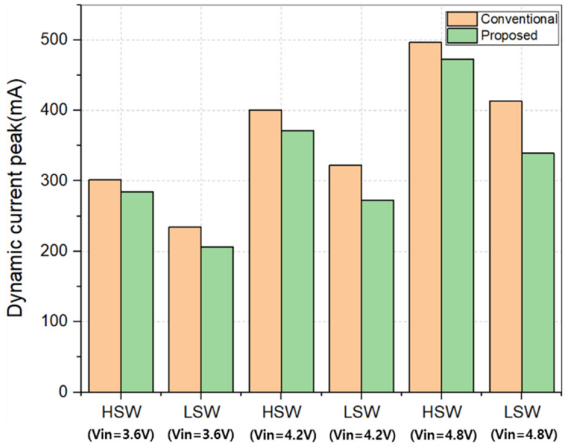


Figure 14. Simulated dynamic current comparison between a conventional gate driver and the proposed non-overlapping gate driver.

Figure 15 shows the measured conversion efficiency over the load currents with 3.6 V input. When the load-current value was more than 15 mA, it was recognized as the heavy-load condition, and the converter activated the VPWM control. When the load-current value was less than 15 mA, it was recognized as the light-load condition, and the proposed selectable adaptive on-time PFM control was activated. A maximum efficiency of 95.7% was achieved with the VPWM control at a maximum load-current of 100 mA. As the load-current decreased, the efficiency gradually decreased. At around 15 mA load current, the PWM efficiency and PFM efficiency crossed over at approximately 80%. At a load current less than 15 mA, the converter operation changed into the proposed selectable adaptive on-time PFM control, where PFM(S1), PFM(S2), PFM(S3), and PFM(S4) are selected cases of its on-time adjustments. Their on-time relationship was Ton(PFM.S4) > Ton(PFM.S3) > Ton(PFM.S2) > Ton(PFM.S1). Their switching frequency relationship was Fsw(PFM.S4) < Fsw(PFM.S3) < Fsw(PFM.S2) < Fsw(PFM.S1). The optimum efficiency was further optimized through fine adaptive operation, which selected PFM(S1) in the t1 section, PFM(S2) in the t2 section, PFM(S3) in the t3 section, and PFM(S4) in the t4 section. The performance summary and comparison of the proposed dual-mode buck converter compared to previous buck converters are shown in Table 1. The proposed buck converter achieved 95.7% maximum efficiency and 0.83 W/mm^2 power density.

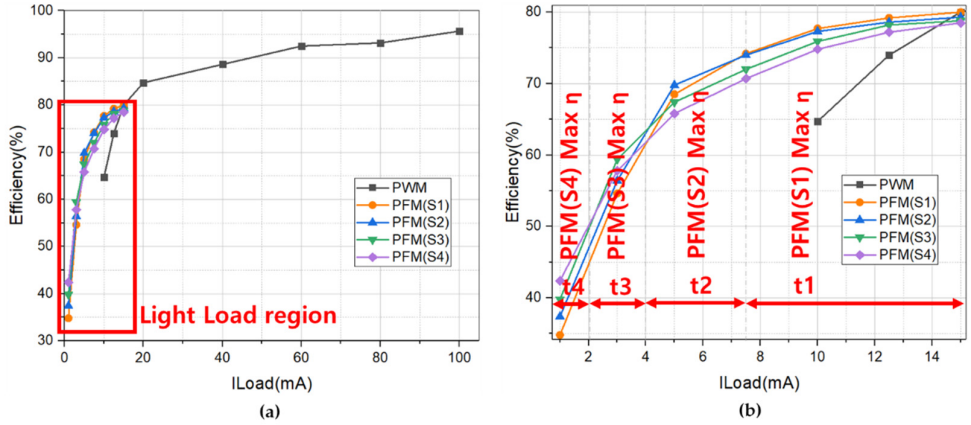


Figure 15. Measured efficiency of the proposed dual-mode buck converter over load current (**a**) for entire load conditions and (**b**) for light-load conditions.

Table 1. Performance summary and comparison.

	[33] TPE '08	[1] TPE '17	[7] JSSC '11	[8] TCASI '11	[9] JSSC '04	[10] JSSC '16	[11] TVLSI '18	**This Work**
Technology	350-nm CMOS	130-nm CMOS	45-nm CMOS	250-nm CMOS	250-nm CMOS	180-nm CMOS	180-nm CMOS	**180-nm CMOS**
Operation Modes	PWM/PFM	PWM/PFM /Retention	PWM/PFM	Proposed Dual-modulation	PWM/PFM	DPWM /PFM/AM	PPFM/DP WM	**PWM/PFM**
Control Method	Voltage-mode	Voltage-mode	Voltage-mode (Digital control)	Voltage-mode	Voltage-mode (Digital control)	Voltage-mode (Digital control)	Voltage-mode (Digital control)	**Voltage-mode**
Input Voltage (V)	2.7–5.0	2.2–3.3	2.8–4.2	3.0–4.5	2.8–5.5	0.55–1.0	0.55–0.18	**3.6–5.4**
Output Voltage (V)	1	1.7	0.4-1.2	1.8	1.0-1.8	0.35-0.5	0.3-0.55	**3.3**
Max. Output Current	460 mA	20 mA	25 0mA	600 mA	400 mA	20 mA	33.3 mA	**100 mA**
L (uH)	10	3	10	1	10	4.7	4.7	**4.7**
COUT (uF)	10	3	2	4.7	47	4.7	4.7	**33**
Max. Switching Frequency (MHz)	0.6	2.5	2	5	1.5	1.6	2	**1**
Peak Efficiency	95% (Measured)	92.4% (Measured)	87.4% (Measured)	92% (Measured)	91.5% (Measured)	92% (Measured)	90.5% (Measured)	**95.7% (Measured)**
Active Area (mm^2)	2.1	0.3	1.16	0.8	2	0.6	0.44	**0.4**
Power Density (W/mm^2)	0.21	0.11	0.09	1.35	0.36	0.02	0.04	**0.83**

4. Conclusions

A dual-mode DC-DC buck converter including a load-dependent, efficiency-controllable scheme was proposed to cope with various IoT applications. For the dual-mode operation, PFM for light-load conditions was designed to have a proposed selectable adaptive on-time control scheme. The PWM structure was utilized for heavy-load conditions, and its driver efficiency was improved by using the proposed non-overlapping driving circuit to reduce dynamic current consumption. Through silicon prototype fabrication and experimental testing, the proposed PFM mode was verified to have four kinds of selectable on-time controls, which would provide finely optimized efficiency depending on light-load conditions. The PWM for the heavy-load condition was designed to have a reduced dynamic-current gate driver circuit, reducing its peak dynamic current by 17.82%. This designed DC-DC buck converter demonstrated a measured maximum efficiency of 95.7% and power density of 0.83 W/mm^2.

Author Contributions: Conceptualization, M.W.K. and J.J.K.; Methodology, M.W.K.; Experiment and verification, M.W.K.; Writing—original draft, M.W.K. and J.J.K. All authors have read and agreed to the published version of the manuscript.

Funding: This work was supported by a National Research Foundation of Korea (NRF) grant funded by the Korea government (MSIT) (2017M1A2A2087833) and by an Institute of Information & communications Technology Planning & Evaluation (IITP) grant funded by the Korea government (MSIT) (No. 2018-0-00756: Development of disposable IoT). It was also supported by the Basic Science Research Program through the National Research Foundation of Korea (NRF) funded by the Ministry of Education (2020R1A6A1A03040570).

Informed Consent Statement: Not applicable.

Data Availability Statement: Not applicable.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Park, Y.-J.; Park, J.-H.; Kim, H.-J.; Ryu, H.-C.; Kim, S.-Y.; Pu, Y.; Hwang, K.C.; Yang, Y.; Lee, M.; Lee, K.-Y. A Design of a 92.4% Efficiency Triple Mode Control DC–DC Buck Converter with Low Power Retention Mode and Adaptive Zero Current Detector for IoT/Wearable Applications. *IEEE Trans. Power Electron.* **2017**, *32*, 6946–6960. [CrossRef]
2. Wu, P.Y.; Tsui, S.Y.S.; Mok, P.K.T. Area- and Power-Efficient Monolithic Buck Converters with Pseudo-Type III Compensation. *IEEE J. Solid-State Circuits* **2010**, *45*, 1446–1455. [CrossRef]
3. Hong, W.; Lee, M. A 7.4-MHz Tri-Mode DC-DC Buck Converter with Load Current Prediction Scheme and Seamless Mode Transition for IoT Applications. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2020**, *67*, 4544–4555. [CrossRef]
4. Lee, T.-J.; Hsu, C.-H.; Wang, C.-C. High Efficiency Buck Converter with Wide Load Current Range using Dual-Mode of PWM and PSM. In Proceedings of the 2019 IEEE International Symposium on Circuits and Systems (ISCAS), Sapporo, Japan, 26–29 May 2019; pp. 1–4. [CrossRef]
5. Park, J.; Lee, H.-M.; Shin, S.-U.; Choi, W.; Hong, S.-W. A 0.46 mm^2 On-Chip Compensated Type-III Buck Converter Using an Inner Feedback Loop with a Seamless CCM/DCM Transition Technique. *IEEE Trans. Power Electron.* **2019**, *35*, 4477–4482. [CrossRef]
6. Cheng, L.; Liu, Y.; Ki, W.-H. A 10/30 MHz Fast Reference-Tracking Buck Converter with DDA-Based Type-III Compensator. *IEEE J. Solid-State Circuits* **2014**, *49*, 2788–2799. [CrossRef]
7. Bandyopadhyay, S.; Ramadass, Y.K.; Chandrakasan, A.P. 20 µA to 100 mA DC–DC Converter With 2.8–4.2 V Battery Supply for Portable Applications in 45 nm CMOS. *IEEE J. Solid-State Circuits* **2011**, *46*, 2807–2820. [CrossRef]
8. Tsai, J.-C.; Huang, T.-Y.; Lai, W.-W.; Chen, K.-H. Dual Modulation Technique for High Efficiency in High-Switching Buck Converters over a Wide Load Range. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2011**, *58*, 1671–1680. [CrossRef]
9. Xiao, J.; Peterchev, A.V.; Zhang, J.; Sanders, S.R. A 4-µA quiescent-current dual-mode digitally con-trolled buck converter IC for cellular phone applications. *IEEE J. Solid-State Circuits* **2004**, *39*, 2342–2348. [CrossRef]
10. Chen, P.-H.; Wu, C.-S.; Lin, K.-C. A 50 nW-to-10 mW Output Power Tri-Mode Digital Buck Converter with Self-Tracking Zero Current Detection for Photovoltaic Energy Harvesting. *IEEE J. Solid-State Circuits* **2016**, *51*, 523–532. [CrossRef]
11. Chen, P.; Cheng, H.; Ai, Y.; Chung, W. Automatic Mode-Selected Energy Harvesting Interface with >80% Power Efficiency Over 200 nW to 10 Mw. *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.* **2018**, *26*, 2898–2906. [CrossRef]
12. Yuan, B.; Liu, M.-X.; Ng, W.T.; Lai, X.-Q. Hybrid Buck Converter with Constant Mode Changing Point and Smooth Mode Transition for High-Frequency Applications. *IEEE Trans. Ind. Electron.* **2020**, *67*, 1466–1474. [CrossRef]

13. Kim, S.J.; Choi, W.-S.; Pilawa-Podgurski, R.G.C.N.; Hanumolu, P.K. A 10-MHz 2–800-mA 0.5–1.5-V 90% Peak Efficiency Time-Based Buck Converter with Seamless Transition between PWM/PFM Modes. *IEEE J. Solid-State Circuits* **2017**, *53*, 814–824. [CrossRef]
14. Leung, K.K.-S.; Chung, H.S.-H. Dynamic hysteresis band control of the buck converter with fast transient response. *IEEE Trans. Circuits Syst. II Express Briefs* **2005**, *52*, 398–402. [CrossRef]
15. Su, F.; Ki, W.-H.; Tsui, C.-Y. Ultra Fast Fixed-Frequency Hysteretic Buck Converter with Maximum Charging Current Control and Adaptive Delay Compensation for DVS Applications. *IEEE J. Solid-State Circuits* **2008**, *43*, 815–822. [CrossRef]
16. Fu, W.; Tan, S.T.; Radhakrishnan, M.; Byrd, R.; Fayed, A. A DCM-Only Buck Regulator with Hysteretic-Assisted Adaptive Minimum-On-Time Control for Low-Power Microcontrollers. *IEEE Trans. Power Electron.* **2015**, *31*, 418–429. [CrossRef]
17. Redl, R.; Sun, J. Ripple-Based Control of Switching Regulators—An Overview. *IEEE Trans. Power Electron.* **2009**, *24*, 2669–2680. [CrossRef]
18. Nashed, M.; Fayed, A.A. Current-Mode Hysteretic Buck Converter With Spur-Free Control for Variable Switching Noise Mitigation. *IEEE Trans. Power Electron.* **2018**, *33*, 650–664. [CrossRef]
19. Yang, W.-H.; Huang, C.-J.; Huang, H.-H.; Lin, W.-T.; Chen, K.-H.; Lin, Y.-H.; Lin, S.-R.; Tsai, T.-Y. A Constant-on-Time Control DC–DC Buck Converter with the Pseudowave Tracking Technique for Regulation Accuracy and Load Transient Enhancement. *IEEE Trans. Power Electron.* **2017**, *33*, 6187–6198. [CrossRef]
20. Lin, Y.-C.; Chen, C.-J.; Chen, D.; Wang, B. A Ripple-Based Constant On-Time Control With Virtual Inductor Current and Offset Cancellation for DC Power Converters. *IEEE Trans. Power Electron.* **2012**, *27*, 4301–4310. [CrossRef]
21. Li, Y.-C.; Chen, C.-J.; Tsai, C.-J. A Constant On-Time Buck Converter with Analog Time-Optimized On-Time Control. *IEEE Trans. Power Electron.* **2020**, *35*, 3754–3765. [CrossRef]
22. Liu, W.-C.; Chen, C.-J.; Cheng, C.-H.; Chen, H.-J. A Novel Accurate Adaptive Constant On-Time Buck Converter for a Wide-Range Operation. *IEEE Trans. Power Electron.* **2019**, *35*, 3729–3739. [CrossRef]
23. Wong, L.; Man, T. Maximum frequency for hysteretic control COT buck converters. In Proceedings of the 13th International Power Electronics and Motion Control Conference, Poznań, Poland, 1–3 September 2008; pp. 475–478.
24. Nam, H.; Ahn, Y.; Roh, J. A buck converter with adaptive on-time PFM control and adjustable output voltage. *Analog. Integr. Circuits Signal Process.* **2011**, *71*, 327–332. [CrossRef]
25. Chuan, N.; Tateishi, T. Adaptive constant on-time (D-CAPTM) control study in notebook applications. In *TI Application Note SLVA281B*; Texas Instruments: Dallas, TX, USA, 2007.
26. Sahu, B. Analysis and design of a fully-integrated current sharing scheme for multi-phase adaptive on-time modulated switching regulators. In Proceedings of the 2008 IEEE Power Electronics Specialists Conference, Rhodes, Greece, 15–19 June 2008; pp. 3829–3835.
27. Sahu, B.; Rincon-Mora, G.A. An Accurate, Low-Voltage, CMOS Switching Power Supply With Adaptive On-Time Pulse-Frequency Modulation (PFM) Control. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2007**, *54*, 312–321. [CrossRef]
28. Tsai, C.-H.; Chen, B.-M.; Li, H.-L. Switching Frequency Stabilization Techniques for Adaptive On-Time Controlled Buck Converter With Adaptive Voltage Positioning Mechanism. *IEEE Trans. Power Electron.* **2016**, *31*, 443–451. [CrossRef]
29. Thi Kim Nga, T.; Park, S.-M.; Park, Y.-J.; Park, S.-H.; Kim, S.; Van Cong Thuong, T.; Lee, M.; Hwang, K.C.; Yang, Y.; Lee, K.-Y. A Wide Input Range Buck-Boost DC–DC Converter Using Hysteresis Triple-Mode Control Technique with Peak Efficiency of 94.8% for RF Energy Harvesting Applications. *Energies* **2018**, *11*, 1618. [CrossRef]
30. Ma, F.-F.; Chen, W.-Z.; Wu, J.-C. A Monolithic Current-Mode Buck Converter with Advanced Control and Protection Circuits. *IEEE Trans. Power Electron.* **2007**, *22*, 1836–1846. [CrossRef]
31. Lee, C.F.; Mok, P. A Monolithic Current-Mode CMOS DC–DC Converter with On-Chip Current-Sensing Technique. *IEEE J. Solid-State Circuits* **2004**, *39*, 3–14. [CrossRef]
32. Zeng, W.-L.; Ren, Y.; Lam, C.; Sin, S.-W.; Che, W.-K.; Ding, R.; Martins, R.P. A 470-nA Quiescent Current and 92.7%/94.7% Efficiency DCT/PWM Control Buck Converter with Seamless Mode Selection for IoT Application. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2020**, *67*, 4085–4098. [CrossRef]
33. Liou, W.-R.; Yeh, M.-L.; Kuo, Y.L. A High Efficiency Dual-Mode Buck Converter IC for Portable Applications. *IEEE Trans. Power Electron.* **2008**, *23*, 667–677. [CrossRef]
34. Chen, C.-L.; Hsieh, W.-L.; Lai, W.-J.; Chen, K.-H.; Wang, C.-S. A new PWM/PFM control technique for improving efficiency over wide load range. In Proceedings of the 2008 15th IEEE International Conference on Electronics, Circuits and Systems, St. Julien's, Malta, 31 August–3 September 2008; pp. 962–965.
35. Wong, L.; Man, T. Adaptive On-Time Converters. *IEEE Ind. Electron. Mag.* **2010**, *4*, 28–35. [CrossRef]
36. Siu, M.; Mok, P.K.T.; Leung, K.N.; Lam, Y.-H.; Ki, W.-H. A voltage-mode PWM buck regulator with end-point prediction. *IEEE Trans. Circuits Syst. II Express Briefs* **2006**, *53*, 294–298. [CrossRef]
37. Lu, M.-X.; Hwang, B.-H.; Chen, J.Y.; Hwang, Y.-S. A sub-1V voltage-mode DC-DC buck converter using PWM control technique. In Proceedings of the 2010 IEEE International Conference of Electron Devices and Solid-State Circuits (EDSSC), Hong Kong, China, 15–17 December 2010; pp. 1–4.
38. Huang, Q.; Zhan, C.; Burm, J. A 30-MHz Voltage-Mode Buck Converter Using Delay-Line-Based PWM Control. *IEEE Trans. Circuits Syst. II Express Briefs* **2017**, *65*, 1659–1663. [CrossRef]