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Comparative Analysis of SVM Techniques for a Five-Phase VSI Based on SiC Devices

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Abstract: Multiphase systems provides benefits compared to three-phase systems, such as improved torque per ampere, high power density, better fault tolerance, lower current per phase (due to power-splitting among a higher number of phases), and lower torque ripple, among others. Depending on the application, the system must meet determined requirements, such as the presence of harmonic content, power losses, and common-mode voltage (CMV) generation. This paper presents a comparative analysis of space vector modulation (SVM) techniques applied to a five-phase voltage source inverter with SiC switches to provide an overview of their performance. The performance of five-phase 2L SVPWM (space vector pulse width modulation), 2L+2M SVPWM, 4L SVPWM techniques, and their discontinuous versions, are analyzed by focusing on harmonic content, power losses, and CMV generation using SiC semiconductor devices. Matlab/Simulink and PLECS simulations are performed to achieve the above mentioned goal. The use of different techniques allows (1) reducing the harmonic distortion when 2L+2M SVPWM and 4L SVPWM are applied, and (2) the switching sequence of the modulation techniques can influence the switching losses. Therefore, the use of SiC switches reduces the switching losses. (3) However, CMV dv/dt increases. Therefore, it is possible to minimize the effects of the CMV dv/dt and amplitude by choosing the adequate technique.

Keywords: space vector modulation; five-phase inverter; discontinuous modulation; common-mode voltage; total harmonic distortion; power losses

1. Introduction

Multiphase machines were first introduced in the 1960s, but it was not until the early 2000s that researchers began to pay attention to them [1,2]. Most of the research has focused on control techniques such as field-oriented control (FOC) [3,4], predictive control [5–7], multi-machine control [8], third-order harmonic current injection for torque enhancement [9,10], and modulation techniques [11–16], among others. Some of the advantages of multiphase over three-phase machines are improved fault tolerance [17–19], improved torque per ampere, lower current per phase, higher reliability, more degrees of freedom, and a reduction in the amplitude of the torque pulsations when increasing their frequency [20]. Thus, these advantages make multiphase machines a better option for applications such as electric traction, eolic energy systems, and other high power industries.

Voltage source inverters (VSIs) are the most common and reliable equipment to feed and control multiphase machines. Similarly, as with three-phase inverters, the modulation techniques for multiphase machines are pulse width modulation (PWM) and space vector modulation (SVM). SVM techniques have their homolog PWM version. Depending on which SVM technique is homologating, its implementation can get complicated. Although SVMs become more complex due to the increase in the number of phases, they provide a clearer view of how the switching sequences

should be selected to achieve different behaviors such as the reduction of switching losses, better use of the DC-Bus voltage, and fault tolerance operation [21]. According to the implemented modulation technique, the VSI's performance will change [22–25].

This paper focuses on the SVM techniques applied to five-phase inverters using silicon carbide (SiC) switches. Figure 1 shows the structure of the five-phase inverter and the implemented load in this work. Because the load of the system is balanced and star-connected with an isolated neutral point, a five-phase system corresponds to a four-dimensional vector space. Applying decoupling transformations to the four-dimensional space two 2-D subspaces are obtained.

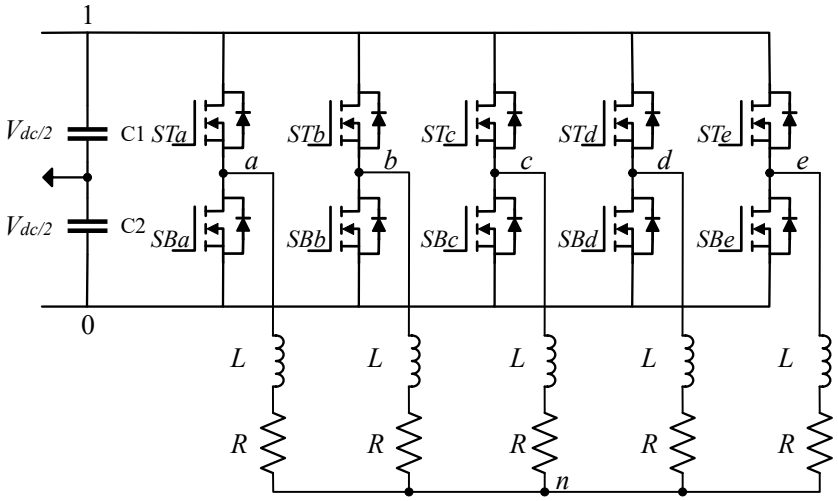


Figure 1. Basic structure of five-phase voltage source inverter (VSI).

Thus far, the three most developed SVM techniques are the two large vector space vector pulse width modulation (SVPWM), two large and two medium vector SVPWM, and four large vector SVPWM (2L SVPWM, 2L+2M SVPWM, and 4L SVPWM respectively). A comparative study of the third- and seventh-order voltage harmonics generated by the 2L SVPWM and 2L+2M SVPWM modulation techniques was conducted [26]. The flux harmonic distortion factor (HDF) was examined [27,28] considering the 2L+2M SVPWM and 4L SVPWM modulation techniques together with their corresponding discontinuous versions.

Interest in wide band-gap (WBG) power devices has increased over time, resulting in the maturation of this technology. This is especially true for SiC devices, which can operate at high temperatures, higher switching frequencies, and higher voltages [29]. Not only is SiC technology mature, but SiC devices are currently readily available in the electronic marketplace. SiC loses less power than conventional silicon devices [30,31]. Thus, the efficiency of the system improves when using SiC devices [32], which are rated to operate at 175 °C; theoretically, they can operate at temperatures as high as 500 °C [33]. The main reason current commercial SiC devices are manufactured for operating at rated temperatures of 175 °C is because of limitations in packaging technology [34].

Operating at high switching frequencies provides systems with fast control response, reduced passive component size, and smaller (therefore less expensive) filters size. In motor applications, high switching frequency causes a lower amplitude torque ripple and high motor efficiency, among other benefits. However, high-frequency modulation techniques produce effects that damage motors. One of these effects is the high dv/dt produced through the motor terminals, which can damage or break down its insulation due to the leakage current [35]. Modulation techniques at high frequencies generate a high common-mode voltage (CMV). CMV produces shaft voltage that exceeds the breakdown voltage of the grease film. Therefore, the discharge current caused by this voltage flows through the bearings. This bearing current causes an increase in electrical erosion, which leads to bearing failure [36–38]. Thus, despite the benefits of SiC devices, modulation techniques are needed to reduce both the amplitude of the CMV and the frequencies where CMV peaks

occur. The amplitude of the CMV combined with its high dv/dt create a pulsating common-mode current (CMC), whose high-frequency content is source of electromagnetic interference (EMI) [39]. Other consequences of the CMV are winding insulation damage, mechanical vibrations, and even total motor failure. These effects are even more pronounced when using SiC switches. Therefore, CMV generation is an important topic for researchers. Some solutions developed for reducing CMV are presented in [40–43], all of which implement modulation techniques or develop hardware for achieving this objective.

In [44], the continuous modulation techniques were comprehensively analyzed based on the harmonic content, power losses, and CMV generation. The novelty and contribution of the current work is the analysis of 12 discontinuous modulation techniques based on the total harmonic distortion (THD), inverter efficiency, and CMV generation. The performance of the 12 techniques was compared with that of the three continuous modulation techniques to present a complete overview of the differences between the application of continuous and discontinuous modulation techniques. CMV was analyzed by considering the dv/dt and its frequency components. To accomplishing these objectives, simulation results were obtained using Matlab (R2018b, MathWorks, Natick, MA, USA)/Simulink (V9.2, MathWorks, Natick, MA, USA) and PLECS software (V4.2.5, Plexim, Zurich, Switzerland). Experimental tests were performed to verify and prove the simulation results.

The rest of this paper is organized as follows: Section 2 introduces the basis of the five-phase SVM techniques. Section 3 describes the behavior of the SVM techniques mentioned in Section 2 by simulation with Matlab/Simulink and PLECS software. In Section 3, experimental results are described that validate the simulation results. In Section 4, the materials and equipment used to perform this analysis are described. Finally, the conclusions are summarized in Section 5.

2. Five-Phase SVM

In a five-phase electrical system that is assumed to have a balanced load while being star-connected with an isolated neutral point, it is possible to apply a decoupling transformation matrix to the five reference voltages. In this case, we use Clarke's transformation [45] to obtain two 2D subspaces as shown in Figure 2. The first subspace, named d_1-q_1, contains harmonics on the order of $10k \pm 1$ ($k = 0, 1, 2, 3, \ldots$). The second subspace, d_2-q_2, contains harmonics on the order of $10k \pm 3$ ($k = 0, 1, 2, 3, \ldots$). The implementation of two-dimensional subspaces helps to simplify how the vectors should be applied to reach the reference vector and, according to the selected switching sequence, it is possible to obtain different performance, such as a harmonic injection, reduction of switching losses, and CMV waveform, among others [44]. Using only the subspace d_1-q_1 reduces the harmonic content of order $10k \pm 3$. However, when the d_2-q_2 subspace is used, it is possible to control the injection of the harmonics of order $10k \pm 3$. Nevertheless, this characteristic was not considered in this work.

Both subspaces are divided into 10 sectors and comprise 32 vectors, which are divided into 2 zero vectors as well as 10 small (in green color), 10 medium (in red color), and 10 large active vectors (in blue color). The magnitudes of the vectors on subspace d_1-q_1 are defined in Table 1. The long vectors in subspace d_1-q_1 are represented as small vectors in subspace d_2-q_2. Conversely, the small vectors in subspace d_1-q_1 are represented as long vectors in subspace d_2-q_2.

The vectors obtain their names according to the inverter leg switching operation based on binary code. Reading from left is the most significant bit, reading from the right is the least significant bit; each digit of the binary code represents the switching state of the legs 'abcde'. The switching states are represented by 1 and 0, which indicate the output voltage levels of $+\frac{V_{dc}}{2}$ and $-\frac{V_{dc}}{2}$, respectively, which correspond to the midpoint of the DC-Bus. Figure 3 shows the switching state of the vector '25'(11001), where the red switches are in a closed state and black switches are in an open state.

The instantaneous phase voltages of each leg are expressed as follows:

$$V_n = V_{dc} \times \left[S_n - \frac{1}{5}(S_a + S_b + S_c + S_d + S_e) \right], \quad (1)$$

where S_n ($n = a, b, c, d, e$) is the switching state of each one of the legs (1 or 0), V_n the instantaneous phase voltage,and V_{dc} the DC-Bus voltage.

Figure 4 shows the 15 SVMs implemented in this paper. 2L SVPWM, 2L+2M SVPWM, and 4L SVPWM are the modulation techniques that were analyzed, together with their four discontinuous versions: discontinuous pulse width modulation-maximum (DPWM-MAX), discontinuous pulse width modulation-minimum (DPWM-MIN), discontinuous pulse width modulation-version 1 (DPWM-V1), and discontinuous pulse width modulation-version 2 (DPWM-V2), respectively.

DPWM-MAX does not use the zero vector V_0 (00000) in the switching sequence, thus causing each leg of the inverter to be in the on-state for a determined amount of time. DPWM-MIN has the opposite effect: rather than stopping using the zero vector V_0, this version does not apply the zero vector V_{31} (11111); therefore, each leg of the inverter will be in the off-state for a determined amount of time.

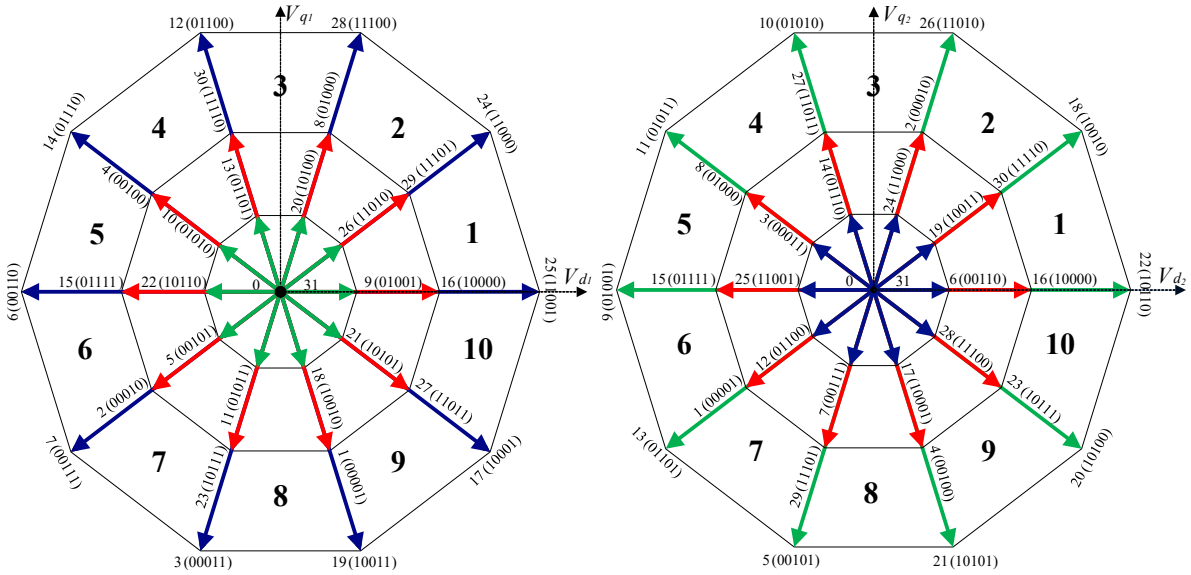


Figure 2. Two-dimension subspaces: (**a**) d_1-q_1 subspace, and (**b**) d_2-q_2 subspace.

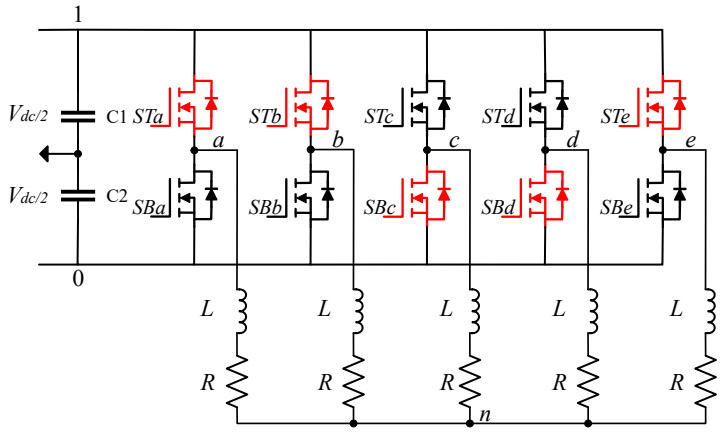


Figure 3. Vector '25'(11001) switching operation.

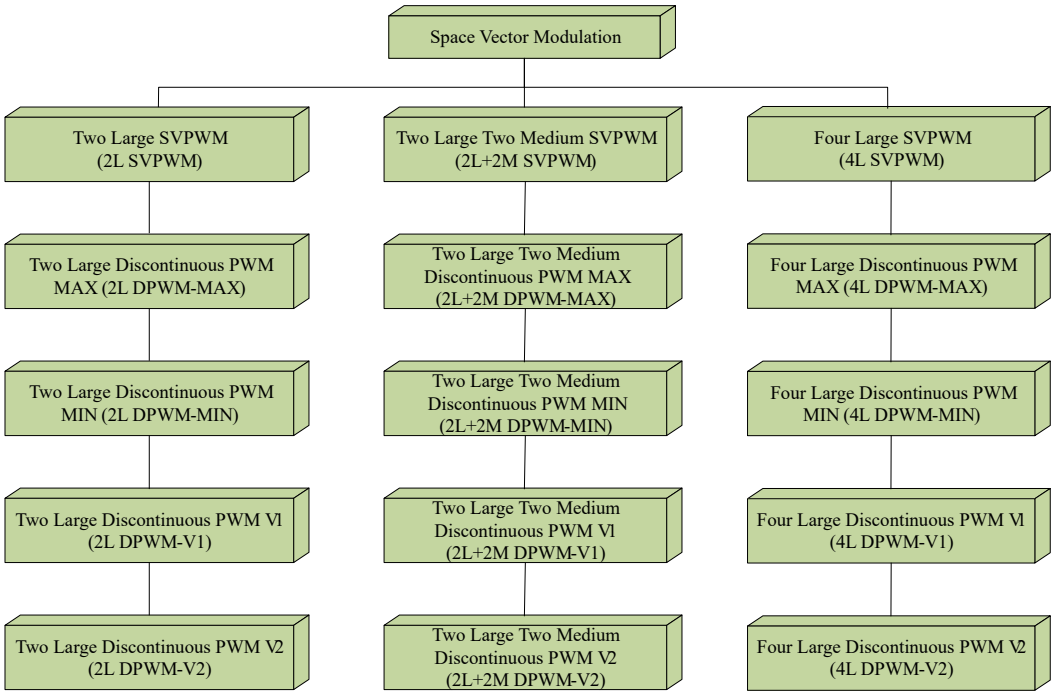


Figure 4. Five-phase inverter space vector modulation.

Table 1. Vectors' magnitudes on the d_1-q_1 subspace.

Vector	Magnitude
Zero vector	$0 * \frac{V_{dc}}{2}$
Small vector	$0.4944 * \frac{V_{dc}}{2}$
Medium vector	$0.8 * \frac{V_{dc}}{2}$
Large vector	$1.2944 * \frac{V_{dc}}{2}$

DPWM-V1 and DPWM-V2 intercalate the disabled zero vectors according to the sector in which the reference vector is located. Hence, if the reference vector is in an odd sector, vector V_{31} is not used for DPWM-V1 and vector V_0 is not used for DPWM-V2. Alternatively, if the reference vector is in an even sector, vector V_0 is not used for DPWM-V1 and vector V_{31} is not used for DPWM-V2.

Table 2 summarizes the references on the modulation techniques used in this work. In the following sections, the modulation techniques applied in this work are briefly defined based on their harmonic content, maximum modulation index, and switching sequence.

Table 2. Reference summary of five-phase SVM techniques.

SVM Technique	References
Two large vectors (2L SVPWM)	[26,46]
Two large and two medium vectors (2L+2M SVPWM)	[26,28,46,47]
Four large vectors (4L SVPWM)	[27,28]
Discontinuous SVM	[28]

2.1. Two Large Vector SVPWM (2L SVPWM)

2L SVPWM operates similarly to space vector modulation for a three-phase inverter. This modulation applies two large active vectors and two zero vectors. One of the features of 2L SVPWM is that it generates low-order harmonic content, especially third-order harmonics. This modulation technique has a modulation index (mi) of 1.2311, which is higher than the modulation index of the other modulation techniques. Hence, applying this technique delivers more current to the

system due to the increase of the DC-Bus use. Figure 5 shows the switching sequence for 2L SVPWM, its filtered output voltage waveform, and the voltage referenced to the DC-Bus midpoint. The main reason for showing the voltage referenced to the DC-bus midpoint is to observe if the technique presents a discontinuity. For this case, no discontinuity was applied. The switching sequence for the odd sectors is V_0, V_B, V_A, V_{31}, V_A, V_B, V_0; for the even sectors, it is V_0, V_A, V_B, V_{31}, V_B, V_A, V_0.

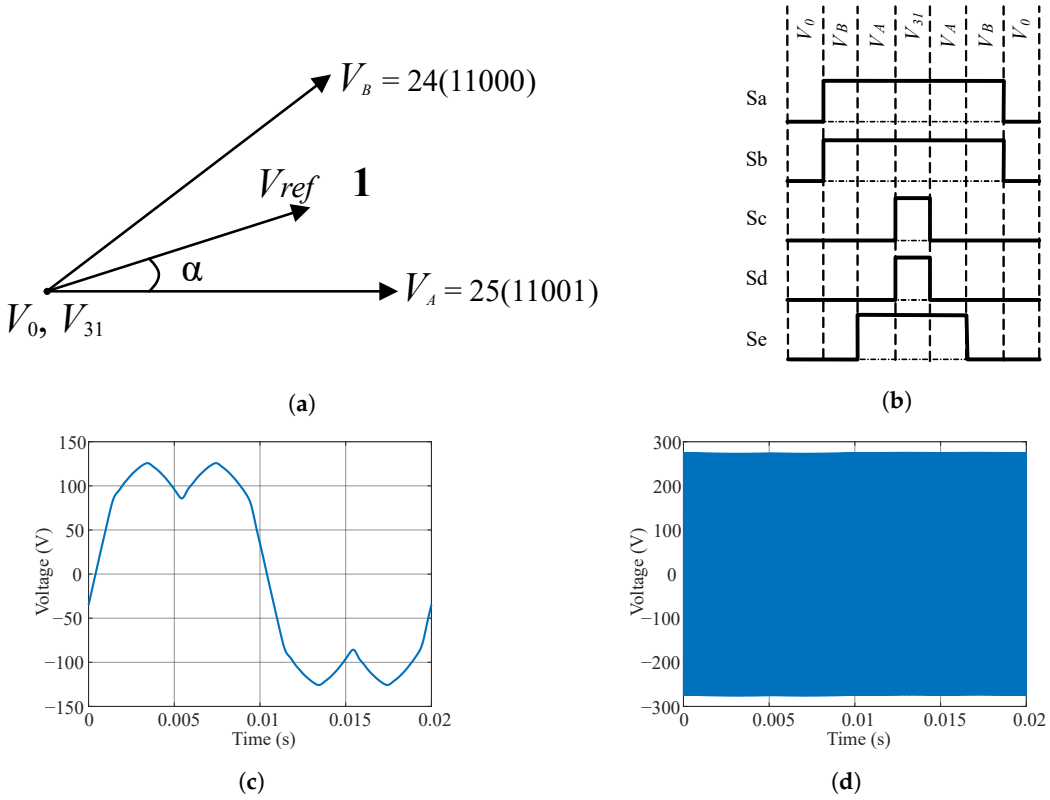


Figure 5. 2L SVPWM modulation technique with a modulation index of 0.5: (**a**) Sector 1 applied vectors, (**b**) odd sector switching sequence, (**c**) filtered output voltage, and (**d**) voltage reference to the DC-Bus midpoint.

Table 3 lists the switching sequence for the discontinuous versions of the 2L SVPWM modulation technique.

Table 3. Switching sequence for 2L SVPWM discontinuous modulation techniques.

Version	Odd Sector	Even Sector
2L DPWM-MAX	V_B, V_A, V_{31}, V_A, V_B	V_A, V_B, V_{31}, V_B, V_A
2L DPWM-MIN	V_0, V_B, V_A, V_B, V_0	V_0, V_A, V_B, V_A, V_0
2L DPWM-V1	V_0, V_B, V_A, V_B, V_0	V_A, V_B, V_{31}, V_B, V_A
2L DPWM-V2	V_B, V_A, V_{31}, V_A, V_B	V_0, V_A, V_B, V_A, V_0

2.2. Two Large and Two Medium Vector SVPWM (2L+2M SVPWM)

This technique uses two large vectors, two medium vectors, and two zero vectors. 2L+2M SVPWM, generates lower harmonic content than 2L SVPWM, and the presence of low-order harmonics is almost null. Furthermore, its maximum modulation index is 1.0515. The switching losses are minimized due to the presence of medium vectors. Figure 6 shows the switching sequence for 2L+2M SVPWM, its filtered output voltage waveform, and the voltage referenced to the DC-Bus midpoint. For the odd sectors, the switching sequence is V_0, V_{AM}, V_{BL}, V_{AL}, V_{BM}, V_{31}, V_{BM}, V_{AL}, V_{BL}, V_{AM},

V_0; for the even sectors, it is V_0, V_{BM}, V_{AL}, V_{BL}, V_{AM}, V_{31}, V_{AM}, V_{BL}, V_{AL}, V_{BM}, V_0. Table 4 list the switching sequence for the discontinuous versions of the 2L+2M SVPWM modulation technique.

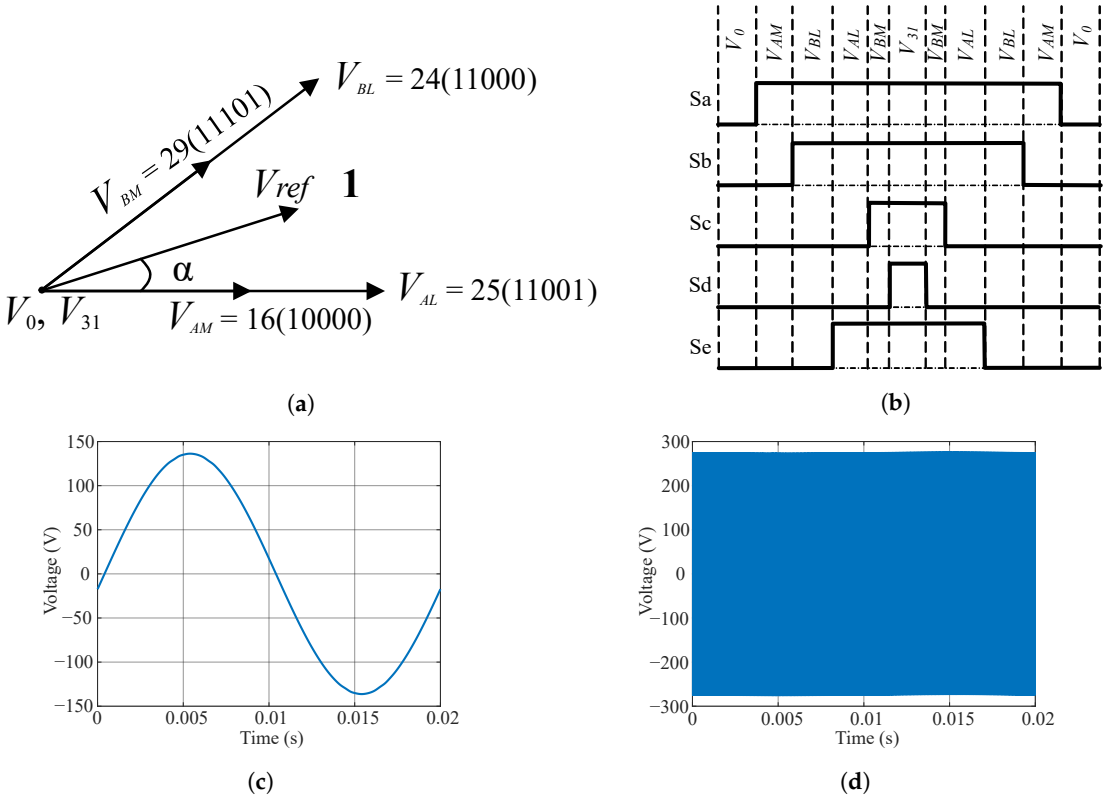


Figure 6. 2L+2M SVPWM modulation technique with a modulation index of 0.5: (**a**) Sector 1 applied vectors, (**b**) odd sector switching sequence, (**c**) filtered output voltage, and (**d**) voltage reference to the DC-Bus midpoint.

Table 4. Switching sequence for 2L+2M SVPWM discontinuous modulation techniques.

Version	Odd Sector	Even Sector
2L+2M DPWM-MAX	V_{AM}, V_{BL}, V_{AL}, V_{BM}, V_{31}, V_{BM}, V_{AL}, V_{BL}, V_{AM}	V_{BM}, V_{AL}, V_{BL}, V_{AM}, V_{31}, V_{AM}, V_{BL}, V_{AL}, V_{BM}
2L+2M DPWM-MIN	V_0, V_{AM}, V_{BL}, V_{AL}, V_{BM}, V_{AL}, V_{BL}, V_{AM}, V_0	V_0, V_{BM}, V_{AL}, V_{BL}, V_{AM}, V_{BL}, V_{AL}, V_{BM}, V_0
2L+2M DPWM-V1	V_0, V_{AM}, V_{BL}, V_{AL}, V_{BM}, V_{AL}, V_{BL}, V_{AM}, V_0	V_{BM}, V_{AL}, V_{BL}, V_{AM}, V_{31}, V_{AM}, V_{BL}, V_{AL}, V_{BM}
2L+2M DPWM-V2	V_{AM}, V_{BL}, V_{AL}, V_{BM}, V_{31}, V_{BM}, V_{AL}, V_{BL}, V_{AM}	V_0, V_{BM}, V_{AL}, V_{BL}, V_{AM}, V_{BL}, V_{AL}, V_{BM}, V_0

2.3. Four Large Vector SVPWM (4L SVPWM)

4L SVPWM modulation applies four large vectors to generate a sinusoidal output voltage signal. Similar to 2L+2M SVPWM, 4L SVPWM has low harmonic content. Its maximum modulation index is 1.0515. This modulation has higher switching losses than the other modulations. However, one advantage of this modulation is the reduction in the amplitude of the common-mode voltage when compared with the other modulation techniques. Figure 7 shows the switching sequence for 4L SVPWM, its filtered output voltage waveform, and the voltage referenced to the DC-Bus midpoint. For the odd sectors, the switching sequence is V_0, V_{CL}, V_{AL}, V_{BL}, V_{DL}, V_{31}, V_{DL}, V_{BL}, V_{AL}, V_{CL}, V_0; for the even sectors, it is V_0, V_{DL}, V_{BL}, V_{AL}, V_{CL}, V_{31}, V_{CL}, V_{AL}, V_{BL}, V_{DL}, V_0. Table 5 lists the switching sequences for the discontinuous versions of the 4L SVPWM modulation technique.

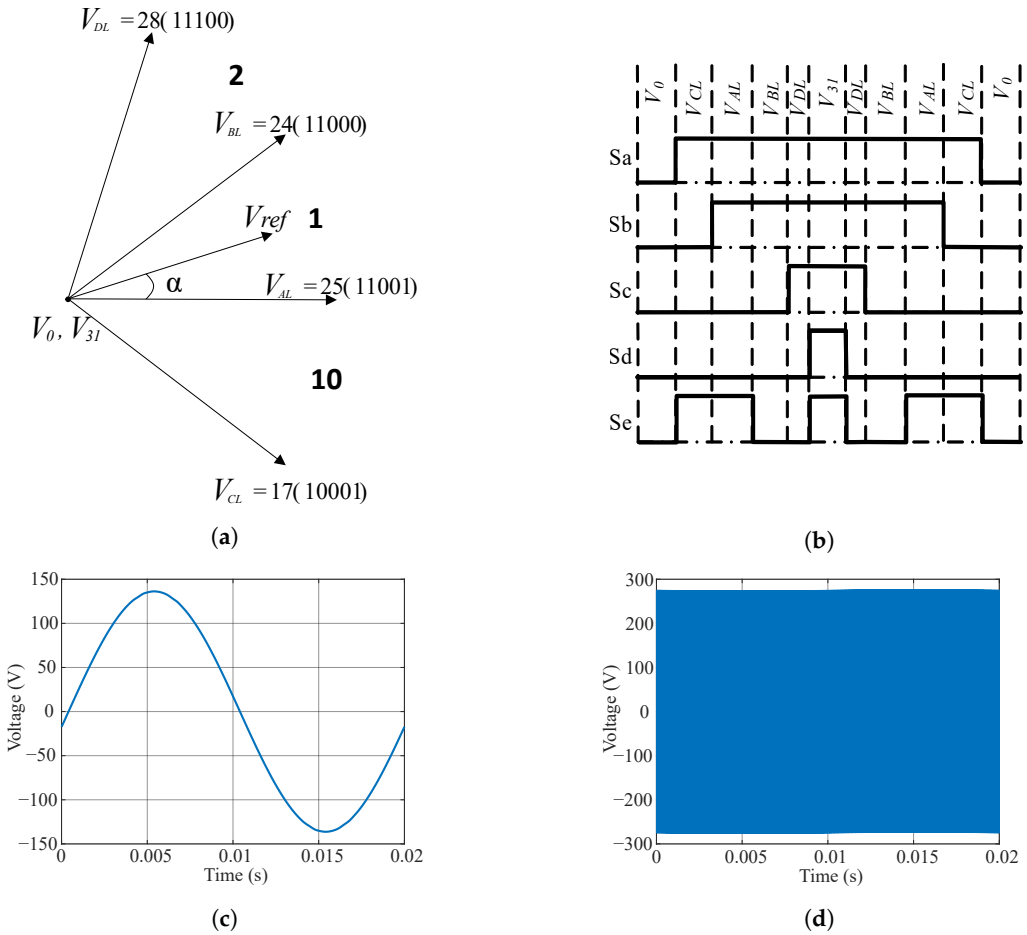


Figure 7. 4L SVPWM modulation technique with a modulation index of 0.5: (**a**) Sector 1 applied vectors, (**b**) odd sector switching sequence, (**c**) filtered output voltage, and (**d**) voltage reference to the DC-Bus midpoint.

Table 5. Switching sequence for 4L SVPWM discontinuous modulation techniques.

Version	Odd Sector	Even Sector
4L DPWM-MAX	$V_{CL}, V_{AL}, V_{BL}, V_{DL}, V_{31}, V_{DL}, V_{BL}, V_{AL}, V_{CL}$	$V_{DL}, V_{BL}, V_{AL}, V_{CL}, V_{31}, V_{CL}, V_{AL}, V_{BL}, V_{DL}$
4L DPWM-MIN	$V_0, V_{CL}, V_{AL}, V_{BL}, V_{DL}, V_{BL}, V_{AL}, V_{CL}, V_0$	$V_0, V_{DL}, V_{BL}, V_{AL}, V_{CL}, V_{AL}, V_{BL}, V_{DL}, V_0$
4L DPWM-V1	$V_0, V_{CL}, V_{AL}, V_{BL}, V_{DL}, V_{BL}, V_{AL}, V_{CL}, V_0$	$V_{DL}, V_{BL}, V_{AL}, V_{CL}, V_{31}, V_{CL}, V_{AL}, V_{BL}, V_{DL}$
4L DPWM-V2	$V_{CL}, V_{AL}, V_{BL}, V_{DL}, V_{31}, V_{DL}, V_{BL}, V_{AL}, V_{CL}$	$V_0, V_{DL}, V_{BL}, V_{AL}, V_{CL}, V_{AL}, V_{BL}, V_{DL}, V_0$

2.4. Discontinuous Space Vector Modulation

In this paper, the discontinuous modulations constitute modified techniques that allow maintaining a switching device's turn-on or turn-off state to increase its conduction time during zero vectors and when decreasing the switching states during zero vectors. The discontinuous versions implemented in this work are DPWM-MAX, DPWM-MIN, DPWM-V1, and DPWM-V2. Thus, the switching sequences of the discontinuous techniques for 2L SVPWM, 2L+2M SVPWM, and 4L SVPWM modulations are listed in Tables 3–5, respectively.

2.4.1. DPWM-MAX

This discontinuous version disables zero vector V_0 and uses only zero vector V_{31}. The activation time of V_0 is added to V_{31}; consequently, the upper switches for each leg of the inverter will remain in the on-state for a longer period of time. This modulation causes the lower switches to suffer less wastage because their switching states and on-times are reduced. Figure 8 shows the output waveform and voltage reference to the midpoint of the DC-Bus. The applied discontinuity can be observed in the voltage referenced to the DC-Bus midpoint as shown in Figure 8d–f. The upper switch of the leg remains closed during a determined time, and the V_0 switching state never occurs, allowing the reduction of the switching losses. The output voltage waveform remains similar to their corresponding continuous modulation technique. 2L DPWM-MAX presents a longer discontinuity due to the application of only two active vectors. Thus, each vector activation time is longer compared to those of 2L+2M DPWM-MAX and 4L DPWM-MAX that use four active vectors.

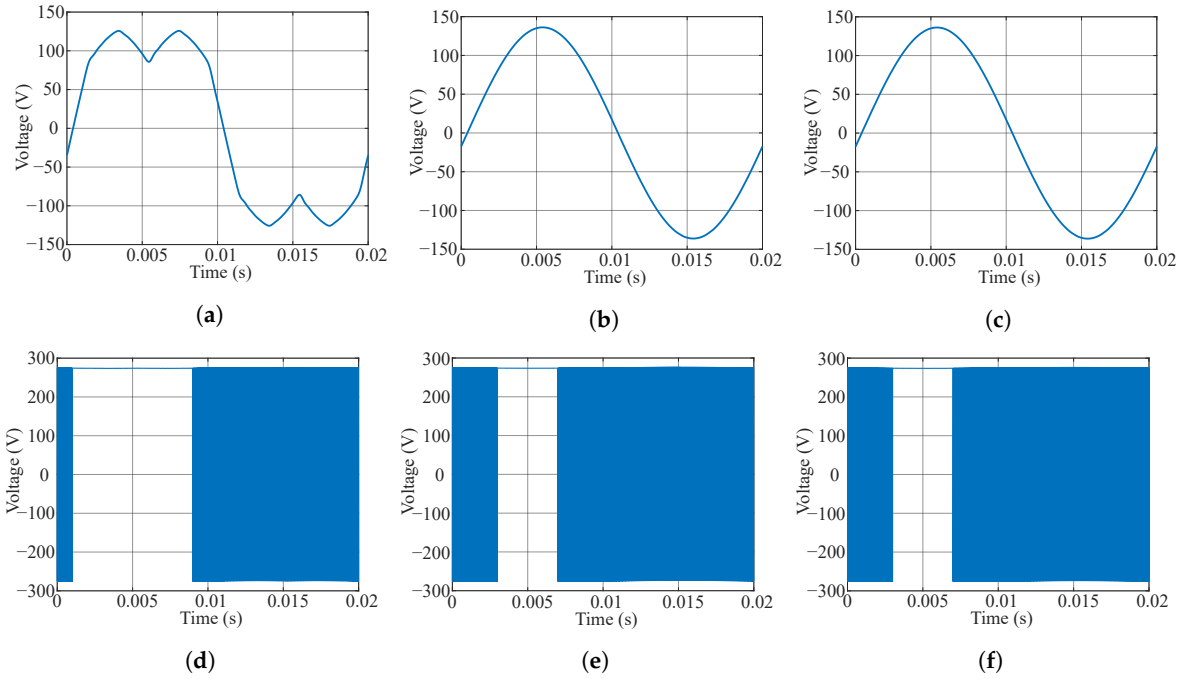


Figure 8. DPWM-MAX modulation techniques with modulation index of 0.5: (**a**) 2L-filtered output voltage, (**b**) 2L+2M-filtered output voltage, (**c**) 4L-filtered output voltage, (**d**) 2L voltage reference to the DC-Bus midpoint, (**e**) 2L+2M voltage reference to the DC-Bus midpoint, and (**f**) 4L voltage reference to the DC-Bus midpoint.

2.4.2. DPWM-MIN

Unlike DPWM-MAX modulation, DPWM-MIN modulation disables any application of vector V_{31} and add its activation time to V_0. Thus, the lower switches of each leg of the inverter remain in the on-state for a longer period of time. Therefore, the upper switches suffer less wastage because their operation times are reduced. Figure 9 shows the output waveform and voltage reference to the DC-Bus midpoint. Figure 9d–f show how the discontinuity is applied. The lower switch of the leg remains closed during a determined time, and the V_{31} switching state never occurs, reducing the switching losses. The output voltage waveform remains similar to their corresponding continuous modulation technique. As in the DPWM-MAX techniques, 2L DPWM-MIN presents a longer discontinuity due to the application of only two active vectors. Therefore, its switching losses are lower than the 2L+2M DPWM-MIN and 4L DPWM-MIN.

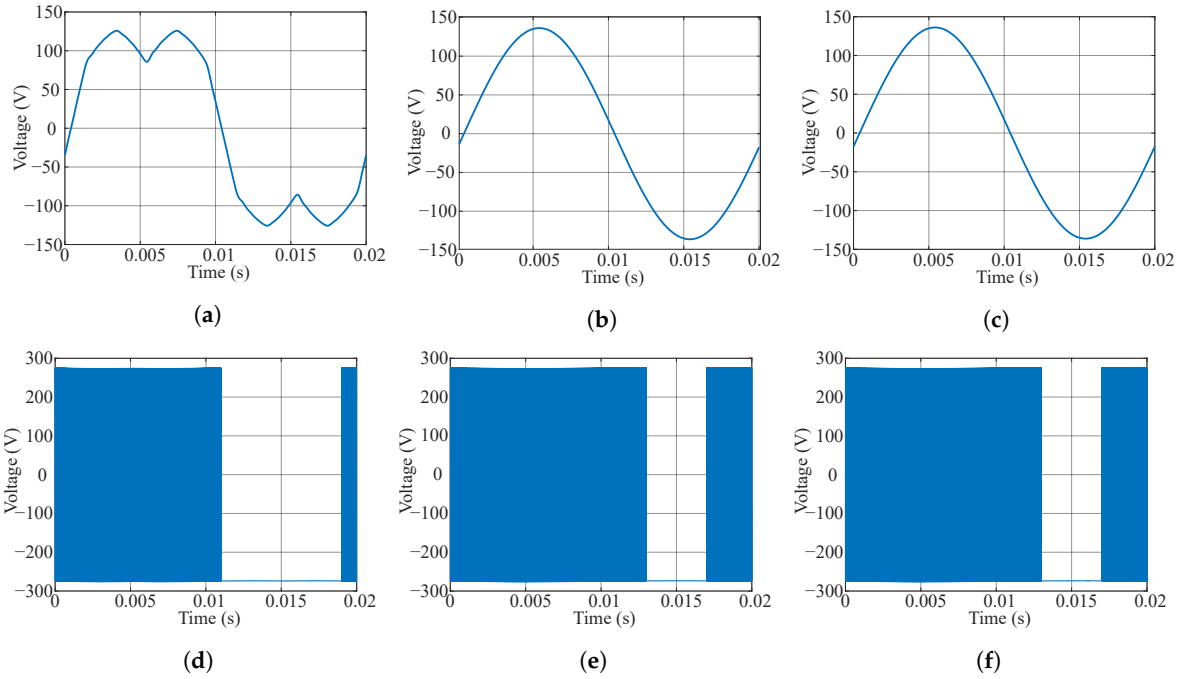


Figure 9. DPWM-MIN modulation techniques with modulation index of 0.5: (**a**) 2L-filtered output voltage, (**b**) 2L+2M-filtered output voltage, (**c**) 4L-filtered output voltage, (**d**) 2L voltage reference to the DC-Bus midpoint, (**e**) 2L+2M voltage reference to the DC-Bus midpoint, and (**f**) 4L voltage reference to the DC-Bus midpoint.

2.4.3. DPWM-V1 and DPWM-V2

The DPWM-V1 and DPWM-V2 modulation techniques are a combination of the DPWM-MAX and DPWM-MIN modulation techniques. In DPWM-V1, vector V_{31} is not used if the reference vector is in an odd sector; vector V_0 is disabled when the reference vector is in an even sector. Alternatively, DPWM-V2 operates inversely by disabling vector V_0 when the reference vector is in an odd sector; vector V_{31} is disabled when the reference vector is in an even sector. Figure 10 shows the output waveform and voltage reference to the DC-Bus midpoint when DPWM-V1 is applied. According of the location of the reference vector, the discontinuity is applied as shown in Figure 10d–f. These techniques reduce the switching losses by sharing the discontinuity symmetrically. Furthermore, the output voltage waveform is similar to their corresponding continuous modulation technique.

Some benefits of using discontinuous modulation are:

- Less stress on the semiconductor devices, depending on which version is applied;
- Lower switching losses than those of their corresponding continuous modulation;
- Good relationship of harmonic content with its continuous versions;
- Reduction of the CMV dv/dt transitions.

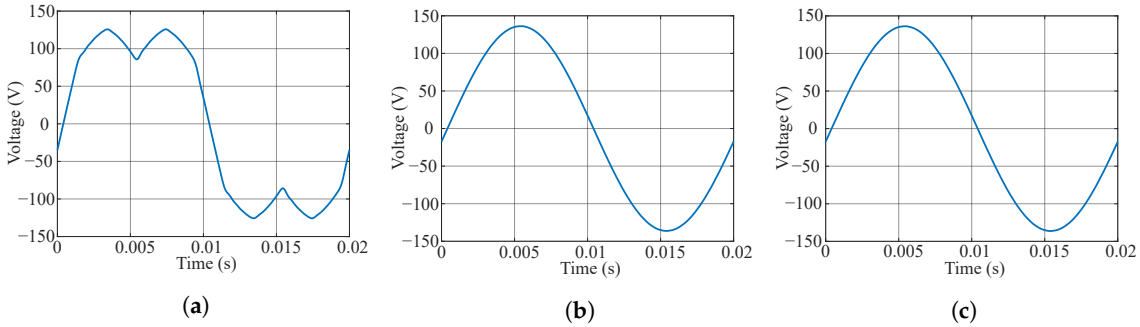


Figure 10. *Cont.*

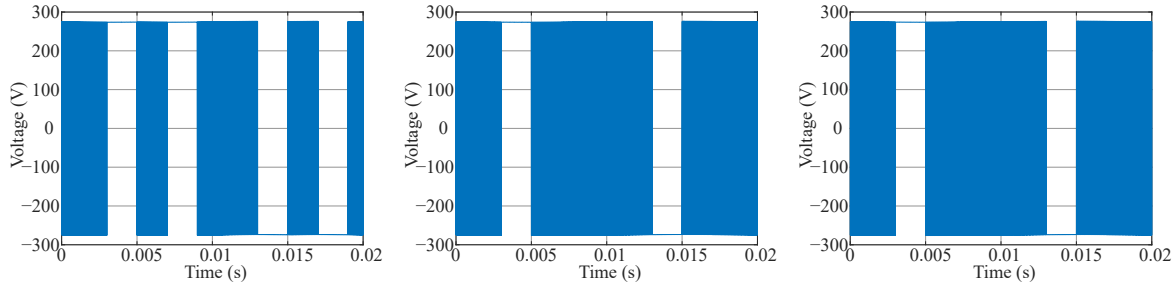


Figure 10. DPWM-V1 modulation techniques with modulation index of 0.5: (**a**) 2L-filtered output voltage, (**b**) 2L+2M-filtered output voltage, (**c**) 4L-filtered output voltage, (**d**) 2L voltage reference to the DC-Bus midpoint, (**e**) 2L+2M voltage reference to the DC-Bus midpoint, and (**f**) 4L voltage reference to the DC-Bus midpoint.

One drawback of the DPWM-V1 and DPWM-V2 modulation techniques is the energy of CMV-frequency components. At a lower modulation index, the energy of the CMV-frequency components is higher. For a modulation index close to 1, the energy of the CMV-frequency components decreases.

3. Results

3.1. Simulation Results

Our results were obtained through Matlab/Simulink and PLECS simulations. Figure 11 shows the Matlab/Simulink and PLECS simulation scheme. The modulation techniques were implemented using Matlab/Simulink. Meanwhile, the inverter was modeled in PLECS directly using the SiC parameters from the component manufacturer, to calculate the semiconductor power losses. The load is a resistor-inductance (RL) star-connected. The modulation index of the reference voltage increased in 0.1 intervals until it reached a modulation index of 1.0515. Then, we compared the total harmonic distortion (THD), weighted total harmonic distortion (WTHD), common-mode voltage (CMV), power losses, and efficiency. Table 6 contains the simulation parameters used in this document. The SiC power device used in the simulation was a Cree MOSFET C2M0160120D; its electrical properties are listed in Table 7. Figure 12 shows two power loss look-up tables of the Cree MOSFET C2M0160120D used to perform the power loss calculations in PLECS. These tables are according to the current, voltage, and junction temperature applied to the SiC devices. Figure 12a describes the turn-on losses of the SiC MOSFETs, while Figure 12b defines their conduction losses. There is another look-up table, similar to Figure 12a, for the turn-off losses of the semiconductors.

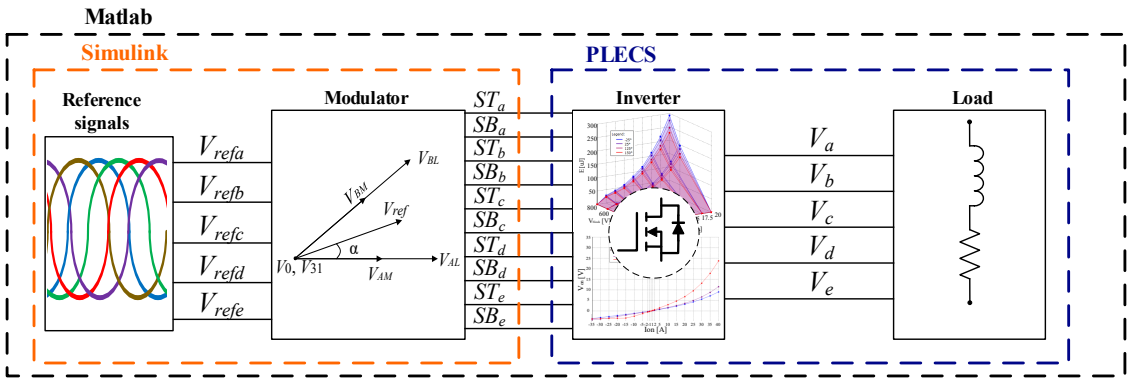


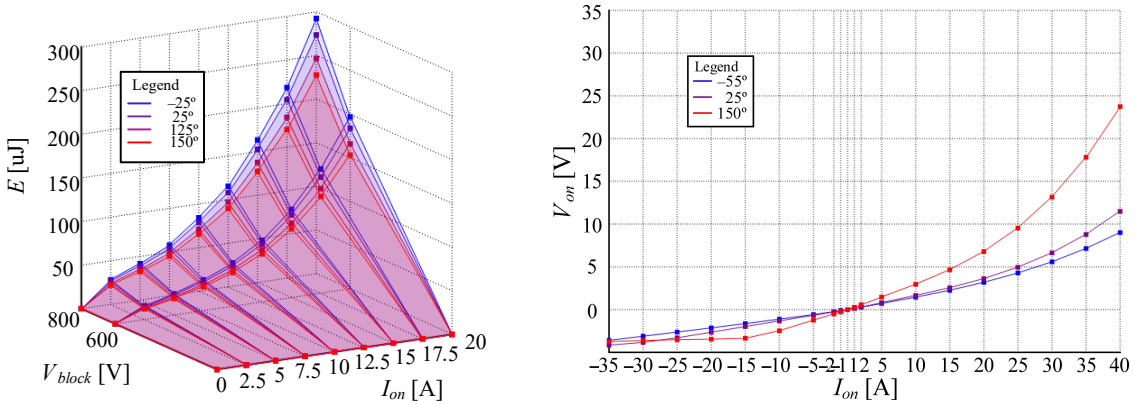
Figure 11. Matlab/Simulink and PLECS simulation scheme.

Table 6. Simulation parameters.

Parameter	Value
Resistance, R	34 Ω
Inductance, L	6 mH
DC-Bus	550 V
Fundamental frequency	50 Hz
Switching frequency	50 kHz
External gate resistor, Rg(ext)	6.5 Ω
Junction temperature	125 °C

Table 7. C2M0160120D electrical characteristics.

Parameter	Value
Breakdown voltage, V_{block}	1200 V
Drain current, I	19 A
Gate-source voltage max	−10/+25 V
Gate-source voltage used	−5/+20 V
On-state resistance, $R_{DS(on)}$	290 mΩ
Diode forward voltage	3.1 V
Continuous diode forward current	19 A



(**a**) (**b**)

Figure 12. Power loss look-up tables of C2M0160120D: (**a**) Turn-on losses; and (**b**) conduction losses.

3.1.1. Analysis of Total Harmonic Distortion (THD) and Weighted Total Harmonic Distortion (WTHD)

THD and WTHD were used to evaluate the output voltages. These are defined as follows:

$$THD(\%) = 100\sqrt{\frac{\sum_{n=2}^{\infty} V_{n,RMS}^2}{V_{1,RMS}^2}}, \quad (2)$$

where $V_{n,RMS}$ is the RMS value voltage of the n-harmonic component, and $V_{1,RMS}$ is the RMS value of the voltage fundamental component.

$$WTHD(\%) = 100\sqrt{\frac{\sum_{n=2}^{\infty} \frac{V_{n,RMS}}{n}^2}{V_{1,RMS}^2}}, \quad (3)$$

where n is the harmonic component, $V_{n,RMS}$ is the RMS value voltage of the n-harmonic component, and $V_{1,RMS}$ is the RMS value of the voltage fundamental component.

Figure 13 shows the output voltage THD. 2L SVPWM and its discontinuous versions have higher THD due to the presence of low-order harmonics. Figure 14 validates this statement, as 2L SVPWM modulation has higher WTHD due to the presence of third- and seventh-order harmonics. All the 2L+2M SVPWM and 4L SVPWM modulation harmonic contents decrease considerably as the modulation index increases.

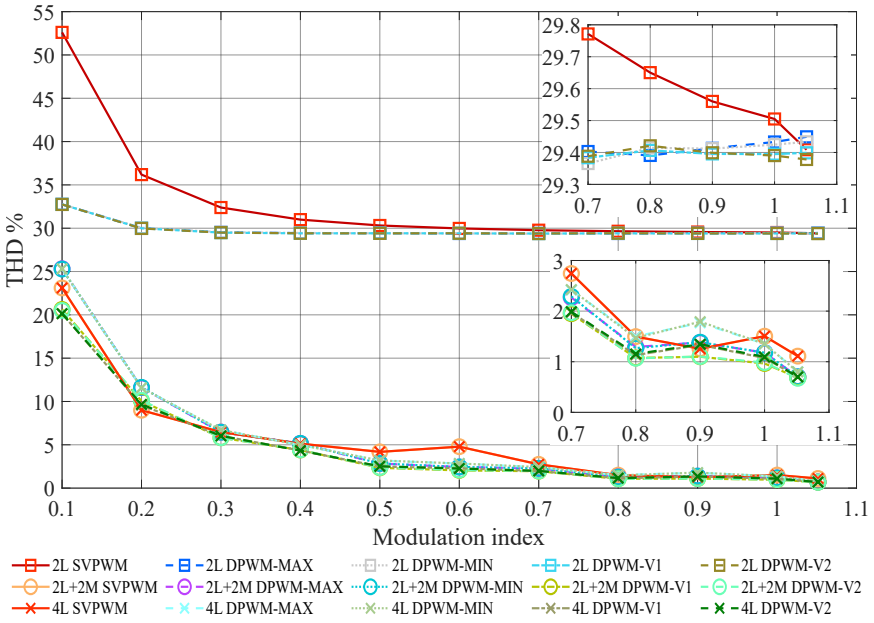


Figure 13. Output voltage total harmonic distortion (THD) comparison.

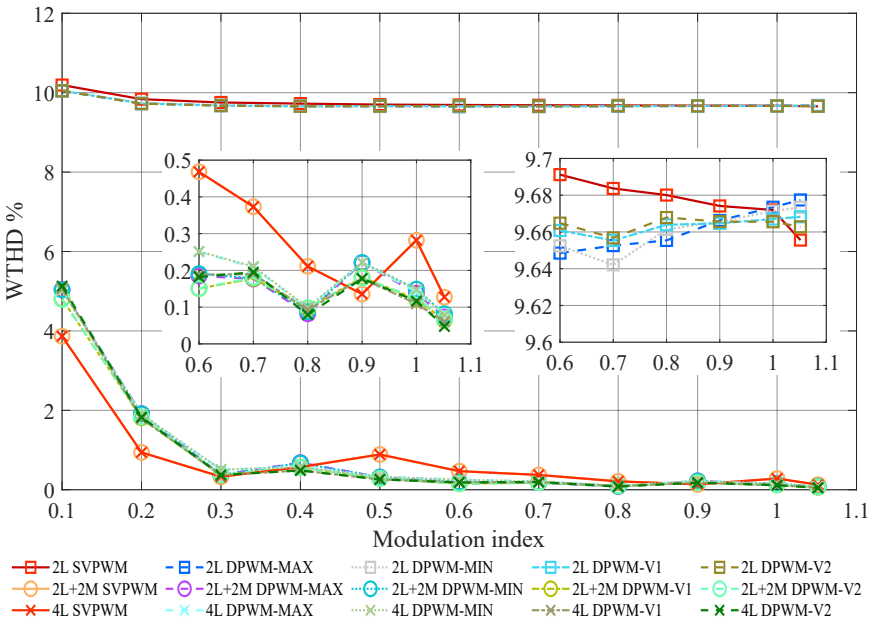


Figure 14. Output voltage weighted total harmonic distortion (WTHD) comparison.

3.1.2. Common-Mode Voltage (CMV) Analysis

In electrical machines applications, CMV causes bearing failures, mechanical vibrations, winding insulation damage, and EMIs. Each modulation generates a different CMV depending on the type of vector applied. Table 8 shows the CMV values generated for every vector in the d_1-q_1 space.

Table 8. Common-mode voltage (CMV) values of each vector on d_1-q_1.

Vector	CMV Value
Zero vector	0.5 * V_{dc}
Small vector	0.1 * V_{dc}
Medium vector	0.3 * V_{dc}
Large vector	0.1 * V_{dc}

To illustrate the behavior of the CMV waveforms generated by different modulation techniques, Figure 15 shows the CMV waveforms of the 2L SVPWM, 2L+2M SVPWM, and 4L SVPWM techniques.

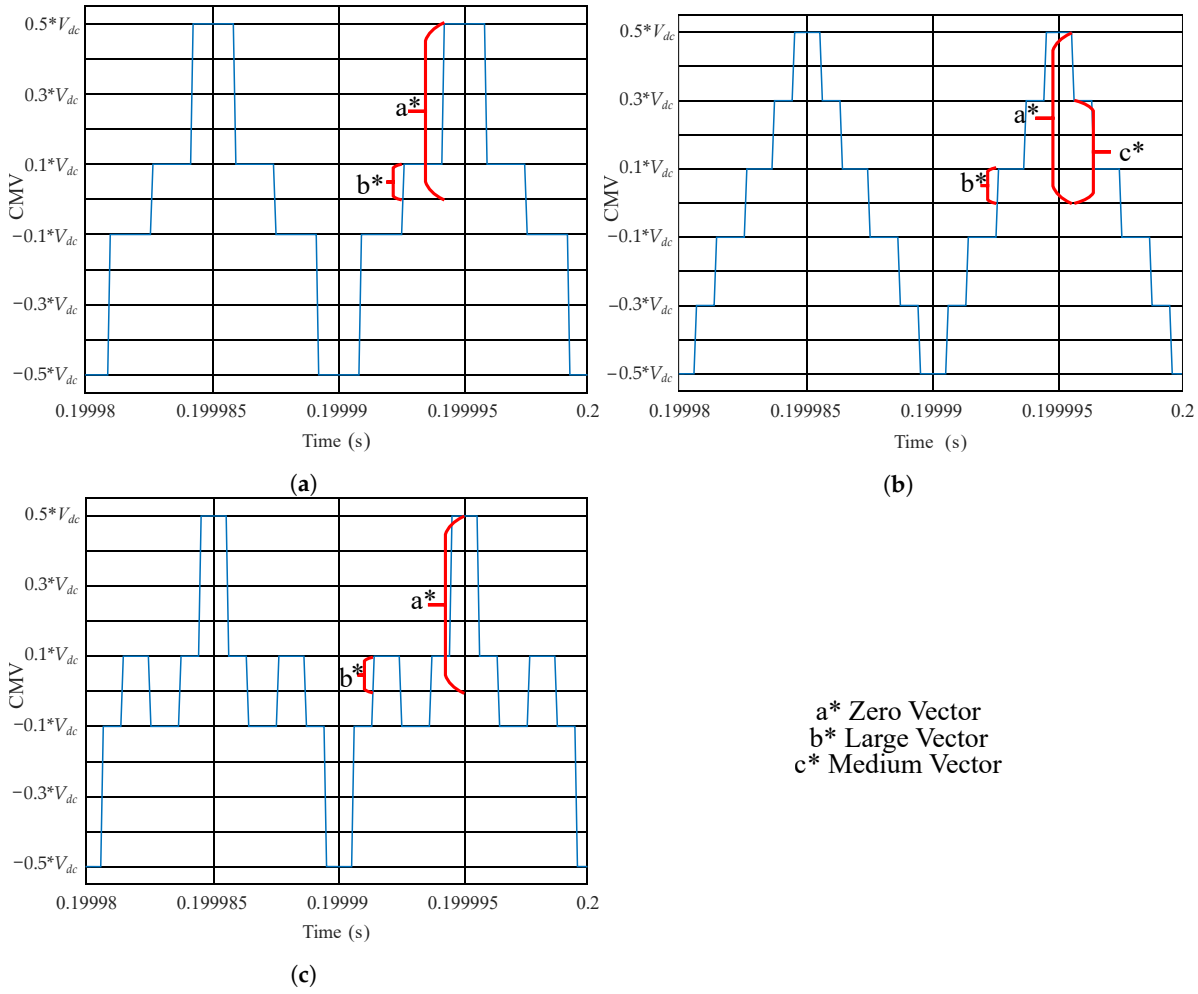


Figure 15. CMV waveforms of the techniques: (**a**) 2L SVPWM, (**b**) 2L+2M SVPWM, (**c**) 4L SVPWM.

In Figure 15, two significant characteristics are analyzed: the CMV amplitude and the dv/dt caused by variations in the CMV's amplitude [48]. Table 9 shows the CMV dv/dt values that each modulation could generate. The dv depends on the DC-Bus and the switching sequence. The dt values depend on the turn-on and turn-off characteristical times of the semiconductors devices.

Table 9 shows the dv/dt levels generated for each one of the modulation techniques. A higher level of dv/dt (0.4 * V_{dc}/dt) is observed only when the 2L and 4L modulation techniques are implemented due to the use of only large vectors. The 2L+2M modulation techniques only present dv/dt values of 0.2 * V_{dc}/dt because of the medium vectors used.

The discontinuous modulation techniques reduce the transitions of the CMV waveform, as shown in Table 9. The 2L and 4L discontinuous techniques reduce two of the 0.4 * V_{dc}/dt transitions compared

with the 2L and 4L SVPWM techniques. The 2L+2M discontinuous techniques reduce two of the $0.2 * V_{dc}/dt$ transitions compared with the 2L+2M SVPWM.

Table 9. Five-phase modulation techniques CMV dv/dt values and number of transitions in a switching period.

Modulation Technique	*dv/dt* Level	Number of Transitions	*dv/dt* Level	Number of Transitions
2L SVPWM	$0.2 * V_{dc}/dt$	2	$0.4 * V_{dc}/dt$	4
2L DPWM-MIN	$0.2 * V_{dc}/dt$	2	$0.4 * V_{dc}/dt$	2
2L DPWM-MAX	$0.2 * V_{dc}/dt$	2	$0.4 * V_{dc}/dt$	2
2L DPWM-V1	$0.2 * V_{dc}/dt$	2	$0.4 * V_{dc}/dt$	2
2L DPWM-V2	$0.2 * V_{dc}/dt$	2	$0.4 * V_{dc}/dt$	2
2L+2M SVPWM	$0.2 * V_{dc}/dt$	10	$0.4 * V_{dc}/dt$	–
2L+2M DPWM-MIN	$0.2 * V_{dc}/dt$	8	$0.4 * V_{dc}/dt$	–
2L+2M DPWM-MAX	$0.2 * V_{dc}/dt$	8	$0.4 * V_{dc}/dt$	–
2L+2M DPWM-V1	$0.2 * V_{dc}/dt$	8	$0.4 * V_{dc}/dt$	–
2L+2M DPWM-V2	$0.2 * V_{dc}/dt$	8	$0.4 * V_{dc}/dt$	–
4L SVPWM	$0.2 * V_{dc}/dt$	6	$0.4 * V_{dc}/dt$	4
4L DPWM-MIN	$0.2 * V_{dc}/dt$	6	$0.4 * V_{dc}/dt$	2
4L DPWM-MAX	$0.2 * V_{dc}/dt$	6	$0.4 * V_{dc}/dt$	2
4L DPWM-V1	$0.2 * V_{dc}/dt$	6	$0.4 * V_{dc}/dt$	2
4L DPWM-V2	$0.2 * V_{dc}/dt$	6	$0.4 * V_{dc}/dt$	2

By applying the fast Fourier transform (FFT) and (4) to the CMV signal, it is possible to obtain the energy analysis of the CMV frequency components. This value allows us to quantify the energy of the CMV-frequency components generated for each modulation.

$$E_{norm} \approx \sum_{i=1}^{\infty} \left[\frac{x(i)}{\frac{V_{dc}}{2}} \right]^2, \tag{4}$$

where E_{norm} is the normalized energy of the CMV, $x(i)$ is the FFT spectrum CMV element, and V_{dc} is the DC-Bus voltage. Figure 16 shows the CMV normalized energy analysis of every modulation based on the variation in the modulation index.

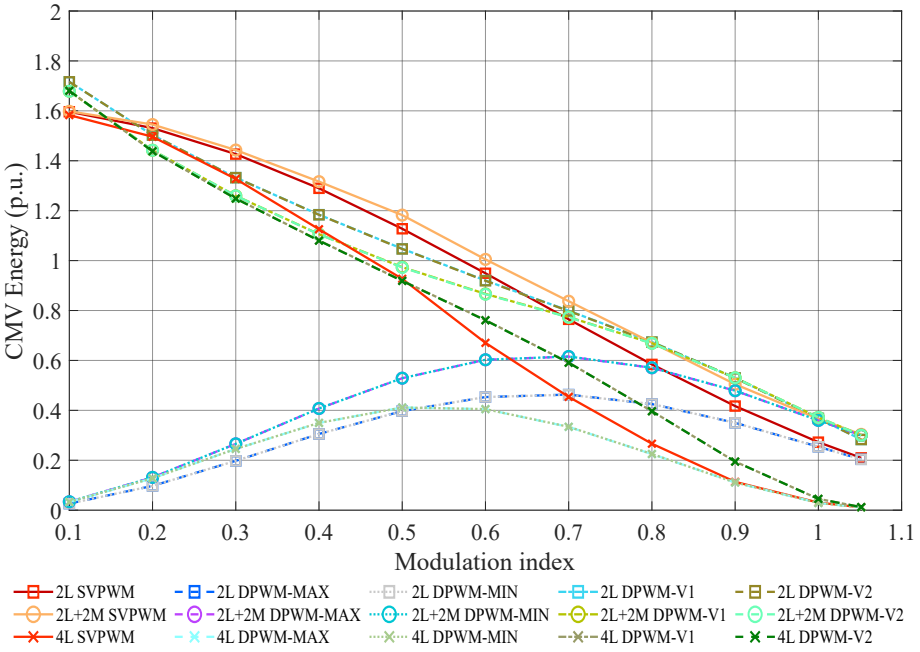


Figure 16. CMV energy analysis comparison.

Figure 16 shows that 4L DPWM-MAX and 4L DPWM-MIN reduces the CMV energy frequency components in a greater proportion because of using only four large vectors. 4L SVPWM produces only four levels of tension: two with 10% of the DC-Bus and two with 50% of it. Although 2L SVPWM also uses large vectors, its difference from 4L SVPWM lies in the switching sequence having only two large vectors. Therefore, the operation time of the zero vectors in 2L SVPWM is longer than that of to the zero vectors in 4L SVPWM. 2L+2M SVPWM produces six levels of tension in the CMV: two at 10%, two at 30%, and two at 50% of the DC-Bus. The reductions in the CMV's time and amplitude depend on the modulation index, because the higher the modulation index, the less conduction time of the zero vectors. Therefore, the active time of the voltage level generated by the zero vectors is reduced. This reduction directly affects the amplitude of the CMV-frequency components.

Despite the application of the discontinuous techniques helping to reduce the dv/dt transitions, these transition reductions affect the behavior of the frequency components, with repercussions on the CMV energy. Depending on the modulation index, the activation time of the only zero vector in the switching sequence is longer than that of the other vectors; as the modulation index increases, this time decreases. Therefore, the CMV energy of the frequency components depends on whether the zero vectors are applied and how long they remain active, as shown in Figure 16.

The dv/dt is higher in the 2L and 4L SVPWM techniques. This is due to only two voltage levels of CMV being produced by the large and zero vectors. 2L+2M SVPWM has the lowest dv/dt due to applying the medium vectors in the switching sequence.

3.1.3. Power Losses and Efficiency Analysis

The efficiency of power converters is an important topic. Depending on which modulation technique is applied, the efficiency in the power converter may vary because power losses vary according to technique. The efficiency is defined as:

$$\eta(\%) = \left(\frac{P_{out}}{P_{in} + P_{condloss} + P_{swtloss}} \right) \times 100, \tag{5}$$

where P_{out} is the inverter output power, $P_{condloss}$ is the conduction losses in the power devices, and $P_{swtloss}$ is the switching losses in the power devices. Therefore, the conduction and switching losses are defined as:

$$P_{condloss} = \frac{1}{T_s} \int_0^{T_s} (V_{F0} + R_{on} I_F) \times I_F dt, \tag{6}$$

where V_{F0} is the threshold voltage, R_{on} is the on resistance, T_s is the period of the fundamental frequency and I_F is the forward current.

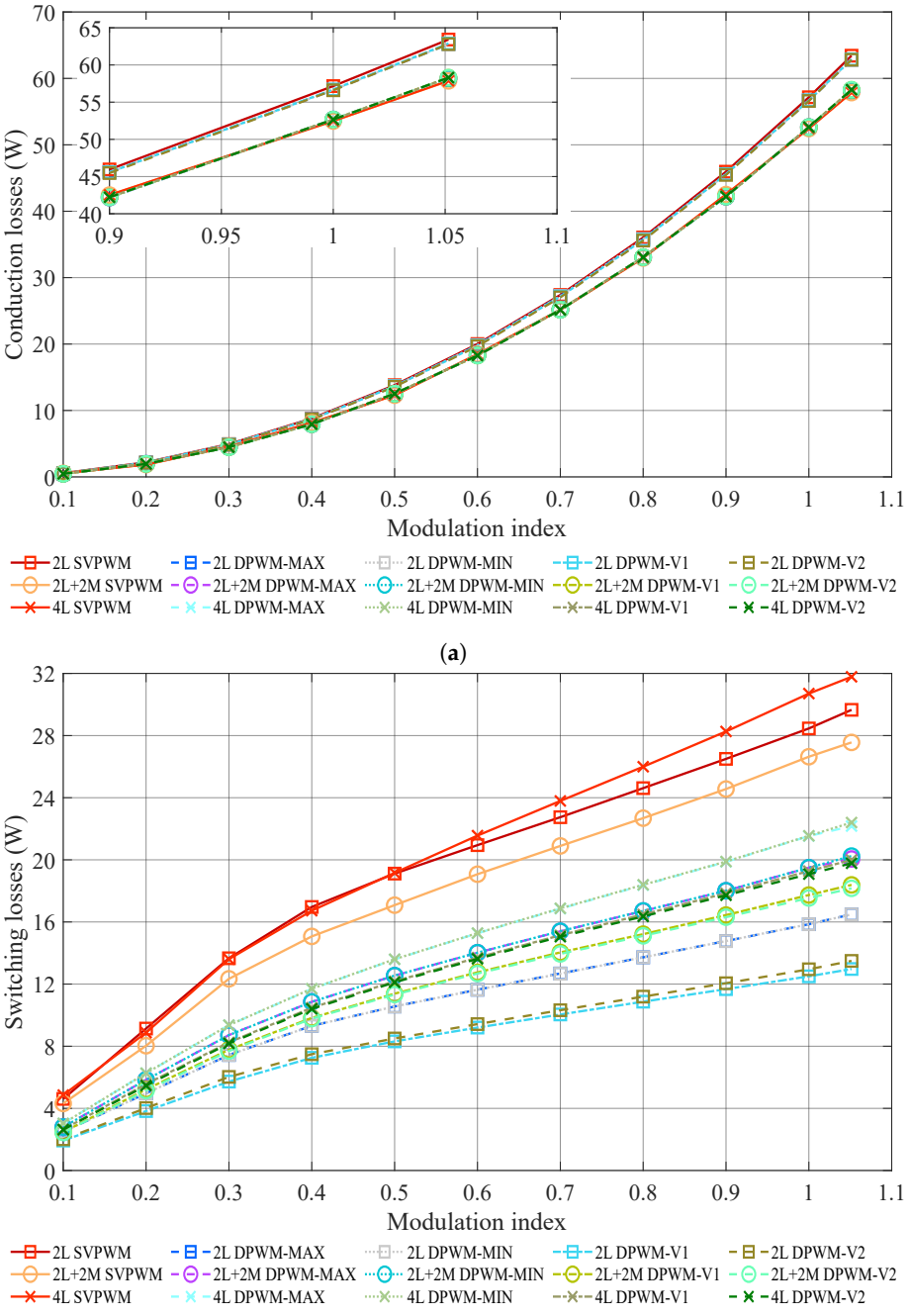
$$P_{swtloss} = \frac{1}{T_s} \sum_{j=1}^{nT_s} [E_{onj}(I_F, V_{offs}) + E_{offj}(I_F, V_{offs})], \tag{7}$$

where E_{on} and E_{off} are the turn-on and turn-off energy dissipated during the change of state, nT_s is the number of transitions in one fundamental period, I_F is the on-state current running through the power devices and V_{offs} is the voltage in the off-state.

Figure 17 shows the total power losses. 2L SVPWM and its corresponding discontinuous versions experience greater conduction losses because the power devices turn-on in pairs. Analysis of the switching losses for these simulation parameters indicated that the use of SiC power devices leads to greater conduction losses and affects the efficiency of the inverter.

The switching losses are lower than the conduction losses. 2L+2M SVPWM experiences fewer switching losses because the power devices turn themselves on and off one by one until they complete the switching sequence. In 2L SVPWM, changing the switching states from the zero to the active vectors (and vice versa) requires by activating or deactivating two switches simultaneously. 4L SVPWM produces higher switching losses because one of the legs turns on and off three times for every

switching sequence. Discontinuous modulation has lower switching losses because the switching sequence is shorter and the active time of the zero vectors is longer than with continuous modulation.



(**a**)

(**b**)

Figure 17. Power losses: (**a**) conduction losses, and (**b**) switching losses.

Figure 18 shows the inverter efficiency under each implemented modulation. With a modulation index of less than 0.5, continuous modulation (2L, 2L+2M, and 4L SVPWM) has the lowest efficiency, whereas the discontinuous versions (DPWM-MAX, DPWM-MIN, DPWM-V1, and DPWM-V2) have the highest due to having the lowest switching losses. With a modulation index greater than 0.5, the efficiency values were similar for all simulations.

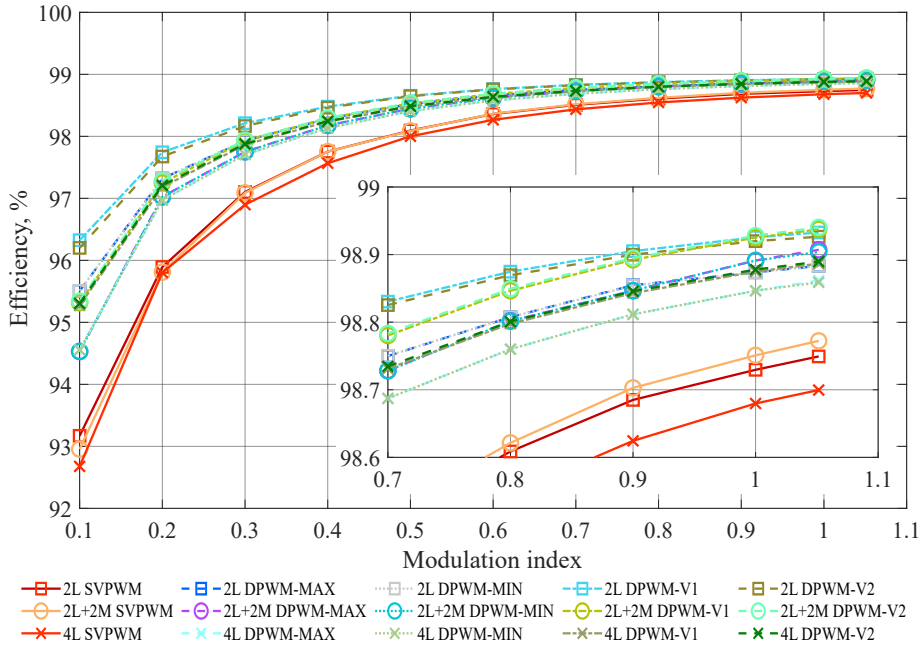


Figure 18. Inverter efficiency.

3.2. Experimental Results

Figure 19 shows the experimental setup. This setup is consisted of a scaled 5 kW VSI that used the previously simulated SiC MOSFETs (C2M0160120D). The converter was supplied by a 200 V DC source. At the output, a star-connected load with a 34 Ω resistor and a 1.45 mH inductance was used. The modulation techniques were implemented on a dSPACE DS1006 and a DS5203 FPGA board. For measuring the voltages a high-resolution oscilloscope, high voltage differential probes were used. The obtained data were processed with Matlab to calculate the THD, efficiency, and CMV generation. The converter output power is measured using a digital power meter. In Section 4, a more detailed explanation of the experimental setup can be founded.

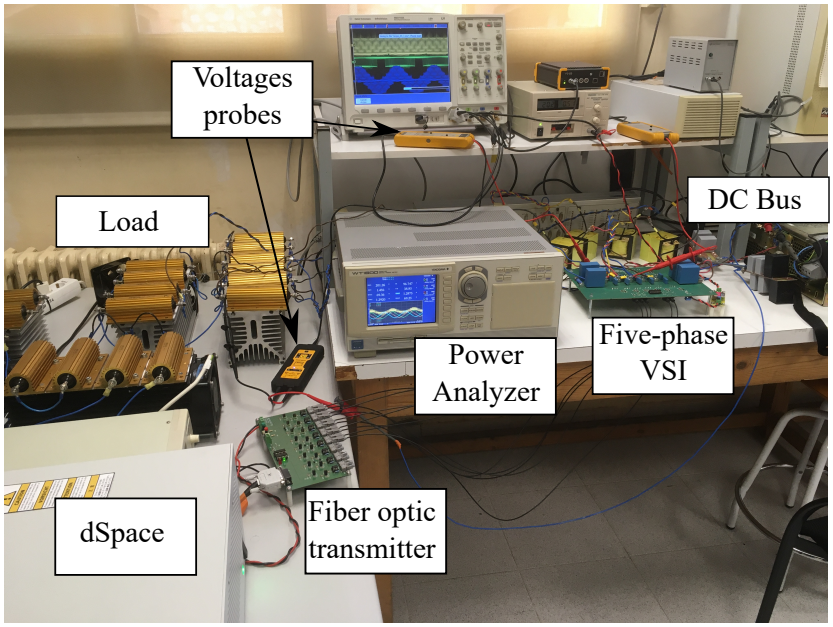


Figure 19. Experimental setup.

Tables 10 and 11 validate the THD and WTHD simulation results. 2L SVPWM and its discontinuous versions have higher THD and WTHD due to the presence of third-order harmonics. 2L+2M SVPWM, 4L SVPWM, and their discontinuous versions have lower THD and WTHD due to the reduce amplitude of the low-order harmonics content.

Table 10. Experimental THD.

Modulation Technique	Modulation Index			
	0.3	**0.5**	**0.7**	**0.9**
2L SVPWM	29.20%	29.16%	29.29%	29.21%
2L DPWM-MIN	29.40%	29.14%	29.16%	29.05%
2L DPWM-MAX	29.11%	29.00%	29.04%	29.04%
2L DPWM-V1	29.00%	29.04%	28.97%	28.99%
2L DPWM-V2	29.17%	29.04%	28.96%	28.96%
2L+2M SVPWM	3.02%	2.45%	2.16%	1.36%
2L+2M DPWM-MIN	4.72%	3.25%	2.87%	2.27%
2L+2M DPWM-MAX	4.41%	3.39%	3.00%	2.79%
2L+2M DPWM-V1	4.63%	3.55%	3.25%	2.77%
2L+2M DPWM-V2	4.89%	3.95%	3.44%	2.84%
4L SVPWM	3.03%	2.53%	2.21%	1.41%
4L DPWM-MIN	4.03%	3.76%	3.23%	2.35%
4L DPWM-MAX	3.80%	3.46%	3.07%	2.89%
4L DPWM-V1	3.95%	3.68%	3.26%	2.96%
4L DPWM-V2	4.14%	3.72%	3.13%	3.02%

Table 11. Experimental WTHD.

Modulation Technique	Modulation Index			
	0.3	**0.5**	**0.7**	**0.9**
2L SVPWM	9.62%	9.58%	9.65%	9.62%
2L DPWM-MIN	9.69%	9.61%	9.61%	9.57%
2L DPWM-MAX	9.59%	9.56%	9.57%	9.57%
2L DPWM-V1	9.51%	9.55%	9.55%	9.55%
2L DPWM-V2	9.59%	9.56%	9.54%	9.54%
2L+2M SVPWM	0.44%	0.44%	0.47%	0.38%
2L+2M DPWM-MIN	0.98%	0.60%	0.63%	0.61%
2L+2M DPWM-MAX	0.95%	0.84%	0.78%	0.73%
2L+2M DPWM-V1	0.68%	0.63%	0.59%	0.53%
2L+2M DPWM-V2	0.76%	0.64%	0.64%	0.52%
4L SVPWM	0.49%	0.47%	0.49%	0.43%
4L DPWM-MIN	0.88%	0.83%	0.77%	0.79%
4L DPWM-MAX	0.87%	0.85%	0.74%	0.69%
4L DPWM-V1	0.72%	0.79%	0.70%	0.66%
4L DPWM-V2	0.79%	0.80%	0.73%	0.67%

Table 12 provides the normalized energy of the CMV. As with the simulation results, the DPWM-MAX and DPWM-MIN present less CMV energy. Also, 4L SVPWM reduces the energy of the high-frequency components for modulation index greater than 0.6.

Regarding inverter efficiency, the discontinuous techniques performed better compared with the continuous modulation techniques, as shown in Figure 20. These results validate those in Figure 18. 2L DPWM-V1 and DPWM-V2 performed the best due to alternation of the discontinuity.

Table 12. Experimental CMV normalized energy.

Modulation Technique	Modulation Index			
	0.3	**0.5**	**0.7**	**0.9**
2L SVPWM	1.76	1.43	1.01	0.59
2L DPWM-MIN	0.49	0.64	0.57	0.56
2L DPWM-MAX	0.50	0.64	0.57	0.55
2L DPWM-V1	1.61	1.37	0.98	0.68
2L DPWM-V2	1.61	1.37	0.99	0.68
2L+2M SVPWM	1.75	1.45	1.07	0.68
2L+2M DPWM-MIN	0.69	0.90	0.79	0.63
2L+2M DPWM-MAX	0.70	0.90	0.80	0.63
2L+2M DPWM-V1	1.60	1.45	1.03	0.67
2L+2M DPWM-V2	1.60	1.46	1.03	0.67
4L SVPWM	1.62	1.14	0.60	0.38
4L DPWM-MIN	0.54	0.63	0.47	0.34
4L DPWM-MAX	0.54	0.62	0.46	0.34
4L DPWM-V1	1.54	1.12	0.78	0.33
4L DPWM-V2	1.53	1.12	0.78	0.33

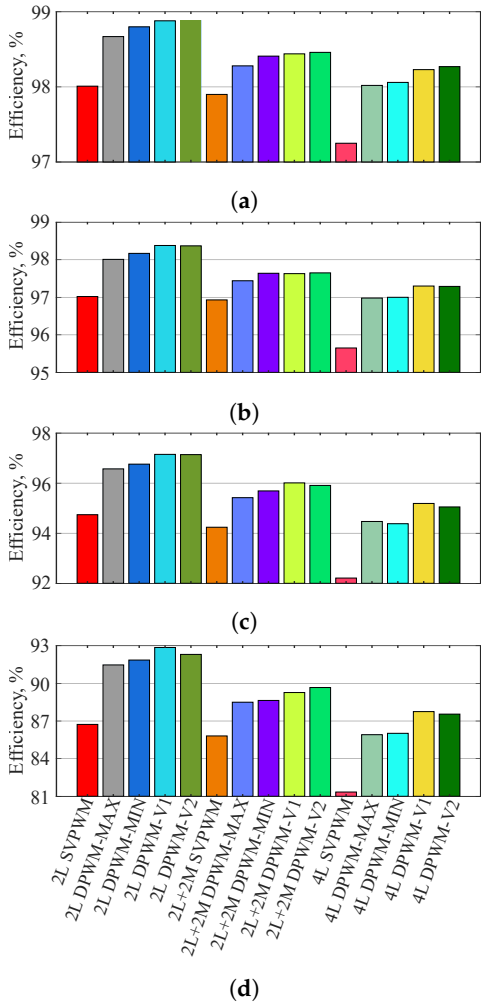


Figure 20. Experimental efficiency at modulation index values of: (**a**) 0.9, (**b**) 0.7, (**c**) 0.5, and (**d**) 0.3.

Table 13 provides a comparative summary of all the modulation techniques and their performance.

Table 13. Performance comparison between each modulation.

General Features	Efficiency mi $\leq$ 0.5	Efficiency mi > 0.5	Switching Losses	Conduction Losses	CMV *dv*/*dt* Max. Level	CMV *dv*/*dt* Transitions	CMV Freq. Comps Energy mi $\leq$ 0.6	CMV Freq. Comps Energy mi > 0.6	Voltage THD
2L SVPWM	Low	High	High	Moderate	0.4 * V_{dc}	6	High	Moderate	High
2L DPWM-MIN	Medium	High	Moderate	Moderate	0.4 * V_{dc}	4	Low	Moderate	High
2L DPWM-MAX	Medium	High	Moderate	Moderate	0.4 * V_{dc}	4	Low	Moderate	High
2L DPWM-V1	High	High	Low	Moderate	0.4 * V_{dc}	4	High	Moderate	High
2L DPWM-V2	High	High	Low	Moderate	0.4 * V_{dc}	4	High	Moderate	High
2L+2M SVPWM	Low	High	High	Moderate	0.2 * V_{dc}	10	High	Moderate	Low
2L+2M DPWM-MIN	Medium	High	Moderate	Moderate	0.2 * V_{dc}	8	Low	Moderate	Low
2L+2M DPWM-MAX	Medium	High	Moderate	Moderate	0.2 * V_{dc}	8	Low	Moderate	Low
2L+2M DPWM-V1	Medium	High	Moderate	Moderate	0.2 * V_{dc}	8	High	Moderate	Low
2L+2M DPWM-V2	Medium	High	Moderate	Moderate	0.2 * V_{dc}	8	High	Moderate	Low
4L SVPWM	Low	High	High	Moderate	0.4 * V_{dc}	10	High	Low	Low
4L DPWM-MIN	Medium	High	Moderate	Moderate	0.4 * V_{dc}	8	Low	Low	Low
4L DPWM-MAX	Medium	High	Moderate	Moderate	0.4 * V_{dc}	8	Low	Low	Low
4L DPWM-V1	Medium	High	Moderate	Moderate	0.4 * V_{dc}	8	High	Low	Low
4L DPWM-V2	Medium	High	Moderate	Moderate	0.4 * V_{dc}	8	High	Low	Low

4. Materials and Methods

Matlab R2018b and Simulink V9.2 were used to implement all the modulation techniques mentioned in this paper. The inverter was modeled using PLECS blockset V4.2.5 to calculate the losses according to the thermal and electrical properties provided by the manufacturer [49]. The SiC semiconductor device's electrical characteristics were obtained from the manufacturer (CREE Wolfspeed), which introduced directly to the PLECS MOSFET component to obtain the power losses as provided in the SiC device data sheet. The CMV, THD, and WTHD analyses were performed from the data obtained from Simulink and processed in Matlab.

The experimental setup consisted of a VSI that used the previously simulated SiC MOSFETs (C2M0160120D). On the AC side, there was a five-phase star-connected RL load with values of 34 Ω and 1.45 mH. The DC-bus of the converter was supplied by a 200 V DC source. The modulation techniques were implemented on a dSPACE DS1006 and a DS5203 FPGA board. Voltages were measured with a high-resolution oscilloscope (Agilent InfiniiVision MSO7104A) and high voltage differential probes (PMK BumbleBee). The obtained data were processed in MATLAB to calculate the THD, efficiency, and CMV generation. The converter output power was measured using a digital power meter (Yokogawa WT1600).

5. Conclusions

Each modulation performs differently; for this reason, the modulation technique that complies with the needs of each specific system and application must be selected.

2L SVPWM can deliver more current to the system due to its higher modulation index, although low-order harmonics are present. It can be used to enhance torque production in multiphase machine applications. Conversely, the 2L SVPWM discontinuous versions provide the best efficiency because they generate less switching losses.

If the objective is for the harmonic content to be low in the output voltages and currents, then the best options are 2L+2M SVPWM, 4L SVPWM and their discontinuous versions. However, if the goal is to reduce the effects of the CMV-frequency components, the 4L SVPWM modulation should be applied for modulation index values over 0.6, even though this modulation has the lowest efficiency due to its high switching losses. The DPWM-MAX and DPWM-MIN modulations should be applied when low CMV and low switching losses are required. This is particularly true for the 4L DPWM-MAX and 4L DPWM-MIN modulations.

The efficiency difference is due to the switching losses since conduction losses are similar in each modulation. SiC devices allow the system to operate at higher frequencies with fewer power losses. However, this impacts the generation of CMV, especially on the dv/dt effects. As the switching frequency increases, the CMV dv/dt changes are more frequent. Thus, to minimize the dv/dt effects, the 2L+2M SVPWM techniques are the best option because they introduce an additional amplitude level of CMV due to the application of the medium vectors. Nevertheless, if the system requires a reduction in the energy of CMV-frequency components , it is essential to apply the discontinuous techniques to meet this requirement.

However, the selection of modulation technique depends on the application and system requirements. If the application is driving a motor, the 2L+2M DPWM-V1 and DPWM-V2 modulation techniques would be the best options. Their efficiency ranges from moderate to high depending on the applied modulation index, they have the lowest harmonic content, and the maximum amplitude of their dv/dt is 0.2 of the value of the DC-Bus.

If harmonic injection is used to improve torque in electric motors, the 2L DPWM-V1 and DPWM-V2 techniques should be chosen due to their high efficiency in the inverter and their low CMV dv/dt transitions. However, the maximum amplitude of the dv/dt is 0.4 of the value of the DC-Bus.

For applications where the high-frequency components of the CMV affect the system due to their resonance frequency, the 4L DPWM-MAX and 4L DPWM-MIN techniques must be applied. This technique reduces the amplitude of the high-frequency CMV components. However, the efficiency of the system is compromised due to its higher switching losses.

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