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Stability Analysis and Optimal Design for Virtual Impedance of 48 V Server Power System for Data Center Applications

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Abstract: In the past literature on virtual impedance to series systems, most of the discussion focused on stability without in-depth research on the system design of the series converter and the overall output impedance. Accordingly, this study takes an open-loop resonant LLC converter series-connected closed-loop Buck converter as an example. First, the conditions required for the direct connection of the small-signal model in the series, the effect of feedback compensation on the input impedance of the load stage, the operating frequency, and passive components of the two-stage converter are discussed in detail—the relationship between the matching and the output impedance. Afterwards, a mathematical model is used to discuss the effect of adding parallel virtual impedance on the output impedance of the overall series converter and then derive an optimized virtual impedance design. Finally, an experimental platform of 48 V to 12 V and maximum wattage of 96 W are implemented. The output impedance of the series converter is measured with an impedance analyzer to verify the theoretical analysis proposed in this paper.

Keywords: output impedance; stability analysis; virtual impedance

1. Introduction

The series converter architecture is used extensively in various applications to compensate for the shortcomings of single-stage converters incapable of having both high efficiency and wide voltage conversion ratio. In the data center [1], the common voltage conversion rates are 48 V to 12 V, 48 V to 6 V, 48 V to 4 V, depending on the demand of the load side and the performance of maximum efficiency to choose the most appropriate voltage conversion rate. The typical combination of series converters is generally divided into two stages. The front stage uses open-loop operation, which performs preliminary voltage regulation or pure electrical isolation. The latter stage uses closed-loop control to regulate the output voltage. The switching characteristics of the open-loop LLC converter operating at the first resonance frequency can enable the switch between zero-voltage-switching (ZVS) and zero-current-switching (ZCS), and efficiently convert 48 V to suitable intermediate voltage amplitude. The subsequent Buck converter's duty cycle can be designed to be larger, and a lower voltage power switch can be used to reduce the switch on-resistance and improve the conversion efficiency of the Buck converter. This approach maximizes the efficiency of the overall two-stage converter.

With regard to the familiar series converter combination in the recent application of point of load (POL) power supply in the data center [2], the series architecture used is roughly divided into two categories: open-loop LLC series closed-loop Buck and open-loop switching tank converter (STC) [3,4] series closed-loop Buck. This combination of STC series closed-loop Buck has the advantages of high efficiency and high-power density. However, in applications where high voltage conversion and

high-power transmission or isolation are required on the primary and secondary sides, the LLC series Buck converter remains the most widely used combination. Accordingly, the current study chooses to take the open-loop LLC series closed-loop Buck converter as an example circuit for discussion based on the above reasons.

The main point of the series converter's design is to first focus on the stability of the two-stage series and then to the overall output impedance of the series converter. In the discussion of stability, the Middlebrook stability criterion [5] has existed for many years. It uses the correlation between the input and output impedance of the front and back stages to explain the series system's stability. With Middlebrook's theory of stability criterion, several methods for solving series stability have been proposed one after another. Roughly three types of methods are available: the first category refers to the passive components to increase system damping [6,7]. A reliable and straightforward circuit characterizes this method, but the circuit increases additional losses by adding passive components and resistance. The second category is the process of dynamically increasing the decoupling capacitance [8]. Although this type of method reduces losses than the first type, it increases the complexity of control and the number of components used and reduces the overall converter's power density and reliability. The third type is the process of feeding the virtual impedance [9,10]. This type of method uses sampling voltage and current signals to add to the original control loop in the form of control blocks to achieve virtual impedance. Compared with the second type, the overall converter's power density can be maintained because no additional power components are required.

The virtual impedance method can be divided into two types: changing the output impedance of the source converter and changing the input impedance of the load converter. However, with the example architecture of this article, the source-level LLC converter is an open-loop operation. Accordingly, the virtual impedance method of changing the load-level converter's input impedance is selected. The load-level virtual impedance can be divided into series and parallel [11]. Owing to the need to adapt the detection current to achieve the purpose of the series virtual impedance, the current uses the parallel load-level virtual impedance method after considering the cost and control complexity.

However, in the past literature discussing virtual impedance to series systems, most of the discussion focused on stability without in-depth research on the system design of the series converter and the overall output impedance. The literature [12] puts forward a virtual impedance design method for a series system under the premise of a constant power load to make the system stable. However, the article does not discuss the output impedance seen by the overall system's load end after adding the virtual impedance. The literature [13] proposed a series-type virtual impedance to modify the source-side converter's output impedance, thereby satisfying the system's stability and reducing the output impedance of the source-side converter at the same time. However, in server power applications, the post-stage usually uses an open-loop LLC architecture to reduce the complexity and cost of control and increase the overall converter's robustness.

Accordingly, the current study takes the open-loop LLC series closed-loop Buck converter as an example. First, the conditions required for the direct connection of the small-signal model in series, the effect of feedback compensation on the input impedance of the load stage, the operating frequency, and passive components of the two-stage converter are discussed in detail—the relationship between the matching and the output impedance. Afterwards, a mathematical model was used to discuss the effect of adding parallel virtual impedance on the output impedance of the overall series converter and then derive an optimized virtual impedance design.

This article is organized as follows. Section 1 introduces the research background and literature review. Section 2 reviews the small-signal model of the basic Buck and LLC converter. Furthermore, it discusses the particular conditions of a direct series connection with these models. Section 3 presents the feedback compensation carried out for the Buck converter of the load stage in the series converter, and the correlation between its closed-loop input impedance and the compensator is explained. Section 4 reviews Middlebrook's stability criterion and discusses the design criteria of the resonant tank of the previous-stage LLC converter from the perspective of stability and overall output impedance.

Section 5 reviews the principle, implementation method, and design constraints of the parallel virtual impedance. Section 6 discusses the impact of virtual impedance on the output impedance of the overall converter and analyzes the best virtual impedance design criteria. Section 7 verifies the derivation's correctness by simulating and implementing the circuit according to the results derived from the Section 6. Section 8 concludes the entire article.

2. Individual Review of the Small-Signal Model of LLC and Buck Converters and Discussion on the Conditions for the Direct Connection of Small-Signal Models

Figure 1 shows an LLC converter with a turns ratio of one. According to the derivation of literature [14–16], Figure 2 shows the small-signal LLC converter model. ω_s is the angular frequency of the switching frequency, and ω_o is the resonance frequency of L_r and C_r.

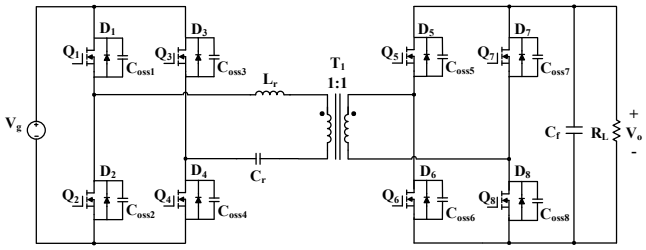


Figure 1. Circuit diagram of LLC converter.

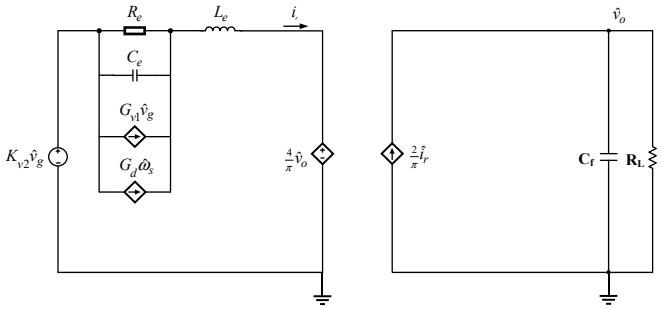


Figure 2. Small-signal model of LLC converter.

Although Figure 2 contains three disturbance sources such as K_{v2}, G_{v1}, and G_d, $\hat{\omega}_s$ is zero given that the LLC converter operates in an open loop. When discussing the output impedance, the disturbance will only leave the disturbance of the output voltage and set the disturbance $\hat{v}_g$ of the input voltage to zero. Thus, when discussing the output impedance, we must only understand the three parameters of R_e, C_e, and L_e. The equations are as follows:

$$R_e = \frac{L_e\left|X_{eq}\right||\omega_s - \omega_o|}{R_{eq}}, \tag{1}$$

$$C_e = \frac{1}{L_e(\omega_s - \omega_o)^2}, \tag{2}$$

$$L_e = L\left(1 + \frac{{\omega_o}^2}{{\omega_s}^2}\right), \tag{3}$$

where X_{eq} and R_{eq} are

$$X_{eq} = \omega_s L_r - \frac{1}{\omega_s C_r}, \tag{4}$$

$$R_{eq} = \frac{8}{\pi^2} R_L. \tag{5}$$

When the switching frequency of the designed LLC converter is equal to the resonant frequency, X_{eq} can be obtained as infinity according to Equation (4), R_e can be obtained as zero according to Equation (1), and C_e can be obtained as infinity according to Equation (2); and according to Equation (3) available L_e is twice of L_r. Then, through the conversion between the dependent voltage source and current source in Figure 2, the output impedance model of the LLC converter can be equivalent to the impedance of $\left(\frac{\pi^2}{4}\right)L_r$ in parallel with the output capacitor C_f and the load resistance R_L as shown in Figure 3.

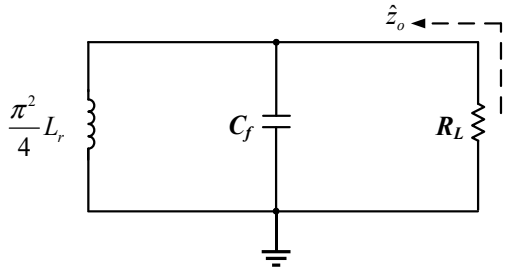


Figure 3. Output impedance equivalent circuit of LLC converter.

Figure 4 illustrates the Buck converter's small-signal model, and its small-signal modeling method is built using the switch state averaging method [17]. The equivalent switching small-signal model is established by averaging the switching states. With the Buck converter's LC filter (L_O, C_O and r_{Co}), the small-signal model of the Buck converter can be established.

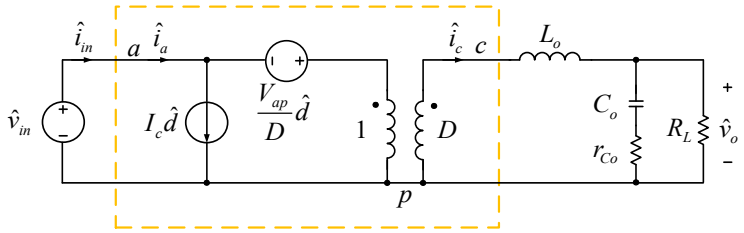


Figure 4. Small-signal model of Buck converter.

However, when discussing the small-signal model of a single converter individually, the input voltage source is an ideal constant voltage source. Therefore, considering the significant changes in the input voltage during the state's derivation variables of each component is unnecessary. In the actual series system, considering that the post-stage converter's input voltage is no longer an ideal constant voltage source, the small-signal model of the entire machine in the series system should be re-modeled by the state-space averaging method. In practical applications, multi-level converters may use different control mechanisms for individual control, such as the frequency conversion control commonly used in LLC converters and Buck converters' pulse-width-modulation (PWM) control. Using different control modes will make it difficult for the entire system to be modeled using the state-space averaging method. Thus, when analyzing the small-signal model of the system in series, most of the individual small-signal models are directly connected in series for analysis.

Figure 5 is a small signal direct series model of an open-loop LLC series Buck converter. The figure can be simplified as an LC filter connected in series with a Buck converter.

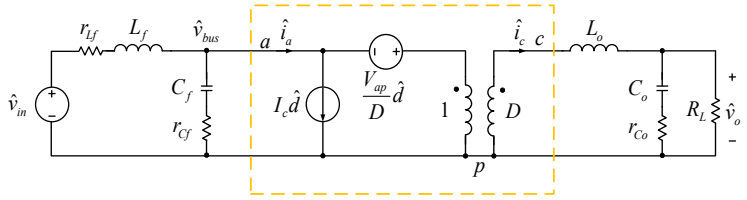
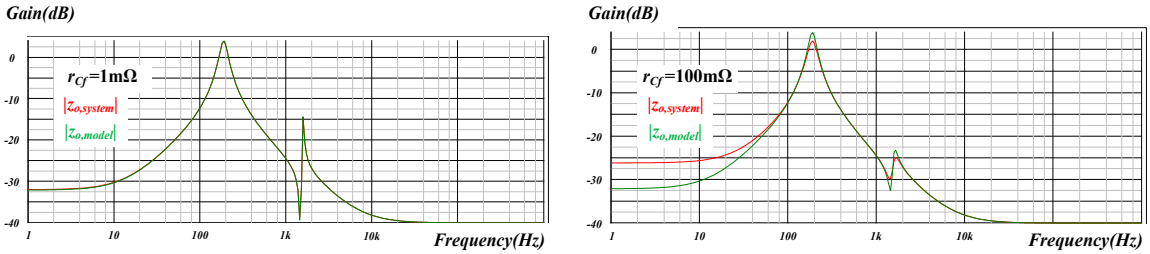


Figure 5. Small signal model of an open-loop LLC series Buck converter.

However, the direct series approximation method must pay attention to the voltage disturbance value on the previous stage's output capacitor. Under the general design, the capacitor's voltage ripple value comes from the parasitic series resistance (ESR) of the selected capacitor. Therefore, the more significant the ESR of the intermediate stage capacitor, the more significant the error of small signal model directly connected in series. Figure 6 is a Bode plot of the open-loop Buck converter's output impedance with an LC filter in series with different r_{cf}. The remaining circuit parameters are $D = 0.5$, $L_o = 33$ µH, $C_o = 2.2$ mF, $r_{C\,o} = 10$ mΩ, $C_f = 100$ µF, $L_f = 1$ mH, $r_{Lf} = 100$ mΩ, $R_L = 3$ Ω. We can verify from the results of Figure 6a,b that when the r_{cf} is large, the error between the small-signal model and the actual system will be significant. Therefore, in the design, the capacitor with smaller ESR is used as much as possible. Apart from increasing the overall converter efficiency, it also helps simplify the analysis of small signals.



(**a**) (**b**)

Figure 6. Bode plot of the output impedance of an LC filter in series with Buck: (**a**) r_{cf} = 1 mΩ; (**b**) r_{cf} = 100 mΩ.

3. Relation between Compensation Design and Input Impedance in Series System

The cascade system's $\hat{d}$-to-$\hat{v}_o$ transfer function G_{dvcas} can be derived from the cascade small-signal model in Figure 5. When designing the post-stage Buck compensator, G_{dvcas} must be designed to meet the loop gain's stability. In this paper, the symbol C_v is used to indicate the compensator's transfer function.

The output and input impedance of the front-to-back converters in the series system will affect the overall cascade architecture's stability. Therefore, the analysis separates the LC filter of the previous stage from the Buck converter of the latter stage and discusses the input impedance characteristics of the Buck converter of the latter stage in this section. Figure 7 shows a control block diagram of a simple post-stage Buck converter, which adopts a voltage mode control method for closed-loop control.

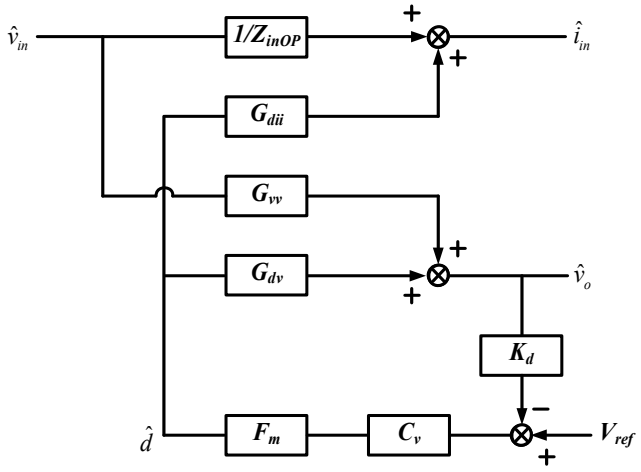


Figure 7. Control block diagram of Buck converter with voltage mode control.

K_d in Figure 7 is the feedback voltage division ratio, F_m is the modulation gain from sawtooth to PWM, and the remaining system transfer functions can be derived from Figure 4 as follows:

$$Z_{inOP}(s) = \frac{\hat{v}_{in}}{\hat{i}_a} = \frac{1}{D^2}[sL_o + (\frac{1}{sC_o} + r_{Co})\|R_L], \tag{6}$$

$$G_{dii}(s) = \frac{\hat{i}_a}{\hat{d}} = \frac{DV_{in}}{R_L} + \frac{DV_{in}}{sL_o + (r_{Co} + \frac{1}{sC_o})\|R_L}, \tag{7}$$

$$G_{vv}(s) = \frac{\hat{v}_o}{\hat{v}_{in}} = D\frac{R_L\|(\frac{1}{sC_o} + r_{Co})}{sL_o + R_L\|(\frac{1}{sC_o} + r_{Co})}, \tag{8}$$

$$G_{dv}(s) = \frac{\hat{v}_o}{\hat{d}} = V_{in}\frac{R_L\|(\frac{1}{sC_o} + r_{Co})}{sL_o + R_L\|(\frac{1}{sC_o} + r_{Co})}. \tag{9}$$

To obtain the closed-loop input impedance Z_{inCL}, the control block diagram in Figure 7 shows the following:

$$\hat{i}_{in} = \hat{v}_{in}\frac{1}{Z_{inOP}} + \hat{d}G_{dii}, \tag{10}$$

$$\hat{d} = (\hat{v}_{in}G_{vv} + \hat{d}G_{dv})(-K_d)C_vF_m. \tag{11}$$

The relationship between $\hat{d}$ and $\hat{v}_{in}$ can be summarized as (11) as

$$\hat{d} = \frac{G_{vv}(-K_d)C_vF_m}{1 + T_v}\hat{v}_{in}, \tag{12}$$

where T_v is the loop gain:

$$T_v = K_dC_vF_mG_{dv}. \tag{13}$$

Substituting Equation (12) into Equation (10) can derive the closed-loop output impedance Z_{inCL} as

$$\begin{aligned} Z_{inCL} &= \frac{\hat{v}_{in}}{\hat{i}_{in}}\Big|_{CL} \\ &= \frac{1}{\frac{1}{Z_{inOP}} + \frac{-K_DG_{vv}C_vF_mG_{dii}}{1+Tv}} \\ &= \frac{1}{\frac{1}{Z_{inOP}} + \frac{-T_v}{1+T_v}\frac{G_{vv}G_{dii}}{G_{dv}}} \end{aligned}. \tag{14}$$

Substituting Equations (6)–(9) into Equation (14), we can further obtain the following:

$$Z_{inCL} = \left.\frac{\hat{v}_{in}}{\hat{i}_{in}}\right|_{CL} = \frac{1}{\frac{T_v}{1+T_v}\left(-\frac{D^2}{R_L}\right) + \frac{1}{1+T_v}\left(\frac{1}{Z_{inOP}}\right)}. \quad (15)$$

Observation Equation (15) shows that if we want the closed-loop input impedance to be a fixed value $\left(-R_L/D^2\right)$, Equation (15) must meet two conditions. Condition one: $|T_v| \gg 1$. Condition two: $|T_v| \gg |1/Z_{inOP}|$. Figure 8 is a Bode plot of the closed-loop input impedance at different T_v, the remaining circuit parameters are $D = 0.5$, $L_o = 33$ µH, $C_o = 2.2$ mF, $r_{Co} = 10$ mΩ, $C_f = 100$ µF, $L_f = 1$ mH, $r_{Lf} = 100$ mΩ, $R_L = 3$ Ω. As shown in Figure 8, under the design using T_{v1} closed-loop gain, given that the $|T_v| \gg |1/Z_{inOP}|$ is not satisfied within the closed-loop bandwidth, the input impedance characteristic within the closed-loop bandwidth is not a fixed negative resistance value. In the design using T_{v2} closed-loop gain, it can be regarded as a fixed impedance value within the closed-loop bandwidth because the condition of $|T_v| \gg |1/Z_{inOP}|$ is satisfied. Therefore, in the compensator's design, we must pay special attention to whether condition two is met, and it cannot be directly assumed that Z_{inCL} is a fixed value within the closed-loop bandwidth.

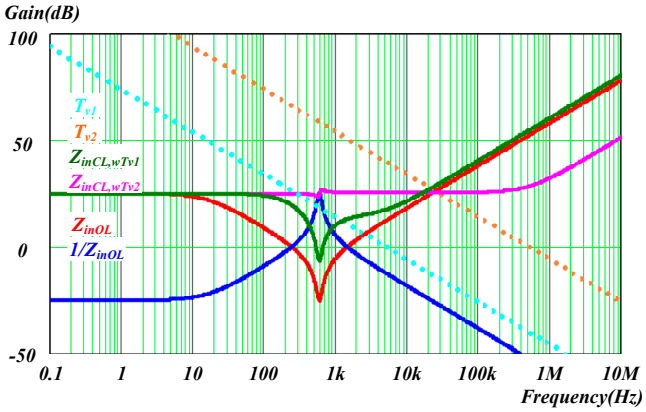


Figure 8. Bode plot of closed-loop input impedance at different T_v.

4. Middlebrook Stability Criterion and Corresponding LLC Design Choices

Middlebrook stability criterion must discuss the output and input impedance of the front and rear converters. Figure 9 is a schematic diagram of a typical cascade system utilized to define each symbol. Among them, Z_{oS} is the output impedance of the previous stage, and Z_{iL} is the input impedance of the latter stage.

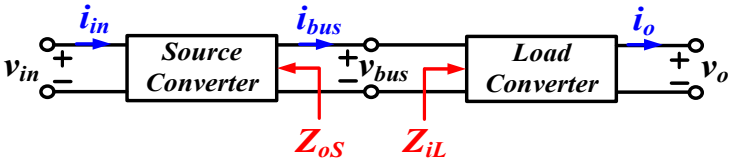


Figure 9. Schematic diagram of a typical series system.

To discuss the stability of the serial system, Figure 10 presents a two-port network diagram based on the serial system of Figure 9.

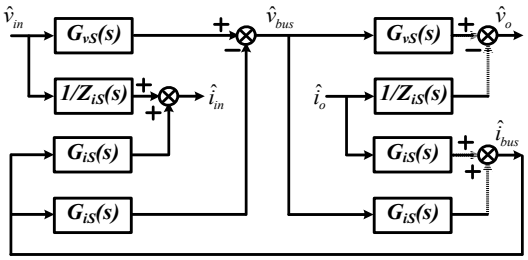


Figure 10. Dual-port network diagram of the series system.

Four system transfer functions can be derived from Figure 10:

$$\left.\frac{\hat{i}_{in}(s)}{\hat{v}_{in}(s)}\right|_{\hat{i}_o=0} = \frac{G_{vS}(s)G_{iS}(s)/Z_{iL}(s)}{1+T_m(s)} + \frac{1}{Z_{iS}(s)}, \tag{16}$$

$$\left.\frac{\hat{v}_o(s)}{\hat{v}_{in}(s)}\right|_{\hat{i}_o=0} = \frac{G_{vS}(s)G_{vL}(s)}{1+T_m(s)}, \tag{17}$$

$$\left.\frac{\hat{i}_{in}(s)}{\hat{i}_o(s)}\right|_{\hat{v}_{in}=0} = \frac{G_{iS}(s)G_{iL}(s)}{1+T_m(s)}, \tag{18}$$

$$\left.\frac{\hat{v}_o(s)}{\hat{i}_o(s)}\right|_{\hat{v}_{in}=0} = -Z_{oL}(s) - \frac{G_{iL}(s)G_{vL}(s)Z_{oS}(s)}{1+T_m(s)}, \tag{19}$$

where

$$T_m(s) = \frac{Z_{oS}(s)}{Z_{iL}(s)}. \tag{20}$$

As can be seen from Equations (16)–(20), even if the previous stage's converters and the later stage are stable when the ratio T_m between the output of the front- and post-stage converter's input impedance is unstable, the overall series system will remain unstable. This phenomenon is Middlebrook's stable criterion. Figure 11 is a Bode diagram of the output impedance of the front stage and the rear stage's output impedance in a typical unstable series system. Its circuit characteristics can be regarded as an LC filter in the front stage and a power converter with a constant power load in the rear stage. The symbol Z_{oSP} is the peak value of the output impedance of the previous stage. According to the derivation in Section 3, the closed-loop input impedance of the fixed power load's power converter is a specific value. Moreover, the particular value can be derived according to the following steps.

Assuming that the converter efficiency is 100%, the output power P_o is

$$i_{BUS}v_{BUS} = P_o. \tag{21}$$

Under closed-loop operation, the output power is constant, and the output power is independent of the value of the input voltage. Therefore,

$$i_{BUS} = P_o/v_{BUS}. \tag{22}$$

Then, the fixed value part of the input impedance $Z_{inConst}$ can be derived by definition as follows, and this impedance is a negative resistance characteristic.

$$\begin{aligned} Z_{inConst} &= \left.\frac{dv_{BUS}}{di_{BUS}}\right|_{DC} \\ &= \left.\frac{dv_{BUS}}{d(P_o/v_{BUS})}\right|_{DC} \\ &= \left.\frac{-{v_{BUS}}^2}{P_o}\right|_{DC} \\ &= \frac{-{V_{BUS}}^2}{P_o} \end{aligned}. \tag{23}$$

As can be seen from Figure 11, at frequencies f_1 and f_2, T_m *(s)* has insufficient phase margin. When the frequency is f_{sp}, T_m *(s)* has insufficient gain margin. Therefore, this series system is unstable.

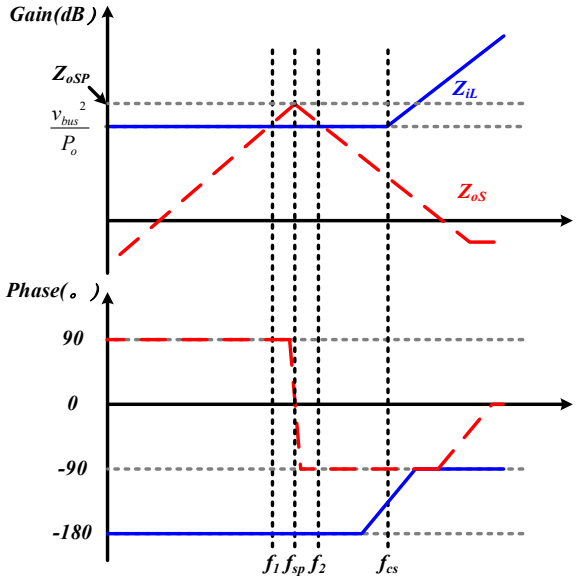


Figure 11. Bode plot of an unstable series system of LC filter in series with constant power load converter.

After understanding the Middlebrook stability criteria and the system Bode plot of Figure 11, the open-loop LLC converter's output impedance can be known as an LC parallel architecture in Section 1, which is consistent with the output impedance of the LC filter. Therefore, the same concept can explain how to design the LLC converter to stabilize the series system. Two design methods exist to stabilize the series system as shown in Figure 12. The first method is to reduce the value of Z_{oSP} to prevent T_m *(s)* from having a gain of equal to 1, as shown by Z_{oS1} in Figure 12. However, this method must increase the LLC converter's system damping so that the system adds additional losses. The second method is to design the resonant frequency of the LLC converter far enough, far higher than the zero-crossing frequency of the latter stage constant power converter, and raise the input impedance of the latter stage converter higher than the LLC output at any frequency. The impedance is shown as Z_{oS2} in Figure 12. However, this method will force the LLC converter's resonant frequency to be at least higher than the post-stage converter's bandwidth when the post-stage converter's system bandwidth is very high. Furthermore, the series system's overall output impedance cannot rely on closed-loop gain for sufficient attenuation. Apart from increasing the driver's driving loss, the high-frequency LLC converter will also increase the prominence of the effects of non-ideal parasitic elements on the resonant element, thereby increasing the complexity of the system as well. Therefore, in practice, other methods must be considered to solve the instability of the cascade system.

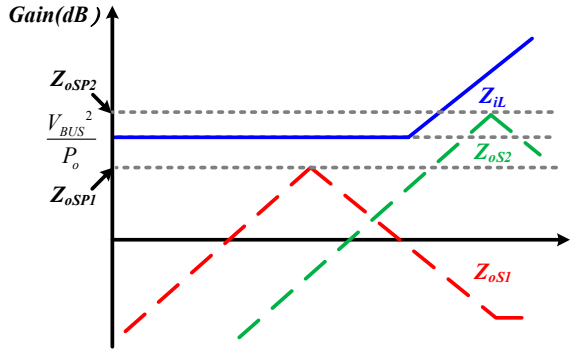


Figure 12. Two ways to design an LLC converter to stabilize a series system.

5. Design and Implementation of Parallel Type Virtual Impedance

Compared with the serial-type virtual impedance, the parallel-type virtual impedance requires no additional current sensing components in manufacturing and has a lower cost, higher converter efficiency, and stable and straightforward system. Therefore, this thesis uses parallel virtual impedance to perform follow-up research.

The principle of the parallel-type virtual impedance is to create virtual impedance and connect the virtual impedance parallel to the input impedance of the post-stage converter, thereby stabilizing the series system. Figure 13 illustrates its physical meaning.

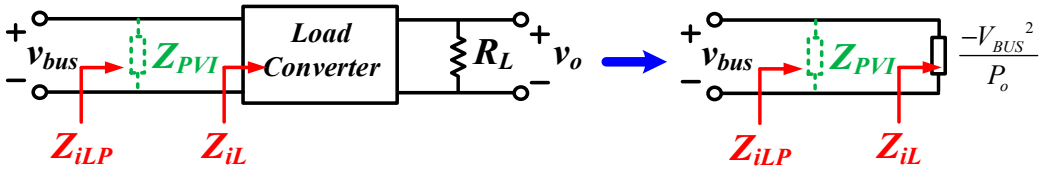


Figure 13. Physical meaning of the parallel type virtual impedance.

The symbol Z_{iLP} is defined as the overall input impedance value after the parallel virtual impedance is added. The mathematical expression is:

$$Z_{iLP}(s) = Z_{iL}(s) \| Z_{PVI}(s) = \frac{Z_{iL}(s) Z_{iL}(s)}{Z_{iL}(s) + Z_{iL}(s)}. \tag{24}$$

To stabilize the series system, the input impedance value of the subsequent stage can be changed in two ways: first, the phase of Z_{iLP} is adjusted to provide sufficient phase margin when $T_m\ (s) = 1$; second, the gain of Z_{iLP} is adjusted to raise the gain of Z_{iLP} higher than Z_{oSP} at any frequency and thus provide sufficient margin for $T_m\ (s)$. Among them, the process of adjusting the phase is not as good as that of adjusting the gain to improve stability [11]. Moreover, the design and implementation of the analog circuit are susceptible to the phase shift of the analog filter. Consequently, the current study chooses to change Z_{iLP} gain mode.

Given that Z_{iLP} can be higher than Z_{oSP} under any loading conditions to ensure the series system's stability, the design method of designing Z_{PVI} can be divided into two states from no-load and full-load as the starting point for the design. Figure 14 presents a design example.

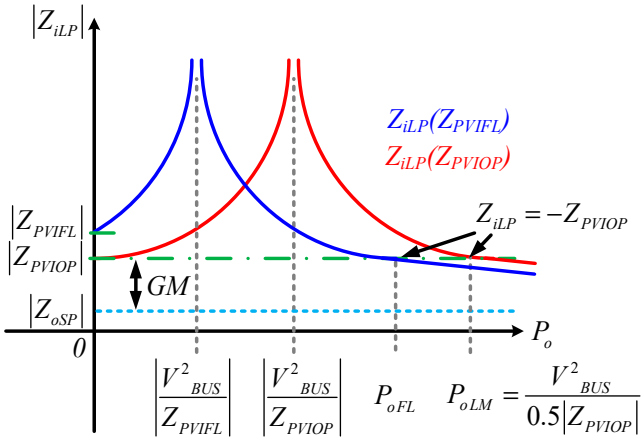


Figure 14. Curve of output load versus $|Z_{iLP}|$ under different Z_{PVI} designs.

$Z_{iLP}\ (Z_{PVIOP})$ in Figure 14 is a curve of $|Z_{iLP}|$ designed with the output no-load as the starting point. When the post-stage converter is no-load, the overall input impedance of the post-stage contains

only Z_{PVIOP}. Thus, the design of Z_{PVIOP} must only consider the peak value of Z_{oSP} and the required gain margin GM. The design formula of Z_{PVIOP} is as follows:

$$Z_{PVIOP} = |Z_{oSP}|10^{\frac{GM}{20}}. \tag{25}$$

Observing the curve Z_{iLP} (Z_{PVIOP}), if one wishes to meet the situation where one can have more than gain margin GM under any load, the maximum output wattage of the converter P_{oLM} will be limited. If the output load is higher than P_{oLM}, the gain margin of Z_{iLP} from Z_{oSP} will be insufficient. Therefore, the converter must consider the full load and no-load conditions. Z_{iLP} has sufficient gain margin GM, and Z_{iLP} is equal to $|Z_{PVIOP}|$ at the maximum output wattage P_{oLM}. To satisfy this condition, under the maximum output wattage P_{oLM}, the input impedance Z_{iL} of the original converter must be equal to $-0.5Z_{PVIOP}$ to achieve the following: $Z_{iLP} = Z_{PVIOP} \| -0.5Z_{PVIOP} = -Z_{PIOP}$. Then, the maximum output wattage P_{oLM} can be derived:

$$P_{oLM} = \frac{2V^2{}_{BUS}}{Z_{PVIOP}}. \tag{26}$$

Therefore, the full load wattage P_{oFL} of the designed converter must be less than P_{oLM}. However, the Z_{PVI} design method is based on the fully loaded P_{oFL}, and the result is shown as the curve Z_{iLP} (Z_{PVIFL}) in Figure 14. To make the overall input impedance equal to $|Z_{PVIOP}|$ under full-load P_{oFL} and any load below full-load P_{oFL} can have more than GM gain margin, the right half of the curve Z_{iLP} (Z_{PVIOP}) must be selected. The two lines of curve Z_{iLP} and level $|Z_{PVIOP}|$ must intersect when the load point is P_{oFL}; at this time, $Z_{iLP} = -Z_{PVIOP}$. The design formula of Z_{PVIFL} is as follows:

$$Z_{PVIFL} = \frac{Z_{PVIOP}}{\frac{P_{oFL}Z_{PVIOP}}{V^2{}_{BUS}} - 1}. \tag{27}$$

From Formulas (25) and (27), we know that within the following range of Z_{PVI} design, the system can be stabilized under any load. Additionally, the gain margins at different load points are different, but the gain margin is higher than GM:

$$Z_{PVIOP} \leq |Z_{PVI}| \leq Z_{PVIFL}. \tag{28}$$

After understanding the design criteria and scope of Z_{PVI}, the control block diagram of Z_{PVI} implementation is reviewed in [11] as shown in Figure 15.

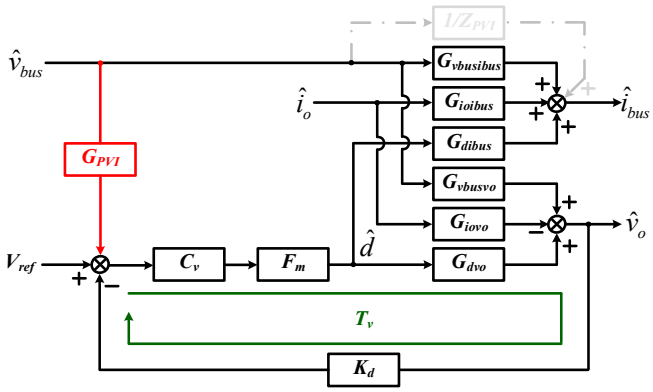


Figure 15. Control block diagram of the realization of parallel virtual impedance.

In Figure 15, C_v is the compensator's transfer function, F_m is the modulation gain of the sawtooth wave, and K_d is the feedback voltage division gain. As can be seen from the control block diagram, if

creating virtual impedance is desired through the feedforward method in the control block, the control blocks must meet the following:

$$\hat{v}_{bus}\frac{1}{Z_{PVI}(s)} = \hat{v}_{bus}G_{PVI}(s)C_v(s)F_mG_{dibus}(s)\frac{1}{1+T_v(s)}, \tag{29}$$

where

$$T_v(s) = C_v(s)F_mG_{dvo}(s)K_d. \tag{30}$$

After finishing Formula (29), the transfer function of G_{PVI} is as follows:

$$G_{PVI}(s) = \frac{1}{Z_{PVI}(s)}\frac{1+T_v(s)}{C_v(s)F_mG_{dibus}(s)}. \tag{31}$$

In practice, G_{PVI} can be simplified conditionally. When $T_v \gg 1$, G_{PVI} can be simplified to $G_{PVIappr}$, facilitating the implementation of the circuit:

$$\begin{aligned} G_{PVIappr}(s) &= \frac{1}{Z_{PVI}(s)}\frac{1+T_v(s)}{C_v(s)F_mG_{dibus}(s)}\Big|_{T_v(s)\gg 1} \\ &\cong \frac{1}{Z_{PVI}(s)}\frac{G_{dvo}(s)K_d}{G_{dibus}(s)} \end{aligned}. \tag{32}$$

Notably, this control block is derived using the small-signal model of a simple post-converter. Taking the Buck converter as an example, referring to the Buck small-signal model of Figure 4, the input voltage symbol $\hat{v}_{in}$ is changed to $\hat{v}_{bus}$, and the input current $\hat{i}_{in}$ is changed to $\hat{i}_{bus}$. Then, we can obtain the following:

$$\begin{aligned} G_{dibus}(s) &= \frac{\hat{i}_{bus}}{\hat{d}}\Big|_{\hat{v}_{bus}=0} \\ &= \frac{DV_{bus}}{R_L} + \frac{DV_{bus}}{sL_o+\left(\frac{1}{sC_o}+r_{Co}\|R_L\right)} \end{aligned}, \tag{33}$$

$$\begin{aligned} G_{dvo}(s) &= \frac{\hat{v}_o}{\hat{d}}\Big|_{\hat{v}_{bus}=0} \\ &= V_{bus}\frac{\left(\frac{1}{sC_o}+r_{Co}\|R_L\right)}{sL_o+\left(\frac{1}{sC_o}+r_{Co}\|R_L\right)} \end{aligned}. \tag{34}$$

6. Effect of Virtual Impedance on the Overall Converter's Output Impedance and the Optimal Design of Virtual Impedance

From the explanation in Section 5 and Equation (28), it can be seen that the setting of Z_{PVI} is not a fixed value, but can be set within a range. When $Z_{PVIOP} \le |Z_{PVI}| \le Z_{PVIFL}$, the converter can make the system stable without exceeding the full load. Therefore, this section discusses how much Z_{PVI} parameters should be set to have the best overall output impedance performance after the power stage's circuit parameters are determined.

This section first discusses the effect of the converter's overall output impedance after adding the virtual impedance. Afterwards, the optimal design of the required impedance is explained mathematically.

As can be seen from the deduction of Section 5, the control block constructs Z_{PVI}. Therefore, when discussing the overall converter's output impedance, the small-signal model of the converter cannot be directly connected in parallel with the physical resistance, which must be re-derived by the control block. When discussing the output impedance in a closed loop, the input voltage disturbance $\hat{v}_{in}$ is set to zero, and the disturbance current $\hat{i}_o$ is fed from the output to observe its disturbance to the output voltage $\hat{v}_o$. Given that the duty cycle disturbance $\hat{d}$ in the closed-loop system is controlled by the output voltage $\hat{v}_o$ and the interstage voltage $\hat{v}_{bus}$, the duty cycle disturbance $\hat{d}$ is not zero when discussing the closed-loop output impedance. Figure 16 illustrates a small signal model referring to Figure 5, setting the input voltage disturbance $\hat{v}_{in}$ to zero and discussing the closed-loop output impedance's small-signal model.

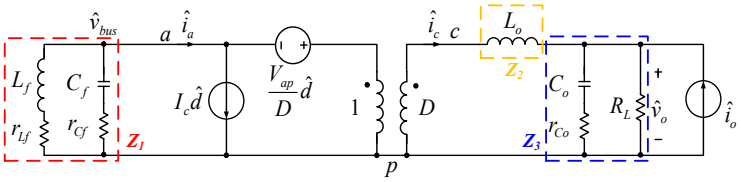


Figure 16. Small-signal model of the output impedance of an LC filter in series with a closed-loop Buck converter.

Figure 17 presents a block diagram of calculating individual transfer functions regarding Figure 16; a controller and a feedforward term G_{PVI} are added, and a control block diagram with virtual impedance is drawn.

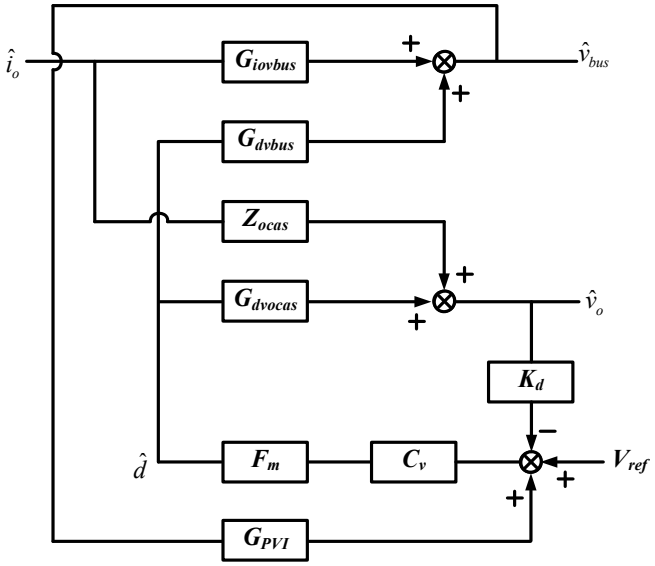


Figure 17. Control block diagram of an LC filter's output impedance in series with a closed-loop Buck converter with virtual impedance.

The transfer function of individual control blocks can be derived from Figure 16 as follows:

$$\begin{aligned} G_{iovbus}(s) &= \frac{\hat{v}_{bus}}{\hat{i}_o}\Big|_{\hat{d}=0} \\ &= \frac{1}{D}\left(Z_3 \| Z_2 + D^2 Z_1\right)\frac{D^2 Z_1}{D^2 Z_1 + Z_2} \end{aligned}, \tag{35}$$

$$\begin{aligned} G_{dvbus}(s) &= \frac{\hat{v}_{bus}}{\hat{d}}\Big|_{\hat{i}_o=0} \\ &= \frac{-DV_{IN}}{R_L}\left[Z_1 \| \frac{1}{D^2}(Z_2+Z_3)\right], \\ &\quad -\frac{V_{IN}}{D}\frac{Z_1}{Z_1+\frac{1}{D^2}(Z_2+Z_3)} \end{aligned} \tag{36}$$

$$\begin{aligned} Z_{ocas}(s) &= \frac{\hat{v}_o}{\hat{i}_o}\Big|_{\hat{d}=0} \\ &= Z_3 \| \left(Z_2 + D^2 Z_1\right) \end{aligned}, \tag{37}$$

$$\begin{aligned} G_{dvocas}(s) &= \frac{\hat{v}_o}{\hat{d}}\Big|_{\hat{i}_o=0} \\ &= \frac{-DV_{IN}}{R_L} Z_1 D \frac{Z_3}{D^2 Z_1 + Z_2 + Z_3} \\ &\quad + \frac{V_{IN}}{D} D \frac{Z_3}{D^2 Z_1 + Z_2 + Z_3} \end{aligned}. \tag{38}$$

From Figure 17, the nodal equation can be written as follows:

$$\hat{v}_o = \hat{i}_o Z_{ocas} + \hat{d} G_{dvocas}, \tag{39}$$

$$\hat{d} = (-K_d\hat{v}_o + G_{PVI}\hat{v}_{bus})C_vF_m, \tag{40}$$

$$\hat{v}_{bus} = \hat{i}_oG_{iovbus} + \hat{d}G_{dvbus}. \tag{41}$$

Equation (41) is substituted into Equation (40), and $\hat{d}$ is expressed as a function of $\hat{v}_o$ and $\hat{i}_o$. Then, $\hat{d}$ is brought into Equation (39), the output impedance with virtual impedance $Z_{ocasWpvi}$ can be obtained as

$$\begin{aligned} Z_{ocasWpvi} &= \frac{\hat{v}_o}{\hat{i}_o}\Big|_{w,Z_{PVI}} \\ &= \frac{Z_{ocas} + \frac{G_{iovbus}G_{PVI}C_vF_mG_{dvocas}}{1-G_{dvbus}G_{PVI}C_vF_m}}{1+\frac{K_DC_vF_mG_{dvocas}}{1-G_{dvbus}G_{PVI}C_vF_m}} \\ &= \frac{Num(Z_{ocasWpvi})}{Den(Z_{ocasWpvi})} \end{aligned}. \tag{42}$$

The output impedance of the closed loop without adding the virtual impedance Z_{ocasCL} is

$$\begin{aligned} Z_{ocasCL} &= \frac{\hat{v}_o}{\hat{i}_o}\Big|_{w/o,Z_{PVI}} \\ &= \frac{Z_{ocas}}{1+T_{vcas}} \\ &= \frac{Num(Z_{ocasCL})}{Den(Z_{ocasCL})} \end{aligned}, \tag{43}$$

where

$$T_{vcas} = K_DC_vF_mG_{dvocas}. \tag{44}$$

Figure 18 is a design example to compare the Bode plot of $|Z_{ocasWpvi}|$ and $|Z_{ocsCL}|$. Tables 1 and 2 in Section 7 show the circuit parameter values nd compensator design parameters. This section uses the G_{PVI} parameters of the exact solution described according to Equation (32). The $G_{PVIappr}$ parameters listed in Table 2 are simplified versions, which are easily implemented in analog circuits.

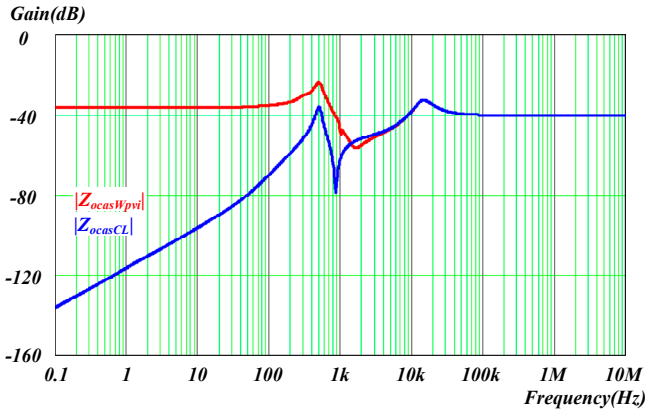


Figure 18. Bode plot of $|Z_{ocasWpvi}|$ and $|Z_{ocsCL}|$.

As can be seen from Figure 18, in the performance of the overall output impedance in the low-frequency band, the output impedance of the system without adding the virtual impedance will perform better. To explore this phenomenon, we compare Equation (40) with Equation (41).

First, = the denominators of $Z_{ocasWpvi}$ and Z_{ocasCL} are compared. According to $Den(Z_{ocasWpvi})$, the denominator of $Z_{ocasWpvi}$, when individual gain products $G_{dvbus}G_{PVI}C_vF_m$ and $K_DC_vF_mG_{dvocas}/G_{dvbus}G_{PVI}C_vF_m$ are much greater than 1, $Den(Z_{ocasWpvi})$ can be approximated as follows:

$$\begin{aligned} Den(Z_{ocasWpvi}) &= 1 + \frac{K_DC_vF_mG_{dvocas}}{1-G_{dvbus}G_{PVI}C_vF_m} \\ &\cong \frac{K_DC_vF_mG_{dvocas}}{G_{dvbus}G_{PVI}C_vF_m} \\ &= Den_{appr}(Z_{ocasWpvi}) \end{aligned}. \tag{45}$$

Substituting G_{PVI} of Formula (32) into Formula (45), Den_{appr} $(Z_{ocasWpvi})$ can be obtained:

$$Den_{appr}(Z_{ocasWpvi}) = \frac{K_D C_v F_m G_{dvocas}}{G_{dvbus} G_{PVI} C_v F_m} = \frac{G_{dvocas} G_{dibus}}{-G_{dvbus} G_{dvo}} Z_{PVI} \quad . \tag{46}$$

Substituting G_{PVI} of Formula (32) into Formula (45), Den_{appr} $(Z_{ocasWpvi})$ can be obtained:

$$Den_{appr}(Z_{ocasWpvi}) = \left(\frac{1}{Z_1} - \frac{D^2}{R_L}\right) Z_{PVI}. \tag{47}$$

Given that Z_1 can be regarded as approximately r_{Lf} in the low-frequency band, $Den_{appr}(Z_{ocasWpvi})$ can be regarded as a limited value in the low-frequency band. To reduce the steady-state error, the loop gain T_{vcas} will design extremely high gain in the low-frequency band. Therefore, it can be seen from Equation (43) that $Den(Z_{ocasCL})$ also has exceptionally high gain in the low-frequency band and is much larger than that of Den_{appr} $(Z_{ocasWpvi})$.

Figure 19 presents a Bode diagram of $|Den(Z_{ocasWpvi})|$, $|Den_{appr}(Z_{ocasWpvi})|$ and$|Den(Z_{ocasCL})|$. As can be seen from Figure 19, in the low frequency band, $|Den(Z_{ocasCL})|$ is greater than $|Den(Z_{ocasWpvi})|$. In the low frequency band, $|Den(Z_{ocasWpvi})|$ and $|Den_{appr}(Z_{ocasWpvi})|$ coincide with each other.

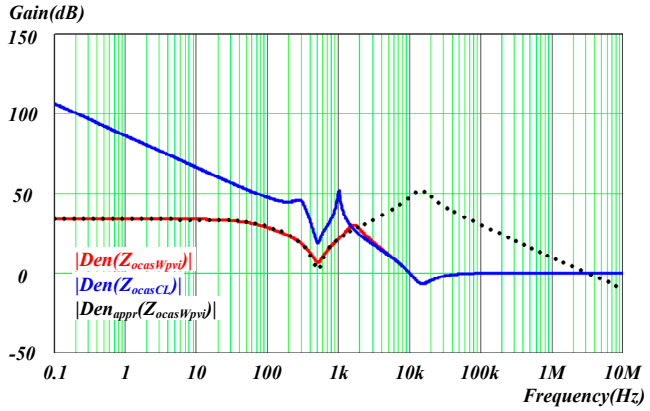


Figure 19. Bode plot of |Den($Z_{ocasWpvi}$)|, |Den_{appr}($Z_{ocasWpvi}$)| and |Den(Z_{ocasCL})|.

We now compare the numerator terms of $Z_{ocasWpvi}$ and Z_{ocasCL}. Figure 20 is a Bode plot of $|Num(Z_{ocasWpvi})|$ and $|Num(Z_{osCasCL})|$. By observing Figure 20, $|Num(Z_{ocasWpvi})|$ can be seen as higher than $|Num(Z_{osCasCL})|$ in the low-frequency band. Then, we compare the numerator terms of $Z_{ocasWpvi}$ and Z_{ocasCL}. Figure 20 presents a Bode plot of $|Num(Z_{ocasWpvi})|$ and $|Num(Z_{osCasCL})|$. By observing Figure 20, $|Num(Z_{ocasWpvi})|$ can be seen as higher than $|Num(Z_{osCasCL})|$ in the low-frequency band.

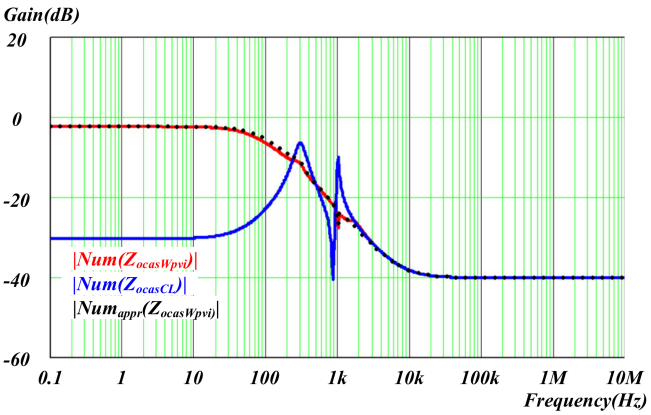


Figure 20. Bode plot of |Num($Z_{ocasWpvi}$)|, |Num_{appr}($Z_{ocasWpvi}$)| and |Num(Z_{ocasCL})|.

To explain this phenomenon, the performance of $Num(Z_{osCasCL})$ is first observed at low frequencies:

$$\begin{aligned} Num(Z_{ocasCL})\big|_{\sim DC} &= Z_{oCas}|_{\sim DC} \\ &= Z_3 \| \left(Z_2 + D^2 Z_1 \right) \Big|_{\sim DC} \\ &\cong R_L \| r_{Lf} D^2 \end{aligned} . \tag{48}$$

Second, $Num(Z_{ocasWpvi})$ is observed. Similarly, when $G_{dvbus} G_{PVI} C_v F_m$ is much higher than 1, Formula (48) is approximated as follows:

$$\begin{aligned} Num\left(Z_{ocasWpvi}\right) &= Z_{oCas} + \frac{G_{iovbus} G_{PVI} C_v F_m G_{dvo}}{1 - G_{dvbus} G_{PVI} C_v F_m} \\ &\cong Z_{oCas} + \frac{G_{iovbus} G_{PVI} C_v F_m G_{dvo}}{-G_{dvbus} G_{PVI} C_v F_m} \\ &= Num_{appr}\left(Z_{ocasWpvi}\right) \end{aligned} . \tag{49}$$

Equations (34)–(37) are substituted into Equation (49), and the performance of $Num_{appr}(Z_{ocasWpvi})$ at low frequencies is discussed as follows:

$$\begin{aligned} Num_{appr}\left(Z_{ocasWpvi}\right)\big|_{\sim DC} &= \left. \frac{\frac{{Z_3}^2}{R_L + Z_2 + Z_3}}{+ \frac{Z_1 D^2 Z_3 - {Z_3}^2 + Z_2 Z_3}{Z_1 D^2 + Z_2 + Z_3}} \right|_{\sim DC} \\ &\cong \frac{R_L}{2} + \frac{D^2 r_{Lf} R_L - {R_L}^2}{D^2 r_{Lf} + R_L} \end{aligned} . \tag{50}$$

As can be seen from Equations (48) and (50), in the case of low-frequency response and $D^2 r_{Lf}$ is much smaller than R_L, $|Num(Z_{ocasWpvi})|$ is higher than $|Num(Z_{osCasCL})|$ in the low-frequency band. Figure 20 also points out that $|Num_{appr}(Z_{ocasWpvi})|$ and $|Num(Z_{osWpvi})|$ coincide in the low-frequency band.

By deriving the numerator and denominator terms of $Z_{ocasWpvi}$ and Z_{ocasCL}, the $Num(Z_{ocasWpvi})$ of the denominator in the low-frequency band is smaller than $Num(Z_{ocasCL})$, and the numerator $Den(Z_{ocasWpvi})$ in the low-frequency band is higher than $Den(Z_{ocasCL})$. Therefore, in the overall output impedance performance of the low-frequency band, $|Z_{ocasWpvi}|$ is higher than $|Z_{ocasCL}|$. Although the system's stability is improved after adding the virtual impedance, it will sacrifice the transient response of the output.

Reviewing Equation (47), we can find that the gain of $Den_{appr}(Z_{ocasWpvi})$ is proportional to Z_{PVI}. That is, the larger the Z_{PVI}, the smaller the $|Z_{ocasWpvi}|$. With Figure 14 and Equation (29), we can see that to minimize $|Z_{ocasWpvi}|$, the design of Z_{PVI} should choose $Z_{PVI} = Z_{PVIFL}$. Figure 21 presents a Bode plot comparing $|Z_{ocasWpvi}|$ under different Z_{PVI}. From Figure 21, $|Z_{ocasWpvi}|$ is found to have the minimum value under the design with $Z_{PVI} = Z_{PVIFL}$.

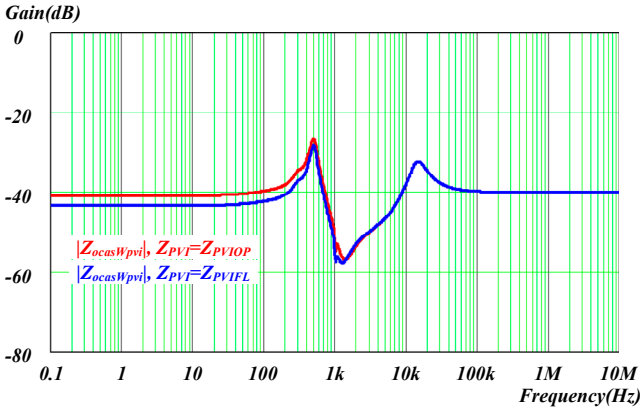


Figure 21. Bode plots of $|Z_{ocasWpvi}|$ under different Z_{PVI} designs.

After adding the virtual impedance, the output impedance of the overall converter will increase. Therefore, in practice, the G_{PVI} feed-forward term will be added to a band-pass filter. Apart from adding the isolated DC term to the control loop, the Z_{PVI} is only involved in the system in the frequency band that must increase the input impedance of the subsequent stage, thereby reducing the impact on the overall output impedance.

7. Simulation and Implementation Results

When the series system of the LLC series Buck is unstable, the stress on the resonant element will largely increase and the element will become damaged. Therefore, the verification uses the equivalent LC filter series Buck converter as the experimental platform. Therefore, the LC filter's input voltage V_{in} is set to 48 V to simulate the output voltage of the LLC converter, and the impedance of the resonant tank is converted according to the turns ratio of the transformer (400/48).

The design example used in this paper is to observe and verify the stability of the system and the overall output impedance, both of which are affected by the addition of virtual impedance. The parameter design of the circuit is designed based on the limitation of the measuring instrument. Since the electronic load Chroma 63204 can only generate the disturbance current up to 20 kHz, to observe the change of the overall output impedance before and after adding virtual independence, the resonance frequency of the source equivalent LC filter is designed to be about 500 Hz. The gain of Z_{oS} seen by the post-stage stage is slightly larger than the Z_{inCL} seen by the second-stage converter under full load operation; this makes the series system unstable without adding virtual impedance. So when the converter's full-load output wattage is set to 96 W and the Bus voltage is 48 V, the component parameters of the post-stage LC filter can be designed. The closed-loop crossover frequency of the final converter is designed to be 10 kHz. Under the general design concept, the crossover frequency is about 1/6 to 1/10 times the switching frequency, so the Buck converter's switching frequency is set to 100 kHz. In order to make the Z_{inCL} before the crossover frequency a fixed value, the resonance frequency of the LC filter of the Buck converter is about 600Hz, away from the closed-loop crossover frequency, and a lower peak value of $|1/Z_{inOP}|$ is designed. Such circuit design parameters make it easier to design the compensator so that the closed-loop gain T_v has enough gain to meet $|T_v| \gg |1/Z_{inOP}|$.

Table 1 shows the parameter value of the series circuit, and Table 2 presents the transfer function of the feedback voltage divider, compensator, feedforward term and band pass filter, and other control terms. Figure 22 illustrates a system wiring diagram to understand the connection relationship of each transfer function.

Table 1. Circuit parameters.

Symbol	Parameter Name	Specification
f_{sw}	Switching frequency	100 kHz
V_{in}	Input voltage	48 V
V_{bus}	Inter-stage voltage	48 V
D	Duty cycle	0.25
R_L	Full load resistance	1.5 Ω
L_f	Filter inductance	1 mH
r_{Lf}	Filter inductance series resistance	0.5 Ω
C_f	Filter capacitance	100 μF
r_{Cf}	Filter capacitance series resistance	1 nΩ
L_o	Output inductance	33 μH
C_o	Output capacitance	2200 μH
r_{Co}	Output capacitance series resistance	10 mΩ

Table 2. Control parameters.

Symbol	Parameter Name	Specification
K_d	Feedback voltage division ratio	2.5/12
C_v	Compensator	$\frac{(1+2.64\times10^{-4}s)(1+3.16\times10^{-4}s)}{2.534\times10^{-5}s\times(1+2.4\times10^{-5}s)(1+1.676\times10^{-5}s)}$
$G_{PVIappr}$	Approximate feedforward term	$\frac{1}{Z_{PVI**}}\frac{2.5}{12}\left(\frac{1806.14}{602.45+s}\right)$
F_m	Sawtooth modulation coefficient	1/3
G_{HPF}	High pass filter	$\frac{1}{1+\frac{1}{0.01s}}$
G_{LPF}	Low pass filter	$\frac{1}{1+\frac{s}{0.33\times10^5}}$
Z_{PVIOP}	Virtual impedance setting (no load)	42 Ω
Z_{PVIFL}	Virtual impedance setting (full load)	56 Ω

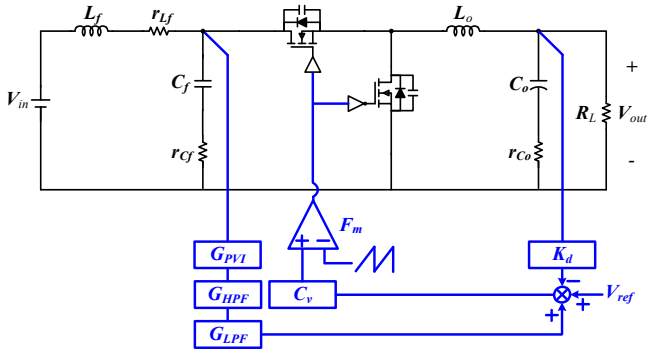


Figure 22. System wiring diagram.

Figure 23 shows the results of design and simulation cross-validation to prove that the mathematical model is consistent with the circuit simulation results. As can be seen from Figure 23, the maximum value of $|Z_{oSP}|$ is approximately 20.25 dB. To stabilize the system under no load, $Z_{PVI} = Z_{PVIOP}$ is designed to be 42 Ω, thereby generating a gain margin of approximately 6 dB in the system. According to Equation (26), the maximum output wattage P_{oLM} is 109.7 W. The designed full load wattage is 96 W; then, the load resistance of the full load can be reversed to 1.5 Ω. Figure 23 shows the calculation results obtained from the parameters in Tables 1 and 2. At this time, for the Z_{PVI**} parameter in G_{PVI}, $Z_{PVI**} = Z_{PVIOP}$ is selected. Before the system adds the virtual impedance, the phase margin is approximately 1 dB, and the system is in an unstable state. After adding the virtual impedance to the system, the input impedance of the subsequent stage can be increased in the frequency range of 15.9 Hz to 5.3 kHz, and the gain margin is increased by approximately 6dB, which stabilizes the series system.

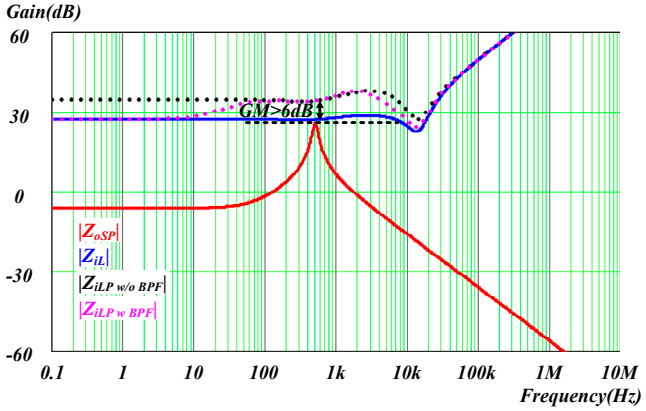


Figure 23. Bode plot of input impedance comparison before and after adding virtual impedance.

After analyzing the frequency domain response, Figure 24 presents the time domain verification results. Figure 24a shows the simulation result. The virtual impedance is not added before t = 50 ms, and the system shows oscillation. After t = 50 ms, the virtual impedance feedforward loop is added to the system, and the system is stabilized. Figure 24b shows the test result of the physical circuit. Moreover, before the virtual impedance feedforward is added, the system shows oscillation. After putting in the virtual impedance feedforward loop, the system returns to stability. In Figure 24b, the voltage disturbance amplitude when v_{BUS} and v_O are unstable is smaller than the voltage amplitude under ideal conditions. The reason is that the voltage source used in the experiment is not an ideal voltage source. It only has a unidirectional power transmission function instead of bidirectional power transmission and contains its equivalent series impedance. Therefore, the simulation results using an ideal voltage source are different from the actual experimental results. However, the experimental results can still highlight adding virtual impedance to stabilize the series system.

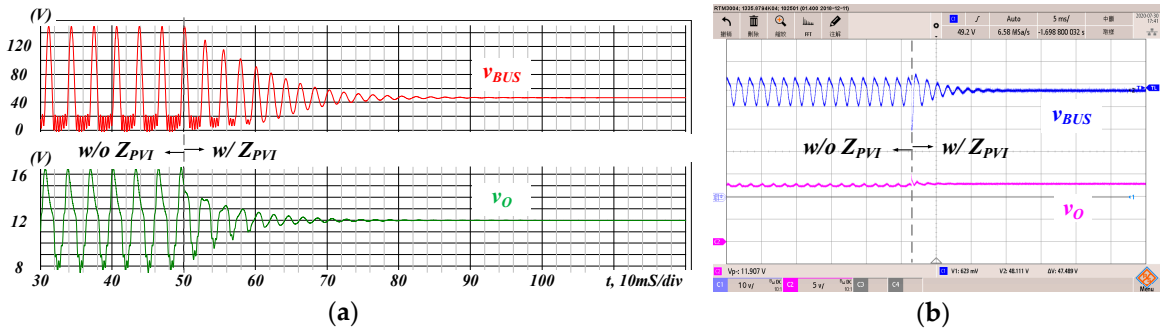


Figure 24. System waveform before and after adding virtual impedance (**a**) simulation results (**b**) actual measurement results (scale v_{BUS} [Ch1]: 50V/div; i_O [Ch2]: 5A/div; v_O [Ch3]: 20 V/div; time: 1 ms/div).

To measure the effect of different Z_{PVI} on the overall output impedance, we switch the band-pass filter to a high-pass filter to increase the output impedance's observable range. It can be inferred from Equation (28), and Z_{PVI} is designed with the load resistance of R_L = 1.5 Ω, then, Z_{PVI} = Z_{PVIFL} = 56 Ω.

Z_{PVI} is set to Z_{PVI} = Z_{PVIOP} = 42 Ω and Z_{PVI} = Z_{PVIFL}= 56 Ω, respectively. Two feedforward designs are placed into the system. The input voltage source is Chroma 62150H-1000. The spectrum analyzer NF FRA5096 is used with the electronic load Chroma 63204 to scan the overall output impedance of the two different designs as shown in Figure 25. As can be seen from Figure 25, under the design of Z_{PVI} = Z_{PVIFL} = 56 Ω, the overall output impedance is small. The correctness of the deduction in Section 6 is verified.

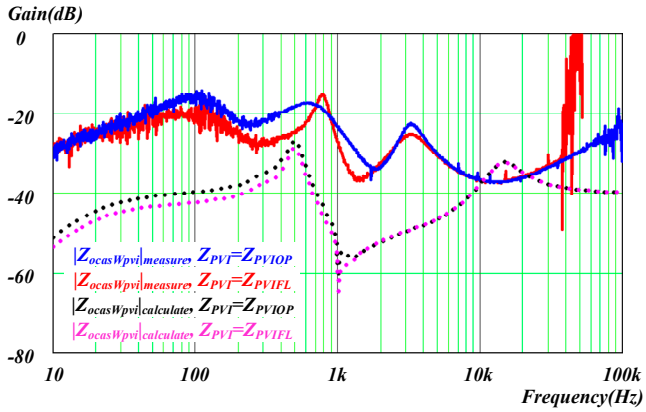


Figure 25. Measurement results and theoretical calculation results of overall output impedance.

However, the actual measurement results are not entirely consistent with the results derived from the mathematical model. The reason is that the input voltage source is not an ideal voltage source.

The actual instrument used as a voltage source has its own output impedance, plus the error on the measuring instrument, these two factors make the measured overall output impedance data differ from the ideal theoretical calculation result. Nonetheless, the trend of the curve is consistent with the description of this paper.

8. Conclusions

This thesis takes the LLC series Buck as an example circuit to study the system stability conditions of a two-stage series system and the overall series system's output impedance performance. The entire series system's small-signal model can be directly connected in series using the individual converter's small-signal model when the ESR of the output capacitor in the individual converter is relatively small. In discussing the cascade system's stability, if the input impedance of the downstream converter is to be approximated to a specific value of negative impedance, it is necessary to check whether the open-loop input impedance and closed-loop gain meet the approximate conditions. The Middlebrook criterion has described the stability conditions of the two-stage series system. Designing a two-stage converter based on this criterion may make the converter unable to achieve the best efficiency, making the converter design a compromise between stability and efficiency performance. In order to achieve a more flexible design of the converter, the control loop is adopted to add virtual impedance to improve the system stability.

Although the parallel virtual impedance can increase the system's stability, it will increase the overall output impedance. This research establishes a complete mathematical discussion of this phenomenon to understand the design limitations when applying the parallel virtual impedance and how to choose the most appropriate design to reduce the impact of the overall output impedance. As can be seen from the mathematical derivation, the design of Z_{PVI} must meet the series system's stability gain margin requirements at any load conditions below full load wattage P_{oFL} of the designed converter, so the design of Z_{PVI} must meet $Z_{PVIOP} \leq |Z_{PVI}| \leq Z_{PVIFL}$. Among them, set $Z_{PVI} = Z_{PVIFL}$ is the best design for parallel virtual impedance to get the lowest overall output impedance. Besides, in order to further reduce the effect of virtual impedance on the overall output impedance, a band-pass filter is needed to reduce the effect of feedforward on the overall output impedance.

The mathematical model and simulation in this paper are cross-validated to prove the correctness of the mathematical model. Furthermore, an impedance analyzer measures the actual circuit to validate this paper's mathematical derivation and discussion.

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