energies

MDPI

Article

A Novel Cascaded Multilevel Converter Topology Based on Three-Phase Cells—CHB-SDC †

Renner Sartório Camargo [1,2,3,*], Daniel Santamargarita Mayor [2], Alvar Mayor Miguel [4], Emilio José Bueno [2] and Lucas Frizera Encarnação [3]

1 Department of Control and Automation Engineering, Federal Institute of Espírito Santo (IFES), Rod. ES010, Serra 29173-087, Brazil
2 Department of Electronics, Alcalá University (UAH), Plaza San Diego S/N, 28801 Madrid, Spain; daniel.santamargarit@uah.es (D.S.M.); emilio.bueno@uah.es (E.J.B.)
3 Department of Electrical Engineering, Federal University of Espírito Santo (UFES), Av. Fernando Ferrari, 514, Vitória 29075-910, Brazil; lucas.encarnacao@ufes.br
4 Department of Power Electronics, Siemens Gamesa, 28043 Madrid, Spain; amayor.soria@gmail.com
* Correspondence: rscamargo@ifes.edu.br; Tel.: +55-27-98132-9988
† This paper is an extended version of our paper published in 2020 IEEE 29th International Symposium on Industrial Electronics (ISIE), "A Novel Cascaded Multilevel Converter Topology Based on Three-Phase Cells with Model Predictive Control", Delft, The Netherlands, 17–19 June 2020; pp. 1161–1166.

Received: 6 August 2020; Accepted: 11 September 2020; Published: 14 September 2020

Abstract: This paper proposes a new cascaded multilevel converter topology based on three-phase H bridge cells with a common DC-link structure. The proposed multilevel converter topology main advantages, compared with literature renowned multilevel converters topologies, are discussed in the paper, such as modularity, construction, implementation cost, and DC voltage ripple mitigation. Despite presenting an elementary structure and easy implementation, the use of classic PWM switching strategies is not feasible for this topology, causing the appearance of several short-circuit states between its capacitors. Thus, a graph theory algorithm combined with a model predictive control is also proposed in this work to identify and avoid the new cascaded multilevel converter short-circuit switching states and, concomitantly, guaranteeing the converter output power quality. In order to validate the presented topology applicability, a low voltage synchronous static compensators (STATCOM) with an optimal switching vector model predictive control (OSV-MPC) is implemented in a hardware-in-the-loop platform. The real-time experimental results prove the proposed multilevel topology and the OSV-MPC control strategy effectiveness.

Keywords: multilevel converter; CHB; model predictive control; CHB-SDC; STATCOM; real-time; OPAL

1. Introduction

In the last decade, the electric energy demand increase caused by the use of high-power industrial loads, the incentive to decentralized generation, as well as the need for better energy generation systems integration, including renewable energy sources, have presented themselves as major challenges for the electrical systems' operators [1,2]. In order to provide, for example, the proper energy matrix integration [3], the electrical systems stability maintenance, or even the reactive power compensation in offshore wind farms, the use of advanced power electronic devices is essential to meet the requirements for the modern grid's operation, electricity quality included [4]. Additionally, the smart grid concept is increasingly present in the electrical infrastructure, and such equipment can add resilience to the power systems, making their responses to emergency situations more robust [5].

Encouraged by this technological demand for power electronic devices, specific equipment has been developed to improve electrical energy quality and stability and reliability of power networks. [2,6,7]. However, the rapid expansion in electricity demand culminated in a voltage level increase, in order to reduce costs in the cable infrastructure and, consequently, the values referring to losses by Joule effect in electrical installations. This voltage increase could exceed the semiconductor switches' physical limits, making it impossible to use conventional converters directly connected to medium voltage grids [8,9].

Based on the technological deficit regarding semiconductor switches' physical voltage limit, the interest for multilevel converters in high-power applications in medium voltage distribution systems has grown significantly [10]. Multilevel converters have some benefits over conventional converters, including the ability to synthesize more voltage levels, the use of lower power semiconductor devices [1], less harmonic distortion due to the stepped level voltage output, less noise generation, and ease of operation at lower switching frequencies [9].

Despite the multilevel converters' operational benefits, their main disadvantage is the high cost due to the increase in the number of components as the voltage levels increase, limiting their use in higher value-added applications.

Therefore, this work is motivated by the presentation of a new modular multilevel converter topology, with reduced cost compared to the structures most used today, to expand this technology's reach to a more significant number of applications, mainly in low and medium voltages. However, despite having fewer components, this proposal presents several short-circuit states when used with switching based on pulse width modulation, requiring the development of its own strategy to activate its switches.

In this context, this work provides, in addition to an innovative multilevel converter topology, a solution for the short-circuit states elimination based on high frequency with model predictive control (MPC), capable of not only eliminating the short-circuit stages in the capacitors but also to explore all the switching states remaining without losing the converter controllability and power quality.

The topology proposed in this work can replace the classic cascaded H bridge converter (CHB) in several power electronic applications involving multilevel converters, such as: back-to-back (B2B) converters for driving motors or static loads [11]; solid state transformers (SST) for connecting a wide variety of energy sources to the power grid [12]; unified power quality conditioners (UPQC) to actively improve the quality of electricity [13]; synchronous static compensators (STATCOM) for compensating reactive power, mitigating harmonics, and improving power factor [14,15]; and others.

In most cases, the applications mentioned use multilevel converters, depending on the voltage level involved, connecting rectifier stages to inverter stages through a DC-link. The use of multilevel CHB in some applications requires galvanic isolation stages, usually provided by high or low-frequency transformers to avoid short-circuit stages inherent to these topologies [16,17]. In this CHB- single DC (SDC) proposal, if there is a possibility of implementing a three-phase converter structure and using a reduced number of components, the isolation stages could be eliminated, further reducing the cost of these applications.

With the current regulation regarding the generation and electric energy commercialization and new restrictions imposed by economic and environmental factors, there was an increase in the participation of wind generation in the power system [18].

Most wind farms use doubly-fed induction generator (DFIG) systems because of the several advantages this machine offers, such as increased efficiency and the ability to decouple the control of active power and reactive power for better integration in the power grid. However, due to the fact that the DFIG has the stator directly coupled to the grid, being more sensitive to faults and unstable wind characteristics, power plants based on wind generation have stability problems when connected to the power grid. Under these conditions, STATCOM presents itself as a good solution for dynamic reactive power compensation according to grid voltage variation.

In addition to wind farms applications, STATCOM can act as a voltage regulator, power flow control, transient stability, and dampening power oscillation, among others. Besides, the use of H bridge cells is a good option for STATCOM applications, due to the DC-link capacitors' presence, which helps to reduce the current total harmonic distortion (THD), keeping its amplitude index close to 1.0, especially when these devices provide reactive power to the system [18].

Due to the modernity of applications that require actuators based on power electronics, STATCOM was chosen to prove the functioning of the proposed CHB-SDC topology and validate the switching strategy based on MPC in order to eliminate the short-circuit states inherent to this structure.

The paper is organized as follows: Section 2 presents a comparison between the most used topologies of multilevel converters, mainly regarding the evolution of the number of its components. Section 3 presents a study of the short-circuit states inherent to the proposed topology, and a comparison between this new converter topology and the classical CHB topology. Section 4 presents the model predictive control developed for the CHB-SDC with a STATCOM functionality. Section 5 presents the OPAL-RT hardware-in-the-loop platform results and compares and analyzes the steady-state and dynamic performance of the CHB-SDC with two distinct classical CHB designs, followed by the conclusions in Section 6.

2. Multilevel Topologies' Comparison

There are several multilevel converter topologies available in the literature and some are more frequently used in medium voltage applications, such as the diode-clamped multilevel converter (DCMC) [2,19], the capacitor-clamped multilevel converter (CCMC) [2,20], the modular multilevel converter (MMC) [2,21,22], and the cascaded H bridge converter (CHB) [2,23,24]. However, the DCMC and CCMC topologies, as shown in Figure 1, have an almost exponential relationship between the output voltage levels and the number of components required by the converts. This exponential relationship is due to the DCMC and CCMC topologies' nonmodularity structure, requiring a massive increase in the diode/capacitor ratio. Thus, some authors [23,25] proposed structure modifications in order to incorporate the modularity in the DCMC and CCMC topologies, presenting a mixed-level hybrid multilevel cell (MHMC) using three-level single-phase DCMC or CCMC cells in order to compose the three-phase multilevel converters (MHMC DCMC and MHMC CCMC). Therefore, as shown in Figure 1, even presenting a linear relationship, an advantage from the modularity structure, MHMC DCMC, and MHMC CCMC topologies present higher electrical components and DC voltage oscillation with twice the power grid fundamental frequency (2ω), usual in single-phase converter structures.

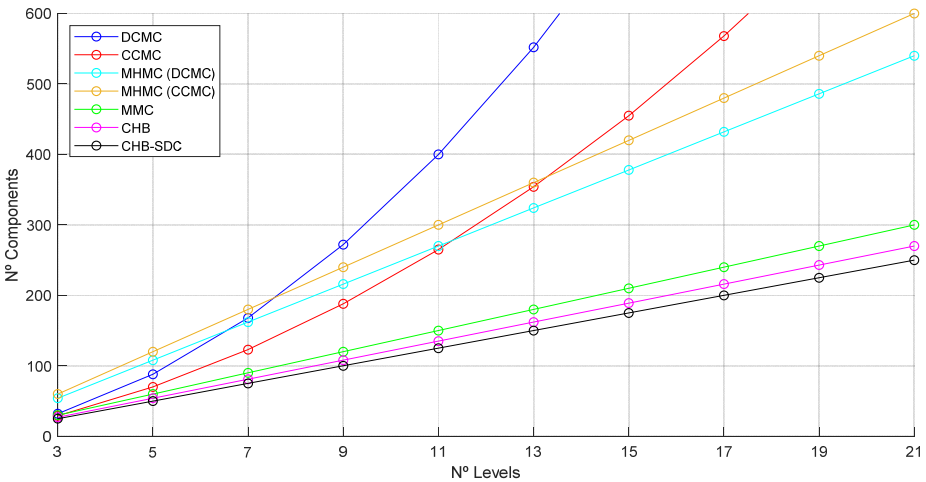


Figure 1. Elements quantities comparison required for each multilevel converter according to the number of levels.

There is also the asymmetric hybrid multilevel cells (AHMC) topology [23,25] that proposes a moderate growth in the number of components required versus voltage levels number. However, the AHMC topology does not have modular characteristics and presents a very complex DC-link capacitor voltage control due to the different DC voltage values [25].

Among the different topologies, only the CHB, MMC, and MHCM have modular structures, allowing additional connection of cell series connection. Furthermore, the CHB topology stands out with fewer components than other topologies, as shown in Figure 1.

Inherent to its construction, the CHB has a large number of capacitors due to its single-phase structure [9]. This particularity imposes the need for an elaborated DC-link voltage control, however less complex than the MHCM. Besides, each DC-link presents voltage oscillation with twice the power grid fundamental frequency, compromising, in some cases, the synthesized voltage. Such voltage oscillation is characteristic of converters and rectifiers with single-phase topology, not observed in devices with typical three-phase characteristics [26].

The comparison between the most used topologies and the structure proposed in this paper is shown in Table 1. The CHB-SDC structure is the only one that presents a small evolution in the number of components, having modularity and absence of 2ω-oscillation, simultaneously.

Table 1. Comparison between multilevel topologies.

Topology	Number of Components	Modularity	2ω Oscillation
DCMC	very high	no	no
CCMC	high	no	no
MHMC (DCMC)	high	yes	yes
MHMC (CCMC)	high	yes	yes
MMC	low	yes	yes
CHB	low	yes	yes
CHB-SDC	very low	yes	no

Therefore, in order to propose an upgrade to the classical CHB structure, this work suggests a new power converter topology that can be used in a wide variety of applications. This proposed topology also uses H bridge cells, like the single-phase based CHB, utilizing, however, a three-phase DC-link structure, employing three times fewer capacitors when compared to the conventional single-phase CHB topology [9]. Furthermore, this topology is also free from the low-frequency DC-link energy oscillation typical from single-phase converters. A constructive elements comparison between the new topology proposed (named Cascaded H Bridge Converter with Single DC-link (CHB-SDC)) and other classic topologies in the literature is shown in Figure 1, considering the same voltage level numbers to be synthesized, demonstrating that the CHB-SDC has a better number of components versus voltage level ratio when compared to the other topologies discussed [9].

However, despite the constructive simplicity, fewer structural components, and the DC-link voltage oscillation mitigation, CHB-SDC provides many short-circuit states if a switching strategy based on pulse width modulation is used [27], making this topology unfeasible when used with these classic switching strategies [9]. The short-circuit states analysis of the proposed topology will be presented and developed in Section 3.

3. The CHB-SDC Analysis

This section presents the main advantages of CHB-SDC topology over the classic CHB and then presents an analysis of short-circuit states in the new proposal.

3.1. The CHB-SDC Topology

As previously mentioned, this paper suggests a new power converter topology, employing three times fewer capacitors than classic CHB due to its three-phase structure, thus, reducing the total cost of the converter, and reducing the DC-link voltage control complexity [9].

The CHB classical multilevel structure and the CHB-SDC topology are shown in Figure 2a,b, respectively, where its H bridge structures can be observed, as well as its modular attributes, which is important for defective cell replacement [28,29], and also for future expansion of its quantity, for example [30,31]. The main constructive difference between the compared topologies refers to the capacitor connections and the DC-links designing, which have single-phase structures in the traditional CHB and three-phase structure in the CHB-SDC topology [9].

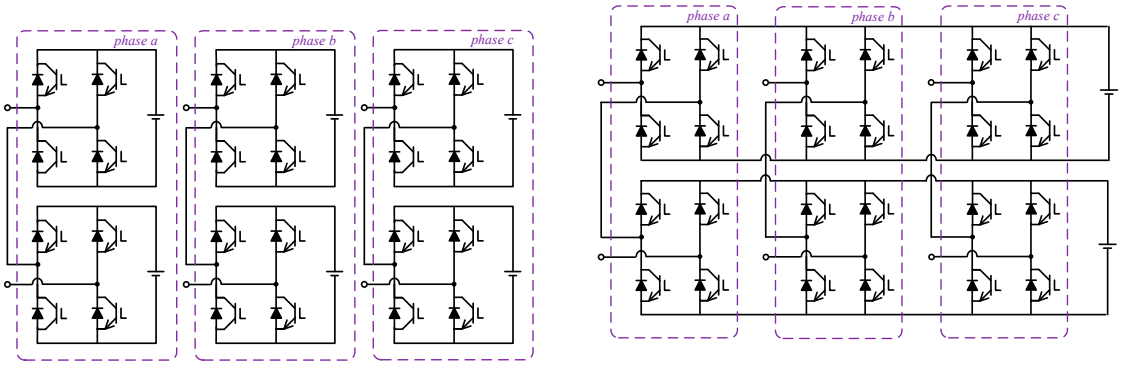


Figure 2. Structural comparison between topologies: (**a**) classical multilevel cascaded H bridge converter (CHB) topology; (**b**) proposed CHB-single DC (SDC) topology [9].

Regarding the number of capacitors necessary to produce the appropriate DC-link ripple values, the CHB-SDC structure, besides presenting a smaller number of capacitors than single-phase structures, presents total capacitance values, on average, six times lower than the classical CHB topology [27,32–35]. Some studies claim that these values can be up to 10 times lower [28,36–38], demonstrating evident superiority of three-phase structures over single-phase structures in terms of the total capacitance.

The Equations (1) [27] and (2) [28] used in this work represent the total capacitance for the CHB and the CHB-SDC, respectively.

$$C_{CHB} = \frac{P}{\omega \cdot U_{DC} \cdot \Delta U} \tag{1}$$

$$C_{CHB-SDC} = \left(\frac{1}{10}\right)\frac{P}{\omega \cdot U_{DC} \cdot \Delta U} \tag{2}$$

where C_{CHB} and $C_{CHB-SDC}$ are the total CHB and CHB-SDC capacitance, respectively. P is the total converter power. ω the grid angular frequency. U_{DC} is the DC link voltage average. ΔU is the DC link voltage ripple.

It is important to highlight that the values obtained by (1) and (2) represent the total converter capacitance values, that is, even though CHB-SDC has three times fewer capacitors, it has 10 times less total capacitance used than the classic CHB for the same voltage ripple values design. That is, considering $C_{CHB} = 10 \cdot C_{\text{CHB-SDC}}$, and $N_{CHB} = 3 \cdot N_{CHB-SDC}$, where N_{CHB} and $N_{CHB-SDC}$ are the CHB and CHB-SDC amount of capacitors, respectively, the values of individual capacitors in both topologies are expressed by (3) and (4):

$$C_{iCHB-SDC} = \frac{C_{CHB-SDC}}{N_{CHB-SDC}} \tag{3}$$

$$C_{iCHB} = \frac{C_{CHB}}{N_{CHB}} = \frac{10 \cdot C_{CHB\_SDC}}{3 \cdot N_{CHB-SDC}} = \left(\frac{10}{3}\right)\frac{C_{3\varnothing}}{N_{CHB-SDC}} = \left(\frac{10}{3}\right)C_{iCHB-SDC} \tag{4}$$

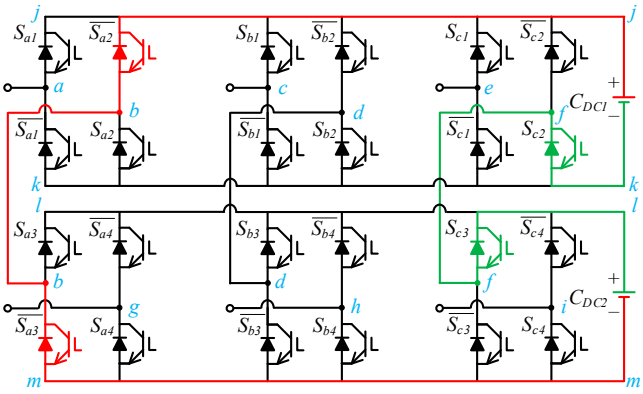
where $C_{iCHB-SDC}$ and C_{iCHB} are the CHB-SDC individual capacitor value and CHB individual capacitor value, respectively.

So, for a given DC link ripple value, not only does the CHB structure has three times more capacitors than the CHB-SDC structure but each CHB individual capacitor will have a capacitance value $\frac{10}{3}$ times greater than the CHB-SDC individual capacitor, which increases the equipment cost and volume.

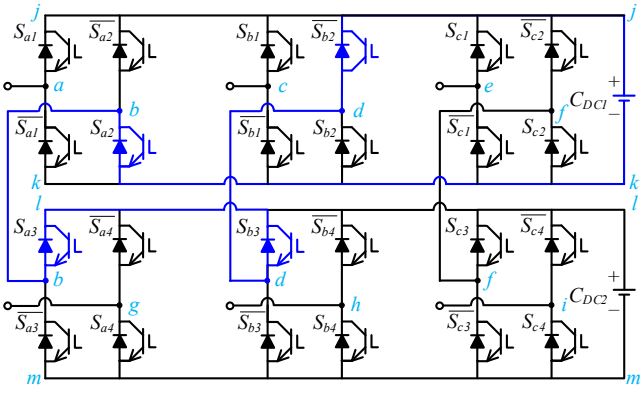
3.2. Converter Short-Circuit States Analysis

For the CHB-SDC short-circuit analysis, a five-level output phase voltage converter was chosen, as shown in Figure 2b, which can be connected directly to the grid or to a load, or through a transformer. CHB-SDC has some switching states in which one or both capacitors are short-circuited, which could damage the converter [9]. Since these failures occur in several switching states, these converters cannot be used without an additional stage capable of avoiding their natural short circuits using PWM strategies, for example [27].

The effective methodology development capable of mapping the prohibitive states becomes a critical barrier to be overcome during studies about the short-circuit stages inherent to this converter. Therefore, a path analysis taken by the electric current in each different state combination of each converter switch is necessary. This condition is illustrated in Figure 3, where each of the 24 semiconductor switches in this topology has two possible states (*ON* or *OFF*), being possible 2^{24}, that is, 16,777,216 different switching states.

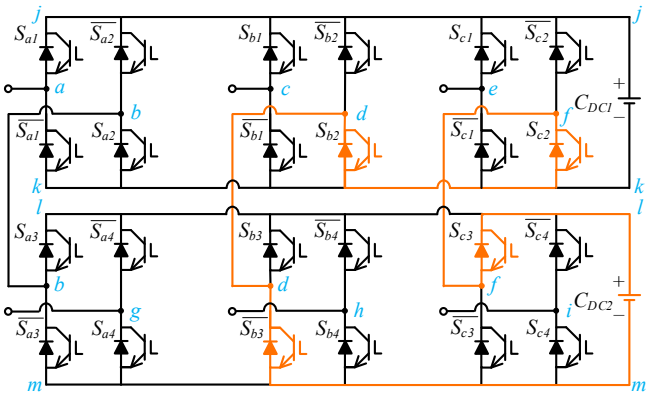


(**a**)



(**b**)

Figure 3. *Cont.*



(**c**)

Figure 3. CHB-SDC short-circuit current path examples: (**a**) C_{DC1} and C_{DC2} in short-circuit [9]; (**b**) C_{DC1} in short-circuit; (**c**) C_{DC2} in short-circuit.

However, the switches in the same H bridge module arm are interlocked, that is, the S_{a1} switch has an opposite state to the $\overline{S_{a1}}$ switch, for example. This strategy, known as unipolar modulation, reduces the number of control signals and, as a result, reduces the number of different switching states.

Due to this converter structural peculiarity virtue, it can be controlled with just 12 processed signals, referring to the S_{nm} switches (where $n = a, b, c$ and $m = 1, 2, 3, 4$). Thus, the amount of possible combinations reduces to 2^{12}, that is, 4096 distinct states, sharply sparing the required processing capability.

The graph theory was applied to map all possible converter switching states and identify each of its allowed or prohibited states. This theory consists of a mathematical branch intended to study relationships between objects of a given set, producing abstract graphic structures known as graphs. A graph is represented by a set of so-called vertices and their interdependent relations known as edges. In the studied converter case, each electrical node was classified as a vertex and each switch as an edge, thus allowing to trace all the existing electrical current paths. One of many prohibited states identified in the referred converter is highlighted in red and green in Figure 3, where both capacitors (C_{DC1} and C_{DC2}) are short-circuited.

Figure 4 illustrates the converter graph, showing all possible CHB-SDC connections where we can observe the existence of three possible short-circuit types: the first one with the C_{DC1} capacitor in the fault state, that is, with the j point connected to the k point; the second with the C_{DC2} capacitor in short-circuit, that is, with the l point connected to the m point; and, finally, the third, with the C_{DC1} and C_{DC2} capacitors, simultaneously, in short-circuit, that is, with the j point connected to the m point and the k point connected to the l point, simultaneously. The colored lines in Figure 4 correspond to the short circuits highlighted in Figure 3.

Thus, with the graph theory applied to this five-level converter, a computer algorithm was developed, capable of gathering each one of the 4096 possible paths and mapping the converter's unipolar switching states [9,11,17,38]. However only 640 states are useful for equipment operation, that is, these combinations do not generate short-circuit states. Such amount represents less than 16% of all possible combinations.

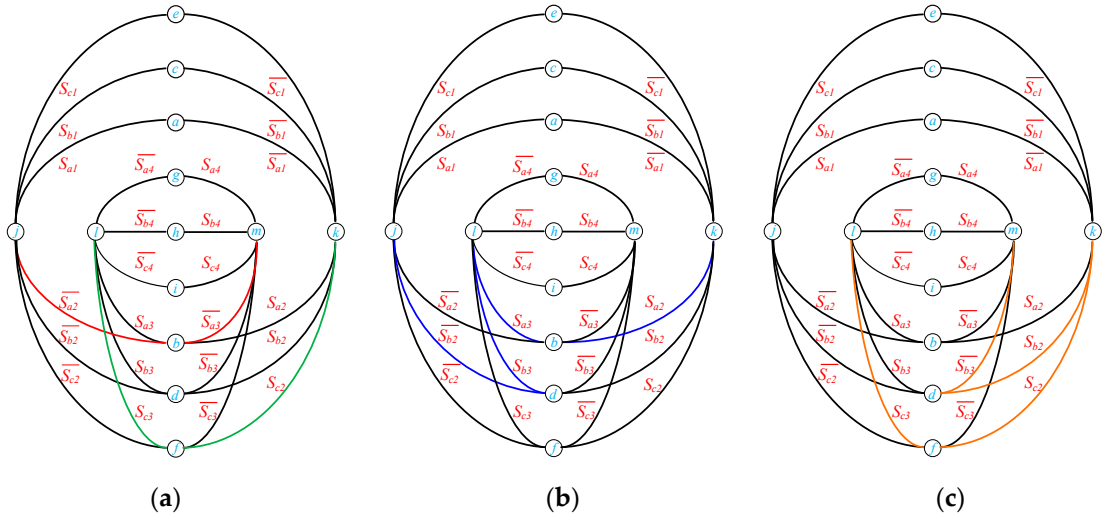


Figure 4. Graphs for CHB-SDC short-circuit states analysis: (**a**) C_{DC1} and C_{DC2} in short-circuit [9]; (**b**) C_{DC1} in short-circuit; (**c**) C_{DC2} in short-circuit.

Although the vast majority of switching states represent prohibitive states, that is, short-circuit states, the converter is able to synthesize all five voltage levels per phase, as shown in Figure 5, where the red dots represent the possible three-phase vector voltage. This characteristic is essential for building a three-phase sinusoidal wave with low total harmonic distortion (THD), a fundamental condition for the use of the CHB-SDC in several power electronics equipment, as the STATCOM mentioned above.

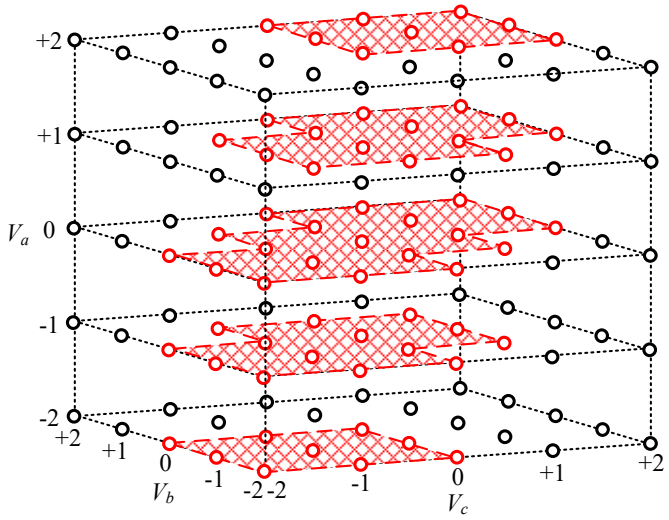


Figure 5. Possible voltage vectors per phase after restrictions [9].

4. Model Predictive Control

Model predictive control has been a research and development topic since the 1970s when it was initially introduced into the process industry [39–41]. The MPC has a broad concept, involving many areas, its central concept being the prediction, based on a mathematical model, of all the future system states, given a determined time horizon. An optimized control action is then chosen to minimize the cost function, which is based on a reference and the predicted states. As the cost function optimization requires much computational effort, only from the 1990s on [42], with the significant technological

advancement of microprocessors, this strategy was proposed and studied as a promising alternative for the control of energy converters and drives [43].

The use of the control in power electronics converters is restricted to the set of equipment possible switching states. Thus, the MPC becomes a feasible option with less implementation complexity [23,41].

Among all the MPC classifications in the literature, the most applied to power electronics converters is the optimal switching vector (OSV-MPC), used in this work, which has low implementation complexity and fast dynamic response even though it was the first predictive control strategy developed. This strategy consists of scanning each possible switching state and its objective is to get the best combination of semiconductor switches that produces the smallest error between the desired reference and the signal to be built in the next time step only [23]. Therefore, this type of predictive control produces a harmonic content spread across the frequency spectrum due to its variable switching frequency, thus increasing the passive filter design complexity for the application in which it is applied [41,44].

Figure 6 shows the overview operation of the OSV-MPC applied to the CHB-SDC with a STATCOM application, which e_{Sn} and i_{Sn} are the measured voltages and currents source, U_{DCn} are the measured DC-link voltages, U^*_{DCn} are the DC-link voltage references, U_n are the synthesized STATCOM voltages, $P(k+2)$ and $Q(k+2)$ are the predicted active and reactive powers, $p_{loss}(k+2)$ is the required change in the active power flow in order to regulate the DC-link capacitor voltage [45,46], $P^*(k+2)$ and $Q^*(k+2)$ are the active and reactive reference powers, k and k+2 is the actual and predicted states after two time steps in order to compensate the processing delay signals, N is the total prediction states, S_{opt} is the optimal switching state and n is the phase to which it refers (a, b, or c).

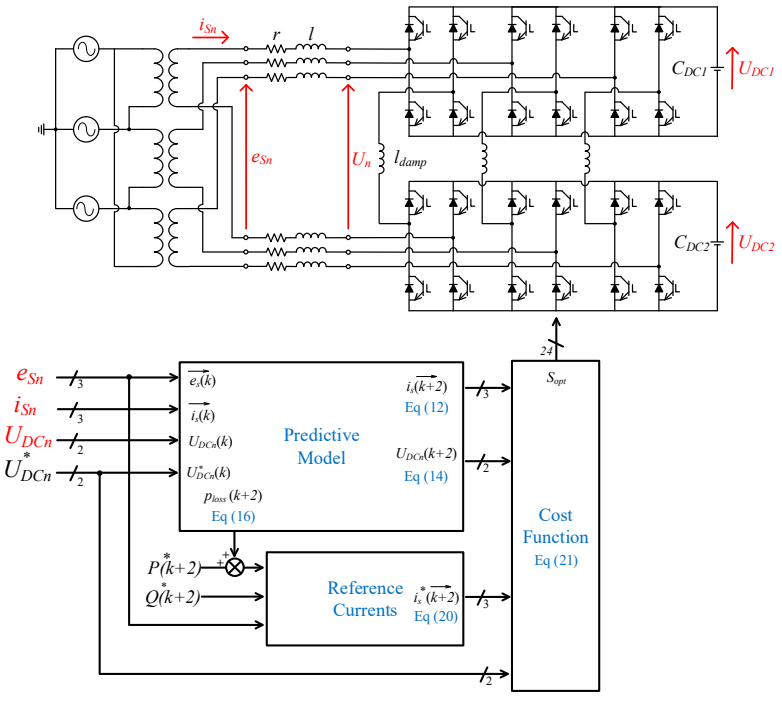


Figure 6. Graphical description of CHB-SDC synchronous static compensators (STATCOM) topology using model predictive control (MPC).

4.1. STATCOM Model Predictive Control

The STATCOM basic mathematical development using CHB-SDC topology is demonstrated as follows, in which C_{DCk} is the DC-link capacitor voltage, r and l are the RL resistance and inductance filter, and l_{damp} is the damping inductance to reduce the current peak between upper and lower H bridge modules [9,47].

Thus, the STATCOM voltage U_n, considering C_{DC1} and C_{DC2} with the same voltage value (U_{DC}), can take on $[-2U_{DC,} - U_{DC}, 0, +U_{DC}, +2U_{DC}]$ values, that is, five voltage levels. But it is important to point out that the MPC uses the present and predicted DC-link voltage values to perform the calculations [48,49].

The current equation in the RL filter loop is given by (5) using the Kirchhoff voltage law [9,45]:

$$e_{Sn} - 2l\frac{di_{Sn}}{dt} - 2ri_{Sn} - l_{damp}\frac{di_{Sn}}{dt} - U_n = 0 \tag{5}$$

Applying the Euler numerical integration method, the system discrete equation is presented in (6), being T_s the sample time for discretizing.

$$e_{Sn}(k) - \frac{2l}{T_s}(i_{Sn}(k) - i_{Sn}(k-1)) - 2ri_{Sn}(k) - \frac{l_{damp}}{T_s}(i_{Sn}(k) - i_{Sn}(k-1)) - U_n^N = 0 \tag{6}$$

For the continuation of the mathematical development, it must be considered that the source voltage value is the same for the next time step and that the source current between two consecutive time steps will be the same for the next instant. These estimates are due to the power grid frequency being much lower than the switching frequency [17,46].

With these approaches, the model can be simplified, and, after mathematical development, Equations (7)–(9) are obtained. Equation (9) represents the predicted current.

$$e_{Sn}(k) - \frac{2l}{T_s}(i_{Sn}(k+1) - i_{Sn}(k)) - 2ri_{Sn}(k) - \frac{l_{damp}}{T_s}(i_{Sn}(k+1) - i_{Sn}(k)) - U_n^N(k+1) = 0 \tag{7}$$

$$\left(\frac{2l + l_{damp}}{Ts}\right)i_{Sn}(k+1) = e_{Sn}(k) + \frac{2l}{T_s}i_{Sn}(k) + \frac{l_{damp}}{T_s}i_{Sn}(k) - 2ri_{Sn}(k) - U_n^N(k) = 0 \tag{8}$$

$$i_{Sn}(k+1) = \frac{T_s}{2l + l_{damp}}\left(e_{Sn} + \frac{2l}{T_s}i_{Sn}(k) + \frac{l_{damp}}{T_s}i_{Sn}(k) - 2ri_{Sn}(k) - U_n^N(k)\right) \tag{9}$$

The term U_n^N represents the STATCOM module voltage multiplied by the respective switching function $S_{nx}(k)$, which x is the module index (upper or lower) according to Equation (10):

$$U_n^N(k) = S_{n1}(k) \cdot U_{DC1}(k) + S_{n2}(k) \cdot U_{DC2}(k) \tag{10}$$

The function $S_{nx}(k)$ represents all possible switching states in each converter module, equal to -1, 0 or 1, respectively, when a negative, neutral or positive voltage is produced at the module output.

The predicted DC-link capacitor voltages, $U_{DCx}(k+1)$, can be obtained taking into account its present value as well as the current contribution of each phase [46,48], relating them to the capacitance value and its switching functions, presented in (11), where C is the capacitor capacitance.

$$U_{DCx}(k+1) = U_{DCx}(k) + \frac{T_s}{C}(S_{ax} \cdot i_{Sa}(k) + S_{bx} \cdot i_{Sb}(k) + S_{cx} \cdot i_{Sc}(k)) \tag{11}$$

At the kth time instant, the MPC performs a scan through Equations (9) and (11) and uses the converter inherent switching function $S_{nx}(k)$, in order to predict the currents determined by $i_{Sn}(k+1)$ and the converter voltages expressed by $U_{DCx}(k+1)$. Afterward, a cost function is computed, using a combination between the reference signals and the predicted values, thus, selecting the optimal control by choosing the switching states that produce the lowest cost function value.

However, this strategy implementation in practice can only be applied in the $(k+1)$th time instant due to the hardware computational delay [44,46]. Thus, a step time delay must be inserted in the system to compensate for this peculiarity.

Therefore, at the kth time instant, the MPC computes the $(k + 1)$th system state through the Equations (9) and (11). Subsequently, the control effects a new scan, but this time, using the calculated $(k + 1)$th values to predict the $(k + 2)$th values, represented through (12) to (14), only the cost function is calculated, and the optimal vector is chosen [46,50].

$$i_{Sn}(k+2) = \frac{T_s}{2l + l_{damp}}\left(e_{Sn} + \frac{2l}{T_s}i_{Sn}(k+1) + \frac{l_{damp}}{T_s}i_{Sn}(k+1) - 2ri_{Sn}(k+1) - U_n^N(k+1)\right) \quad (12)$$

$$U_n^N(k+1) = S_{n1}(k+1)\cdot U_{DC1}(k+1) + S_{n2}(k+1)\cdot U_{DC2}(k+1) \quad (13)$$

$$U_{DCx}(k+2) = U_{DCx}(k+1) + \frac{T_s}{C}(S_{ax}\cdot i_{Sa}(k+1) + S_{bx}\cdot i_{Sb}(k+1) + S_{cx}\cdot i_{Sc}(k+1)) \quad (14)$$

When the reference signals are calculated, the coupling between the active power and the DC-link capacitor's voltages must be taken into account, that is, the DC-links regulation requires an extra active power amount that causes an additional active power flow related to the capacitors in order to keep these voltages close to the set reference values [9,46]. This real power p_{loss} is the sum of each capacitor power portions p_{DCx}, as shown in Equations (15) and (16) [46].

$$p_{DCx}(k+2) = \frac{C}{T_s}\left[(U_{DCx}{}^*(k+2))^2 - (U_{DCx}(k+1))^2\right] \quad (15)$$

$$p_{loss}(k+2) = \sum_{x=1}^{2} p_{DCx}(k+2) \quad (16)$$

The active and reactive reference powers, $P^*(\mathrm{k}+2)$ and $Q^*(\mathrm{k}+2)$, are determined by the system operator and used to reference currents calculation through instantaneous power theory [51]. The required capacitor power p_{loss} is added to the active power reference becoming in the total active power reference $P^*_{T(K+2)}$, as shown in Equation (17).

$$P_T^*(k+2) = p_{loss}(k+2) + P^*(k+2) \quad (17)$$

In the STATCOM developed in this work, the active reference power $P^*(k+2)$ was null, being used only to supply the internal capacitors losses (16). The reactive power reference is provided by an author's free choice pattern in order to cover situations of reactive supply and consumption, however, $Q^*(\mathrm{k}+2)$ can be originated according to the end-user needs, either through a factor power control or any other desired.

Thus, $P_T^*(\mathrm{k}+2)$, $Q^*(\mathrm{k}+2)$, and e_{Sn} pass through a $\alpha\beta$-current calculation transformation and then through an inverse Clarke transformation to build the reference currents $i^*_{sn}(k+2)$ [51], as are expressed from (18) to (20).

$$\begin{bmatrix} e_{S\alpha}(k+1) \\ e_{S\beta}(k+1) \end{bmatrix} = \sqrt{\frac{2}{3}}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}\begin{bmatrix} e_{Sa}(k+1) \\ e_{Sb}(k+1) \\ e_{Sc}(k+1) \end{bmatrix} \quad (18)$$

$$\begin{bmatrix} i^*_{S\alpha}(k+1) \\ i^*_{S\beta}(k+1) \end{bmatrix} = \frac{1}{e_{S\alpha}(k+1)^2 + e_{S\beta}(k+1)^2}\begin{bmatrix} e_{S\alpha}(k+1) & e_{S\beta}(k+1) \\ e_{S\beta}(k+1) & -e_{S\alpha}(k+1) \end{bmatrix}\begin{bmatrix} P_T^*(k+2) \\ Q_T^*(k+2) \end{bmatrix} \quad (19)$$

$$\begin{bmatrix} i^*_{Sa}(k+1) \\ i^*_{Sb}(k+1) \\ i^*_{Sc}(k+1) \end{bmatrix} = \sqrt{\frac{2}{3}}\begin{bmatrix} 1 & 0 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}\begin{bmatrix} i^*_{S\alpha}(k+1) \\ i^*_{S\beta}(k+1) \end{bmatrix} \quad (20)$$

4.2. Cost Function

The MPC cost function main objective applied to STATCOM is to scan all possible switching combinations and choose which state has the smallest error between the reference currents and the predicted currents, in addition to the smallest error between the reference and the predicted DC-link capacitor voltages. However, since the prohibitive states must be avoided, there is also the addition of a penalty in the cost function.

The expression for the cost function adopted in this study is shown in (21), where g^N is the cost for all the switching states, W_{ia}, W_{ib}, W_{ic}, W_{UDC1} and W_{UDC2} are the weight factors and P_{en} is the described penalty [46].

$$\begin{aligned} g^N = {} & W_{ia}[i^*_{sa}(k+2) - i_{sa}(k+2)]^2 + W_{ib}\left[i^*_{sb}(k+2) - i_{sb}(k+2)\right]^2 \\ & + W_{ic}[i^*_{sc}(k+2) - i_{sc}(k+2)]^2 + W_{UDC1}\left[U^*_{DC1}(k+2) - U_{DC1}(k+2)\right]^2 \\ & + W_{UDC2}\left[U^*_{DC2}(k+2) - U_{DC2}(k+2)\right]^2 + P_{en} \end{aligned} \tag{21}$$

In this work, a null active power reference, $P^*(\mathrm{k}+2) = 0$, was used in order to obtain the equipment behavior only as a provider of reactive power, as a STATCOM. Furthermore, as all possible converter states are known, whether they are prohibitive or not, it was decided to use only the switching states that do not cause short circuits in equipment, saving computational processing and thus suppressing the term P_{en} in Equation (21) [9].

5. Experimental Results

In order to demonstrate, not only the CHB-SDC superiority over the classic CHB but also its technical feasibility, the experimental results of both structures were compared on a real-time platform. For the experiment, the topologies were applied as a STATCOM device with similar characteristics and the same voltage and current levels.

Both converters are configured with five-level phase-voltage, connected in a 400 V rms grid voltage, and providing ±25 kVAr reactive power. The CHB-SDC is controlled by the OSV-MPC described previously, and the CHB uses a classical set of linear controls, with a combination of global and cluster DC voltage balancing, well established in the literature [7,52], combined with a classical multicarrier phase shift pulse width modulation (PSPWM).

5.1. Real-Time Platform

A powerful hardware-in-the-loop (HIL) platform has been used to experimentally investigate the CHB-SDC STATCOM operation [53,54]. The OPAL-RT 5700, using a potent processor, can allow a high-frequency drive solution providing complete OSV-MPC implementation and power plant emulation through the eFPGASIM tool present in the equipment.

This HIL implementation has an optional computer as a supervisor, connected to the hardware, setting the references and some element values, with access to the generated waveforms. The signals were obtained through the signal acquisition boards and the oscilloscope Yokogawa DL750 connected to I/O ports. This architecture is shown in Figure 7a, and the implementation image in Figure 7b.

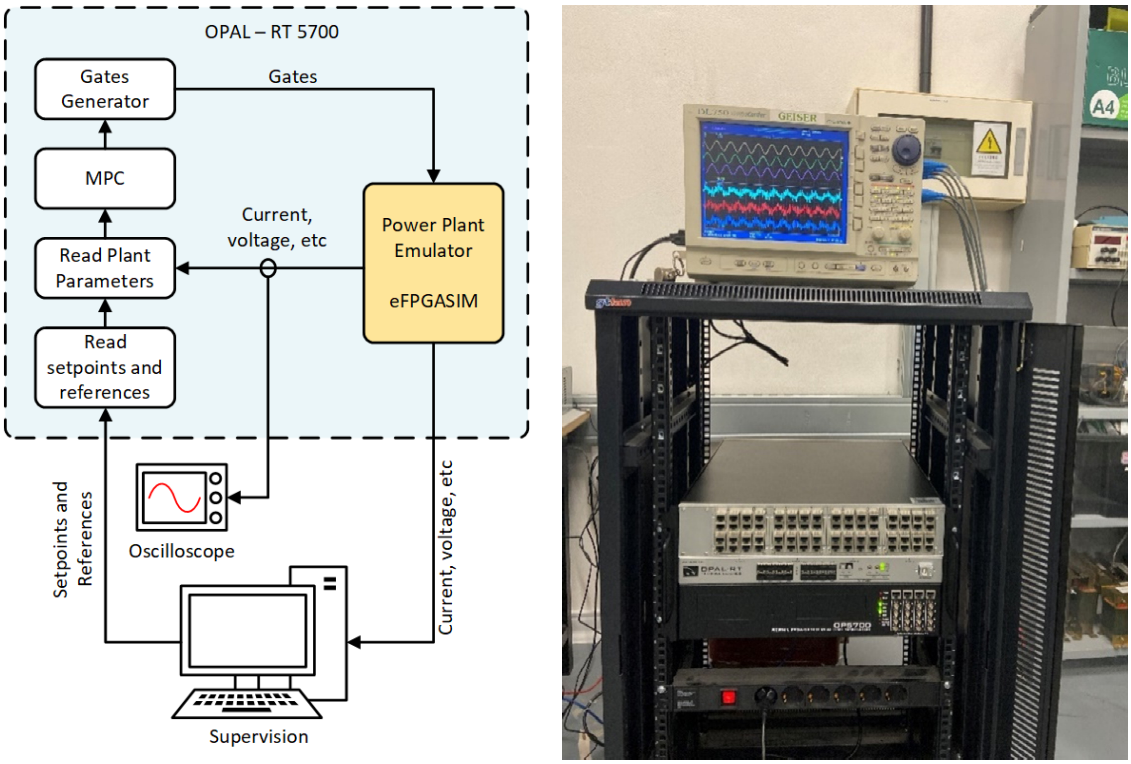


Figure 7. Hardware-in-the-loop implementation: (**a**) OPAL-RT 5700 Flowchart; (**b**) Implementation image with emphasis on signals in the oscilloscope.

As previously mentioned, the computational hardware delay considered is one-time step, being necessary to perform all calculations and comparisons related to (k + 1)th values and to predict the (k + 2)th states system [53,54].

Some experimental results obtained on the OPAL-RT 5700 platform through signal acquisition plates and the Yokogawa DL750 oscilloscope are shown in Figure 8, where it is possible to observe the synthesis of the grid current and the STATCOM voltage signals, as well as the voltage variation of the DC-link of the capacitors. Clearer and more elaborate experimental results will be shown below, from Figure 9.

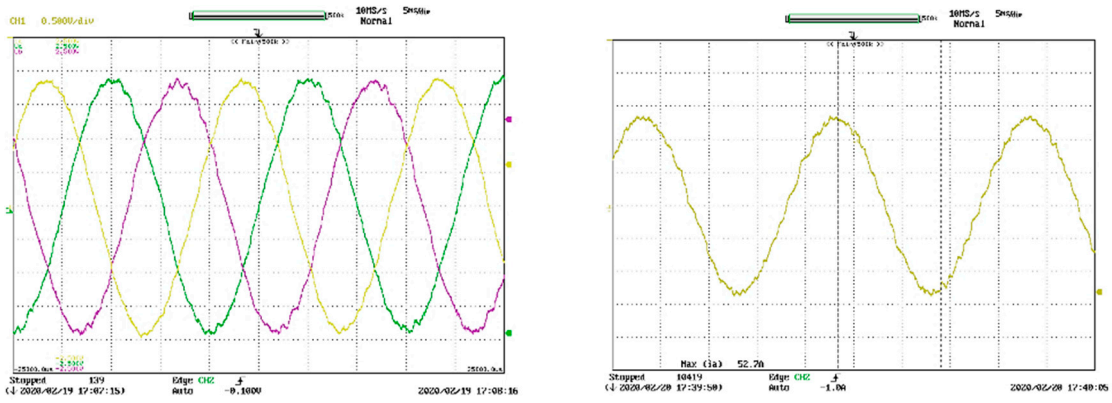


Figure 8. *Cont.*

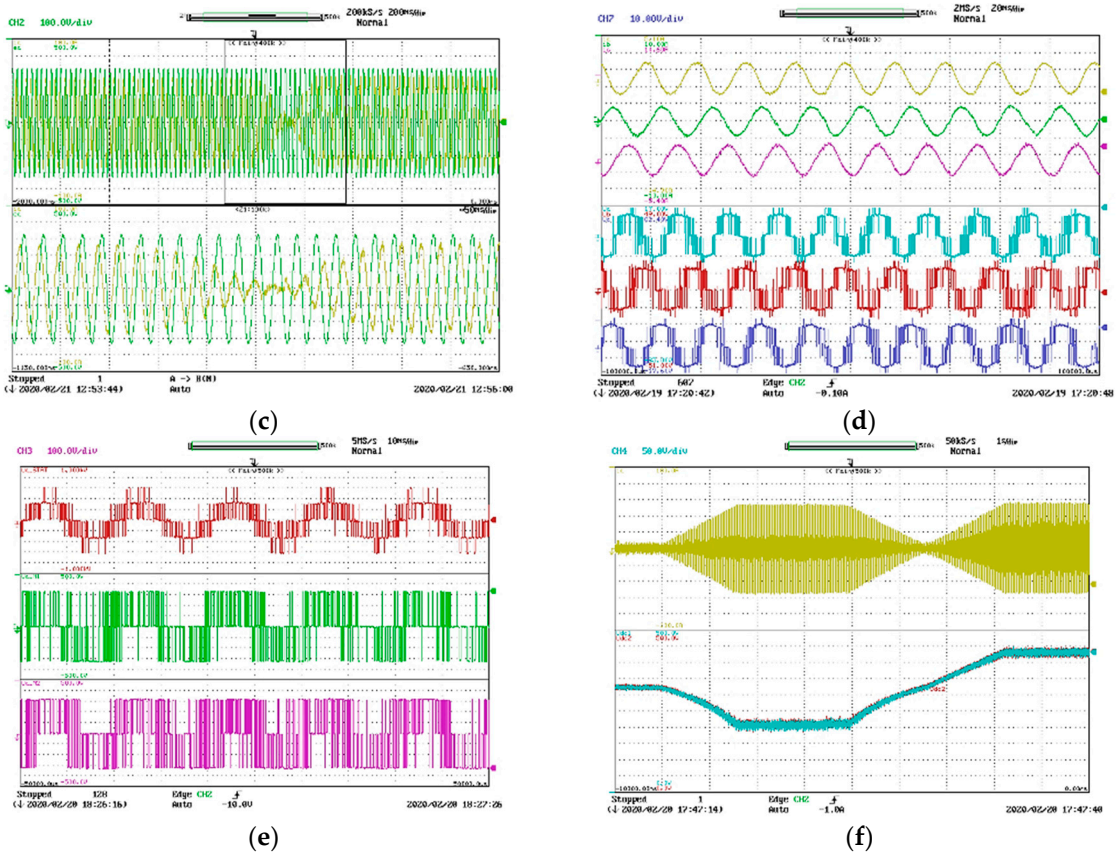


Figure 8. Experimental results: (**a**) three-phase grid currents; (**b**) single-phase grid current; (**c**) single-phase grid current in changing mode; (**d**) grid currents and synthesized STATCOM voltages in the same screen; (**e**) synthesized STATCOM voltage and its voltage per module; (**f**) capacitor DC-link voltages variation.

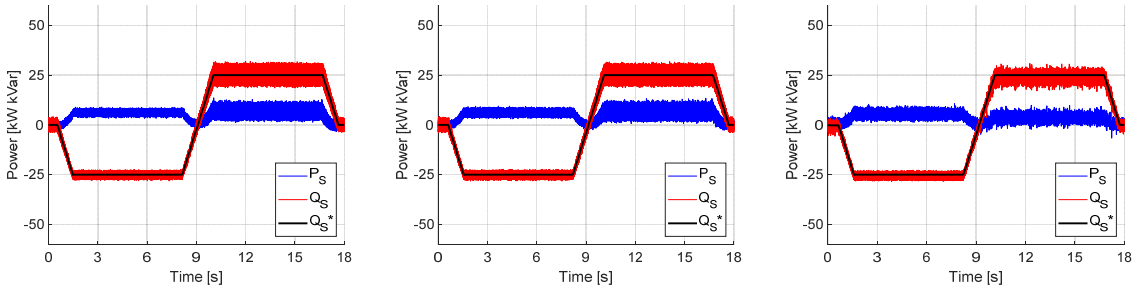


Figure 9. Active and reactive power: (**a**) CHB $(4000\ \mu F)$; (**b**) CHB $(1200\ \mu F)$; (**c**) CHB-SDC $(1200\ \mu F)$.

5.2. Results

The five-level CHB-SDC and the CHB experimental results configured as STATCOM are verified by means of implementation in OPAL-RT 5700 in order to demonstrate the proposal viability.

Thus, two comparisons between the converters were developed: one with equal DC-link voltage ripple values; and another with equal capacitance individual values.

When using a $1{\cdot}10^{-4}s$ time step (T_s) to call the OSV-MPC functions, the control analyzes whether it needs to change the state of any switch, thus producing a variable switching frequency that is not expressed exactly by the T_s value. As the CHB-SDC OSV-MPC provides the semiconductor switches activation in the three phases, simultaneously, it was necessary to observe the average number of changes per cycle per phase produced by the converter with the adopted time step value. Thus, for a

CHB PSPWM, a 2 kHz carrier frequency was chosen in order to generate the same 40 switchings per cycle per phase observed in the CHB-SDC OSV-MPC with $1{\cdot}10^{-4}s$ T_s.

5.2.1. Equal DC-Link Voltage Ripple

This comparison between CHB and the proposed topology uses the same DC-link voltage ripple per capacitor in order to observe the difference in design capacitance values.

Equation (1) was used to design the CHB capacitors, where the maximum ripple is designed for 11 V. The DC-link voltage average is 300 V, the angular frequency is $2{\cdot}\pi{\cdot}50$, and the power is 25 kW.

According to (1):

$$C_{CHB} = \frac{25{\cdot}10^3}{2{\cdot}\pi{\cdot}50{\cdot}300{\cdot}11} = 24,114.4\ \mu F\ \approx 2400\ \mu F \tag{22}$$

This is, since the CHB has six capacitors, where each device has approximately 4000 μF. Thus, for this experiment, all ripple value (in CHB and in CHB-SDC topology) are equal, approximately 11 V.

5.2.2. Equal Capacitance

This comparison between CHB and the CHB-SDC topologies uses the same capacitance values per capacitor in order to observe the difference in the DC-link voltage ripple.

Equation (2) was used to dimension the proposed topology capacitors, where the maximum ripple designed is 11 V; the other parameters are the same as in the previous implementation.

According to (2):

$$C_{CHB-SDC} = \frac{25{\cdot}10^3}{10{\cdot}2{\cdot}\pi{\cdot}50{\cdot}300{\cdot}11} = 2411.44\ \mu F\ \approx 2400\ \mu F \tag{23}$$

This is, since CHB-SDC topology has only two capacitors, each device has approximately 1200 μF. Thus, for this experiment, all capacitors (in CHB and in CHB-SDC topologies) are equal, with 1200 μF individual capacitance. It's important to note the CHB total capacitance is six times the individual values, because it has six capacitors, equal to 7200 μF.

The system parameters used are shown on Table 2.

Table 2. System parameter specifications.

Parameter	Symbol	CHB Equal Ripple	CHB Equal Capacitance	CHB-SDC
Rms grid line voltage	e_s	400 V	400 V	400 V
Grid frequency	f_s	50 Hz	50 Hz	50 Hz
STATCOM power	S_{nom}	±25 kVA	±25 kVA	±25 kVA
MPC time step	T_s	-	-	$1e^{-4}$s
Sampling time	T_{samp}	$5e^{-5}s$	$5e^{-5}s$	$5e^{-5}s$
Carrier frequency	f_c	2.0 kHz	2.0 kHz	-
Damping inductance	l_{damp}	1 mH	1 mH	1 mH
Filter inductance	l	5 mH	5 mH	5 mH
Filter resistance	r	200 mΩ	200 mΩ	200 mΩ
DC-link voltage	U_{DC}	220 V – 400 V	220 V – 400 V	220 V – 400 V
DC-link capacitance	C_{DC}	4000 μF	1200 μF	1200 μF
total capacitance	C_{TOT}	24,000 μF	7200 μF	2400 μF

The complete experimental results obtained on the OPAL-RT 5700 platform through signal acquisition plates and the oscilloscope are shown from Figure 9, where in each figure, the images (a) refer to CHB with 11 V ripple (equal DC voltage ripple), the images (b) refer to CHB with 1200 μF individual capacitance (equal capacitance), and the images (c) refer to CHB-SDC with 11 V ripple and 1200 μF individual capacitance.

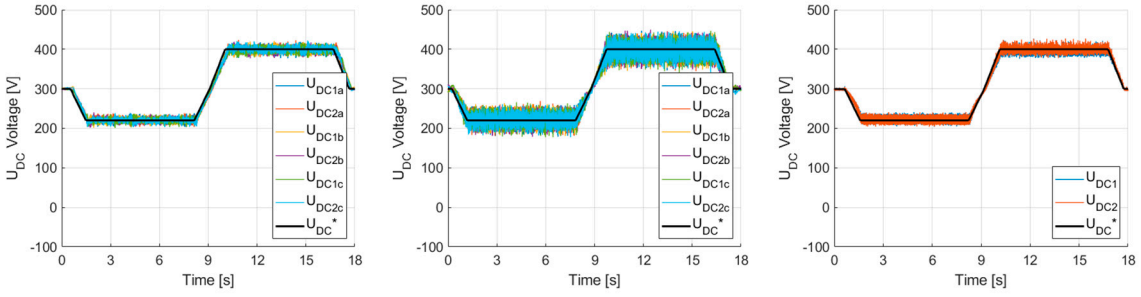
The oscilloscope data was imported into the MATLAB software only for better graphical presentation, having not been manipulated and maintaining their originality.

The reference powers are specified to validate the proposed topology and control system strategy, maintaining a null active power, $P^*(k+2) = 0$, and ranging the reactive power, $Q^*(k+2)$, from -25 kVAr to $+25$ kVAr to observe the converters steady-state and dynamic performances in the same conditions.

The CHB and CHB-SDC behaviors due to reactive power variation are demonstrated in Figure 9, presenting in both CHB configurations higher active power ripple than in CHB-SDC, although all of them are set to 0 W as the central value. These ripples are observed also in CHB reactive power curves when the STATCOM requires positive *VArs*, being the classic controllers present in this topology challenging to tune. Furthermore, CHB-SDC presents an automatic and fast synchronization with the grid, minimizing the power errors and showing well-defined curves.

DC-link capacitor voltages analysis is one of the most crucial investigation points for the converters, since their perfect functioning depends on consistent design and adequate capacitance values, being the main topic of the comparison between the chosen topologies. Therefore, for better converters response, the reference DC-link capacitor voltages adapt to the required power, increasing or decreasing according to its variation, therefore when the STATCOM needs to consume reactive power, the DC-link voltage values reduce. In contrast, when the equipment needs to provide reactive power, the DC-link voltage values rise. For no reactive power required, DC-link capacitor voltages feature 300 V; for -25 kVAr, DC-link capacitor voltages feature 220 V, and to $+25$ kVAr, DC-link capacitor voltages feature 380 V, as shown in Figure 9.

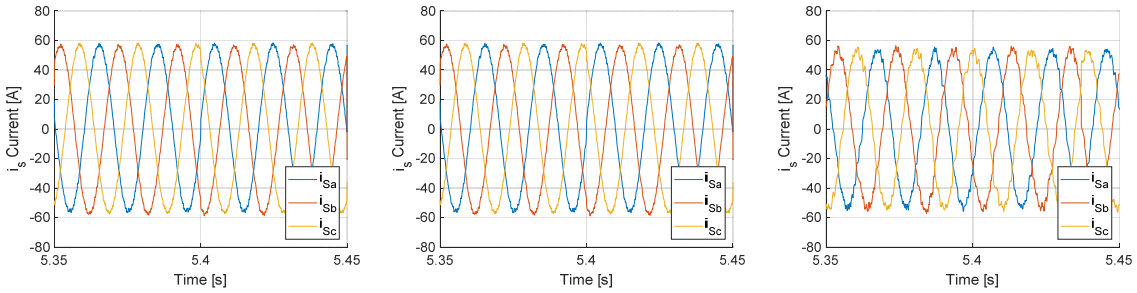
As designed, the DC-link ripple voltage of the CHB with 4000 μF individual capacitance, Figure 10a, and the CHB-SDC with 1200 μF individual capacitance, Figure 10c, present approximately 11 V. On the other hand, the DC-link ripple voltages of the CHB with 1200 μF individual capacitance, Figure 10b, presents approximately 45 V. These values demonstrate in this regard the superiority of the CHB-SDC over the CHB, presenting, as previously mentioned, three times fewer capacitors and 10 times less total capacitance required to obtain the same level of DC voltage ripple.



(**a**) (**b**) (**c**)

Figure 10. Capacitor DC-link voltages: (**a**) CHB (4000 μF); (**b**) CH (1200 μF); (**c**); CHB-SDC (1200 μF);.

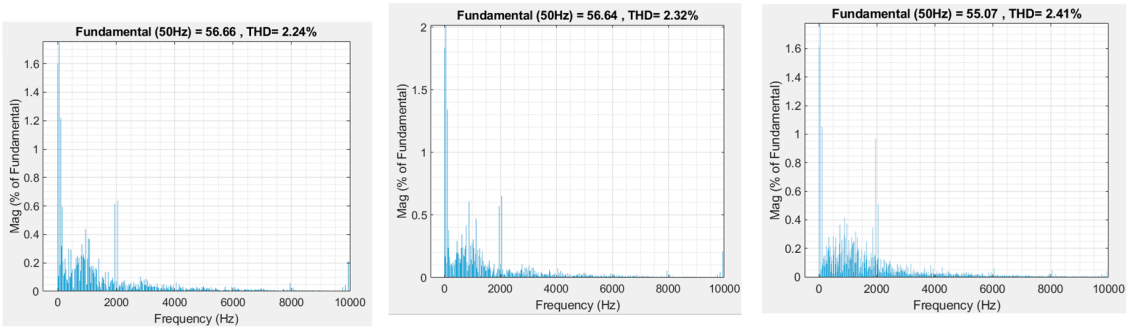
The STATCOM three-phase synthesized currents are shown in Figure 11 and do not exhibit significant harmonic distortions, presenting remarkable similarity among the converters and preserving its sinusoidal shape when power is required. We can observe that the CHB-SDC currents show high-frequency ripple higher than CHB currents due to the variable switching frequency, typical of OSV-MPC control since a PWM technique is not used. However, the difference between the THD of topologies is numerically insignificant.



(**a**) (**b**) (**c**)

Figure 11. Three-phase grid currents: (**a**) CHB $(4000\ \mu F)$; (**b**) CHB $(1200\ \mu F)$; (**c**) CHB-SDC $(1200\ \mu F)$.

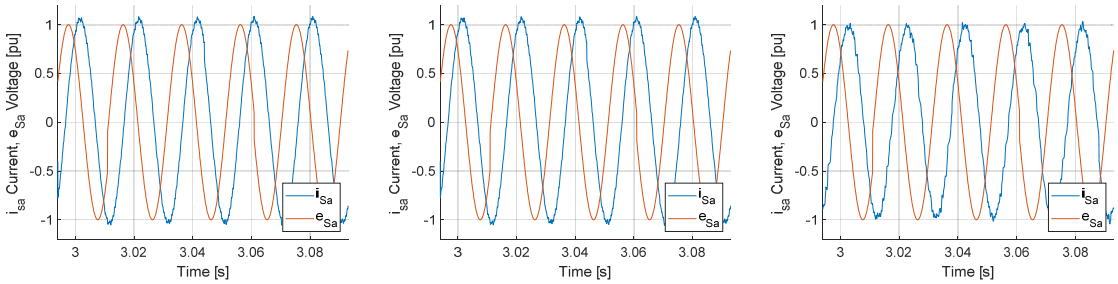
Figure 12 shows the converter's current harmonic spectrum in the inductive mode, presenting in both CHB implementations concentration close to the carrier frequency and, in the CHB-SDC close to 2 kHz. It is important to note the similarity between the frequency spectrum of the two topologies, even though the MPC does not have a fixed switching frequency.



(**a**) (**b**) (**c**)

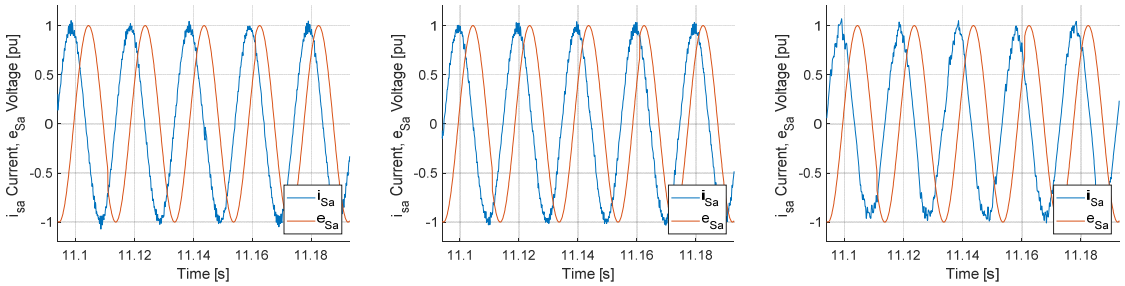
Figure 12. Grid current harmonic spectrum in inductive mode: (**a**) CHB (4000 μF); (**b**) CHB $(1200\ \mu F)$; (**c**) CHB-SDC $(1200\ \mu F)$.

When the STATCOM is in inductive mode, requiring reactive power, the synthesized current lags the grid voltage, while it is in capacitive mode, providing reactive power, the current leads the voltage. This behavior can be noted in Figures 13 and 14, where only the phase *a* voltage and current are presented. The THD values are shown in Table 3.



(**a**) (**b**) (**c**)

Figure 13. One phase grid current in inductive mode: (**a**) CHB $(4000\ \mu F)$; (**b**) CHB $(1200\ \mu F)$; (**c**) CHB-SDC $(1200\ \mu F)$.



(**a**) (**b**) (**c**)

Figure 14. One phase grid current in capacitive mode: (**a**) CHB $(4000\ \mu F)$; (**b**) CHB $(1200\ \mu F)$; (**c**) CHB-SDC $(1200\ \mu F)$.

Table 3. Comparison between the current total harmonic distortion of topologies.

Operation Mode	CHB Equal Ripple	CHB Equal Capacitors	CHB-SDC
inductive mode	2.24%	2.32%	2.41%
capacitive mode	4.08%	4.79%	4.98%

We can observe that, even with an extremely reduced capacitance when compared to the CHB topology and, having restrictions to several switching states, the CHB-SDC is able to provide a current waveform with little THD difference when compared with the CHB PSPWM, meeting the harmonic requirements and Electromagnetic compatibility [55,56].

Figure 15 shows the dynamics performance when the STATCOM reactive power shifts from inductive to capacitive mode, showing a continuous change in the current amplitude and angle concerning the grid voltage. This behavior corroborates with the perfect equipment functioning, showing in practice the possibility of operation in both situations. The MPC applied to the CHB-SDC shows agility when changing the load, presenting behavior similar to CHB using classic control, being represented in the synthesized currents.

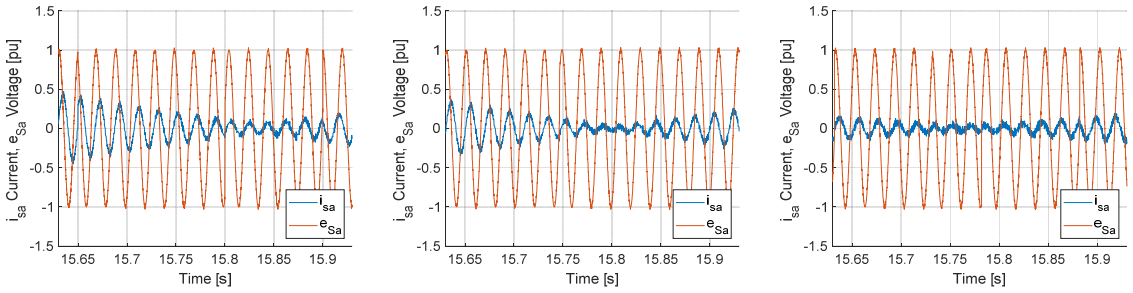


Figure 15. One phase grid current in changing mode: (**a**) CHB (4000 μF); (**b**) CHB (1200 μF); (**c**) CHB-SDC (1200 μF).

The three-phase voltage waveforms generated at the converter terminals (U_n), before the filters, are shown in Figure 16 and the synthesized output phase-voltages can be observed.

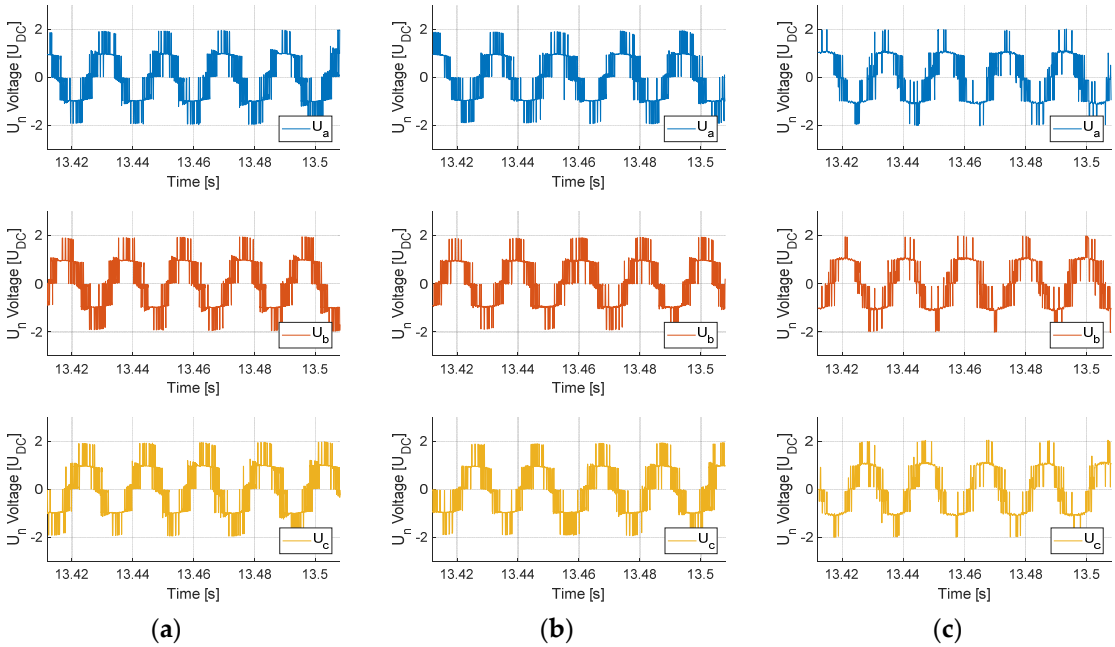


Figure 16. Three-phase synthesized STATCOM voltage: (**a**) CHB (4000 μF); (**b**) CHB (1200 μF); (**c**) CHB-SDC (1200 μF).

All the voltage waveforms have magnitude and frequency consistent with the desired specifications, with 120° lag among the phases as expected, and the differences resulting from each condition can be observed.

The outputs inherent to the classic CHB topology present the five voltage levels quite pronounced and well-defined, presenting better results the smaller the DC-link ripple is. Thus, for CHB with 1200 μF individual capacitance, the oscillations present in the DC-link are higher in the voltage waveforms than those observed in the CHB with 4000 μF individual capacitance.

From another perspective, the voltage waveforms produced by the CHB-SDC with OSV-MPC, present unusual waveform, with relatively fewer states in $\pm 2U_{DC}$ voltage levels.

Since the number of short-circuit states surpasses 80% of the possible states in this topology, the predictive control chooses, through intrinsic equations, the best switching sequence that will provide the best waveform to be synthesized most similarly to the desired one.

It is important to remember that the three-phase switching occurs simultaneously, once they share the same capacitor, the switching states of each one of them should be taken into account. For this specific five-level application, the values related to $\pm 2U_{DC}$ in each phase is the one that presents the smallest number of available possibilities.

However, it is worth mentioning that this peculiarity does not significantly affect the synthesized currents THD, presenting small variation among the harmonic distortion values for configurations that use CHBs with classic controls.

The voltage synthesized in each module is shown in Figure 17, presents more oscillation the smaller the DC-link ripple is and they are very pronounced in CHB with 1200 μF capacitors for the same reasons than previously explained in Figure 16, once that the sum of each module values produces the phase voltages.

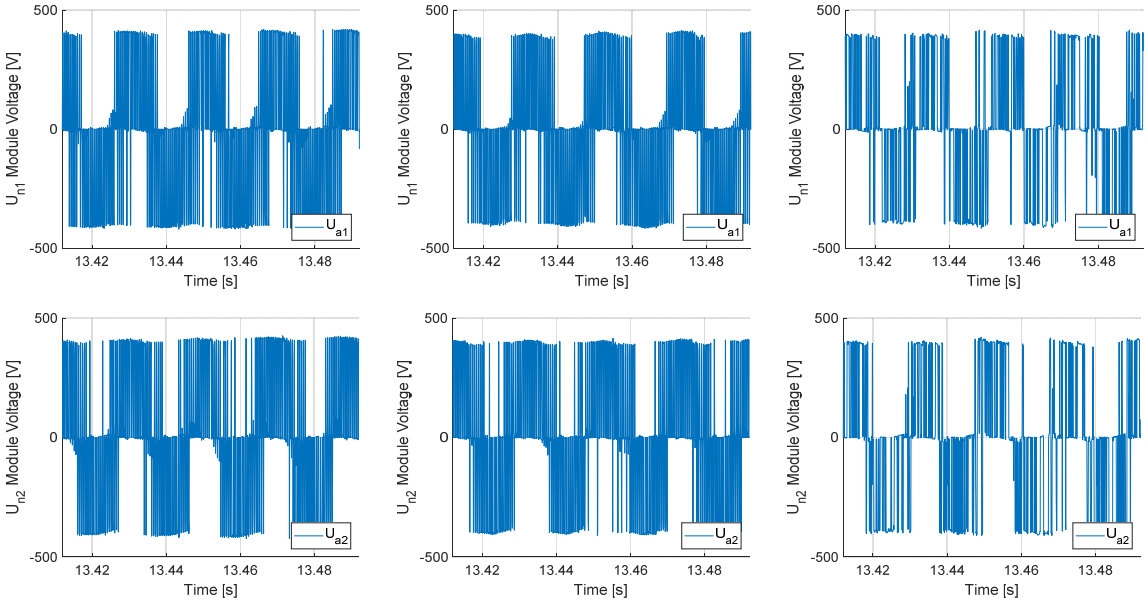


Figure 17. Synthesized STATCOM voltage per module: (**a**) CHB (4000 μF); (**b**) CHB (1200 μF); (**c**) CHB-SDC (1200 μF).

The CHB-SDC presents small oscillations and the switching pattern is less uniform than in CHB because the MPC control searches the best module voltage value taking into account the values of other phases. This phenomenon also has little influence on the current THD.

The results obtained experimentally demonstrate similar operation between the two compared topologies (CHB and CHB-SDC), mainly when they operate under the same power specifications and DC-link ripple. In such a situation, the CHB-SDC has 10 times less capacitance than the classic CHB.

Additionally, the proposed converter's three-phase structure, compared to the CHB's single-phase structure, drastically and naturally reduces the oscillations in the DC-links, providing quite ease control implementation via software.

This control, which in CHB, features 15 classic controllers and 6 signal filters to suit any application with five voltage levels, requires a clustered balancing control between the phases and individual balancing control between the two cascaded converters inside each cluster per phase. The tuning of all these gains becomes complex, spending a great deal of time. Furthermore, the individual balance control does not work when the reactive power reference is zero, imposing a practical limitation [51].

The CHB-SDC control does not even have an integral proportional controller, directly receiving voltage, current, and reference signals, and choosing the best switching state only via software,

presenting extremely fast responses to required power variations, being its adaptation simple and fast. The comparison between topologies is shown in Table 4.

Table 4. Comparison between five voltage levels topologies.

	CHB Same Ripple	CHB Same Capacitors	CHB-SDC
number of components	30	30	26
number of capacitors	6	6	2
individual capacitance	4000 μF	1200 μF	1200 μF
total capacitance	24,000 μF	7200 μF	2400 μF
structure	single-phase	single-phase	three-phase
2 ω ripple	yes	yes	no
amplitude ripple	11 V	46 V	11 V
low-pass filters	6	6	0
control elements	15	15	0
THD inductive mode	2.24%	2.32%	2.41%
THD capacitive mode	4.08%	4.79%	4.98%

The choice of the reactive power reference standards with variation in the capacitor DC-link voltages was intended to observe the CHB-SDC functioning using OSV-MPC during rapid variations of the reference signals and to analyze the ability to deal with the present transients in the systems, presenting a fast and adequate response as expected.

As the aim of the work is to present a new topology, show one of its applications and demonstrate the possibility of controlling it by switching strategies different from conventional PWM, complex fault detection strategies were not added to the MPC, being the generation of references produced through calculations from instantaneous power theory, and the use of a reduced time step, fast and effective enough to satisfy the objectives of this work. According to the literature, MPC-based controls are used to provide better responses than some controls of the active fault-tolerant controller (AFTC) and passive fault-tolerant controller (PFTC) type [18,57,58].

However, the structure of OSV-MPC, by not using control elements, allows the implementation of more elaborate failure detection controls (FTC), some of which are used in other branches of electronics, opening a vast field of studies related to these topics [59,60].

6. Conclusions

This article presents a new topology proposal for power converters, as a classical CHB upgrade with potential applications in a diverse range of equipment to be studied and developed, using a STATCOM as an application example.

CHB-SDC topology would not have been possible to implement a few decades ago due to the various short-circuit states inherent to the use of the known PWM switching strategies. However, as actual processors can perform various calculations in tiny time intervals, a model-based predictive control strategy could be used with a full scan to provide only safe switching states, mapped using an offline mathematical tool based on the graph theory.

The results obtained by the study and investigation of the proposed topology proved to be attractive and in accordance with the theory involved, presenting fast power variations and response, as well as the DC-link capacitor voltage control, being developed totally in the MPC platform.

In order to demonstrate the superiority of the CHB-SDC proposal with MPC over the CHB used nowadays, were proposed comparisons with two different configurations using classical control and, thus, obtaining undeniable CHB-SDC structural advantages.

The STATCOM experimental implementation on the HIL platform became necessary to prove the real execution of the CHB-SDC with the control and drive equipment available on the market. The results obtained using the OPAL-RT 5700 equipment present the perfect functioning of the CHB-SDC

as STATCOM, showing remarkably similar and consistent results with those generated by CHBs with classic control based on similar projects with same power and ripple on the capacitors DC-links.

The main advantages of the CHB-SDC topology over the CHB topology refer to the construction costs and the ease of controlling the parameters inherent to the project, since CHB-SDC presents 10 times less capacitance and three times fewer capacitor devices than same power and ripple CHB specifications. Due to its three-phase structure, the CHB-SDC also does not present 2ω oscillations in the capacitor voltages as observed in the classic CHB, which have single-phase structures.

Added to such features is the ease in the regulation of DC-link voltages due to its three-phase structure, being developed entirety via MPC with few code lines, against the 15 controllers necessary for the same control in the classic CHB topology, which makes it extremely difficult to tune the proportional and integral gains and the low-pass filters time constants.

Considering the structural analyzes and the results obtained experimentally, we can conclude that the CHB-SDC topology presents itself as a modern classic CHB upgrade, having lower cost and less complexity of construction and control, due to the use of powerful processors developed and popularized in the recent years, which provide operating with only 16% of the permitted states and obtain results compatible with topologies that operate with PWM switching.

Author Contributions: Conceptualization, R.S.C., E.J.B. and L.F.E.; Formal analysis, R.S.C.; Funding acquisition, E.J.B. and L.F.E.; Methodology, R.S.C., E.J.B. and L.F.E.; Project administration, E.J.B. and L.F.E.; Software, R.S.C.; Supervision, E.J.B. and L.F.E.; Validation, R.S.C., D.S.M. and A.M.M.; Visualization, R.S.C.; Writing—original draft, R.S.C.; Writing—review & editing, R.S.C., D.S.M., A.M.M., E.J.B. and L.F.E. All authors have read and agreed to the published version of the manuscript.

Funding: This research was funded by: Spanish Ministry of Science, Innovation and Universities under the INERCIA0 project with grant number RTI2018-098865-B-C3; Community of Madrid with grant number IND2018/IND-9493; Espírito Santo Research and Innovation Support Foundation—FAPES with grant number 536/2018 and Institutional Internationalization Program–CAPES PrInt.

Acknowledgments: Thanks to the Universidad de Alcalá for providing equipment, physical structure and support from professors and students; to the Federal University of Espírito Santo, for the logistical support and assistance from professors and staff; and to the Federal Institute of Espírito Santo, for allowing me to use my working hours to conduct research with other educational institutions.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Camargo, R.S.; Nunes, W.T.; Dallapicula, D.M.; Encarnacao, L.F.; Simonetti, D.S.L. Design and Analysis Methodology for Modular Multilevel Converters (MMC). *IEEE Lat. Am. Trans.* **2018**, *16*, 1105–1112. [CrossRef]
2. Zhang, G.; Li, Z.; Zhang, B.; Halang, A.W. Power Electronic Converters: Past, Present and Future. *Renew. Sustain. Energy Rev.* **2018**, *81*, 2028–2044. [CrossRef]
3. Acha, E.; Agelidis, V.; Anaya-Lara, O.; Miller, T.J.E. *Power Electronic Control in Electrical Systems*, 1st ed.; Newnes: Oxford, UK, 2002.
4. Peña-Alzola, R.; Roldán-Pérez, J.; Emilio, B.; Huerta, F.; Campos-Gaona, D.; Liserre, M.; Burt, G. Robust Active Damping in LCL-Filter-Based Medium-Voltage Parallel Grid Inverters for Wind Turbines. *IEEE Trans. Power Electron.* **2018**, *33*, 10846–10857. [CrossRef]
5. Feng, L.; Qunru, Z.; Qian, W. Research on reactive power compensation optimization design based on equivalent model of offshore wind farm. In Proceedings of the 2014 IEEE PES Asia-Pacific Power and Energy Engineering Conference (APPEEC), Hong Kong, China, 7–10 December 2014.
6. Zhang, W.; Zhang, X.; Liu, W.; Li, W. Modeling and simulation of aviation static inverter based on dymola and modelica. In Proceedings of the IEEE International Conference on Aircraft Utility Systems (AUS), Beijing, China, 10–12 October 2016.
7. Nunes, W.T.; Encarnação, L.F.; Aredes, M. An Improved Asymmetric Cascaded Multilevel D–STATCOM with Enhanced Hybrid Modulation. *Electronics* **2015**, *4*, 311–328. [CrossRef]
8. Freitas, W.; Morelato, A.; Xu, W.; Fujio, S. Impacts of AC Generators and DSTATCOM Devices on the Dynamic Performance of Distribution Systems. *IEEE Trans. Power Deliv.* **2005**, *20*, 1493–1501. [CrossRef]

9. Camargo, R.S.; Mayor, S.D.; Fernandes, L.D.M.; Miguel, A.M.; Bueno, E.J.; Encarnação, L.F. A Novel Cascaded Multilevel Converter Topology Based on Three-Phase Cells with Model Predictive Control. In Proceedings of the 29th IEEE International Symposium on Industrial Electronics, Delft, The Netherlands, 17–19 June 2020.
10. Maswood, I.; Tafti, H.D. *Advanced Multilevel Converters and Applications in Grid Integration*; Wiley: Hoboken, NJ, USA, 2019.
11. de Oliveira, V.R.; Renner, S.C.; Bueno, E.J.; Encarnação, L.F. Predictive Control on Multilevel Back-to-Back Cascade H-Bridge Driving an Induction Motor. In Proceedings of the 29th IEEE International Symposium on Industrial Electronics, Delft, The Netherlands, 17–19 June 2020.
12. Bifaretti, S.; Zanchetta, P.; Watson, A.; Tarisciotti, L.; Clare, J.C. Advanced power electronic conversion and control system for universal and flexible power management. *IEEE Trans. Smart Grid* **2011**, *2*, 231–243. [CrossRef]
13. Bhosale, S.S.; Bhosale, Y.N.; Chavan, U.M.; Malvekar, S.A. Power Quality Improvement by Using UPQC: A Review. In Proceedings of the 2018 International Conference on Control, Power, Communication and Computing Technologies (ICCPCCT), Kannur, India, 23–24 March 2018.
14. Ma, Y.; Huang, A.; Zhou, X. A Review of STATCOM on The Electric Power System. In Proceedings of the 2015 IEEE International Conference on Mechatronics and Automation (ICMA), Beijing, China, 2–5 August 2015.
15. Shinde, O.K.; Pulavarthi, V.B. STATCOM converters and control: A review. In Proceedings of the 2017 International Conference on Data Management, Analytics and Innovation (ICDMAI), Pune, India, 24–26 February 2017.
16. She, X.; Huang, A.Q. Solid State Transformer in the Future Electrical System. In Proceedings of the IEEE Power and Energy General Meeting (PES), Vancouver, BC, Canada, 21–25 July 2013.
17. Oliveira, F.S.; Encarnação, L.F.; Camargo, R.S.; Bueno, E.J. Multilevel Back-to-Back Cascaded H-Bridge Converter with Model Predictive Control. In Proceedings of the IECON 2019—45th Annual Conference of the IEEE Industrial Electronics Society, Lisbon, Portugal, 14–17 October2019.
18. Wang, L.; Truong, D.-N. Stability Enhancement of DFIG-Based Offshore Wind Farm Fed to a Multi-Machine System Using a STATCOM. *IEEE Trans. Power Syst.* **2013**, *28*, 2882–2889. [CrossRef]
19. Nabae, A.; Takahashi, I.; Akagi, H. A New Neutral-Point Clamped PWM Inverter. *IEEE Trans. Ind. Appl.* **1981**, *IA-17*, 518–523. [CrossRef]
20. Meynard, T.A.; Fadel, M.; Aouda, N. Modeling of Multilevel Converters. *IEEE Trans. Semiconduct. Ind. Electron.* **1997**, *44*, 356–364. [CrossRef]
21. Leniscar, A.; Marquard, R. An Innovative Modular Multilevel Converter Topology Suitable for a Wide Power Range. In Proceedings of the IEEE Bologna PowerTech Conference, Bologna, Italy, 23–26 June 2003.
22. Akagi, H. Classification, Terminology, and Application of the Modular Multilevel Cascade Converter (MMCC). *IEEE Trans. Power Electron.* **2011**, *26*, 3119–3130. [CrossRef]
23. Rodriguez, J.-S.; Lai, F.; Zheng, P. Multilevel inverters: A survey of topologies, controls, and applications. *IEEE Trans. Ind. Electron.* **2002**, *49*, 724–738. [CrossRef]
24. Wang, C.; Li, Y. A Survey on Topologies of Multilevel Converters and Study of Two Novel Topologies. In Proceedings of the 2009 IEEE 6th International Power Electronics and Motion Control Conference, Wuhan, China, 17–20 May 2009.
25. Khomfoi, S.; Tolbert, L.M. Chapter 17 Multilevel Power Converter. In *Power Electronics Handbook, Devices, Circuits and Applications*; Elsevier: Amsterdam, The Netherlands, 2005.
26. Bum-Seok, S.; Sinha, G.; Manjrekar, M.D.; Lipo, T.A. Multilevel Power Conversion—An Overview of Topologies and Modulation Strategies. In Proceedings of the 6th International Conference on Optimization of Electrical and Electronic Equipment, Brasov, Romania, 14–15 May 1998; Volume 2.
27. Miranbeigi, M.; Iman-Eini, H.; Asoodar, M. A new switching strategy for transformer-less back-to-back cascaded H-bridge multilevel converter. *IET Power Electron.* **2014**, *7*, 1868–1877. [CrossRef]
28. Davari, P.; Zare, F.; Abdelhakim, A. Active Rectifiers and Their Control. In *Control of Power Electronic Converters and Systems*; Elsevier: London, UK, 2018; Volume 2.
29. Gu, L.; Ruan, X.; Xu, M.; Yao, K. Means of Eliminating Electrolytic Capacitor in AC/DC Power Supplies for LED Lightings. *IEEE Trans. Power Electron.* **2009**, *24*, 1399–1408. [CrossRef]
30. Kjaer, S.B.; Pedersen, J.K.; Blaabjerg, F. A Review of Single-Phase Grid-Connected Inverters for Photovoltaic Modules. *IEEE Trans. Ind. Appl.* **2005**, *41*, 1292–1306. [CrossRef]

31. Kashihara, Y.; Itoh, J.-I. The performance of the multilevel converter topologies for PV inverter. In Proceedings of the 2012 7th International Conference on Integrated Power Electronics Systems (CIPS), Nuremberg, Germany, 6–8 March 2012.
32. Krein, P.T.; Balog, R.S.; Mirjafari, M. Minimum Energy and Capacitance Requirements for Single-Phase Inverters and Rectifiers Using a Ripple Port. *IEEE Trans. Power Electron.* **2012**, *27*, 4690–4698. [CrossRef]
33. Merlin, M.M.C.; Green, T.C.; Mitcheson, P.D.; Moreno, F.J.; Dyke, K.J.; Trainer, D.R. Cell capacitor sizing in modular multilevel converters and hybrid topologies. In Proceedings of the 2014 16th European Conference on Power Electronics and Applications, Lappeenranta, Finland, 26–28 August 2014.
34. Najmi, V.; Wang, J.; Burgos, R.; Boroyevich, D. Reliability modeling of capacitor bank for Modular Multilevel Converter based on Markov State-Space Model. In Proceedings of the 2015 IEEE Applied Power Electronics Conference and Exposition (APEC), Charlotte, NC, USA, 15–19 March 2015.
35. Barbi, I. *Eletrônica de Potência*; UFSC: Santa Catarina, Brazil, 2002.
36. Mechouma, R.; Azoui, B.; Chaabane, M. Three-Phase Grid Connected Inverter for Photovoltaic Systems, a Review. In Proceedings of the 2012 First International Conference on Renewable Energies and Vehicular Technology, Hammamet, Tunisia, 26–28 March 2012.
37. Alfonso-Gil, J.C.; Gimeno-Sales, F.; Segui-Chilet, S.; Orts, S.; Calvo, J.; Fuster, V. New optimization in photovoltaic installations with energy balance with the three-phase utility. In Proceedings of the IEEE International Symposium on Industrial Electronics, ISIE 2005, Dubrovnik, Croatia, 20–23 June2005.
38. de Iiveira, V.M.R.; Camargo, R.S.; Encarnação, L.F.; Bueno, E.J. Field Oriented Predictive Current Control on NPC Driving an Induction Motor. In Proceedings of the 2020 IEEE International Conference on Industrial Technology (ICIT), Buenos Aires, Argentina, 26–28 February 2020.
39. Oliveira, F.S.; Encarnação, L.F.; Camargo, R.S.; Bueno, E. Model Predictive Control on Back-to-Back Parallel-Series Cascaded H-Bridge Converters. In Proceedings of the 2019 IEEE PES Innovative Smart Grid Technologies Europe (ISGT-Europe), Bucharest, Romania, 29 September–2 October 2019.
40. Rodriguez, P.; Teodorescu, R.; Candela, I.; Liserre, M.; Blaabjerg, F. New positive-sequence voltage detector for grid synchronization of power converters under faulty grid conditions. In Proceedings of the 2006 37th IEEE Power Electronics Specialists Conference, Jeju, Korea, 18–22 June 2006.
41. Kouro, S.; Cortes, P.; Vargas, R.; Ammann, U.; Rodriguez, J. Model predictive control: A simple and powerful method to control power converters. *IEEE Trans. Ind. Electron.* **2009**, *56*, 1826–1838. [CrossRef]
42. Rodriguez, J.; Pont, J.; Correa, P.; Lezana, P.; Cortes, P. Predictive Power Control of an AC/DC/AC. em Fourtieth IAS Annual Meeting. In Proceedings of the Conference Record of the 2005 Industry Applications Conference, Kowloon, Hong Kong, China, 2–6 October2005.
43. Vazquez, S.; Rodriguez, J.; Rivera, M. Model Predictive Control for Power Converters and Drives: Advances and Trends. *IEEE Trans. Ind. Electron.* **2017**, *64*, 935–947. [CrossRef]
44. Rodriguez, J.V.; Bueno, E.J.; Larrea, P.L.; Duarte, H.A.; Rodriguez, A. Dynamic performance of a STATCOM under grid disturbances for two different linear controllers. In Proceedings of the IECON 2012—38th Annual Conference on IEEE Industrial Electronics Society, Montreal, QC, Canada, 25–28 October 2012.
45. Tarisciotti, L.; Burgos, C.; Garcia, C.; Rodriguez, J. Finite Control Set Model Predictive Control of parallel three-phase active rectifiers. In Proceedings of the 2020 IEEE International Conference on Industrial Technology (ICIT), Buenos Aires, Argentina, 26–28 February 2020.
46. Tarisciotti, L.; Formentini, A.; Gaeta, A.; Degano, M.; Zanchetta, P.; Rabbeni, R.; Pucci, M. Model Predictive control for Shunt Active Filters with Fixed Switching Frequency. *IEEE Trans. Ind. Appl.* **2016**, *5*, 296–304. [CrossRef]
47. Tarisciotti, L.; Zanchetta, P.; Watson, A.; Bifaretti, S.; Clare, J.C. Modulated Model Predictive Control for a Seven-Level Cascaded H-Bridge Back-to-Back Converter. *IEEE Trans. Ind. Electron.* **2014**, *61*, 5375–5383. [CrossRef]
48. Tianqi, L.; Youyin, W.; Zhanjun, L.; Meijun, L.; Weimao, X.; Yunche, S.; Zhijian, C.; Na, Z. Reactive Power Compensation and Control Strategy for MMC-STATCOM Doubly-Fed Wind Farm. In Proceedings of the 2019 IEEE Innovative Smart Grid Technologies—Asia (ISGT Asia), Chengdu, China, 21–24 May 2019.
49. Roldán-Pérez, J.; Ávila-Martínez, R.; Rodríguez-Cabero, A.; Prodanovic, M.; Bueno, E. LTCL-Filter Active-Damping Design Considerations for Low-Switching-Frequency Grid-Tied VSCs. In Proceedings of the IECON 2018—44th Annual Conference of the IEEE Industrial Electronics Society, Washington, DC, USA, 21–23 October 2018.

50. Xiao, Y.; Wang, Y. Reactive Power Optimal Control of aWind Farm for Minimizing Collector System Losses. *Energies* **2018**, *11*, 3177. [CrossRef]
51. Akagi, H.; Watanabe, E.H.; Aredes, M. *Instantaneous Power Theory and Applications to Power Conditions*; John Wiley and Sons Inc.: Hoboken, NJ, USA, 2007.
52. Akagi, H.; Inoue, S.; Yoshii, T. Control and Performance of a Transformerless Cascade PWM STATCOM with Star Configuration. *IEEE Trans. Ind. Appl.* **2007**, *43*, 1041–1049. [CrossRef]
53. Wu, C.-H.; Xu, Y.-X. The Optimal Control of Fuel Consumption for a Heavy-Duty Motorcycle with Three Power Sources Using Hardware-in-the-Loop Simulation. *Energies* **2020**, *13*, 22. [CrossRef]
54. Sanchez, P.M.; Machado, O.; Bueno, E.; Rodriguez, F.J.; Meca, F.J. FPGA-Based Implementation of a Predictive Current Controller for Power Converters. *IEEE Trans. Ind. Inform.* **2012**, *9*, 1312–1321. [CrossRef]
55. *IEEE Std 519. IEEE Recommended Practice and Requirements for Harmonic Control in Electric Power Systems*; IEEE Standard Association: Piscataway, NJ, USA, 2014.
56. *IEC 61000-4-7:2002/AMD1:2008. International Standard—Electromagnetic Compatibility (EMC)—Part 4–7: Testing and Measurement Techniques*; International Electrotechnical Commission: Geneva, Switzerland, 2008.
57. Saha, C.; Singh, A.K. A Review Article on Fault-Tolerant Control (FTC) and Fault Detection Isolation (FDI) Schemes of Wind Turbine. In Proceedings of the Second International Conference on Microelectronics, Computing & Communication Systems (MCCS 2017), Jharkhand, India, 13–14 May 2017.
58. Yang, X.; Maciejowski, J. Fault-tolerant model predictive control of a wind turbine benchmark. In Proceedings of the 8th IFAC Symposium on Fault Detection, Mexico City, Mexico, 8–11 June 2012.
59. Ju, Z.; Zhang, H.; Tan, Y. Distributed Deception Attack Detection in Platoon-Based Connected Vehicle Systems. *IEEE Trans. Veh. Technol.* **2020**, *69*, 4609–4620. [CrossRef]
60. Zhang, H.; Wang, J. Active Steering Actuator Fault Detection for an Automatically-steered Electric Ground Vehicle. *IEEE Trans. Veh. Technol.* **2017**, *66*, 3685–3702. [CrossRef]