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The Enhanced Average Model of the Smart Transformer with the Wye-Delta Connection of Dual Active Bridges

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Abstract: Nowadays, many power electronics converters (PECs) are connected to the distribution grid, increasing the energy quality requirements in point of common coupling (PCC). One of the promising solutions to improve the energy quality is a smart transformer (ST) characterised by additional benefits in relation to the classical transformer throughout the possibility to implement advanced functionalities in PCC. However, the ST contains a lot of power semiconductor switches, making a problem for simulation software and the computer hardware when the control algorithm and all the ST functionalities are investigated. Usually, the solver algorithms in simulation software are used to create many linear time-varying states spaces, which increases exponentially with the number of switches. Therefore, very important is a model averaging process of the selected advanced ST topology, which is the aim of the paper. The proposed ST average model is compared with full switching models of each ST power conversion stage. It allows for decreasing the simulation time a dozen times, enabling the control algorithm analysis with a full ST model. The proposed solution and results prove steady-state and dynamic behaviour of the average model and provide a comprehensive averaging process for a novel multiple active bridge direct current/direct current (DC/DC) converter inside the ST.

Keywords: smart transformer; solid-state transformer; average model

1. Introduction

The transformer is one of the most important devices in transmission and distribution grids. Thanks to the dynamic development of a novel semiconductor devices, communication and control systems, as well as intelligent and self-controlled microgrids (smartgrids), a new solution of the transformer has been developed. In the beginning, the idea of Solid-State Transformer (SST) has been presented in [1–3]. The main concept of SST is shown in Figure 1. It consists of alternating current-medium voltage/direct current-medium voltage (AC-MV/DC-MV), isolated direct current-medium voltage/direct current-low voltage (DC-MV/DC-LV) and direct current-low voltage/alternating current-low voltage (DC-LV/AC-LV) power electronics converters. It is characterised by several advantages, like high power density, high efficiency, better power quality and control ability [3,4]. In the era of dynamic growth of semiconductor power switches and microcontrollers, the SST has begun more and more advanced and possible to use in the real power system. Taking into consideration many different control solutions for the power electronics converters and communication abilities, the SST idea has evolved into the Smart Transformer (ST).

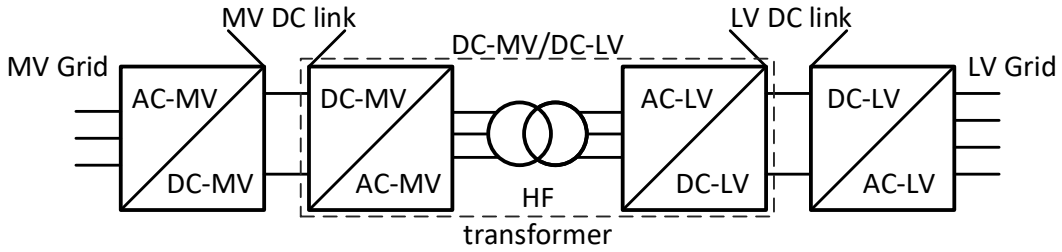

Figure 1. The block scheme of the Solid-State Transformer consisting of different power conversion stages.

The ST is characterised by many additional functionalities in relation to the classical transformer (CT), which is not able to support the grid without any auxiliary devices, for example, current harmonics compensation, reactive power compensations, currents symmetrisation [3,5]. The structure of ST can be different, depending on needs and application [6–8]. One of the ST classifications is based on the available DC-links with different voltage levels (MV, LV), providing a point of common coupling for auxiliary DC loads, renewable energy sources and the local DC microgrids. Each power conversion stage consists of different power electronics converter's structures depending on the application (single H-bridges, modular multilevel converters, cascaded converters, T-type converters, etc.). The most advanced topologies include dozens of semiconductor switches or even more than a hundred elements for high power applications. Additionally, a crucial part of the ST is a high-frequency (HF) transformer. Depending on the application and power electronics converters included in the ST, the significantly different HF transformers are designed and used [2,6,9]. Such an advanced power electronics device is a challenge in simulation research, caused by many switching elements, making the simulated circuit strongly non-linear. The simulation software (e.g., PLECS) creates a linear time-varying (LTV) state space associated with all signals in the model in Equation (1).

$$\begin{aligned} \dot{x} &= A_\sigma x + B_\sigma u \\ y &= C_\sigma x + D_\sigma u \end{aligned} \tag{1}$$

The index σ means that the software creates a set of state-space matrices for each possible state change of switching elements (Appendix A). Therefore, the circuit is represented by numbers of linear time-invariant (LTI) models. Furthermore, an additional observer makes decisions whether changing the LTI state space is necessary. It allows obtaining the linear and time-invariant model for each switch state permutation. Moreover, it efficiently determines the output vector y. However, on the other hand, that method makes many state-space permutations equal to two to the power of n, where n is the total number of switching elements. That means the number of modes grows exponentially with the numbers of switches in the circuit, which requires a lot of memory, computing power and time.

To conduct an efficient analysis of the advanced power electronics devices, such as the ST, a good practice is the design of an average signal model for the analysed circuit [4,10,11]. It is characterised by the controlled voltage and current sources, which replaces all switching elements. As a result, the simulation can be performed for dozens of power electronics converters, taking into consideration a complex control algorithm and significantly decreasing the simulation time in comparison to the full switching model. The average model design technics are well known in the literature for single power electronic converters included in all ST power stages (AC/DC, DC/DC, DC/AC) [4,10–15]. The simple ST average model has also been proposed in the literature, where the DC/DC dual-active bridge (DAB) converter has been replaced by controlled sources and AC/DC and DC/AC converters have been replaced by ideal transformer models [4,12]. That solution focuses mainly on the analysis of the DAB control algorithms, which is the most important part of the ST due to the included HF transformer.

In this paper, a more advanced average model of the ST is proposed, taking into consideration all dynamic behaviours of the real devices, neglecting only switching frequency influences on the measured

voltage and currents. The ST is composed of more than a hundred transistors and diodes (Figure 2). The average models of AC-MV/DC-MV side and DC-LV/AC-LV side power electronics converters are investigated and described in Section 2. The crucial part of the ST, the isolated DC-MV/DC-LV converter average model with wye-delta HF transformer, has been proposed as well. In Section 3, the implemented basic control algorithms have been presented (without advanced functionalities of ST) and the simulation results have been shown and compared with the full switching model of each ST power stage as well as the whole device. In the end, the discussion has been included in Section 4.

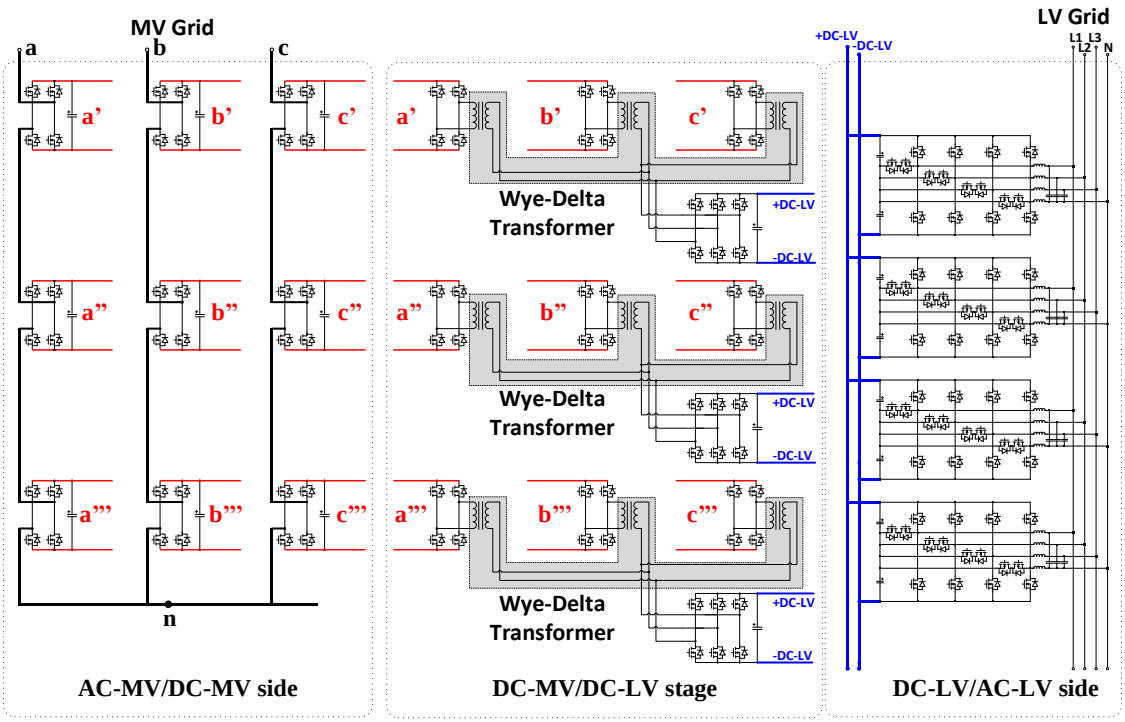

Figure 2. The full model of the considered Smart Transformer (ST) with wye-delta high-frequency (HF) transformers and LV DC link as a point of common coupling for DC systems-model separated for different power stages.

2. Average Model of the ST

Each topology of the ST can be split into power conversion stages, which usually are defined by different voltage levels and types (AC, DC). Based on the knowledge of the average models of single power electronics converters, the whole ST average structure may be composed of average models of every single converter.

2.1. Model of the AC-MV/DC-MV Side of ST

The considered model of the AC-MV/DC-MV side of ST is a cascaded H-bridge converter (CHBC) composed of nine modules, as it is presented in Figure 1. Due to wye-delta connected dual active bridges in the next conversion stage of the ST, there is no possibility to replace the whole CHBC phase leg by the average model, because all nine DC-links are used (Figure 2). Therefore, each of the H-bridge must be averaging. The single module including four transistors and diodes is replaced by a controlled voltage source (CVS) from the AC converter side and a controlled current source (CCS) from the DC side (Figure 3) [16–18]. Taking into consideration the pulse width modulation technique (PWM) in each switching cycle, the voltage v_{AC} is equal to:

$$v_{AC} = D \times v_{DC} \tag{2}$$

where D—is a modulation index from a range <−1, 1>. This relation determines the control signal directly for the CVS in the average model. The converter DC-side represented by the CCS is derived using the principle of power balance. Assuming, that all the losses in the averaged H-bridge model are not relevant to the control algorithm and may be omitted, the power on the DC side p_{DC} is equal to the power on the AC side p_{AC}:

$$p_{AC} = v_{AC} i_{AC} = v_{DC} i_{DC} = p_{DC} \tag{3}$$

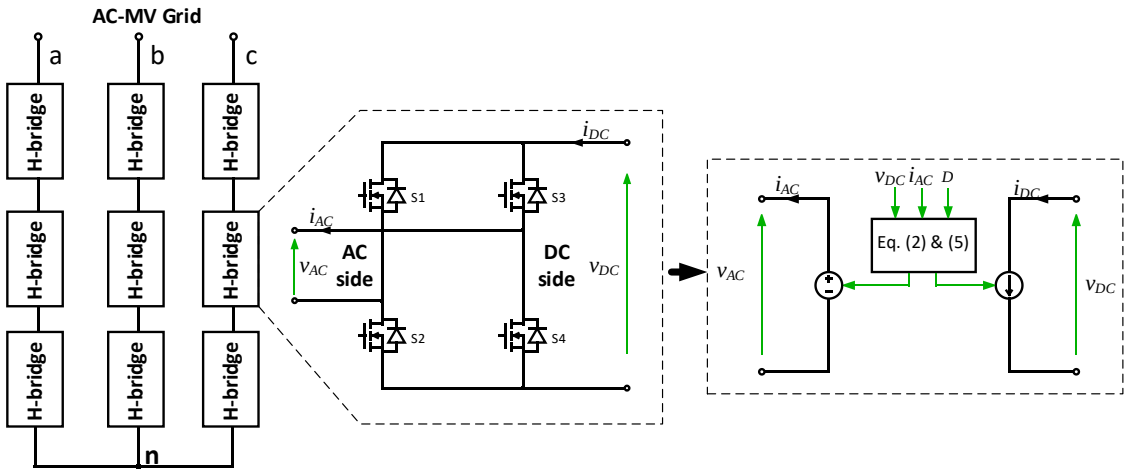

Figure 3. The scheme of the cascaded H-bridge converter used in the ST—full switching and average models of the single module.

Using that relation, the referenced current value for CCS is obtained, as:

$$i_{DC} = \frac{v_{AC} i_{AC}}{v_{DC}} \tag{4}$$

From (2) and (4), the current of CCS is equal:

$$i_{DC} = D \times i_{AC} \tag{5}$$

2.2. Model of the Isolated DC-DC Converter with Wye-Delta Transformer

The isolated DC-DC converter based on a dual-active bridge (DAB) is a common solution for bi-directional energy transfer between different DC systems (e.g., energy storage, isolated photovoltaic (PV) systems) [17,19]. The scheme of DAB is shown in Figure 4a. In past years, the DAB topologies have been deeply developed. The basic topology of two H-bridges connected through a one-phase high-frequency transformer has been reorganised with multilevel converters [9,17,20], a resonant circuit for soft-switching ability [21], and multiple active bridge (MAB) converters with wye-wye, delta-delta or wye-delta transformers [9]. The advanced MAB topologies allow operating with higher voltage levels and transformer ratios, a higher efficiency, a higher power of the converter and post-fault mode. Moreover, the MAB advantages are characterised by lower transistor currents, higher phase-shift control ability, lower current ripples in the DC-links and thanks to the wye-delta high-frequency transformer it can operate with unbalanced loads [9].

The modelled ST topology includes three MAB converters (Figure 2), described in [9]. It simplifies the construction of the ST and improves the maintenance due to power electronics building blocks construction (PEBB). MAB can easily work in a post-fault mode of operation, allowing to replace the damaged module. The high-frequency (HF) transformers second windings inside the MAB are connected to the three-phase converter, reducing the current ripples and voltage fluctuations in the DC-link. In developing the average model of that topology, besides the DAB structure, the implemented

control solution must be considered. The most common option is a phase shift control, with the constant switching frequency and 50% duty cycle of the rectangular pulses [13,19]. Neglecting the losses of the converter and the HF transformer, the power of the single DAB converter controlled by the phase-shift ϕ is equal to:

$$P = \frac{v_{DC\_High} v_{DC\_Low}}{2mf_s L_{eq}\pi}\phi\,(\pi - \phi) \tag{6}$$

where ϕ—phase shift between high frequency voltages v_{AC_High} and v_{AC_Low} (Figure 4a), f_s—switching frequency, L_{eq}—equivalent leakage inductance referred to the transformer primary side (Figure 4b).

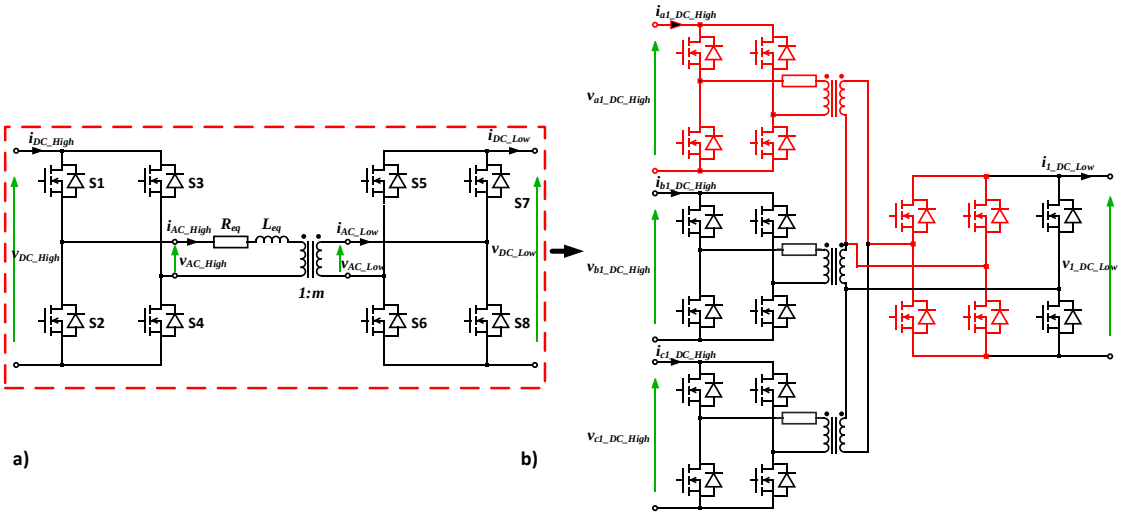

Figure 4. The scheme of the switching model of the proposed single three-phase isolated dual active bridge (DAB), (**a**) the model of the single DAB, (**b**) the model of the implemented multiple active bridge (MAB) structure.

Two common methods of DAB converter averaging have been taken into consideration to implement them in the proposed DC-DC converter topology. One uses the first harmonic approximation (FHA) [13]. Its main assumption is to use only the first harmonic of two rectangular signals and then adequately rescale the amplitudes of them to obtain the same power flow as for a given phase shift. This approach is characterised by easy implementation and shortens time of simulation, but its disadvantage is a difference in detailed and average model dynamics and the necessity of the additional amplitude value correction for the first harmonic signals to receive the same power flow as for the phase shift control.

Therefore, a more precise solution has been used and described. It is based on the DAB averaging with included values of the high-frequency transformer winding resistances R_p, R_s and leakage inductances L_p, L_s as well as the transistor's conduction resistance R_c [22]. The equivalent leakage inductance L_{eq} referred to the primary side of the transformer can be calculated as:

$$L_{eq} = L_p + \frac{L_s}{m^2} \tag{7}$$

where L_p—inductance of primary winding, L_s—inductance of secondary winding, m—transformer turn ratio.

The equivalent resistance R_{eq} is equal to:

$$R_{eq} = R_p + 2R_c + \frac{R_s + 2R_c}{m^2} \tag{8}$$

where R_p—resistance of primary winding, R_s—resistance of the secondary winding, R_c—the conduction resistance of the transistor.

The average model of the considered isolated DC-DC converter is possible to realise with two current sources as a building block of the whole structure (Figure 5). Knowing the measured values of both DC links voltages and equivalent impedance of the DAB's internal circuit, the average currents i_{DC_High} and i_{DC_Low} can be calculated as [22]:

$$i_{DC_{High}} = \frac{\left(v_{DC_{High}} + v'_{DC_{Low}}\right)dT + \left(v_{DC_{High}} - v'_{DC_{Low}}\right)(1-d)T}{TR_{eq}} + \frac{L_{eq}\left(i_{peak1} + \frac{v_{DC_{High}} + v'_{DC_{Low}}}{R_{eq}}\right)\left(e^{-\frac{R_{eq}}{L_{eq}}dT} - 1\right)}{TR_{eq}} + \frac{L_{eq}\left(\frac{v_{DC\_High} - v'_{DC\_Low}}{R_{eq}} - i_{peak2}\right)\left(e^{-\frac{R_{eq}}{L_{eq}}(1-d)T} - 1\right)}{TR_{eq}} \quad (9)$$

$$i_{DC_{Low}} = \frac{-\left(v_{DC_{High}} + v'_{DC_{Low}}\right)dT + \left(v_{DC_{High}} - v'_{DC_{Low}}\right)(1-d)T}{mTR_{eq}} - \frac{L_{eq}\left(i_{peak1} + \frac{v_{DC_{High}} + v'_{DC_{Low}}}{R_{eq}}\right)\left(e^{-\frac{R_{eq}}{L_{eq}}dT} - 1\right)}{mTR_{eq}} + \frac{L_{eq}\left(\frac{v_{DC\_High} - v'_{DC\_Low}}{R_{eq}} - i_{peak2}\right)\left(e^{-\frac{R_{eq}}{L_{eq}}(1-d)T} - 1\right)}{mTR_{eq}} \quad (10)$$

where T—HF transformer current period presented in Figure 6 (half of a switching period T_s), d—phase shift ratio:

$$d = \frac{\phi}{\pi} \quad (11)$$

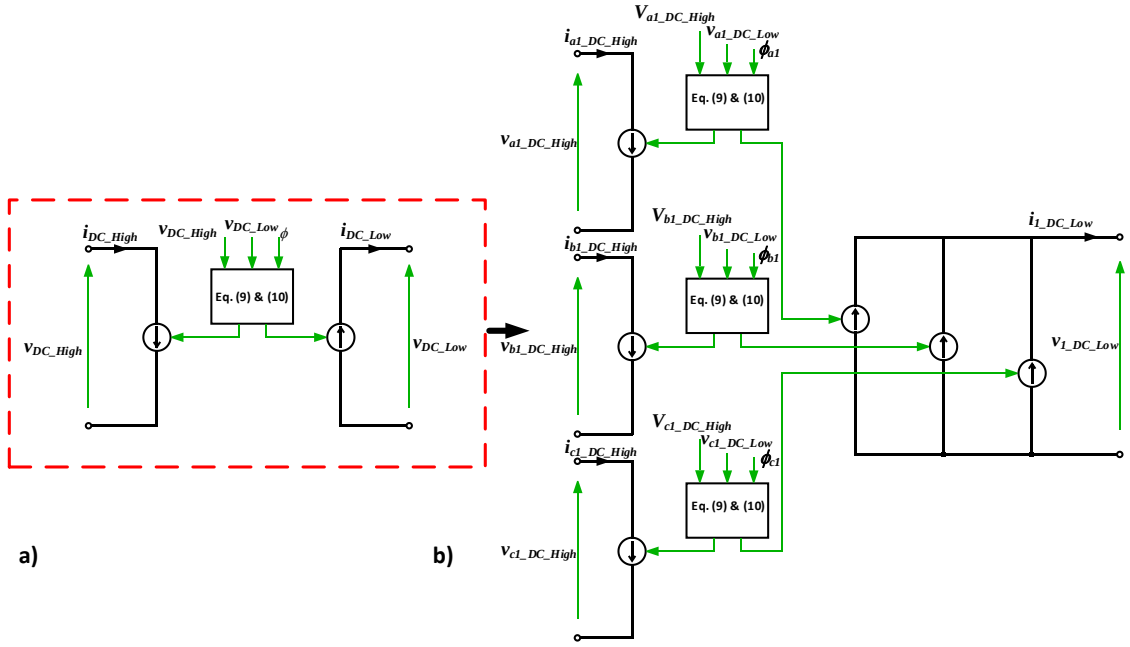

Figure 5. The proposed average model of the MAB, (**a**) average model of the single DAB, (**b**) average model of the full three-phase MAB.

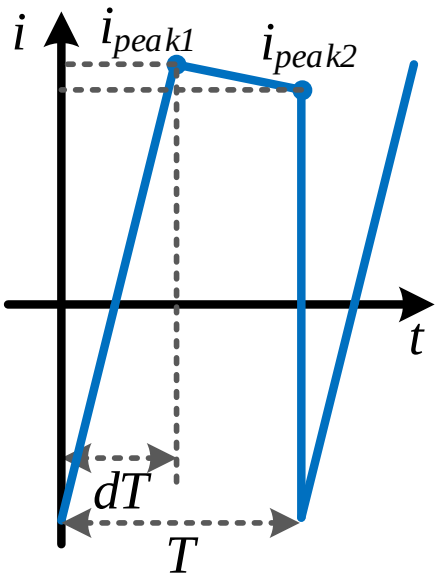

Figure 6. The waveform of the HF transformer current, when the phase-shift control is applied.

v'_{DC_Low}—is a secondary winding voltage referred to the primary side:

$$v'_{DC\_Low} = \frac{v_{DC\_Low}}{m} \tag{12}$$

In the reference currents calculation process, two HF transformer current parameters are needed. First, the value of current peak i_{peak_1} and the value of current peak i_{peak_2} when the current pulse is ending, both presented in Figure 6. Those values are equal to:

$$i_{peak\_1} = \frac{v_{DC\_High} - v'_{DC\_Low} + 2v'_{DC\_Low}e^{-\frac{R_{eq}}{L_{eq}}(1-d)T}}{R_{eq}\left(1+e^{-\frac{R_{eq}}{L_{eq}}T}\right)} - \frac{\left(v_{DC\_High} + v'_{DC\_Low}\right)e^{-\frac{R_{eq}}{L_{eq}}T}}{R_{eq}\left(1+e^{-\frac{R_{eq}}{L_{eq}}T}\right)} \tag{13}$$

$$i_{peak\_2} = \frac{v_{DC\_High} + v'_{DC\_Low} - 2v_{DC\_High}e^{-\frac{R_{eq}}{L_{eq}}dT}}{R_{eq}\left(1+e^{-\frac{R_{eq}}{L_{eq}}T}\right)} + \frac{\left(v_{DC\_High} - v'_{DC\_Low}\right)e^{-\frac{R_{eq}}{L_{eq}}T}}{R_{eq}\left(1+e^{-\frac{R_{eq}}{L_{eq}}T}\right)} \tag{14}$$

Using the described model of the single DAB, the MAB DC-DC converter can be modelled based on the scheme presented in Figure 4b. Using three models of that converter, the whole isolated DC-DC stage of the ST shown in Figure 1 is averaged.

2.3. Model of the DC-LV/AC-LV Side of ST

The considered DC-LV/AC-LV stage of the ST consists of four power electronics converter modules connected in parallel as it is shown in Figure 7, providing redundancy and post-fault operation in the device [9]. Each module is composed of a four-leg T-type converter (Figure 7b), characterised by the divided DC-link to obtain the third level of the output voltage (concerning a classical two-level converter). At the converter output, the common inductive-capacitive (LC) filter is implemented.

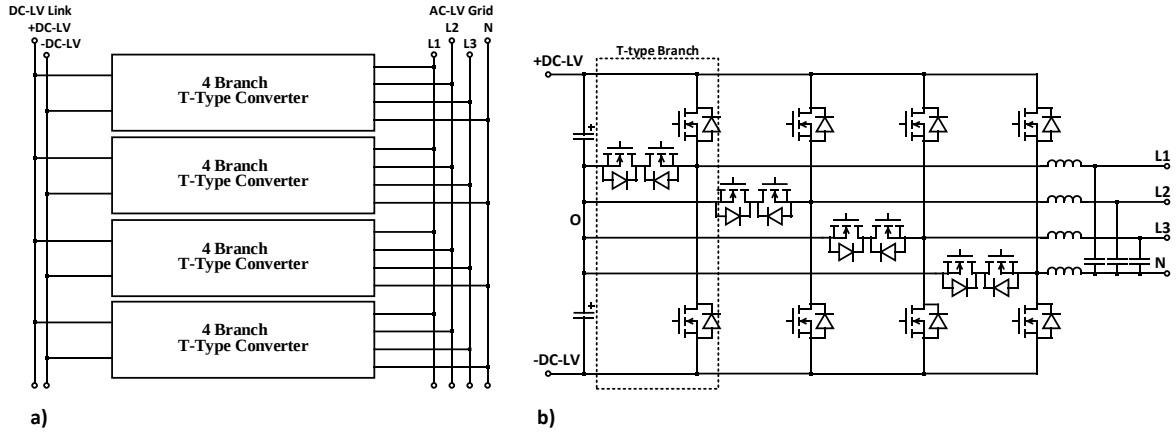

Figure 7. Considered DC-AC converter in the ST structure, composed of four T-type four-leg solutions, (**a**) the block scheme of the four T-type four-leg connection, (**b**) the model of the single T-type four-leg converter.

The averaging procedure of the DC-LV/AC-LV stage of the ST is very similar to the described star-connected CHB converter. The first step is defining a basic module from which it is possible to create the whole considered topology. The main requirement that the average model should meet is the ability to test the complete control algorithm. The common control strategy returns four signals as the modulation index D for one module. Each of the signals determines the average value of the branch voltage v_{AC} between terminals O (the middle point of DC-link) and the phase of each T-Type branch for the switching period T_s, formulated as [14,23,24]:

$$\begin{cases} v_{AC} = D \times v_{DC\_Low\_1}, \ for\ D \geq 0 \\ v_{AC} = D \times v_{DC\_low\_2}, \ for\ D < 0 \end{cases} \tag{15}$$

where $v_{DC\_Low\_1}$ and $v_{DC\_Low\_2}$ are average voltage values across the DC-link upper and lower capacitor, respectively.

Therefore, the basic building block in this part of the ST is the one T-Type branch (Figure 7b). From the converter AC side, the average model can be represented as a controlled voltage source, described by (14). Assuming, that for $D > 0$ the output energy is supplied from capacitor $C1$ and for $D < 0$ the output energy is supplied from capacitor $C2$, an uneven voltage distribution across the capacitors often occurs. To simulate these voltage fluctuations, it is necessary to use two controlled current sources for each T-Type branch from the DC-side point of view. The average current value of those controlled current sources is determined based on the power balance equation, similarly to the CHB converter:

$$\begin{cases} i_{DC\_Low\_X1} = D \times i_{AC} \\ i_{DC\_Low\_X2} = 0 \end{cases} \quad for\ D \geq 0$$
$$\begin{cases} i_{DC\_Low\_X1} = 0 \\ i_{DC\_Low\_X2} = D \times i_{AC} \end{cases} \quad for\ D < 0 \tag{16}$$

where X indicates phases A, B, C, and N.

Taking the above equations into consideration, the average model of the one T-Type module can be realised, as it is shown in Figure 8. Then, the whole DC-LV/AC-LV side of the ST can be obtained by four parallel average models of the one module.

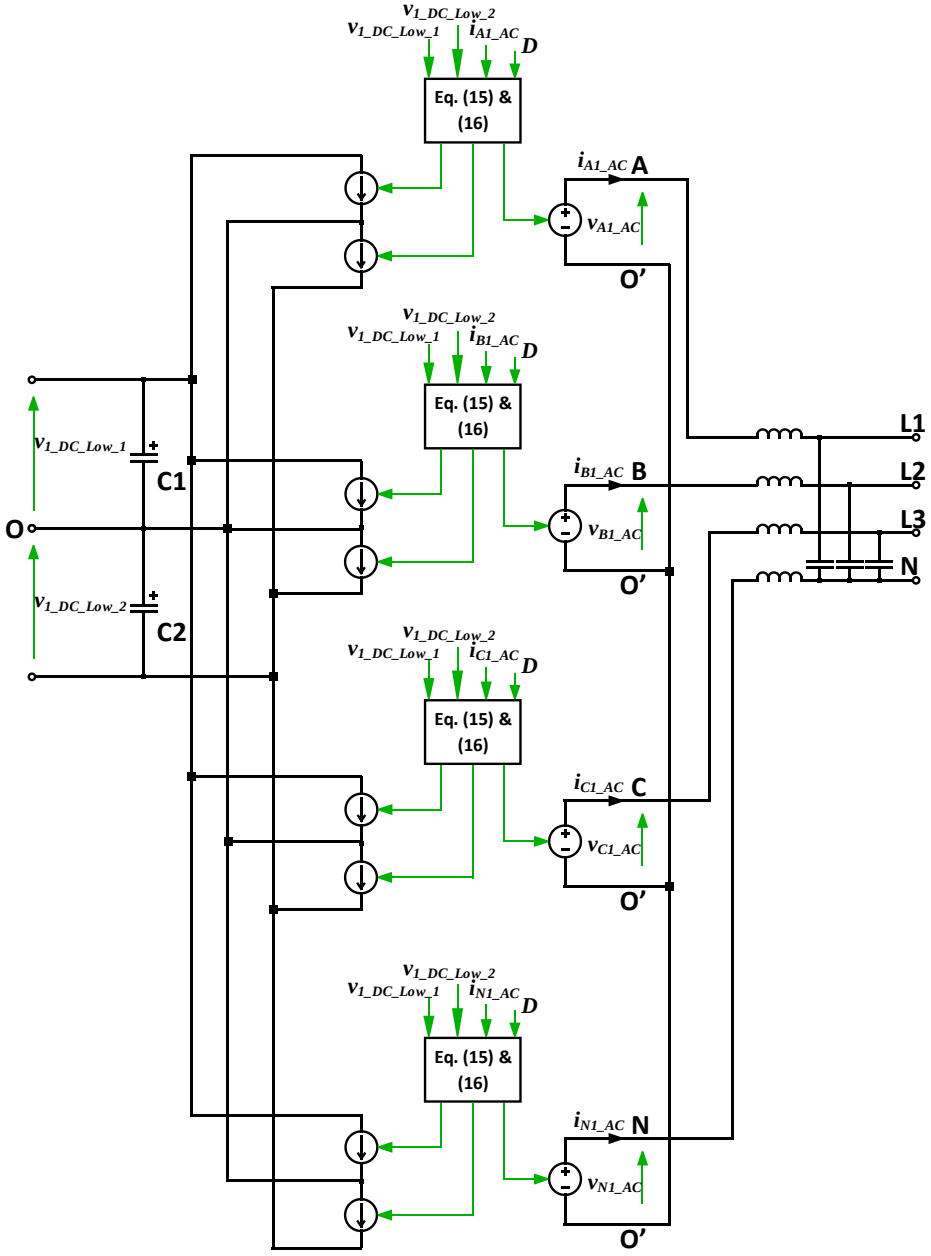

Figure 8. The average model of the one T-type module in the DC-AC converter.

3. Results

The proposed average model of the advanced ST with wye-delta HF transformer has been verified in simulation research. Since the full switching model is difficult to simulate (based on the available hardware and computing capacity) and the attempts to conduct the full model analysis could not be completed with available hardware listed in Table 1 and used software (PLECS), the advantages of the described model have been studied for separated ST power conversion stages. The comparison of the full switching ST model and the ST average model has been performed in simulation research in both cases. In the end, the whole average model has been simulated to observe the ST operation under normal conditions and verified the model correctness.

Table 1. The computer hardware used in the conducted research.

Parameter	Value	Parameter	Value
Operating System	Microsoft Windows 10 Home	Graphic Card	NVIDIA GeForce MX150, with 2 GB GDDR5 VRAM
Processor	Intel Core i7-8550U CPU @ 1.8 GHz, 4 cores	Hard Drive Type	SATA 3.0 M.2 SSD 256 GB
RAM Memory	16 GB DDR4	-	-

The considered model of the ST with the MV grid and LV loads was simulated with the parameters related to the conducted project (Table 2). The assumed voltage, current, power levels are lower than in the real device, where the MV and LV side correspond to the correct normalised levels. The performed analysis is related to the scaled laboratory model of the ST. To compare the real and average model of the ST, the basic control algorithms have been implemented for all power conversion stages. The advanced functionalities of the ST, which do not interfere with the structure of the device, have not been analysed.

Table 2. The ST simulation model parameters.

Parameter	Value	Parameter	Value
AC grid voltage—rms (L-L) (AC-MV side of ST)	3 × 400 (V)	LV DC link capacitors for DAB model	3.96 (mF)
Rated power	10 (kVA)	LC DV link reference value	270 (V)
Grid resistance (AC-MV side of ST)	3 (mΩ)	LV DC link capacitors for T-type converter	2 × 5.28 (mF)
Grid inductance (AC-MV side of ST)	1 (mH)	LC filter single inductance	0.5 (mH)
AC-MV/DC-MV DC link capacitors	9 × 1.65 (mF)	LC filter single capacitance	10 (μF)
AC-MV/DC-MV DC link reference values	9 × 270 (V)	Switching frequency	100 (kHz)
Transformer equivalent leakage inductance	9 × 10 (μH)	LV side AC voltage reference—rms (L-N)	3 × 70.71 (V)
Transformer equivalent winding resistances	9 × 10 (mΩ)	-	-

3.1. Study of the AC-MV/DC-MV Side of ST

The described nine H-bridges (included in CHB) have been controlled by the classical voltage-oriented control (VOC) algorithm [25–27]. The specific description of the VOC algorithm is well-known in the literature and widely used in the power electronics devices. The modulation index d_x for all modules is there obtained based on the inner current control loop with a proportional-resonant (PR) controller tuned to fundamental grid frequency (Figure 9a). The outer DC-link voltage control loop with proportional-integral (PI) controller calculates the referenced current value for the inner control loop. The referenced current is synchronised with the grid voltage vector by utilisation of a phase-locked loop (PLL), which in the considered model based on the second order general integrator (SOGI) [28,29].

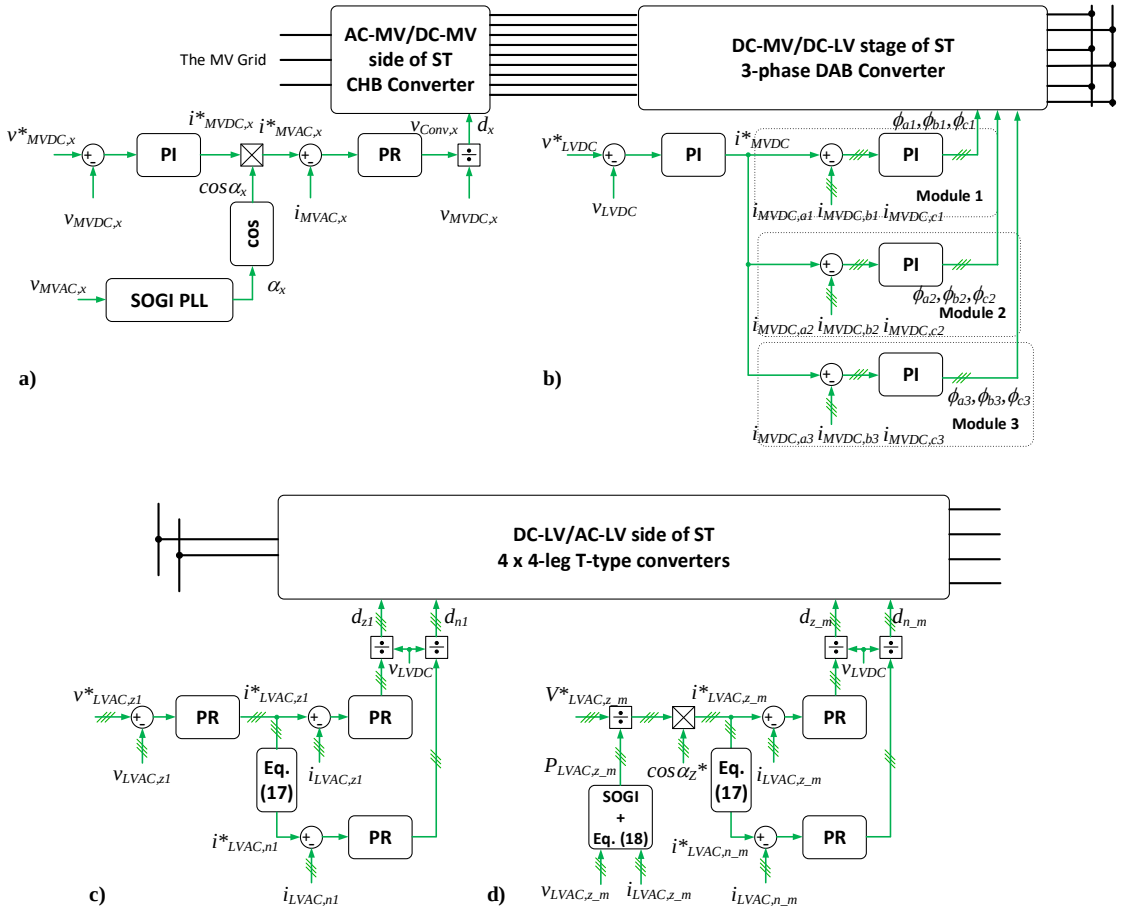

Figure 9. The block scheme of basic control algorithms used in the ST, (**a**) control loops of CHBs for the AC-MV/DC-MV side of ST, (**b**) control loops for MAB for the DC-MV/DC-LV stage of ST, (**c**) control loops for T-type converter as a controlled voltage source for DC-LV/AC-LV side of ST, (**d**) control loops for T-type converter as a controlled current source for the DC-LV/AC-LV side of ST.

The simulation result of the averaged and switched model of this ST power stage is shown in Figure 10. It can be noticed that the results for the same simulation parameters are similar in steady state as well as for the dynamic change of the requested power. The most important advantage of the average model over the full switching model is the simulation time. It has been observed that the simulation time has been reduced 14 times, from 100.8 s to 6.89 s.

3.2. Study of the DC-MV/DC-LV Power Stage of ST—the Isolated MAB DC-DC Converter with Wye-Delta Transformer

For the DC-DC power electronics converter used in the ST structure the common phase shift control algorithm has been implemented [9,12,20,22]. For each of the HF transformers the three phase shifts are calculated (nine in total). The values of phase shifts ϕ_{xy} depend on the inner control loop with PI regulators, which operates on the current error obtained from the measurements in each of nine MV DC-links and referenced values (Figure 9b). Those are obtained by one common outer control loop, of which the main goal is to keep a constant voltage in the LV ST DC-link.

In the observed results shown in Figure 11, the voltages and currents are similar in the steady-state and during the dynamic change of the power. The not significant difference (2%) seen in the phase shift is caused by the simplifications in the described equations for the modelled current sources. In this power conversion stage, the simulation time has been reduced from 400 s to only 12.48 s, which gives 32-times-shorter process.

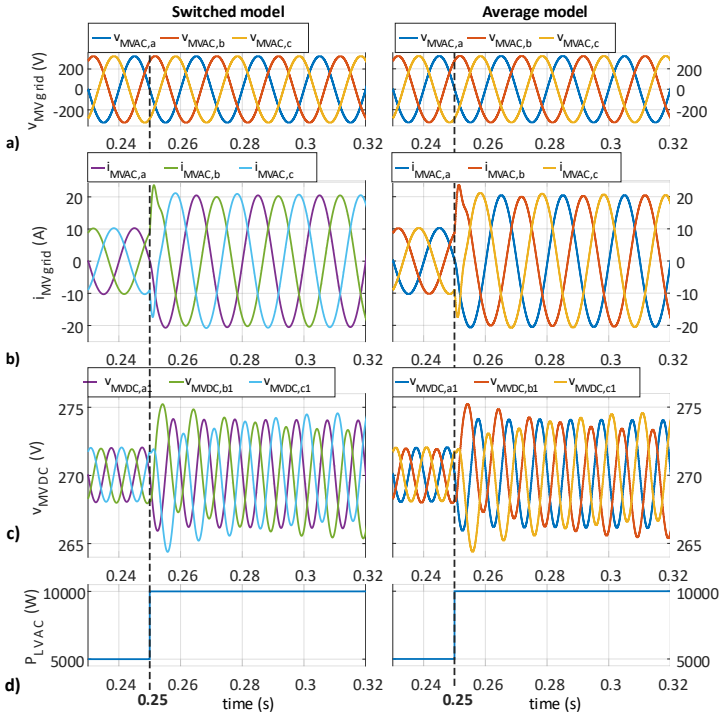

Figure 10. The voltages and currents of the CHB, (**a**) grid voltages on the MV side of ST, (**b**) grid currents, (**c**) DC-link voltages for one module in each phase, (**d**) referenced power value.

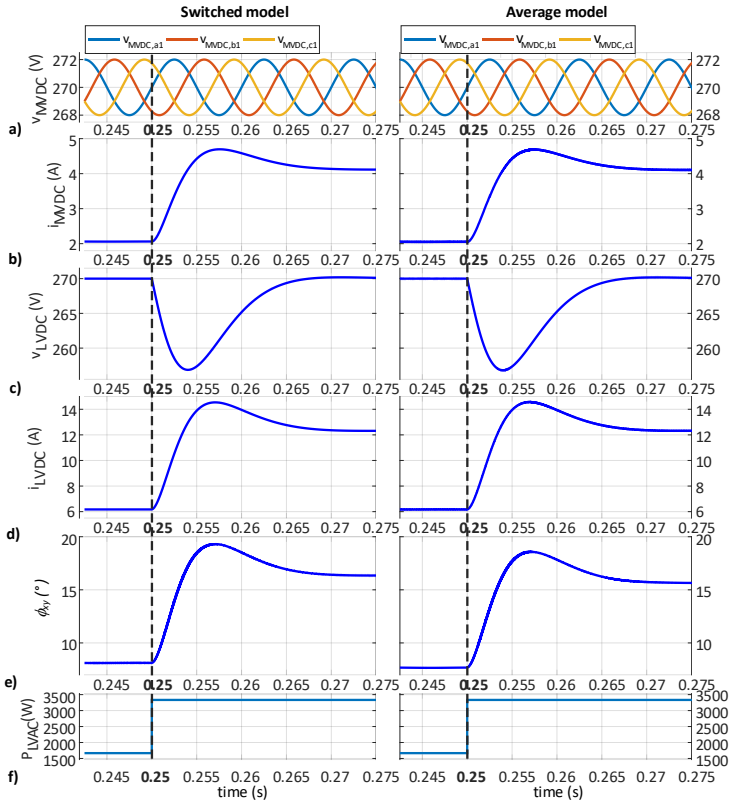

Figure 11. The voltages and currents of the three-phase DAB implemented in the ST, (**a**) DC-link voltages for one module in each phase (one transformer), (**b**) DC-link currents from MV side, (**c**) DC-link voltage from LV side, (**d**) DC-link current from LV side, (**e**) phase shift, (**f**) requested power value.

3.3. Study of the DC-LV/AC-LV Side of ST

The last power conversion stage of the ST has been analysed with the basic control algorithm known in the islanded applications of the power electronics converters [14,24,30]. In the proposed structure of the ST, four T-type converters are working parallelly, hence the master-slave control strategy has been selected to provide the proper operation of the device. One of the converters works as a controlled voltage source (CVS), with an inner current control loop and outer AC voltage control loop (Figure 9c). Both are based on PR controllers and operate in a stationary *abc* reference frame.

The current in a neutral wire of the converter is also controlled, keeping the reference current value i^*_{LVACnx} equal:

$$i^*_{LVACnx} = -\left(i^*_{LVACax} + i^*_{LVACbx} + i^*_{LVACcx}\right) \tag{17}$$

where x is an index of the CVS converter.

Other converters work as a controlled current sources (CCS) synchronised by SOGI-PLL with CVS (Figure 9d). There is only one control loop based on PR controllers, which operates on the current error calculated from measured and referenced values. Those provide equal currents in all four modules. Taking into consideration measured voltages and currents in all modules for each phase in the stationary $\alpha\beta$ reference frame, the average active powers are calculated as:

$$P_z = \sum_{x=1}^{4} \frac{v_{\alpha zx} i_{\alpha zx} + v_{\beta zx} i_{\beta zx}}{2} \tag{18}$$

where x is an index of the T-type converter and z indicates the selected phase a, b, c.

Then, the amplitude of the referenced current is calculated (the same for each converter) and the instantaneous reference current value is obtained with the synchronised vector phase and function $cos\alpha_z$. The modulation indexes d_z as a result of control algorithms are used in averaged and switching models. The obtained results are shown in Figure 12. Notice that the voltages and currents waveforms are comparable for both models in a steady-state and dynamic state of operation. All voltage fluctuations across DC-link capacitors are also included. Moreover, the analysed symmetrical and asymmetrical resistance loads prove that the proposed average model allows conducting reliable research of the control algorithms. In the case of this power conversion stage, the simulation time has been reduced 36 times compared with the switching model (from 723.9 s to 19.78 s).

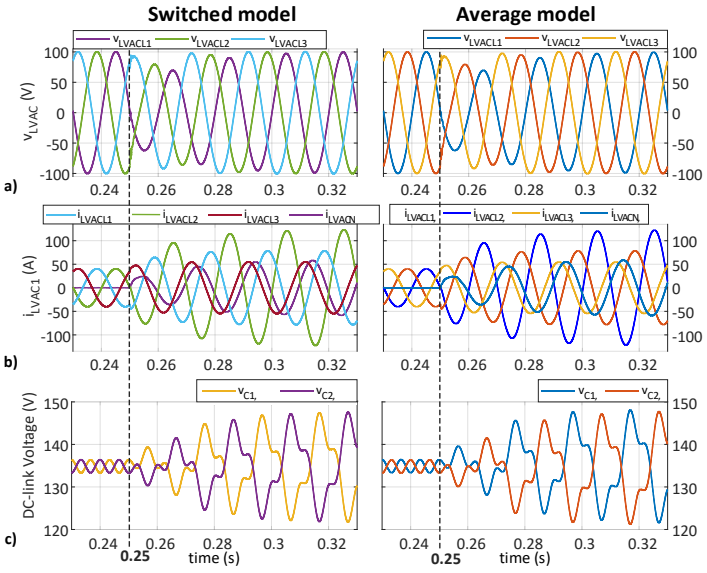

Figure 12. The voltages and currents of the T-type converter, (**a**) LV grid (load) voltages, (**b**) load currents, (**c**) DC-link voltages—across upper and lower capacitors.

3.4. The Complete ST Average Model Analysis

The last performed research was related to the analysis of the whole ST operation, with the described basic control algorithms. The three different conditions have been taken into consideration (Figure 13). First, the symmetrical voltages of the grid from the MV side of the ST and symmetrical loads on the LV side have been studied. Those conditions do not cause the voltage fluctuations in the LV DC link of T-type converters. Moreover, the symmetrical AC components of the DC-link voltages in CHB converters are provided. After the load condition changes, the AC voltage component occurs in the LV DC-link, which is a proper behaviour in that situation. Notice, that the changed power also appears from the grid side (AC-MV/DC-MV side of ST), showing the operation of all converters simultaneously. The last case assumes the worst conditions, when the grid is characterised by asymmetrical voltages and asymmetrical loads are connected through the ST. Then, the problem of unequal DC-link voltages in CHB is observed, but the ST can still provide the proper voltages for the loads. The observed issues should be eliminated by investigation of the more advanced control algorithms.

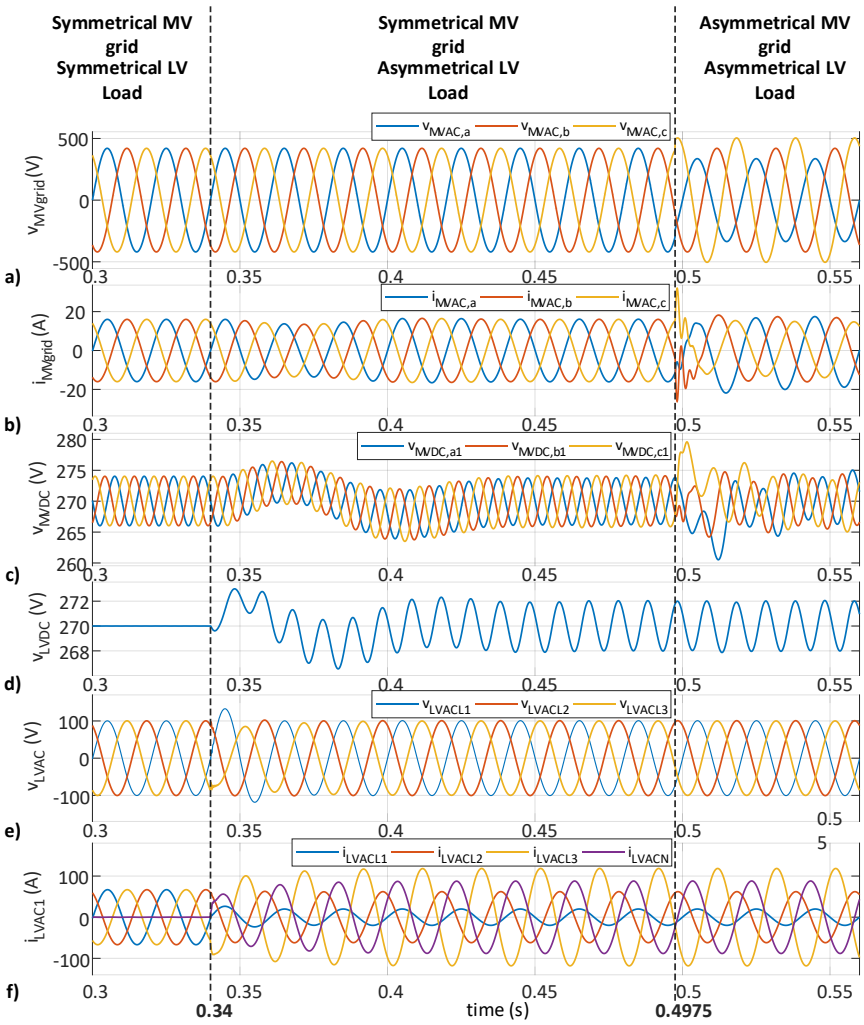

Figure 13. The voltages and currents of the ST—all modules integrated, (**a**) grid voltages on the MV side of ST, (**b**) grid currents, (**c**) DC-link voltages for one module in each phase, (**d**) LV DC-link voltage, (**e**) LV grid (load) voltages, (**f**) load currents.

4. Discussion

The power electronics converters and their applications are strongly developing, increasing the number of semiconductor power switches and making topologies more advanced and functional. The

more complex converters are making it difficult to simulate (depending on the available computer hardware and software) and investigate the advanced control algorithms. One of those solutions is the Smart-Transformer, which is characterised by a lot of switching elements. To perform the simulation in a reasonable time for a full model of the ST and the complete control algorithm, the average process is necessary. This is a well-known solution for single power electronics converters. Based on the small average model of separated power conversion stages and common converter topologies, it is possible to develop a complicated simulation model and analyse new control solutions in steady-state and dynamic states of operation. The novel average model for the developed MAB DC/DC converter used in the considered ST topology has been proposed and studied. The presented results prove that the whole proposed model, built from the averaged small models (building blocks) is significantly faster with the same result of analysis in steady-state and dynamic processes. The simulation times of each power conversion stage mentioned in Sctions 3.1–3.3 for each power energy stage of ST and additionally for the whole ST average model are shown in Table 3. Notice that the simulation time is significantly decreased, and the obtained advantage is the most important in the case of the circuit with a high number of transistors (four T-type 4-leg power electronics converter models).

Table 3. The simulation times of the average model and fully switched model for the selected ST stages and the whole ST.

Power Stage	Average Model	Switching Model
AC-MV/DC-MV side of ST	6.89 s	100.8 s
MAB DC-DC Converter with HF transformer	12.48 s	400.9 s
DC-LV/AC-LV side of ST	19.78 s	723.9 s
Whole ST topology	139.6 s	-

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Appendix A

Table A1. List of symbols.

Symbol	Description
σ	index of the created state-space matrices by the simulation software
ϕ	phase shift between high frequency voltages v_{AC_High} and v_{AC_Low}
α_x	angle of the AC voltage vector of the x H-bridge in CHBC
$\phi_{x1, ..x2, ..x3}$	phase shift between high frequency voltages v_{AC_High} and v_{AC_Low} for each phase x and module of the MAB in the ST
$\alpha_z{}^*$	Referenced voltage vector angle for T-type converters working as a controlled current source
$..^*$	indication of referenced values
$..', ..'', ..'''$	indication of H-bridges in each phase of the cascaded H-bridge converter (CHBC)
$A_\sigma, B_\sigma, C_\sigma, D_\sigma$	state matrix, input matrix, output matrix, direct transition matrix respectively
a, b, c, n	phases of the grid voltages and currents in *abc* reference system
D	modulation index
D	phase shift ratio for DAB converter

Table A1. *Cont.*

Symbol	Description
d_x	modulation index of the x H-bridge in CHBC
$d_{z1, ..z\_m, ..n1 ..n\_m}$	modulation indexes for T-type converters
f_s	switching frequency
i^*_{MVDC}	referenced current value for each H-bridge in Multiple Active Bridge (MAB) from the high voltage side
i_{AC}	AC current of the one H-bridge in CHBC
i_{AC_High}	AC high frequency current of the transformer primary side in the one Dual Active Bridge (DAB)
i_{AC_Low}	AC high frequency current of the transformer secondary side in the one Dual Active Bridge (DAB)
i_{DC}	DC current of the one H-bridge in CHBC
i_{DC_High}	DC current of the one Dual Active Bridge (DAB) from the high voltage side
i_{DC_Low}	DC current of the one Dual Active Bridge (DAB) from the low voltage side
$i_{DC\_Low\_X1}$	reference current value for current source of DC-link upper capacitor for phase X, where X indicates A, B, C, N phase
$i_{DC\_Low\_X2}$	reference current value for current source of DC-link lower capacitor for phase X, where X indicates A, B, C, N phase
$i_{LVAC,n1}$	AV current of the T-type converter working as a controlled voltage source in phase n
$i_{LVAC,z\_m ..n\_m}$	AV current of the T-type converter working as a controlled current source in phase z, where z indicates a, b, c and n is the neutral wire
$i_{LVAC,z1}$	AV current of the T-type converter working as a controlled voltage source in phase z, where z indicates a, b, c
$i_{MVAC,x}$	AC current of the x H-bridge in CHBC
$i_{MVDC,x}$	DC current of the x H-bridge in CHBC
$i_{MVDC,x1 ..2 ..3}$	current values of each H-bridge in Multiple Active Bridge (MAB) from the high voltage side
i_{MVgrid}	AC current of the connected grid form the ST MV side
i_{peak_1}	current peak value when the current rises
i_{peak_2}	current peak value when the current start falling
$L1$, $L2$, $L3$, N	Output lines of the LV T-type converter
L_{eq}	equivalent leakage inductance referred to the transformer primary side
L_p	inductance of the transformer primary winding
L_s	inductance of the transformer secondary winding
m	transformer turn ratio
P	active power
p_{AC}	Instantaneous active power from AC side of the one H-bridge in CHBC
p_{DC}	active power from DC side of the one H-bridge in CHBC
P_{LVAC,z_m}	Average active power of the T-type converter
P_z	Total average active power of all T-type converters used in the ST LV side
R_c	conduction resistance of the transistor in the DAB converter
R_{eq}	equivalent resistance referred to the transformer primary side
R_p	resistance of the transformer primary winding
R_s	resistance of the transformer secondary winding
T	high frequency transformer current period
T_s	switching period
u	input of the dynamic system
V^*_{LVAC,z_m}	Referenced voltage amplitude in phase z, where z indicates a, b, c
v_{AC}	AC voltage of the one H-bridge in CHBC
v_{AC_High}	AC high frequency voltage of the transformer primary side in the one Dual Active Bridge (DAB)
v_{AC_Low}	AC high frequency voltage of the transformer secondary side in the one Dual Active Bridge (DAB)
$vConv,x$	AC referenced voltage of the x H-bridge in CHBC
v_{DC}	DC voltage of the one H-bridge in CHBC
v_{DC_High}	DC voltage of the one Dual Active Bridge (DAB) from the high voltage side
v_{DC_Low}	DC voltage of the one Dual Active Bridge (DAB) from the low voltage side

Table A1. *Cont.*

Symbol	Description
$v_{DC\_Low\_1}$, V_{C1}	average voltage values across DC-link upper capacitor in T-type converter
$v_{DC\_Low\_2}$, V_{C2}	average voltage values across DC-link lower capacitor in T-type converter
v_{LVAC,z_m}	AV voltage of the T-type converter working as a controlled current source in phase z, where z indicates a, b, c
$v_{LVAC,z1}$	AV voltage of the T-type converter working as a controlled voltage source in phase z, where z indicates a, b, c
v_{LVDC}	DC voltage of the one Dual Active Bridge (DAB) from the low voltage side
v_{LVDC}	DC voltage of the T-type converter
$v_{MVAC,x}$	AC voltage of the x H-bridge in CHBC
$v_{MVDC,x}$	DC voltage of the x H-bridge in CHBC
v_{MVgrid}	AC voltage of the connected grid form the ST MV side
x, $\dot{x}$	state-transition matrix of the dynamic system and the derivative of the state-transition matrix respectively
y	output of the dynamic system

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