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AC–DC Flyback Dimmable LED Driver with Low-Frequency Current Ripple Reduced and Power Dissipation in BJT Linearly Proportional to LED Current

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Abstract: In this paper, a dimmable light-emitting diode (LED) driver, along with the low-frequency current ripple decreased and the bipolar junction transistor (BJT) power dissipation reduced, is developed. This driver is designed based on a single-stage flyback converter. On the one hand, the low-frequency output current ripple reduction is based on the physical behavior of the linear current regulator. On the other hand, when the voltage across the LED string is decreased/increased due to dimming or temperature, the output voltage of the flyback converter will be automatically regulated down/up, thereby making the power dissipation in the BJT linearly proportional to the LED current. By doing so, not only the power loss in the linear current regulator will be decreased as the LED current is decreased or the LED temperature rises, but also the output current ripple can be reduced. Furthermore, the corresponding power factor (PF) is almost not changed, and the total harmonic distortion (THD) is improved slightly. In addition, the LED dimming is based on voltage division. Eventually, a 30 W LED driver, with an input voltage range from 85 to 295 V_{rms} and with 24 LEDs in series used as a load, is developed, and accordingly, the feasibility of the proposed LED driver is validated by experimental results.

Keywords: bipolar junction transistor (BJT); current ripple; light-emitting diode (LED); dimmable; linear current regulator; output voltage automatic regulator; power factor (PF); single-stage AC–DC flyback converter; total harmonic distortion (THD)

1. Introduction

As generally recognized, the light-emitting diode (LED) is becoming more attractive in the world due to its small size, light weight, and long life [1,2]. In general, LED drivers with dimming from 100% to 10% are widely used. Adjusting the light level between 10% and 5% is called deep dimming. Modulating the light output through an LED's current is achieved either by pulse width modulation (PWM) switching, or by amplitude control, also known as analog or level dimming. The former allows deep deeming but presents low luminous efficiency and a risk of flicker [3]. The latter is inherently safer with respect to flicker, but changes the LED operating point and hence the colorimetric characteristics [4]. For those reasons, PWM is the preferred method, and the corresponding dimming frequency is kept above 3.6 kHz to meet flicker specifications.

However, if the DC current with the low-frequency current ripple, due to the mains, is applied to the LED, the flickering will also occur [5]. Consequently, how to reduce this ripple is a very important issue. The flickering will make the human body uncomfortable and the human eye tired [6]. On the other hand, As well known, the LED lighting is an energy-saving device. Therefore, if the LED lighting can be dimmable, more energy will be savedm and the corresponding additional cost will be decreased. As well recognized in industrial applications, the DC LED driver can be classified into three types. One is the single-stage constructed by the flyback converter [7], another is the two-stage built up by the flyback and buck converters [8], and the other is the two-stage established by the boost and flyback/forward converters [9]. The first type has a simple structure, low cost, and high efficiency, but with a high low-frequency current ripple. However, the second and third types are of small low-frequency current ripple, but with complex structure, high cost, and low efficiency. Accordingly, the first type has a more serious flickering problem than the other two.

Therefore, how to reduce LED flickering is a research issue in this paper. The literature [10] presents a comprehensive experimental-based labeling methodology for comparing LED performance with reference to light flicker and power factor. The literature [11] presents an auxiliary circuit with battery powering, and by controlling this circuit, a current opposite to the low-frequency current ripple is generated to suppress such a current ripple. The literatures [12,13] adopt the three-phase voltage along with the power factor correction (PFC) to decrease the low-frequency current ripple. The literature [14,15] employs some auxiliary circuits, which will generate energy via different paths and transfer this energy to the output so that the low-frequency current ripple can be inhibited. The literature [16,17] also utilizes the third-order harmonic injection so that the input power pulsation will be smoothed; hence, the low-frequency current ripple can be alleviated, but the corresponding power factor (PF) is degraded. Furthermore, the literature [18,19] employs the valley-fill circuits, which will change the turn-on angle between the input instantaneous power and the input current, so that the low-frequency current ripple can be reduced. However, the above-mentioned methods have a common default of circuit complexity and design difficulty. Consequently, in this paper, a single-stage AC–DC flyback LED driver, together with a linear current regulator having the bipolar junction transistor (BJT) whose power dissipation is only linearly proportional to the LED current, is employed so as to decrease LED low-frequency flicker significantly with PF and total harmonic distortion (THD) slightly influenced. In addition, amplitude dimming from 100% to 10% is adopted herein.

2. Basic Operating Principles of the Proposed Circuit

Figure 1 displays the system block diagram for the proposed LED driver, and Figure 2 briefly illustrates its overall system. Figure 2 shows the proposed circuit with the input voltage v_{ac} and the input current i_{ac} before the bridge diode BD1. This circuit contains three subsystem blocks. The first subsystem block is the main power stage constructed by one single-stage flyback converter with the transformer T_1 having the primary turns of N_1 and the secondary turns of N_2. The second subsystem block is the linear current regulator along with a dimming function built up by one operational amplifier OP_1 used as a buffer with the voltage V_1 at the non-inverting input terminal and the voltage V_2 at the inverting input terminal, one BJT Q_1 operating in the linear region, one current-sensing resistor R_s, and three voltage-dividing resistors R_1, R_2, and VR_1, whose value can be adjustable. The third subsystem block is the output voltage automatic regulator established by one operational amplifier OP_2 used as a subtractor with the voltage V_3 at the non-inverting input terminal and the sensed voltage V_4 at the inverting input terminal, one adjustable precision shunt regulator TL432 providing one reference voltage V_3 of 1.24 V via the circuit voltage V_{CC}, one photocoupler, one controller, and two current-limiting resistors R_x and R_{ref}. Furthermore, the voltages V_o, V_f, and V_s indicate that the output voltage of the flyback converter, the equivalent forward voltage of the LED string, and the voltage across R_s, respectively. In addition, the voltage V_2 is equal to the voltage V_1 based on the virtual ground, and the current I_o is the current flowing through the LED string.

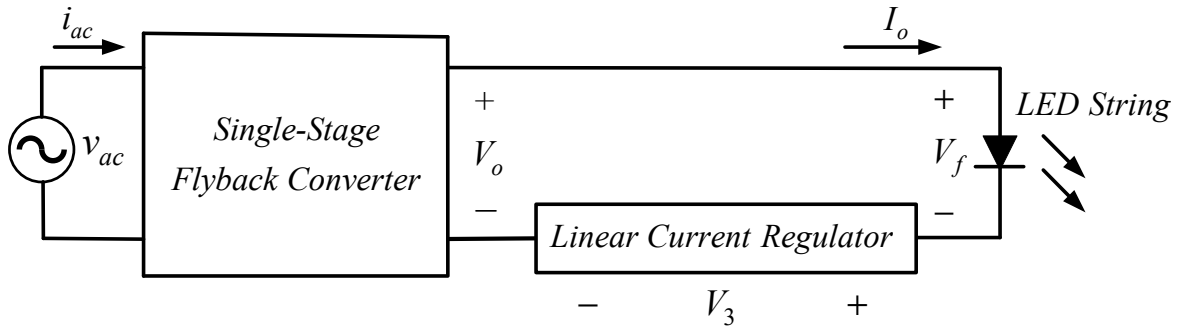


Figure 1. System block diagram.

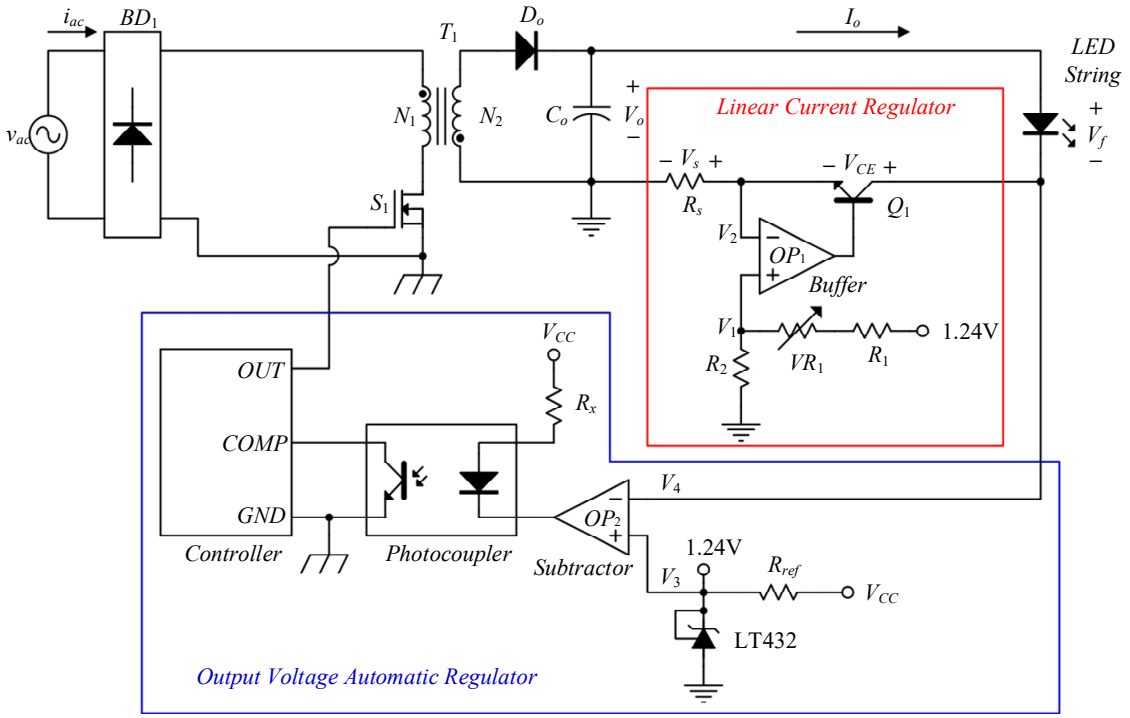


Figure 2. Brief illustration of the overall system for the proposed light-emitting diode (LED) driver.

3. Basic Operating Concept

3.1. Reduction of Low-Frequency Output Current Ripple

Figure 1 displays the basic operating concept for reduction of the low-frequency output current ripple. As generally acknowledged, the single-stage flyback converter, operating under voltage control, can be regarded as a voltage source, and the linear current regulator under current control can be viewed as a current source. Therefore, the internal impedance of the linear current regulator is much larger than the equivalent impedance of the LED string. That is, the voltage ripple on the LED string is much lower than that on the linear current regulator based on the voltage division, thereby causing the corresponding current ripple in the LED string to be reduced significantly.

3.2. System Stability Based on Simple Circuit Concept

From the circuit concept point of view, the voltage source can be regarded as a capacitor with an infinite capacitance and vice versa, and the current source can be viewed as an inductor with an infinite inductance and vice versa [20]. Hence, the circuit in Figure 1 can be considered as a series RLC circuit, consisting of a resistor (R), an inductor (L) and a capacitor (C), and the quality factor Q is the

characteristic impedance Z_o divided by the equivalent resistance of the LED string, called R, where Z_o is $\sqrt{L/C}$, which is equal to one based on the limit concept [21]. Hence, the value Q, equal to Z_o/R, is quite small since the value of R is larger than one, about 50 Ω in this paper, thereby making the phase margin quite large and guaranteeing that the circuit is stable [22].

3.3. Output Voltage Automatic Regulator

From Figure 1, the relationship between the voltages V_o, V_f, V_{CE} and V_s can be represented by

$$V_o = V_f + V_{CE} + V_s. \tag{1}$$

From (1), since the voltage V_s is relatively low, Equation (1) can be rewritten to be

$$V_o \approx V_f + V_{CE}. \tag{2}$$

From (2), under the condition that the voltage V_o is fixed, if the voltage V_f increases, the voltage V_{CE} decreases, whereas if the voltage V_f decreases, the voltage V_{CE} increases. Under a given value of I_o with the corresponding value of V_{CE}, the accompanying power dissipation on Q_1, called P_{Q1}, can be expressed as

$$P_{Q1} = V_{CE} \times I_o. \tag{3}$$

However, under the condition that the voltage V_o and the current I_o are fixed, if the number of LEDs in the LED string is decreased or if the LED temperature is increased, then the voltage V_f will be decreased and the voltage V_{CE} will be increased based on (2). Hence, the power dissipation P_{Q1} will be increased based on (3).

Consequently, from (2), under the condition that the voltage V_{CE} and the current I_o are fixed, if the voltage V_f increases, the voltage V_o increases; otherwise, the voltage V_o decreases. This will be achieved based on output voltage automatic regulation so that the voltage V_{CE} can be kept constant almost at the reference voltage V_3 for any time. Therefore, under a given value of I_o, the accompanying power dissipation can be expressed as

$$P_{Q1} = V_3 \times I_o. \tag{4}$$

Therefore, we can see that the result in (4) will not be affected by any value of V_{CE}. Hence, the lower the load current, the less the power dissipation on Q_1. That means that if the value of V_3 is suitably chosen near the curve knee of the linear region of Q_1 or somewhat more, the power dissipation on Q_1 will be reduced all over the output load range and the input voltage range.

Regarding the corresponding operating principle for the output voltage automatic regulator, it will be described based on Figure 2 as follows. First, the sensed feedback voltage V_4 is sent to the subtractor, and this voltage is subtracted from the reference voltage V_3 to yield an error signal. Then, this error signal is passed to the compensator, named *COMP*, via the photocoupler, to create a desired gate driving signal, which is sent to the switch S_1 via *OUT*. By doing so, the LED driver can operate in the critical conduction mode (CRM) with V_{CE} kept at 1.24 V and hence V_o kept at some variable value, equal to the sum of V_f and 1.24 V, where V_f is a function of the current, temperature, and the number of LEDs. In addition, the CRM pulse width modulation (PWM) control will make the main switch have near-zero voltage switching (NZVS).

3.4. Operating Principle of CRM PWM Control

The waveforms shown in Figure 3 are used to understand the basic operating principle of the CRM PWM control for the single-stage PF flyback converter. From Figure 3, as soon as the zero current at the secondary is from the positive current to zero, the resonance occurs between the primary inductance and the parasitic capacitance of the main switch. Hence, the current at the primary goes to the negative. As soon as such a current goes to zero, the accompanying voltage on the main switch resonates to the minimum value. At this moment, the main switch is turned on with NZVS, and this is

achieved by the auxiliary winding. As seen in Figure 3, the voltage on the auxiliary winding is almost the same as that on the main switch except for the amplitude. Therefore, the zero current detection signal, called *ZCD*, is attained and compared with a fixed threshold voltage inside the CRM PWM integrated circuit (IC); hence, the resulting gate-driving signal v_{gs} is activated.

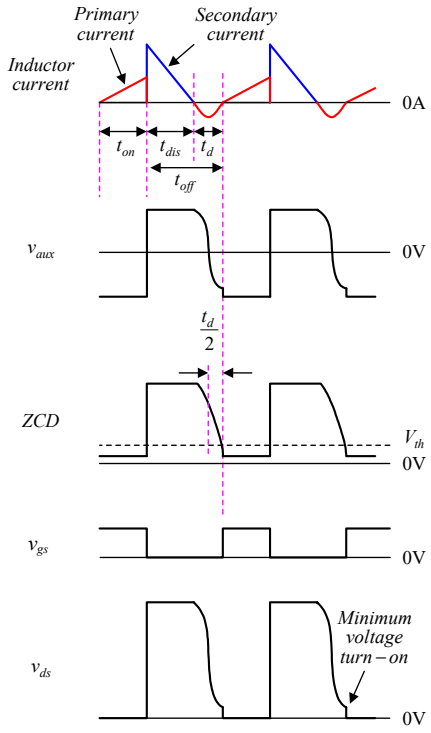


Figure 3. Illustrated waveforms under critical conduction mode (CRM) pulse width modulation (PWM) control.

As for the control loop of the single-stage PF flyback converter based on the L6561 PWM IC [23], it will have a narrow bandwidth (<20 Hz) to maintain control force almost constant over a given line cycle, and this will ensure a high PF. The higher the PF, the larger the inrush current during the turn-on period, and the slower the transient response. Accordingly, the bandwidth will be designed between 10 and 16 Hz. In addition, based on the CRM PWM control, the right-half-plane zero is removed, and only a single left-half-plane pole exists, thereby making the control design relatively easy [22].

The following mathematical derivative is based on CRM with the small value of t_d negligible, as shown in Figure 3. Since this converter operates in CRM with the bandwidth of the voltage loop far lower than that of the mains, the turn-on period T_{on} of the gate-driving signal for the main switch is kept constant at some value, as shown in Figure 4. Therefore, T_{on} can be expressed in terms of L_p, I_m and V_m:

$$T_{on} = \frac{L_p \cdot i_m(\omega t)}{v_{ac}(\omega t)} = \frac{L_p \cdot I_m}{V_m} \tag{5}$$

where L_p is the primary self-inductance, v_{ac} is the AC input voltage, i_m is the current flowing through L_p, ω is the radian frequency of v_{ac}, V_m is the maximum value of v_{ac}, and I_m is the maximum value of i_m.

In addition, the turn-off period t_{off} of the gate driving signal is instead variable and can be expressed by

$$t_{off} = \frac{L_p \cdot I_m \cdot \left|\sin(\omega t)\right|}{n \cdot (V_o + V_F)} \tag{6}$$

where t_{off} is the time duration between the instant of turning off the main switch and the instant of detecting the current flowing through the diode at the secondary to be zero, n is the turns ratio of

the flyback transformer, equal to N_1/N_2, V_o is the output voltage, and V_F is the voltage across the forward-biased diode at the secondary.

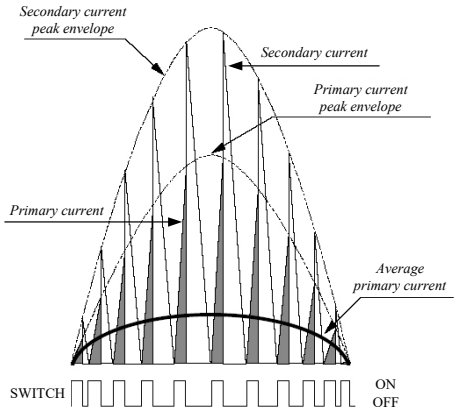


Figure 4. Current waveforms of the single-stage power factor (PF) flyback converter [23].

Therefore, based on (5) and (6), the variable switching period t_s can be represented by

$$t_s = T_{on} + t_{off} = \frac{L_p \cdot I_m \cdot [1 + K_v \cdot |\sin(\omega t)|]}{V_m} \tag{7}$$

where $K_v = V_m/V_R$, $V_R = n \cdot (V_o + V_F)$ and V_R is the voltage reflected from the secondary to the primary.

Hence, the variable switching frequency f_s can be expressed as

$$f_s = \frac{V_m}{L_p \cdot I_m \cdot [1 + K_v \cdot |\sin(\omega t)|]}. \tag{8}$$

Then, the minimum switching frequency $f_{s,min}$ can be obtained as

$$f_{s,\min} = \frac{V_m}{L_p \cdot I_m \cdot (1 + K_v)}. \tag{9}$$

According to (5) and (7), the resulting duty cycle d varied with the mains can be expressed as

$$d = \frac{T_{on}}{t_s} = \frac{1}{1 + K_v \cdot |\sin(\omega t)|}. \tag{10}$$

4. Design Considerations

In the following, the system specifications are given first, and then the design of the magnetizing inductance, output capacitance, dimming control circuit, linear current regulator, and output voltage automatic regulator follow. In the paper, a single LED, belonging to the Edixeon A1 Series, has the rated forward current of 350 mA and the typical forward voltage of 3.4 V. However, the forward voltage adopts 3.6 V due to a tolerance for different dimming current levels. Consequently, if the number of LEDs is chosen to be 24, then the maximum output voltage is 86.4 V plus 1.24 V and the maximum output current is 350 mA. Based on the above-mentioned, the system specifications are shown in Table 1. In addition, the efficiency at the rated load is assumed to 85% and the minimum switching frequency is set at 55 kHz.

Table 1. System specifications without the linear current regulator considered.

Parameter	Specification
Input Voltage (v_{ac})	90–277 V ± 5% (85–295 V)
Input Voltage Frequency (f_{ac})	60 Hz
Maximum Output Voltage ($V_{o,max}$)	86.4 V (= 3.6 V × 24)
Maximum Output Current ($I_{o,max}$)	350 mA
Minimum Output Current ($I_{o,min}$)	35 mA
Converter Efficiency (η)	85%
Minimum Switching Frequency ($f_{s,min}$)	55 kHz
LED String	24 LEDs in series

4.1. Design of Magnetizing Inductance L_m

The design procedure for L_m of the transformer T_1 is based on the application note AN1059 of the L6561 PWM IC [23], which makes the circuit operate in the CRM. In addition, it is assumed that there is no leakage inductance—that is, the coupling coefficient of the transformer is equal to one; hence, L_m is equal to the primary inductance L_p. There are four steps in design of L_m.

4.1.1. Step 1

From Table 1, some parameters will be used in the design, as shown in Table 2.

Table 2. Design parameters used.

Name	Symbol	Value	Unit
Maximum Output Voltage	$V_{o,max}$	86.4	V
Maximum Output Current	$I_{o,max}$	0.35	A
Maximum Output Power	$P_{o,max}$	30.24	W
Converter Efficiency	η	85	%
Minimum Input Voltage	$v_{ac,min}$	85	V_{rms}
Minimum Input Voltage	$v_{ac,max}$	295	V_{rms}
Minimum Switching Frequency	$f_{s,min}$	55	kHz

4.1.2. Step 2

The peak value of the minimum input voltage $v_{pk,min}$, the peak value of the maximum input voltage $v_{pk,max}$, and the rated input power $P_{in,max}$ are calculated as follows:

$$v_{pk,min} = \sqrt{2} \times v_{ac,min} = \sqrt{2} \times 85 = 120.21\text{V} \tag{11}$$

$$v_{pk,max} = \sqrt{2} \times v_{ac,max} = \sqrt{2} \times 295 = 417.19\text{V} \tag{12}$$

$$P_{in,max} = P_{o,max}/\eta = 30.24/0.85 = 35.58\text{W}. \tag{13}$$

4.1.3. Step 3

The expressions of the reflected voltage V_R, the maximum duty cycle D_{max}, and the ratio of $v_{pk,min}$ to V_R, called K_v, are shown below:

$$V_R = n \times (V_{o,max} + V_F) \tag{14}$$

$$D_{max} = \frac{V_R}{v_{pk,min} + V_R} \tag{15}$$

$$K_v = v_{pk,min}/V_R \tag{16}$$

where V_F is generally set at 1 V in the design.

In order to obtain relatively high utilization of the switch, the value of D_{max} is set at about 0.45. Accordingly, the value of n is adjusted based on (14) and (15) so that the value of D_{max} is close to 0.45. In this case, the value of n is set at 1.1. Therefore, the values of V_R, D_{max}, and K_v can be figured out to be

$$V_R = n \times (V_{o,max} + V_F) = 1.1 \times (86.4 + 1) = 96.14\,\text{V} \tag{17}$$

$$D_{max} = \frac{V_R}{v_{pk,min} + V_R} = \frac{96.14}{120.21 + 96.14} = 0.444 \tag{18}$$

$$K_v = v_{pk,min}/V_R = 120.21/96.14 = 1.25. \tag{19}$$

4.1.4. Step 4

The expressions of $F_2(K_v)$, which is a function of K_v, the peak value of the primary self-inductance current $I_{p,pk}$, and the primary self-inductance L_p, are shown below:

$$F_2(K_v) = \frac{0.5 + 0.0014 \times K_v}{1 + 0.815 \times K_v} \tag{20}$$

$$I_{p,pk} = \frac{2 \times P_{in,max}}{v_{pk,min} \times F_2(K_v)} \tag{21}$$

$$L_p = v_{pk,min}/[(f_{s,min} \times I_{p,pk} \times (1 + K_v)]. \tag{22}$$

Based on (13) and (19)–(22), the values of $F_2(K_v)$, $I_{p,pk}$, and L_p can be worked out to be

$$F_2(K_v) = \frac{0.5 + 0.0014 \times K_v}{1 + 0.815 \times K_v} = \frac{0.5 + 0.0014 \times 1.25}{1 + 0.815 \times 1.25} = 0.249 \tag{23}$$

$$I_{p,pk} = \frac{2 \times P_{in,max}}{v_{pk,min} \times F_2(K_v)} = \frac{2 \times 35.58}{120.21 \times 0.249} = 2.382\,\text{A} \tag{24}$$

$$L_p = v_{pk,min}/[(f_{s,min} \times I_{p,pk} \times (1 + K_v)] = 120.21/[(55\text{k} \times 2.382 \times (1 + 1.25)] = 408\,\mu\text{H}.$$

Since the transformer T_1 has the coupling coefficient of one, $L_m = L_p = 408$ μH. Hence, an RM8 core is chosen for T_1 with $N_1 = 51$ turns and $N_2 = 46$ turns.

4.2. Design of C_o

According to Table 1, since the low-frequency output voltage ripple will influence the value of C_o significantly, this ripple is assumed to be smaller than 4% of the maximum output voltage $V_{o,max}$. Accordingly, based on Table 1, the inequality of C_o can be obtained to be [24]:

$$C_o \geq \frac{I_{o,max}}{2 \times \pi \times f_{ac} \times \Delta v_o} = \frac{0.35}{2 \times \pi \times 60 \times 86.4 \times 0.04} = 269\,\mu\text{F}. \tag{25}$$

Hence, one 390 μF/100 V Rubycon capacitor is chosen as C_o.

4.3. Design of Input Filter

A two-order low-pass filter, with one inductor of 3.2 mH and one plastic capacitor of 0.22 μF, is used as an input filter and inserted between the rectifier and the LED driver. Therefore, the corner frequency of this filter is about 6 kHz. In addition, the harmonics for the THD regulations are measured up to the 39th order, equal to 60 Hz × 39 = 2.34 kHz, which is much lower than the corner frequency used. This means that such a filter does affect the THD slightly. Since the value of PF is the product of the displacement factor and the distortion factor, which is a function of THD, this filter does affect the PF slightly, also.

4.4. Components Used

The components used in the circuit is tabulated in Table 3.

Table 3. Component specifications.

Component	Part Name
S_1	IPA90R1K2
D_o	SFF1008G
C_o	390 uF/100 V Rubycon
T_1	A-CORE RM8 with N_1 = 51, N_2 = 46
Q_1	2SD1816
OP_1, OP_2	LM2904
R_s	0.2 Ω
R_1	4.7 kΩ
R_2	0.3 kΩ
VR_1	100 kΩ
R_x	10 kΩ
R_{ref}	4.7 kΩ
V_{CC}	12.3 V
Controller	LD7830
Photocoupler	EL817

4.5. Design of LED Dimming Circuit

From Figure 1, it can be seen that one variable resistor VR_1 is used to change the voltage V_1 and then the voltage V_2 will be varied, so that the output current I_o is altered to achieve LED dimming. In the following equation, the formula for I_o can be represented by

$$I_o = \frac{1.24 \times \left(\frac{R_{c2}}{R_{c1}+R_{c2}+VR_1}\right)}{R_s} \tag{26}$$

From Table 1, the output current locates between 10% and 100% of the maximum output current, namely, between 0.035 and 0.35 A. With the values of R_1 and R_2 set at 4.7 kΩ and 0.3 kΩ, respectively, the maximum output current is 0.372 A as the value of VR_1 is zero, whereas the minimum output current is 0.018 A as the value of VR_1 is 100 kΩ. These two values, covering the dimming current range, are calculated below:

$$I_{o,adj,max} = \frac{1.24 \times \left(\frac{R_{c2}}{R_{c1}+R_{c2}+0}\right)}{R_s} = \frac{1.24 \times \left(\frac{0.3k}{4.7k+0.3k+0}\right)}{0.2} = 0.372\,\text{A} \tag{27}$$

$$I_{o,adj,\min} = \frac{1.24 \times \left(\frac{R_{c2}}{R_{c1}+R_{c2}+100k}\right)}{R_s} = \frac{1.24 \times \left(\frac{0.3k}{4.7k+0.3k+100k}\right)}{0.2} = 0.018\,\text{A}. \tag{28}$$

4.6. Design of Linear Current Regulator

From Figure 1, the output current is determined by the following equation:

$$I_o = \frac{V_s}{R_s} \approx \frac{V_2}{R_s}. \tag{29}$$

Based on the LM2904 datasheet, it can be seen that the maximum offset of the input pin is 7 mV. This means that the value of V_2 should be larger than 7 mV to avoid this IC having an error in action at minimum output current. Hence, the value of V_2 is set at 70 mV, thereby causing the value of R_s to be 0.2 Ω (= 0.07 V/0.35 A).

4.7. Design of Output Voltage Automatic Regulator

4.7.1. Design of V_3

In design of the linear current regulator, the value of V_3 is set at 1.24 V due to a stable voltage of 1.24 V inside the LT432. Hence, we should make sure that the voltage V_{CE} for Q_1 is higher than the voltage $V_{CE,sat}$ to guarantee that Q_1 operates in the linear region. According to the datasheet for Q_1, called 2SD1816, as the current flowing through Q_1 is 410 mA, the corresponding voltage V_{CE} is 1 V, which is larger than the $V_{CE,sat}$ voltage of 0.4 V. In this paper, as the current flowing through Q_1 is 350 mA, the resulting voltage V_{CE} is 1.17 V (= 1.24 V − 0.35 A × 0.2 Ω), guaranteeing that Q_1 operates in the linear region.

4.7.2. Design of R_x and R_{ref}

From Figure 2, the value of V_{CC} is about 12.3 V. According to the industrial experience, the current flowing through R_x is at least 1 mA to make sure that the photocoupler can operate normally. Therefore, the value of R_x is set at 10 kΩ, causing the current in R_x to be 1.09 mA [= (12.3 − 2.4) V/10 kΩ], where 2.4 V is the voltage of the anode of the diode embedded in the photocoupler. On the other hand, the current flowing through R_{ref} is at least 2 mA to make sure that the TL432 can operates normally. Thus, the value of R_{ref} is set at 4.7 kΩ, thereby making the current in R_{ref} be 2.35 mA [= (12.3 − 1.24) V/4.7 kΩ].

5. Experimental Results

5.1. Test Bench for Measurements

The setup used to measure the efficiency will be briefly described. First, as shown in Figure 5, the values of input power, PF, and THD can be obtained from the power meter. Regarding the output power, the output current is read from a current meter, and the output voltage is read from another voltage meter. Therefore, the output power can be attained. Finally, the efficiency is deduced from those two measurements.

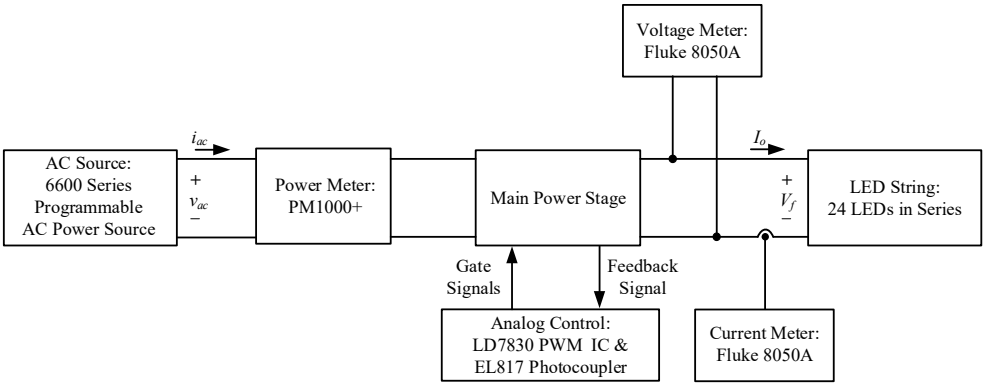


Figure 5. Test bench for measuring efficiency, PF, and total harmonic distortion (THD).

As for measured waveforms, they are also obtained by the instruments shown in Figure 5, along with one additional current amplifier, named Tektronix TCPA300, one additional current probe, named Tektronix TCP305, and one additional isolated oscilloscope, named Tektronix TPS2024B.

5.2. Actual System Circuit

Figure 6 shows the actual system circuit of the proposed LED driver, where the primary auxiliary winding N_3, the diode D_a, the capacitor C_a, and the resistor R_{ZCD} are used to obtain the signal ZCD, and the secondary auxiliary winding N_4, the diode D_b, the capacitor C_b, the transistor Q_2, the Zener Z_{D1}, and the resistor R_{ZD} are employed to generate the circuit voltage V_{CC}.

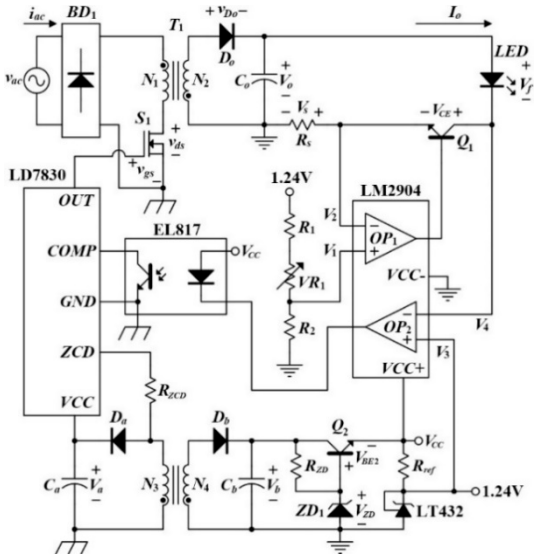


Figure 6. Actual system circuit of the proposed LED driver.

5.3. Measured Waveforms

At 110 and 220 V input voltages and 100% output load, some experimental results, without and with the proposed low-frequency current ripple improved, are given to verify the proposed LED driver.

Under 110 V input voltage and 100% output load, Figure 7 displays the input voltage v_{ac} and the input current i_{ac}, without and with the proposed method, whereas Figure 8 depicts the ripple of V_f, called Δv_f, and the ripple of I_o, called Δi_o, without and with the proposed method. Under 220 V input voltage and 100% output load, Figure 9 displays the input voltage v_{ac} and the input current i_{ac}, without and with the proposed method, whereas Figure 10 depicts the ripple of V_f, called Δv_f, and the ripple of I_o, called Δi_o, without and with the proposed method.

Some comments on measured waveforms will be given as follows:

(1) For both methods, the higher the input voltage, the larger the input current distortion.
(2) For both methods, any value of the input voltage affects the low-frequency output voltage ripple and current ripple slightly.
(3) With the low-frequency current ripple improved, not only the output voltage ripple but also the output current ripple is reduced.

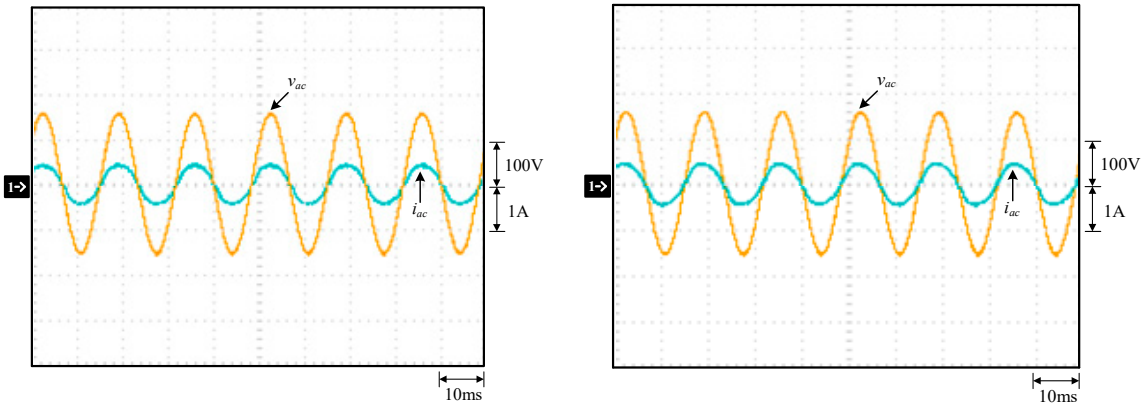
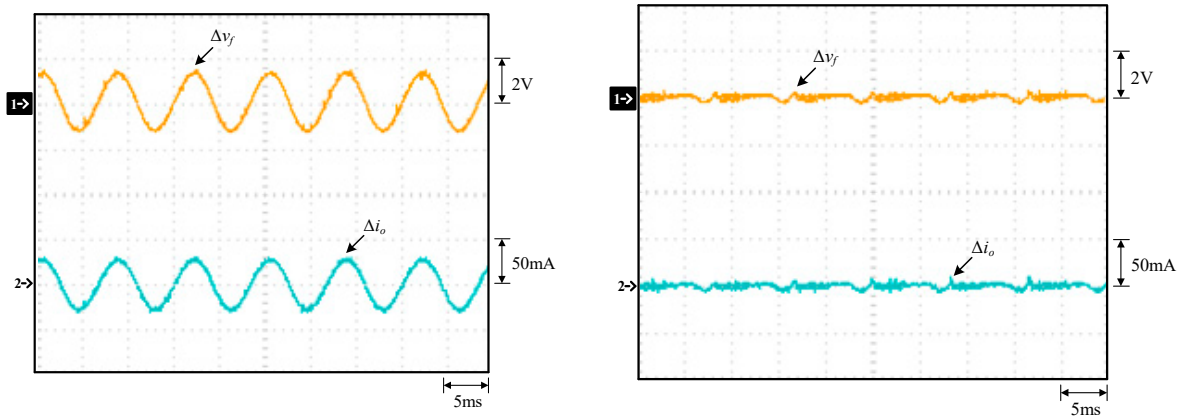
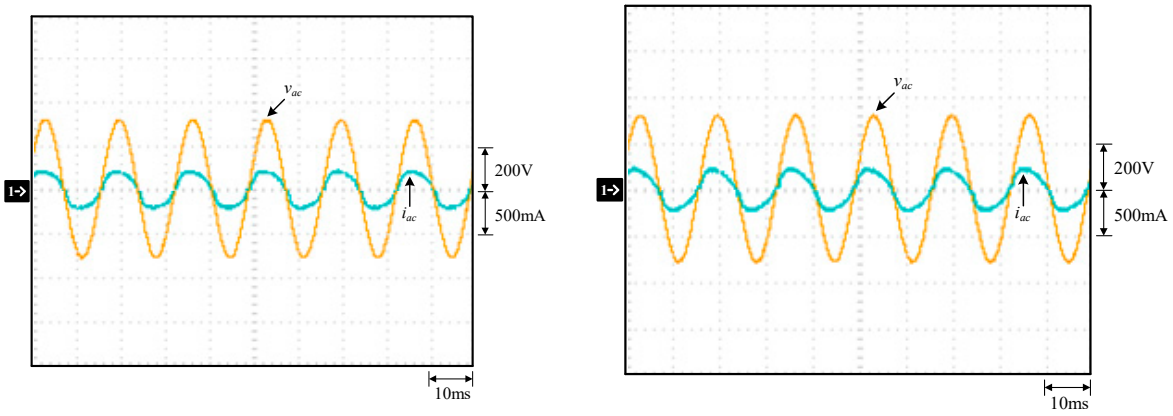


Figure 7. Waveforms under 110 V input voltage and 100% output load: (**a**) without; (**b**) with the proposed low-frequency current ripple improved: (1) v_{ac}; (2) i_{ac}.



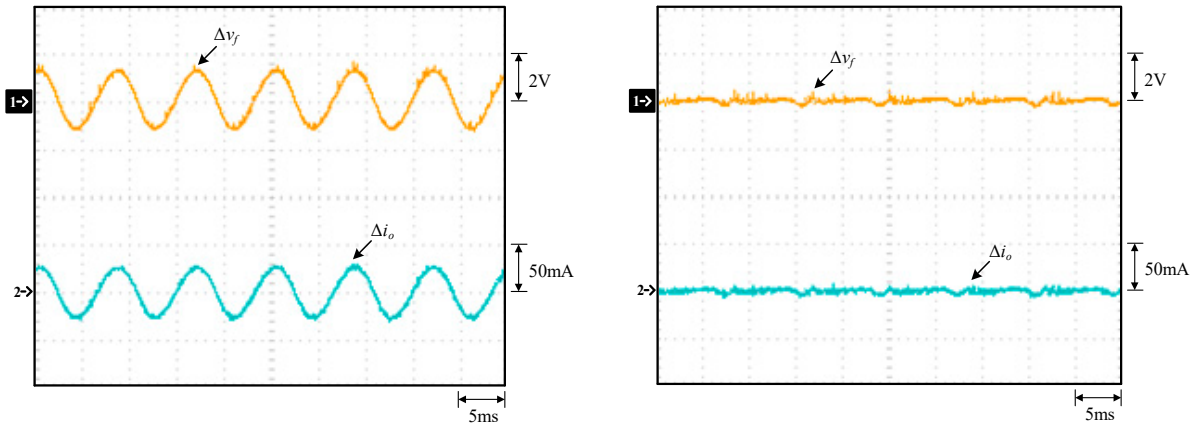
(**a**) (**b**)

Figure 8. Waveforms under 110 V input voltage and 100% output load: (**a**) without; (**b**) with the proposed low-frequency current ripple improved: (1) Δv_f; (2) Δi_o.



(**a**) (**b**)

Figure 9. Waveforms under 220 V input voltage and 100% output load: (**a**) without; (**b**) with the proposed low-frequency current ripple improved: (1) v_{ac}; (2) i_{ac}.



(**a**) (**b**)

Figure 10. Waveforms under 220 V input voltage and 100% output load: (**a**) without; (**b**) with the proposed low-frequency current ripple improved: (1) Δv_f; (2) Δi_o.

5.4. Electrical Data Comparisons

Electrical data curves: In the following, the power factor, harmonic distortion, and output current ripple percentage without and with the low-frequency current ripple improved are discussed as below.

5.4.1. Efficiency Comparison

Efficiency curve: Figure 11 shows curves of efficiency versus output load without and with the low-frequency current ripple improved at the input voltage of 110 V, whereas Figure 12 shows curves of efficiency versus output load without and with the low-frequency current ripple improved at the input voltage of 220 V. From these two figures, the efficiency with a low-frequency current ripple improved is lower than that without a low-frequency current ripple improved by 1.2%. From these two figures, the efficiency at 100% output load with the current ripple improved is 86.3% at the input voltage of 110 V, whereas the efficiency at 100% output load with the low-frequency current ripple improved is 89.2% at the input voltage of 220 V.

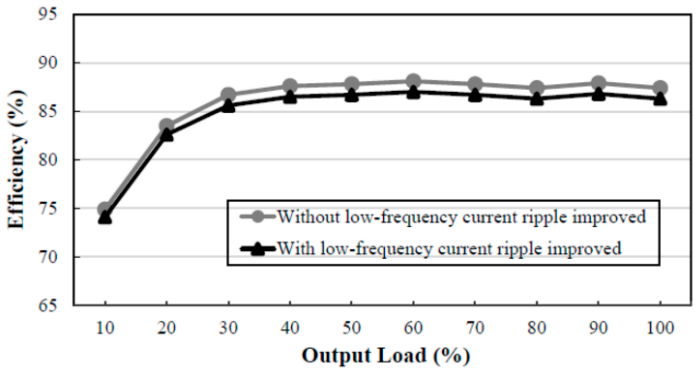


Figure 11. Curve of efficiency versus output load under 110 V input voltage.

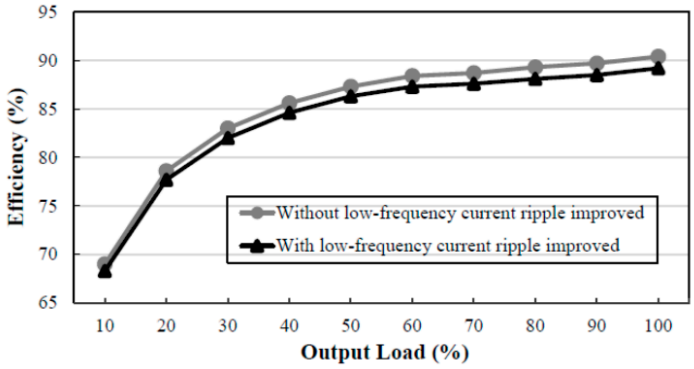


Figure 12. Curve of efficiency versus output load under 220 V input voltage.

5.4.2. Power Factor Comparison

Power factor curve: Figure 13 shows curves of the power factor versus output load without and with the low-frequency current ripple improved at the input voltage of 110 V, whereas Figure 14 shows curves of the power factor versus output load without and with the low-frequency current ripple improved at the input voltage of 220 V. From these two figures, the power factor with the low-frequency current ripple improved is almost the same as that without the low-frequency current ripple improved. From these two figures, the power factor at 50% output load with the low-frequency current ripple improved is 0.994 at the input voltage of 110 V, whereas the power factor at 50% output load with the low-frequency current ripple improved is 0.935 at the input voltage of 220 V.

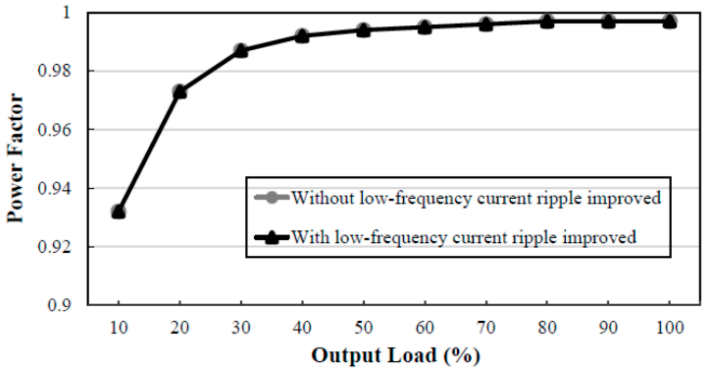


Figure 13. Curve of power factor versus output load under 110 V input voltage.

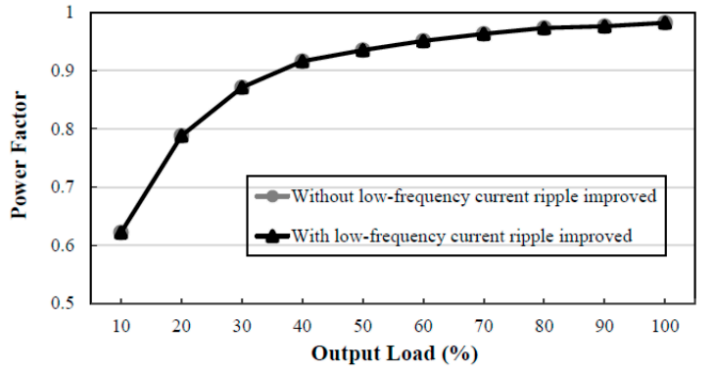


Figure 14. Curve of power factor versus output load under 220 V input voltage.

5.4.3. Total Harmonic Distortion Comparison

Figure 15 shows curves of total harmonic distortion versus output load without and with the low-frequency current ripple improved at the input voltage of 110 V, whereas Figure 16 shows the curves of total harmonic distortion versus output load without and with the low-frequency current ripple improved at the input voltage of 220 V. From these two figures, the total harmonic distortion with the low-frequency current ripple improved is slightly lower than that without the low-frequency current ripple improved. From these two figures, the total harmonic distortion at 50% output load with the low-frequency current ripple improved is 5.6% at the input voltage of 110 V, whereas the total harmonic distortion at 50% output load with the low-frequency current ripple improved is 9.4% at the input voltage of 220 V.

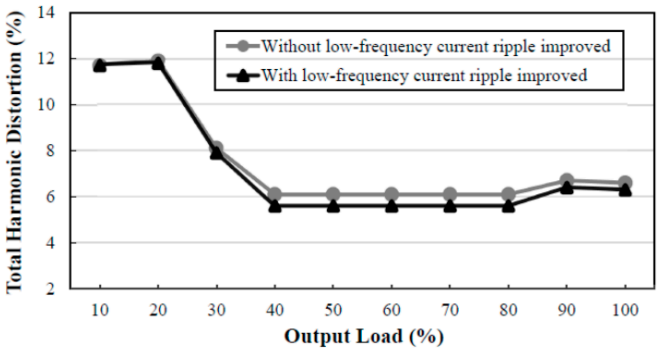


Figure 15. Curve of total harmonic distortion versus output load under 110 V input voltage.

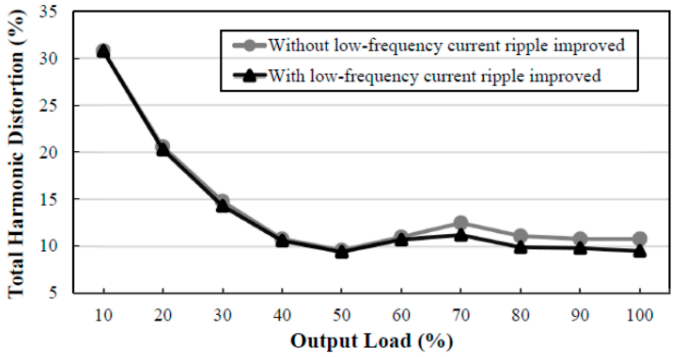


Figure 16. Curve of total harmonic distortion versus output load under 220 V input voltage.

5.4.4. Output Current Ripple Comparison

Figure 17 shows curves of output current ripple versus output load without and with the low-frequency current ripple improved at the input voltage of 110 V, whereas Figure 18 shows curves of output current ripple versus output load without and with the low-frequency current ripple improved at the input voltage of 220 V.

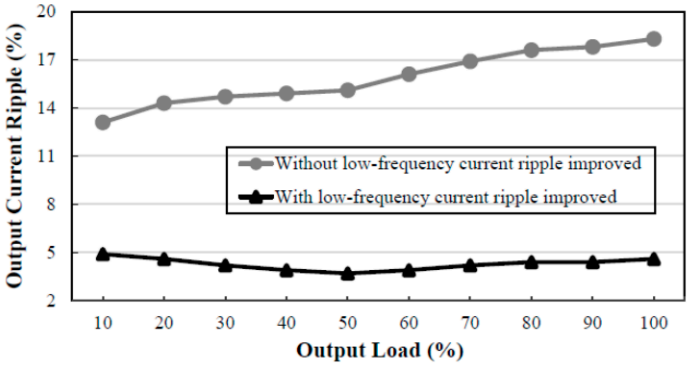


Figure 17. Curve of output current ripple versus output load under 110 V input voltage.

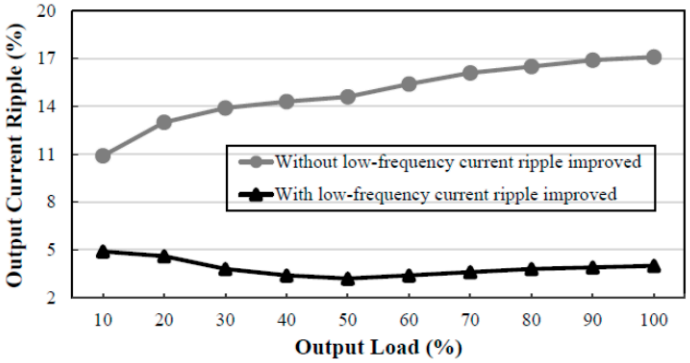


Figure 18. Curve of output current ripple versus output load under 220 V input voltage.

The output current ripple percentage, called $I_{o,ripple}\%$, is defined as

$$I_{o,ripple}\% = (\Delta i_o / I_o) \times 100\%. \quad (30)$$

From Figures 17 and 18 and Tables 4 and 5, it can be seen that with the low-frequency current ripple improved, the output current ripple at 100% output load is lower than that at 10% output load. As compared with the output current ripple percentage without a low-frequency current ripple improved, the output current ripple percentage with the low-frequency current ripple improved can

be reduced by a factor of about four at 100% output load and by a factor of about two at 10% output load. From these two figures, the maximum value of the output current ripple percentage with the low-frequency current ripple improved is 4.9%.

Table 4. Measurements of load percentage versus output current ripple percentage at input voltage of 110 V (OCR: output current ripple).

Output Load [%]	**10**	**20**	**30**	**40**	**50**	**60**	**70**	**80**	**90**	**100**
Traditional OCR [%]	13.1	14.3	14.7	14.9	15.1	16.1	16.9	17.6	17.8	18.3
Proposed OCR [%]	4.9	4.6	4.2	3.9	3.7	3.9	4.2	4.4	4.4	4.6
Improvement Traditional/Proposed	2.7	3.1	3.5	3.9	4.1	4.1	4.1	4.0	4.0	4.0

Table 5. Measurements of load percentage versus output current ripple percentage at input voltage of 220 V.

Output Load [%]	**10**	**20**	**30**	**40**	**50**	**60**	**70**	**80**	**90**	**100**
Traditional OCR [%]	10.9	13.0	13.9	14.3	14.6	15.4	16.1	16.5	16.9	17.1
Proposed OCR [%]	4.9	4.6	3.8	3.4	3.2	3.4	3.6	3.8	3.9	4.0
Improvement Traditional/Proposed	2.2	2.9	3.7	4.2	4.6	4.5	4.5	4.3	4.4	4.3

6. Comparison

Since the proposed circuit belongs to the step-down circuit, we choose the circuit shown in [5] as a comparison. This circuit is constructed by flyback and buck converters. Since there is no show of THD in [5], the comparison items include the power factor, efficiency, and current ripple percentage. From Table 6, we can see that the proposed converter has better performance than the circuit in [5].

Table 6. Comparison between [5] and the proposed.

Comparison Items	**Power Factor**		**Efficiency**		**Current Ripple Percentage**	
Input voltage	110 V	220 V	110 V	220 V	110 V	220 V
[5]	0.99	0.96	83.8%	85.5%	<10%	<10%
Proposed	0.99	0.98	86.3%	89.2%	<5%	<5%

7. Conclusions

In this paper, applying the low-frequency current ripple reduction based on the linear current regulator to the AC-DC flyback LED driver is presented so that LED flickering can be improved. At the same time, adjusting the value of the variable resistor can achieve LED dimming. Furthermore, the output voltage of the flyback converter can be automatically regulated so that the power dissipation in the BJT will be only linearly proportional to the LED current. The results of the comparison between the proposed and the compared are described as following:

(1) The performance on PF between the two is almost the same.
(2) The performance on THD between the two is slightly different.
(3) The maximum difference in efficiency between the compared and the proposed is around 1.2%.
(4) The maximum difference in output current ripple percentage between the compared and the proposed is around 14%.

Author Contributions: Conceptualization, Y.-T.Y.; methodology, K.-I.H.; software, K.-J.L.; validation, Y.-T.Y.; formal analysis, Y.-T.Y.; investigation, K.-J.L.; resources, K.-I.H.; data curation, K.-J.L.; writing—original draft preparation, K.-I.H.; writing—review and editing, K.-I.H.; visualization, K.-J.L.; supervision, K.-I.H.; project administration, Y.-T.Y.; funding acquisition, K.-I.H. All authors have read and agreed to the published version of the manuscript.

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Conflicts of Interest: The authors declare no conflict of interest.

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