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Scaling-Factor and Design Guidelines for Shielded-Capacitive Power Transfer

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Abstract: This paper introduces scaling-factor and design guidelines for shielded-capacitive power transfer (shielded-CPT) systems, offering a simplified design process, coupling-structure optimization, and consideration of safety. A novel scaling-factor-analysis method is proposed by determining the configuration of the coupling structure that improves system safety and increases operating efficiency while minimizing the gap between the shield and the coupler plate. The inductor-series resistance is also analyzed to study the loss efficiency in the shielded-CPT system. The relationship among the shield-coupler gap, distance between the couplers, conductive-plate size, and delivered power is examined and presented. The proposed method is validated by implementing the shielded-CPT system with hardware and the result suggests that the proposed method can be used to design shielded-CPT systems with scaling-factor and safety considerations.

Keywords: capacitive wireless power transfer; wireless power transmission; electric field; shielded-capacitive power transfer; design guidelines

1. Introduction

Capacitive power transfer (CPT) is an alternative approach to wireless power transfer (WPT). Rather than using a magnetic field, CPT uses a quasi-static electric field (EF) to deliver power from the primary side to the secondary side through a capacitor formed by electrodes belonging to physically separate devices [1–3]. Murata Electronics Europe adopted this method, and it has become popular because of good galvanic isolation, low cost, and the potential for operation at a higher frequency rating than that of the magnetic core [4,5]. The CPT system has been widely used in previous applications, such as electric vehicle (EV) charging [6–10], drones [11–13], variable message displays [14], and others. Previous research on low-power [11,15] and high-power [16] applications of CPT has been conducted with a reported efficiency of more than 90%. The CPT system offers advantages in lightweight, contactless, and electromagnetic interference (EMI) reduction. These advantages allow the CPT system to compromise a suitability-integrated system for available EV charging, such as in-vehicle grid interaction [17,18] and the grid-tied plug-in EV charging system [19,20]. In the study by [17,19], the potential of the CPT system can be used to replace the cable between the grid-connected EV Supply Equipment (EVSE)-Plug-in EV (PEV) (EVSE-PEV) and the EV itself.

Furthermore, much research has been conducted on reducing EF emissions using techniques, such as the single-wire system [14,21,22] and the six-plate coupling-interface method [23]. In the study by [23], the coupler has a thickness of 1.9 cm and a gap of 15 cm. The efficiency of the system was reported as 91.6% when delivering power of 1.97 kW, whereas the safety range of EF emissions was >0.4 m from the coupler. However, the method of calculating the resonant and component parameters was too complex. The concept of shielded-CPT was introduced in EV charging applications [24,25], using two extra plates to cover the coupler on each side.

This paper proposes a deep analysis of scaling-factor and design guidelines to achieve a compact shielded-CPT system that meets design requirements and safety considerations. The contributions of this paper are as follows.

- A novel method for analyzing the coupling interface of a shielded-CPT system is introduced. This method allows determination of the configuration of coupling structures intended for overall improved safety and higher operating efficiency in CPT systems while being safe for human use and allowing the possibility of thinner modules.
- A design guideline is introduced for scaling and optimizing the shielded-CPT system such that requirements, specific conditions, and safety level standards are met.

2. Scaling Model and Analysis

The proposed shielded-CPT structure is constructed as a conventional CPT coupling-plate interface with two additional plates behind each side. The coupling structure builds a six-plate CPT system consisting of a power transfer part and a shielding part as seen in Figure 1. With this configuration, the circuit parameter is optimized to the required power and efficiency, the size and distance of the coupling in consideration to the safety level of air breakdown voltage and the stray of EF. By introducing the extra plates, the EF-emission characteristic was observed through field-simulation and hardware experiments [23,24]. In these studies, the six-plate CPT system shows that the EF emission has been reduced significantly compared to the four-plate systems [26].

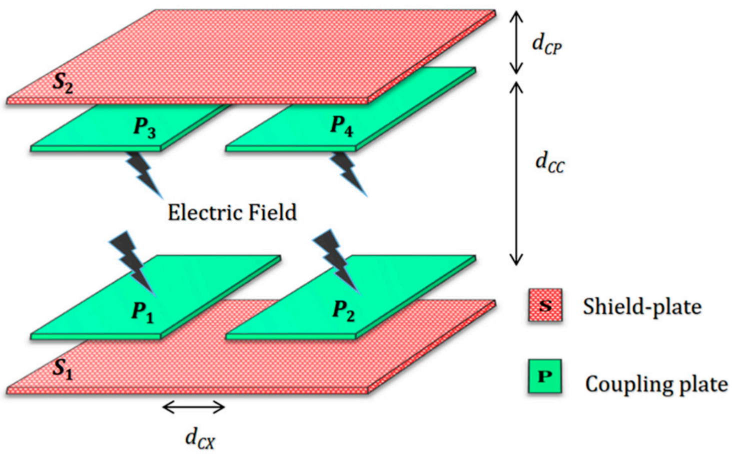


Figure 1. Structure of shielded-capacitive power transfer (CPT) coupling-interface system.

The circuit model of the complete shielded-CPT system is shown in Figure 2. Four parts of the circuit model comprise a WPT system with a capacitive coupling interface. A switch network can be implemented by a single-ended Class-E power amplifier, half-bridge, or full-bridge inverter system [27–30]. A 50 Ω coaxial cable is used in the proposed system, and a balanced-to-unbalanced (Balun) transformer is coupled to the resonant inductors, providing a balanced condition of the voltage waveform and a stable ground reference to the coupling system [31]. For simplicity of modeling, these two parts will be omitted in the scaling-factor analysis.

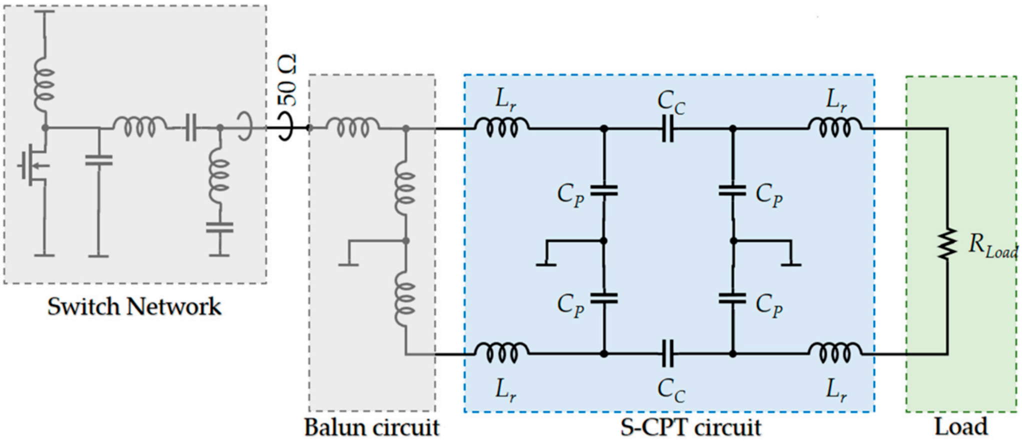


Figure 2. Circuit model of the complete shielded-CPT system.

2.1. Circuit Model Analysis of the Shielded-CPT System

Figure 3 presents the analysis of the coupling interface of the proposed shielded-CPT system. The input-voltage source, V_0, produces a sinewave alternate current (AC) voltage that is applied to the input terminal of the shielded-CPT circuit. Accordingly, the resonant frequency is tuned by the value of the series-resonant inductor, L_r, coupling capacitance, C_C, and parasitic capacitance, C_P, on the primary and secondary sides. The load resistance, R_{Load}, is connected through the resonant inductors in the secondary side. As an assumption, the circuit topology involves of symmetry parameters for both placement and size.

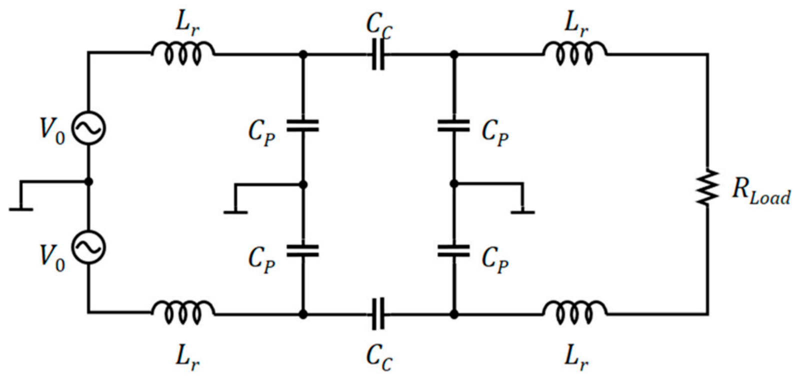


Figure 3. Circuit model for S-CPT-coupling-capacitance analysis.

The shielded-CPT circuit can be analyzed through three approximations. First, the primary (transmitter)-side impedance can be calculated under the assumption that all components on the primary side are modeled by a single parallel resistance, R_L, if a resonant condition occurs between them. Next, the secondary (receiver)-side impedance was assumed to be in a resonant condition with the receiver side; thus, the circuit is modeled by a single parallel resistance, R_L. The last approximation is a combination of the previous two, namely, the primary and secondary impedances match. Secondary-side-impedance-matched analysis is used for this paper. Figure 4 illustrates the simplified circuit model for the process of analyzing the coupling capacitance, C_C. It consists of a single input-voltage source, V_0, with frequency f, connected to the series-resonant inductor, L, with equivalent series resistance (ESR), R_S. The circuit is coupled with the parasitic capacitance, C_P, in parallel with the coupling capacitance, C_C. here we assume that the secondary side has a resonant condition. The load resistance R_{Load} and the L-matching circuit can be simplified as the load, R_L.

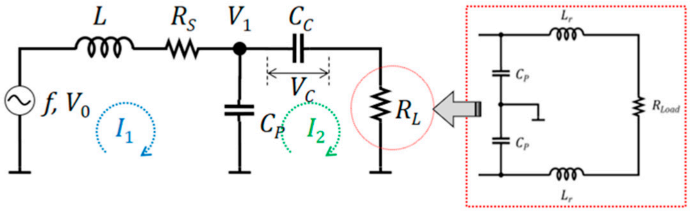


Figure 4. Simplified circuit model for system analysis.

Using the circuit diagram in Figure 4, Equation (1) is obtained based on the sinusoidal approximation for the I_1 current loop with angular frequency, ω, using Kirchhoff laws (KCL):

$$V_0 = (j\omega L + R_S)I_1 + \frac{1}{j\omega C_p}(I_1 - I_2) \tag{1}$$

In addition, applying KCL to the I_2 loop yields the relationship:

$$0 = -\frac{1}{j\omega C_p}I_1 + \left(\frac{1}{j\omega C_p} + \frac{1}{j\omega C_C} + R_L'\right)I_2 \tag{2}$$

From (1) and (2), I_2 is

$$I_2 = \frac{j\omega C_C}{\left\{1 - \omega^2\left(LC_C + LC_p + C_C C_p R_S R_L\right)\right\} + j\omega\left(C_C R_L - \omega^2 L C_C C_p R_L + C_C R_S + C_p R_S\right)} V_0 \tag{3}$$

By substituting this term into (1), I_1 is

$$I_1 = \frac{\left(\frac{C_C + C_p}{C_C} + j\omega C_p R_L\right)}{\left(\frac{C_C + C_p}{C_C} R_S - \omega^2 L C_p R_L + R_L\right) + j\left\{\omega C_p R_S R_L + \omega L \frac{C_C + C_p}{C_C} - \frac{1}{\omega C_C}\right\}} V_0 \tag{4}$$

Under the resonant condition, the corresponding impedance will be purely resistive. Thus, the imaginary part of the total impedance of the circuit equals zero and the resonant inductance L of the circuit can be calculated as

$$L = \frac{C_p {R_L}^2 + \frac{C_C + C_p}{\omega^2 {C_C}^2}}{\omega^2 {C_p}^2 {R_L}^2 + \left(\frac{C_C + C_p}{C_C}\right)^2} \tag{5}$$

From Figure 3, the stress voltage V_1 across the shield plate is found as

$$V_1 = V_0 - (R_S + j\omega L)I_1 \tag{6}$$

where V_0 is the input voltage, R_S is the ESR, $j\omega L$ is the inductor reactance, and I_1 is the current. Using (4), V_1 becomes

$$V_1 = \frac{R_L - j\frac{1}{\omega C_C}}{\left(\frac{C_C + C_p}{C_C} R_S - \omega^2 L C_p R_L + R_L\right) + j\left\{\omega C_p R_S R_L + \omega L \frac{C_C + C_p}{C_C} - \frac{1}{\omega C_C}\right\}} V_0 \tag{7}$$

2.2. Optimization for Minimal Loss by Impedance Matching

The complete system topology of Figure 3 is rearranged with R_0 as the internal characteristic resistance of the power source in Figure 5. An AC-input voltage is applied to the resonant-circuit input. In this analysis, we assume that the total impedance of the coupling interface and the secondary side of the shielded-CPT are matched to $R_L{}'$. To attain a maximum power transfer, the total reflected output impedance must equal the input impedance of the circuit [32]. This relationship is shown in (8):

$$R_0 = j\omega L + \frac{R'_L}{j\omega C R'_L + 1} \tag{8}$$

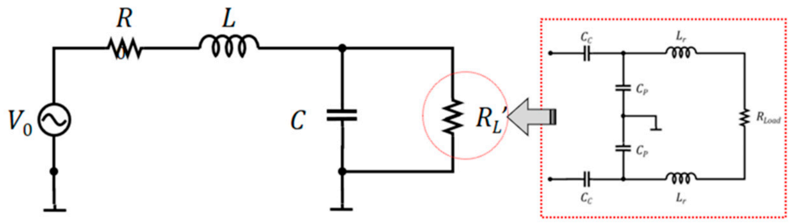


Figure 5. Circuit model for impedance analysis.

By multiplying both the numerator and the denominator by $(1 - j\omega C R_L)$, we have

$$R_0 = \frac{R'_L}{1 + \omega^2 C^2 R'^2_L} + j\omega\left(L - \frac{C R'^2_L}{1 + \omega^2 C^2 R'^2_L}\right) \tag{9}$$

The reactive part of the circuit will be cancelled when it is in the resonant condition. Thus, the matching impedance state can be acquired as

$$R_0 = \frac{R'_L}{1 + \omega^2 C^2 R'^2_L} \tag{10}$$

While the values of capacitance C and inductance L can be acquired from the quality factor Q of the components

$$C = \frac{1}{\omega R'_L}\sqrt{\frac{R'_L}{R_0} - 1} = \frac{Q}{\omega R'_L} \tag{11}$$

$$L = \frac{C R'^2_L}{1 + \omega^2 C^2 R'^2_L} = \frac{R_0 Q}{\omega} \tag{12}$$

The maximum value can be obtained using a derivative method. Therefore, the response to the load resistance R_L from (11) can be calculated by

$$\frac{dC}{dR'_L} = \frac{1}{\omega}\left(\frac{1}{R_L{}'^2}\sqrt{\frac{R_L{}'}{R_0} - 1} - \frac{1}{R'_L}\frac{1}{2R_0\sqrt{\frac{R_L{}'}{R_0} - 1}}\right) \tag{13}$$

$$\frac{dC}{dR'_L} = \frac{1}{\omega}\frac{1}{R'^2_L}\sqrt{\frac{R'_L}{R_0} - 1}\left(1 - \frac{R'_L}{2R'_L - 2R_0}\right) \tag{14}$$

$$\frac{dC}{dR'_L} = 0 \tag{15}$$

From (14) and (15), the relationship between the load resistance, $R_L{}'$, and the internal characteristic resistance, R_0, can then be obtained as

$$R'_L = 2R_0 \tag{16}$$

Thus, the optimum impedance-matching condition can be obtained when the load resistance, $R_L{}'$, is twice the internal characteristic resistance, R_0. Using the KCL method, the gain of the circuit in Figure 5 can be defined as

$$\frac{V_L}{V_0} = \frac{\frac{R'_L}{j\omega C R'_L + 1}}{R_0 + j\omega L + \frac{R'_L}{j\omega C R_L{}' + 1}} \tag{17}$$

Substituting (11) and (16) into (17), we obtain

$$\frac{V_L}{V_0} = \frac{1}{2}\frac{R'_L}{R_0 + jR_0 Q} \tag{18}$$

$$\left|\frac{V_L}{V_0}\right| = \frac{1}{2}\sqrt{\frac{R'^2_L}{{R_0}^2 + {R_0}^2 Q^2}} = \frac{1}{2}\sqrt{\frac{R'_L}{R_0}} \tag{19}$$

For analysis, the parameter of the circuit model is then defined to obtain a correlation in the capacitance, inductance, and circuit gain to the various load values. A square plate 10 cm in height and width achieves a coupling capacitance of 8.9 pF within 1 cm of the gap (see Table 1). The behaviors of the capacitance, inductance, and the circuit gain under various values of impedance are illustrated in Figures 6 and 7.

Table 1. Circuit parameters for ratio-of-resistance analysis.

Parameter	Value	Unit
e_0	8.85×10^{-14}	F/cm
l_C	10	cm
w_C	10	cm
d_C	1	cm
C	8.9×10^{-12}	F

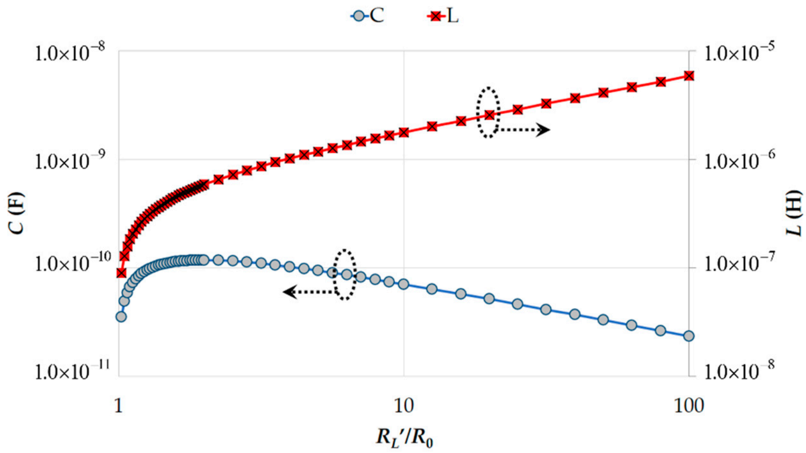


Figure 6. Capacitance and inductance behaviors under various impedance values.

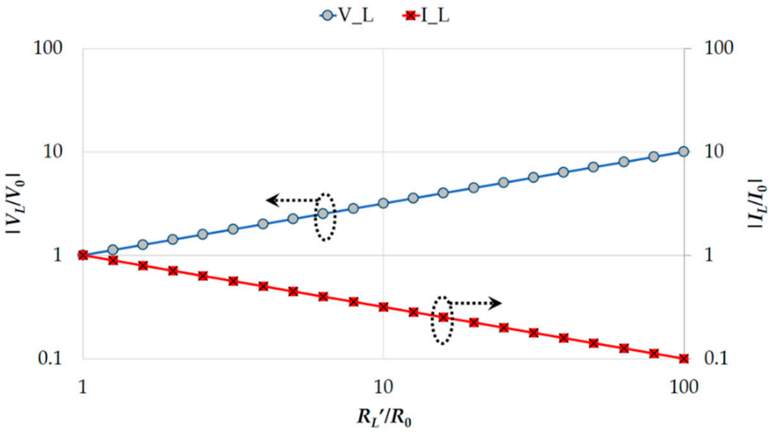


Figure 7. Voltage and current behaviors under various impedance values.

In Figure 6, the shield parasitic capacitance C_P becomes large to obtain a thin coupler unit. However, to develop a large ratio between the load resistance and the internal series resistance, R_L'/R_0, the shield capacitance C_P should be small. Thus, there is a trade-off relationship between the unit thickness and output voltage (Figure 7). With the increase of the load resistance, the load voltage, V_L, increases by a gradient of 1. By contrast, the load current decreases by gradient of −1. On the other hand, a large capacitance requires a small R_L' and the shield capacitance value is limited to 2 for R_L'/R_0. A double-*LC*-resonant-matching system (*LCLC* circuit) may solve this problem.

Figure 8 shows the relationship between the resistance ratio and power loss of the inductor. With increasing R_L', R_S rises because the inductor value increases, but I_L decreases. Thus, the loss in the inductor, P_S, decreases with increasing R_L' because P_S is given by $I_L{}^2R_S$ and the gradients in the log-log plot are roughly 1/2 and −1 for R_S and I_L, respectively. Therefore, P_S decreases with increasing R_L' with a gradient of −3/2 in log-log plot (see Figure 9).

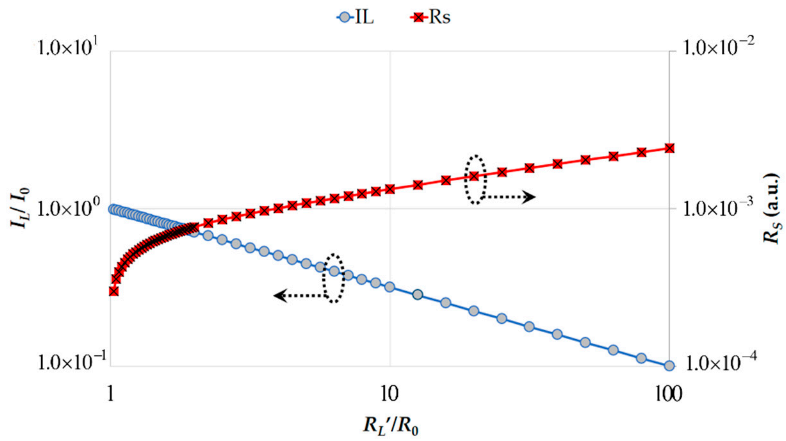


Figure 8. Current and equivalent series resistance (ESR) responses under various impedance values.

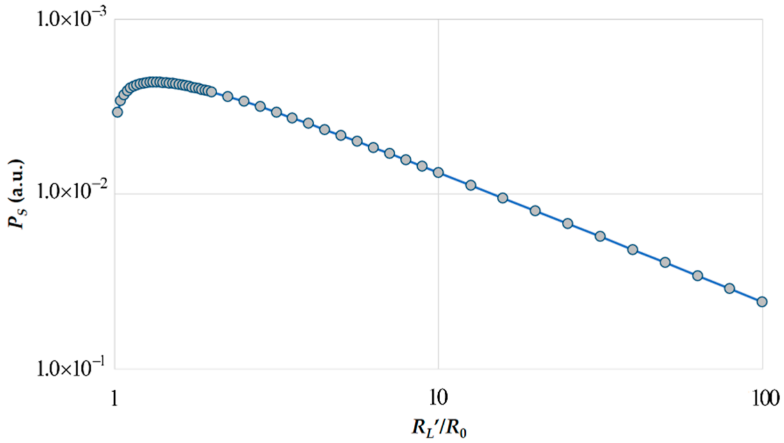


Figure 9. Power loss of the inductor under various impedance values.

2.3. Resonant Inductor Optimization for Minimal Loss

In this subsection, the ESR value of the inductor is investigated. Inductors can be constructed using many types of core materials; one is an air-core-type inductor that uses any non-magnetic material as its core to reduce core losses, i.e., eddy current & stray losses, especially when the operating frequency is very high. However, the use of a non-magnetic core also reduces inductance. Another type is a toroidal-core inductor, the core of which is made from a ferromagnetic material. The advantage of this circular core is that the magnetic field contains extremely low magnetic-flux leaks inside the core. The magnetic field at the core is higher because of a low leakage flow; hence, a toroidal-core inductor will have a higher inductance than a rod or bar-shaped core of the same material [32,33]. Figure 10 shows the dimensions and parameters of a toroidal-core inductor.

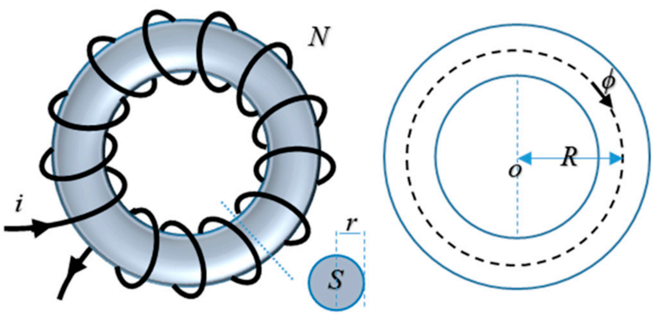


Figure 10. Inductor dimension.

The core inductance can be acquired as

$$L = \frac{N^2 \mu S}{l} = \frac{N^2 \mu \left(\pi r^2\right)}{2\pi R} = \frac{N^2 \mu r^2}{2R} \tag{20}$$

where N is the number of turns, μ is the core-material permeability, S is the core thickness, l is the wire length, R and r represent the core radius and core thickness radius, respectively. The series resistance in the inductor is

$$R_S = \frac{\rho l_w}{S_w} = \frac{\rho(2\pi r N)}{\pi(\phi/2)^2} = \frac{8\rho r N}{\phi^2} \tag{21}$$

$$L_S = \frac{N^2 \mu r^2}{2R}\left(\frac{\phi^4}{64\rho^2 r^2 N^2} {R_S}^2\right) = \frac{\mu \phi^4}{128\rho^2 R} {R_S}^2 \tag{22}$$

Thus, the series resistance R_S can be written as

$$R_S = \frac{8\rho}{\phi^2}\sqrt{\frac{2RL_S}{\mu}} \tag{23}$$

where ϕ and ρ represent the thickness and resistivity of the wire, respectively. The series inductance is

$$L_S = \frac{1}{\omega C_{2C}} \tag{24}$$

Because the current flows through an inductor, its ESR consumes some power. Figure 11 shows the circuit model used to analyze the power loss in a resonant inductor without considering parasitic capacitance, CP. An AC voltage source is connected in series with the ESR RS, the inductance L_S, the coupling capacitance C_C, and the load resistance R_L.

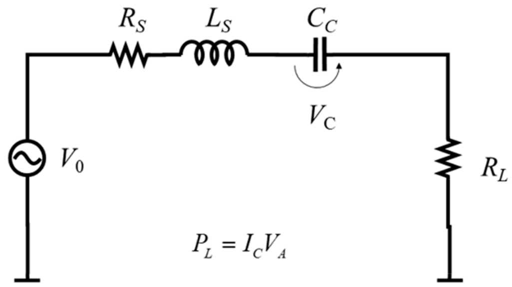


Figure 11. Circuit model for ESR-effect analysis.

The power loss of the impedance-matching inductor, P_S, is defined by

$$P_S = \frac{R_S}{R_L + R_S} P_{in} \tag{25}$$

by substituting R_S from (23) and (24) into (25), P_S can be calculated as

$$P_S = \frac{1}{\frac{\omega R_L \phi^2}{8\sqrt{2}\rho}\sqrt{\frac{C_C \mu}{R}} + 1} P_{in} \tag{26}$$

From (26), the relationship between the coupling capacitance, C_C, and the power loss of the matching inductor, P_S, is illustrated in Figure 12. Amplification of the coupling capacitance results in inductance drops. In addition, the ESR reduces and corresponds to the end product of (26), which is that the power loss decreases. However, because the distance between the couplers is fixed, the capacitance value is limited to a small number. Furthermore, the parasitic capacitance, C_P, will introduce a large value of capacitance that can affect the reduction of ESR, R_S.

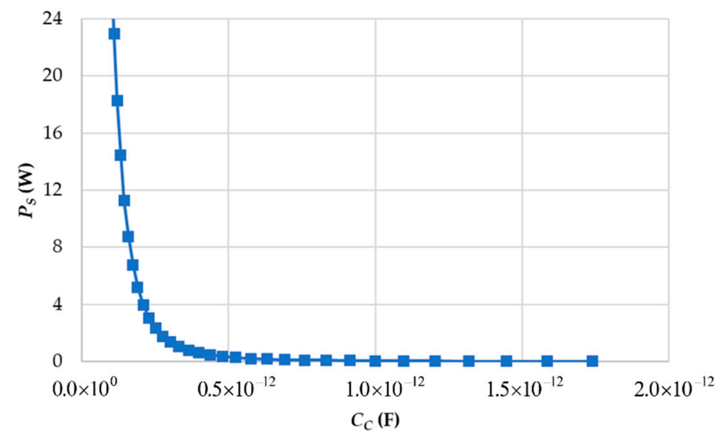


Figure 12. Inductance power loss as a function of coupling capacitance.

The effect of the parasitic capacitance, C_P, can be analyzed using (5). The increase of C_P occurs as the inductance value declines. From (23), the series inductor L_S proportionally influences the ESR, R_S, value. Its behavior is illustrated in Figure 13.

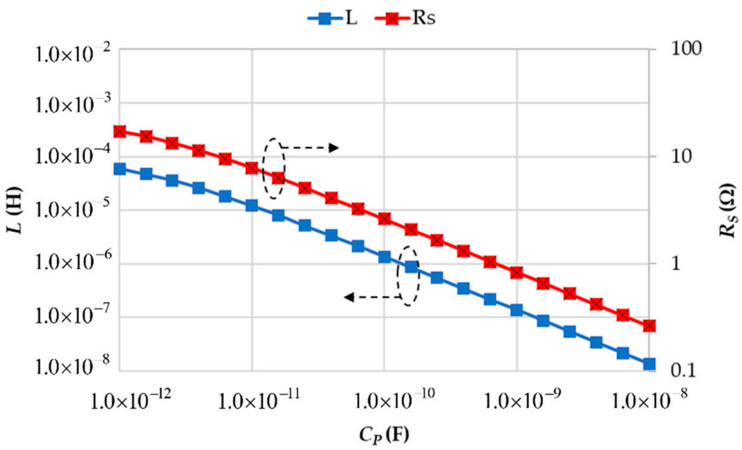
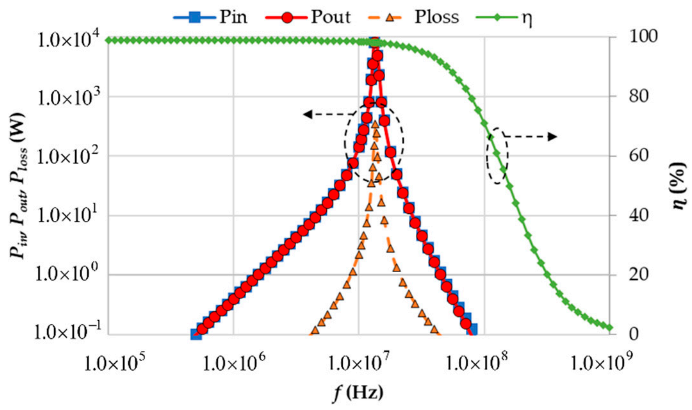


Figure 13. Series resistance of the resonant inductor with the change of the parasitic capacitance.

The relationship between power and efficiency with a frequency response is shown in Figure 14. It can be seen that, by having a lower ESR value (here below 1 Ω, see Figure 14a), less power is lost in the inductor, resulting in more power being delivered. The system may achieve an efficiency of over 95%. On the contrary, when the series resistance of the inductor is greater, it consumes some power, impacting the output power delivered to the load. From Figure 14b, the overall efficiency can be understood to drop. Thus, to minimize the loss caused by the resonant inductor, lower values of ESR result in higher efficiencies. One way to reduce ESR is by implementing a litz wire.



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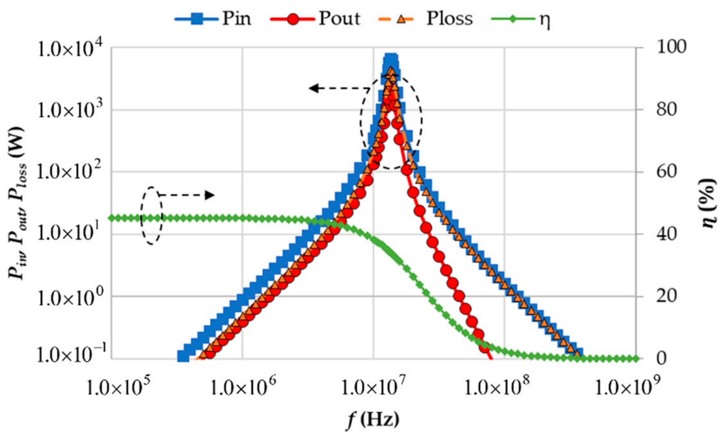


(**b**)

Figure 14. Frequency responses of power and efficiency: (**a**) Lower ESR value; (**b**) Higher ESR value.

2.4. Scaling Design for Various Loads

This subsection analyzes the behavior of power and efficiency under the variation of the load resistance. The resonant-inductance parameters used in this analysis are presented in Table 2. The ESR of the inductor, R_S, was calculated using (23). The value of inductance, L, changes due to parasitic capacitance, C_P. Furthermore, R_S depends on its value. The parameters of the circuit model for power and efficiency analysis are listed in Table 3.

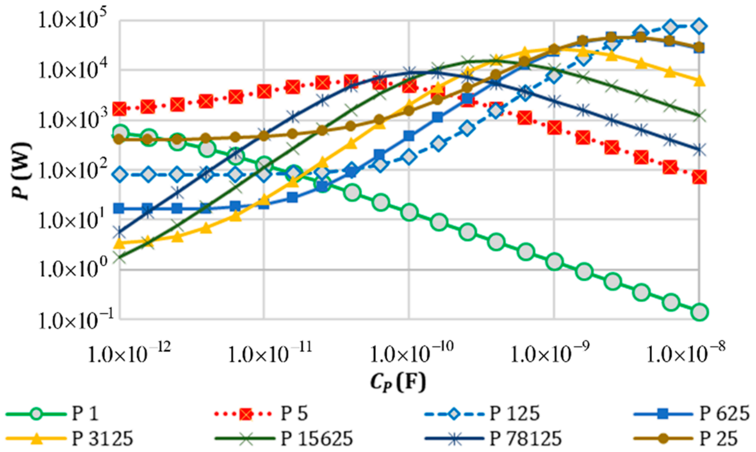
Table 2. Parameters of the inductance model for power and efficiency analysis.

Parameter	Value	Unit
ρ	1.0×10^{-2}	W·cm
ϕ	0.15	cm
R_{core}	2.5	cm
μ_o	1.26×10^{-8}	H/cm
μ_r	10×10^3	

Table 3. Parameters of circuit model for power and efficiency analysis.

Parameter	Value	Unit
C_C	1.33×10^{-12}	F
R_S	(23)	Ω
R_L	1 to 7.8×10^4	Ω
V_0	100	V
L	(5)	H
f	1.36×10^7	Hz
ω	8.5×10^7	rd/s

The behavior of the load resistance to the output power for various values of parasitic capacitance is illustrated in Figure 15a, while Figure 15b draws the load-resistance behavior to the efficiency with the shield parasitic-capacitance variations. The escalation in the load resistance R_L from 1 Ω to 125 Ω (which amplifies C_P from 1 pF to 1 nF) results in power increases. Increasing load resistance is determined to decrease power loss in the inductor.



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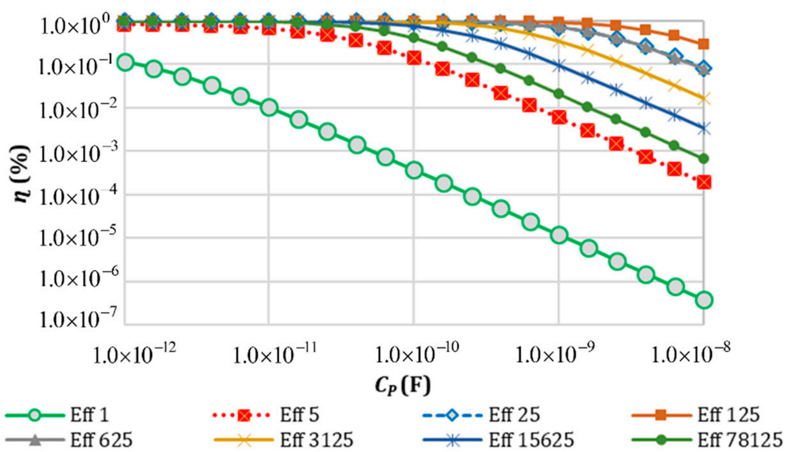

(**b**)

Figure 15. Effects of parasitic capacitance and load-resistance variations upon: (**a**) power behavior; (**b**) efficiency behavior.

2.5. Scaling Design for Various Parasitic Capacitances on the Shield-Coupler Stress Voltage

To acquire a thinner module of the shielded-CPT, the space gap between the shield plate and the coupler plate should be as short as possible. By decreasing the gap, the parasitic capacitance C_P increases. Assuming no stray capacitance on the edges of the plate, it can be estimated as

$$C_P = \frac{\varepsilon_r \varepsilon_0 S_P}{d_{SC}} \tag{27}$$

where d_{SC} and S_P are the gap distance between the shield-coupler plates and shield plate area, respectively. From (7), let us assume that C_C is much smaller than C_P; the stress voltage behavior is inversely proportional to the amount of parasitic capacitance (see (27)). While the gap is smaller, the parasitic capacitance will become greater. Here, increasing C_P will increase the stress voltage V_1. The EF value between the shield-coupler plates, E_{SC}, can be calculated as follows:

$$E_{SC} = \frac{V_1}{d_{SC}} \tag{28}$$

From (28), the EF level is amplified in proportion to the increase in stress voltage. As we know, the EF in air has a breakdown voltage E_{MAX} above 30 kV/cm [34], which is essential for system scaling. From this point, the EF strength between the shield-coupler plates should have a value under E_{MAX}. The effect of parasitic capacitance upon the stress voltage is shown in Figure 16. With decrease in d_{SC}, the capacitance C_P increases. The stress voltage over shield-coupler plates increased, which increased the EF between them proportionally.

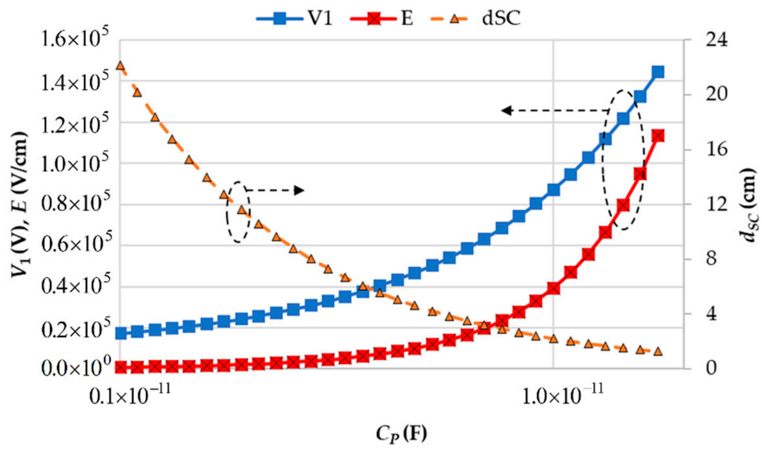

Figure 16. Stress voltage and EF level behavior over parasitic capacitance and gap variations.

3. Design Guidelines and Optimization of the Shielded-CPT System

The following example will demonstrate the design process of shielded-CPT to find optimum scaling and design values. The design step will rely upon the analytical approaches in the previous section. The scaling-factor of the shielded-CPT system will be described under the optimal condition. Several factors must be considered before the hardware is developed. A design guideline for scaling the system such that it meets constraints is shown in Figure 17. The individual unidentified-element values for this design example are L, R_S, and C_P. From (23), R_S is influenced by the L value. How L itself will vary depends on the parasitic capacitance C_P. At this point, we investigate C_P variations as describe in Section 2.5. With variation of C_P, L can be obtained using (5).

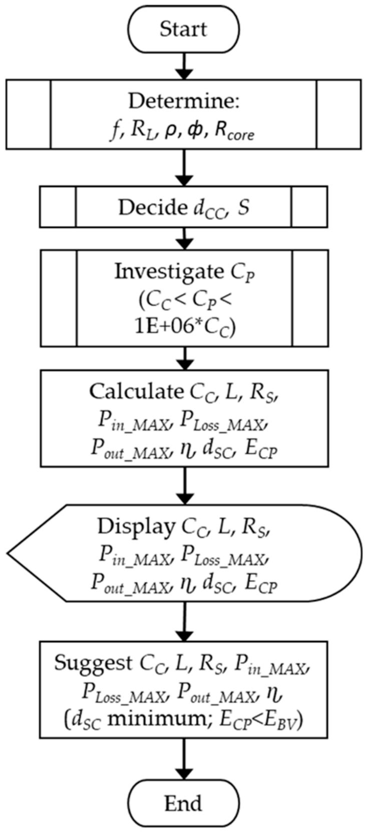

Figure 17. Design guidelines for optimizing the shielded-CPT system.

In this study, the shielded-CPT coupling interface need to transfer the power through the capacitive link at a frequency of 13.56 MHz. The frequency selection is decided by three factors. Firstly, the WPT systems for the high-power applications, requires not only to provide a high power through short-range of distance, but also a compact coupling interface that small enough to be integrated in the EV. The volume and weight of the resonant components are inversely proportional to the frequency. Thus, increasing the frequency by 10 s of MHz leads to weight lessening and power density enhancement [35]. Secondly, for the CPT system, the value of inductance is inversely proportional to the angular frequency in which the high frequency gives a low value of inductance, based on Equation (24). Thus, the inductor will become smaller for higher frequencies, offering an advantage to obtain a compact, lightweight, and small size CPT system. Thirdly, the limitation of the industrial, scientific, and medical (ISM) band for a MHz WPT. A fixed 6.78 MHz frequency as the lowest ISM band frequency is preferred. The international telecommunication union radio (ITU-R) communications sector currently recommends this single frequency on WPT for consumer devices because it has little or no negative impact on other licensed bands. A higher operating frequency in the ISM band, such as 13.56 MHz or 27.12 MHz, could further improve local freedom.

The shielded-CPT is connected to a 50 Ω resistive load. The capacitances of the coupling interface are separated by a distance of over 18 cm, which is the EV body-to-ground clearance requirement, with a plate are of 250 cm^2 corresponding to a main-coupling capacitance of approximately 1.11 pF. Let us assume that ρ= 1.0 × 10^{-4}, where ρ> ρ(Cu), ϕ= 0.15 cm, and the radius of the air core R = 2.5 cm for the resonant inductor parameter. The designated parameters are listed in Table 4.

Table 4. Parameters of the shielded-CPT system for the design example.

Parameter	Value	Unit
ρ	1.0×10^{-4}	W·cm
ϕ	0.15	Cm
R_{core}	2.5	Cm
μ_o	1.26×10^{-8}	H/cm
μ_r	1.0×10^{3}	

The exemplary design results provide several options for the shielded-CPT parameter. Figure 18 shows L and R_S as functions of C_P. The inductance decreases in value (i.e., decreases its size) as the parasitic capacitance increases. Furthermore, the resistance value decreases. To obtain a small and compact module of the shielded-CPT, increasing the capacitance to a higher value is required. Furthermore, this increases power transfer through the couplers since a larger EF occurs.

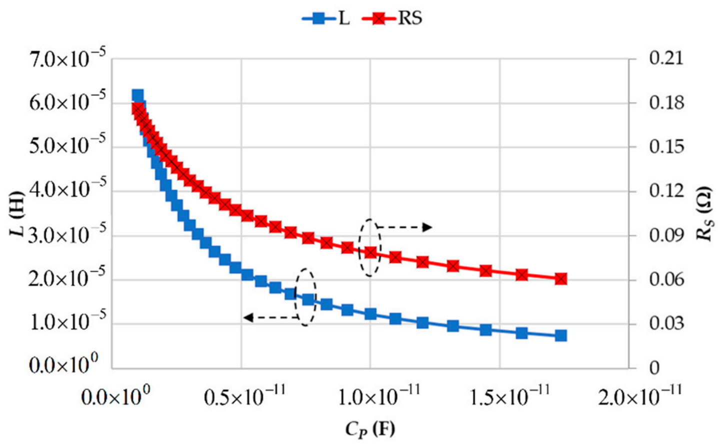

Figure 18. Inductance and series resistance characteristic for various parasitic-capacitance values.

On the contrary, more power transfer does not necessarily mean greater efficiency. Figure 19 illustrates the relationship among the parasitic capacitance to the power input, the power loss in the inductor, and the power output of the shielded-CPT. The efficiency decreases along with the gap between the plates. This occurs due to the increase in the current flowing through the primary-side components, meaning more input power is needed by the system. Thus, its efficiency is inversely proportionate to the compactness of the shielded-CPT module.

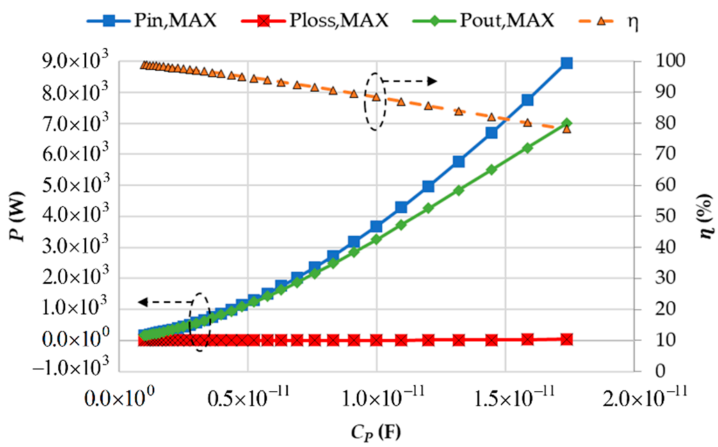

Figure 19. Power and efficiency characteristics for various parasitic-capacitance values.

The EF injected into the shield-coupler plates was limited to the breakdown voltage of air (30 kV/cm), as seen in Figure 20. In this example, at the limit point of 30 kV/cm, the parasitic-capacitance value for safety considerations must be below 2.78 pF. This condition can be obtained when the gap between the shield-coupler plates is much greater than 2.66 cm.

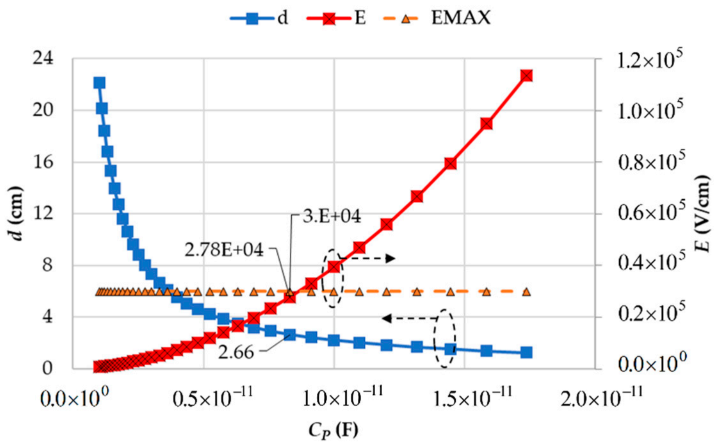

Figure 20. Gap and EF levels for various parasitic-capacitance values.

The minimum gap allowed in this design is shown in Figure 20. With a resonant frequency of 13.56 MHz and a coupler distance of 18 cm, the shielded-CPT coupling structure can be acquired for a gap of 2.92 cm, providing 7.59 pF of parasitic capacitance. 15.6 µH is needed as the total inductance works for resonance-circuit operation. For these parameters, the system is predicted to have an efficiency over 92%. The parameters of the shielded-CPT system in this example are listed in Table 5.

Table 5. Parameters of the shielded-CPT system for the design example.

Parameter	Value	Unit
d_{CC}	18	cm
d_{SC}	2.92	cm
C_C	1.11×10^{-12}	F
C_P	7.59×10^{-12}	F
R_S	0.09	Ω
R_L	50	Ω
V_0	50	V
L	1.56×10^{-5}	H
f	1.36×10^{7}	Hz

4. Hardware Implementation

The parameters obtained in the previous section are used in the hardware implementation. A single-layer PCB FR4 was used to create the coupling interface; the series-resonant inductors were fabricated manually and measured using an impedance network analyzer. The coupling interface of the shielded-CPT-system implementation is shown in Figure 21. The structure of the coupling capacitance follows the designated and optimized configuration.

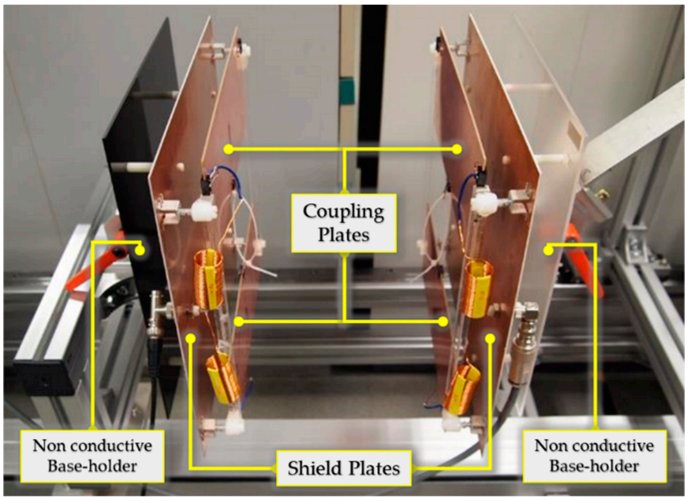

Figure 21. Hardware implementation of the shielded-CPT system.

Table 6 presents the hardware parameters of the shielded-CPT system for the design example. These were acquired from actual measurement of the system. In this implementation, the gap between the shield-coupler plates is about 3 cm. The resonant inductors are divided into four sections: upper and lower sides of the primary and secondary coupling interfaces. Some parameters exhibit differences from their calculated values due to manual production.

Table 6. Hardware parameters of the shielded-CPT system for the design example.

Parameter	Value	Unit
S_P	30.5×30.5	cm^2
S_C	10×25	cm^2
d_{CC}	18	cm
d_{CP}	3	cm
d_{CX}	10	cm
L_{t1}	7.86×10^{-6}	H
L_{t2}	7.65×10^{-6}	H
L_{r1}	8.2×10^{-6}	H
L_{r2}	7.6×10^{-6}	H

The efficiency of the coupling capacitance of the shielded-CPT system was measured using vector network analyzer. The coupling was connected to the measurement unit via a 50 Ω coaxial cable on both the transmitter and receiver sides. The measured S-parameter of the coupling is shown in Figure 22. The curve S [2,1] presents the power delivered from the transmitter to the receiver. Meanwhile, the curve S [1,1] presents the reflected power through the transmitter. At 13.56 MHz, the shielded-CPT in the hardware implementation has a delivered power above 0.86, equal to an efficiency above 86%.

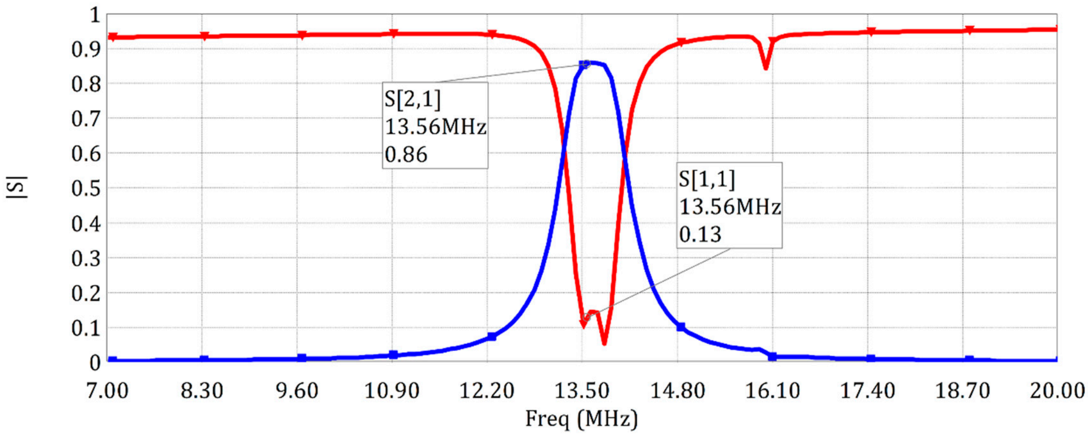

Figure 22. The gain of the hardware implementation of the shielded-CPT system.

A comparison between the design guidelines and the hardware implementation is presented in Table 7. The efficiencies of the design guidelines and the hardware implementation agree to within 93%. Since the implementation has a different parameter value, it affects the precision of the designated system.

Table 7. Comparison of results between the design guidelines and the hardware implementation.

Parameter	Value by Design	Value by Hardware	Unit	Similarity
S_P	10×25	30.5×30.5	cm^2	0.27
S_C	10×25	10×25	cm^2	1
d_{CC}	18	18	cm	1
d_{CP}	2.92	3	cm	0.98
d_{CX}	n.a.	10	cm	-
L_{t1+2}	15.6	15.5×10^{-6}	H	0.99
L_{r1+2}	15.6	15.8×10^{-6}	H	0.99
Eff	92	86	%	0.93

Figure 23 illustrates the EF emission that is analyzed using QuickField™ software. Most of the radiated EF appears between the coupling and shield plates over 20 kV/m. This condition deals with the calculated value of EF in Section 3 (Figure 20). However, the EF emission behind the shield plate is between 0 and 2 kV/m.

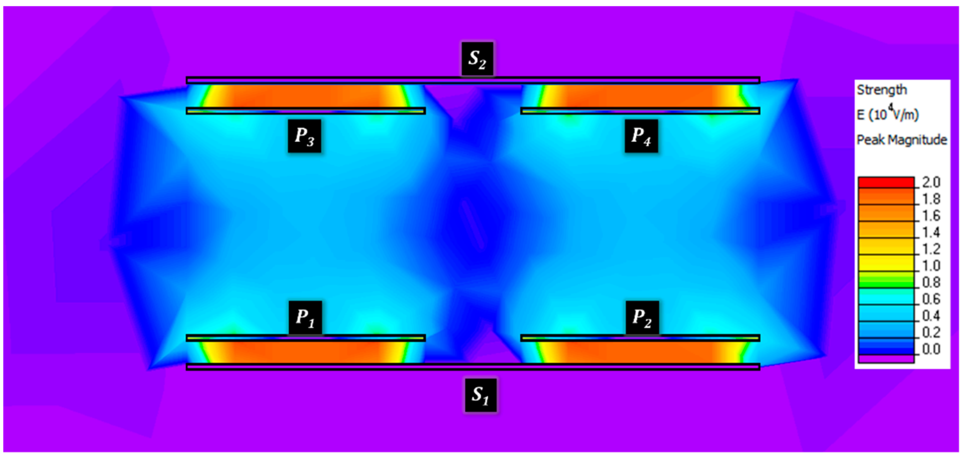

Figure 23. The EF emission of shielded-CPT system.

The highest EF denoted by red shows the value of 20 kV/m. Meanwhile, the lowest emission is shown by dark blue with an EF value between 0 and 2 kV/m. The ICNIRP guidelines and IEEE standards [36,37] mention 48.4 V/m and 60.75 V/m as the safety level of EF radiation for general public exposure limit under the operating frequency of 13.56 MHz. Figure 24 shows the EF emissions of the shielded-CPT system with a distance increase from (a) beside the coupling interface and (b) behind the shield plate. The emissions besides the coupling interface are measured over 1 kV/m. Its emissions are decreased to over 100 V/m when the distance is approximately 7.5 cm beside the coupler. Moreover, increasing the distance over 10 cm obtains a lower EF emission. However, the proposed shielded-CPT successfully reduced the emission behind the shield plate to below 10 V/m when the distance is less than 35 cm, which is reduced to below 1 V/m, meeting the ICNIRP and IEEE regulations.

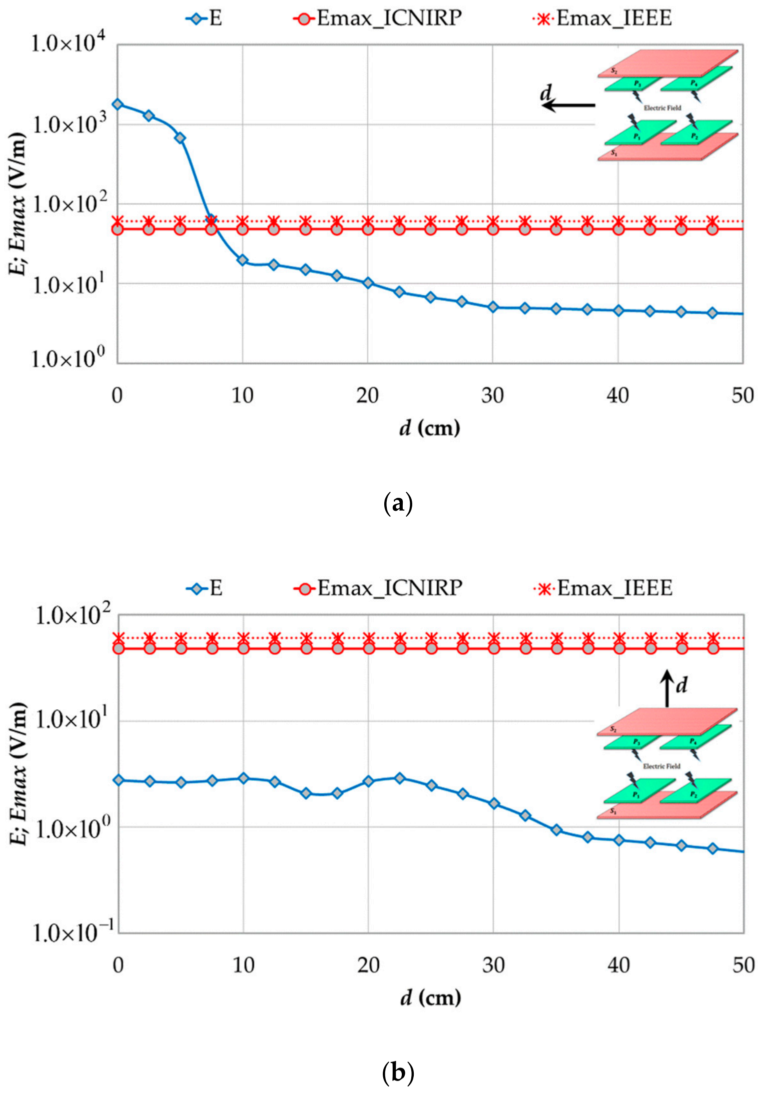

Figure 24. The EF emission of shielded-CPT system: (**a**) beside the coupling interface, (**b**) behind the shield plate.

5. Conclusions

This paper introduced scaling-factor and design guidelines for shielded-CPT. The theoretical design and analytical approach were described in detail with a simplified circuit model for analytical purposes.

From the EF and stress voltage of the shield-coupler plates, it was found that the stress voltage was proportional to the parasitic capacitance, C_P. The distance between the shield plate and coupler,

d_{SC}, needs to be minimized to obtain a thin and compact module. However, a larger C_P results in a strengthened stress voltage, which is limited to 30 kV/cm for safety considerations.

The power loss in the series inductor was investigated and found to be proportional to the inductance value. However, increasing C_P will reduce the value of L and result in low-power loss. The scaling used in the design was presented together with various load results; it was found that increasing R_L will decrease the inductor's power loss.

Process and procedure of scaling and designing the shielded-CPT was followed by analysis of the behavior of each factor, including voltage, current, power, parasitic capacitance, and system efficiency. Finally, the design guidelines for the shielded-CPT system were introduced. The design example for the hardware implementation was conducted successfully for the proposed method. It was found that, using these guidelines, an impressive hardware-parameter calculation and implementation was obtained. Thus, the proposed method can be recommended for designing shielded-CPT systems with scaling-factor and safety consideration.

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References

1. Dai, J.; Ludois, D.C. Capacitive Power Transfer through a Conformal Bumper for Electric Vehicle Charging. *IEEE J. Emerg. Sel. Top. Power Electron.* **2016**, *4*, 1015–1025. [CrossRef]
2. Huang, L.; Hu, A.P.; Swain, A.; Dai, X. Comparison of two high frequency converters for capacitive power transfer. In Proceedings of the 2014 IEEE Energy Conversion Congress and Exposition (ECCE), Pittsburgh, PA, USA, 14–18 September 2014; pp. 5437–5443.
3. Yusop, Y.; Saat, S.; Ghani, Z.; Husin, H.; Nguang, S.K. Capacitive power transfer with impedance matching network. In Proceedings of the 2016 IEEE 12th International Colloquium on Signal Processing & Its Applications (CSPA), Malacca, Malaysia, 4–6 March 2016; pp. 124–129.
4. Funato, H.; Kobayashi, H.; Kitabayashi, T. Analysis of transfer power of capacitive power transfer system. In Proceedings of the 2013 IEEE 10th International Conference on Power Electronics and Drive Systems (PEDS), Kitakyushu, Japan, 22–25 April 2013; pp. 1015–1020.
5. Lu, F.; Zhang, H.; Hofmann, H.; Mi, C. A Double-Sided LCLC Compensated Capacitive Power Transfer System for Electric Vehicle Charging. *IEEE Trans. Power Electron.* **2015**, *30*, 6011–6014. [CrossRef]
6. Li, C.; Zhao, X.; Liao, C.; Wang, L. A graphical analysis on compensation designs of large-gap CPT systems for EV charging applications. *CES Trans. Electr. Mach. Syst.* **2018**, *2*, 232–242. [CrossRef]
7. Lu, J.; Zhu, G.; Lin, D.; Zhang, Y.; Jiang, J.; Mi, C.C. Unified Load-Independent ZPA Analysis and Design in CC and CV Modes of Higher Order Resonant Circuits for WPT Systems. *IEEE Trans. Transp. Electrif.* **2019**, *5*, 977–987. [CrossRef]
8. Vu, V.B.; Dahidah, M.; Pickert, V.; Phan, V.T. An Improved LCL-L Compensation Topology for Capacitive Power Transfer in Electric Vehicle Charging. *IEEE Access* **2020**, *8*, 27757–27768. [CrossRef]
9. Regensburger, B.; Kumar, A.; Sinha, S.; Xu, J.; Afridi, K.K. High-Efficiency High-Power-Transfer-Density Capacitive Wireless Power Transfer System for Electric Vehicle Charging Utilizing Semi-Toroidal Interleaved-Foil Coupled Inductors. In Proceedings of the 2019 IEEE Applied Power Electronics Conference and Exposition (APEC), Anaheim, CA, USA, 17–21 March 2019; pp. 1533–1538.
10. Estrada, J.; Sinha, S.; Regensburger, B.; Afridi, K.; Popovic, Z. Capacitive wireless powering for electric vehicles with near-field phased arrays. In Proceedings of the 2017 47th European Microwave Conference (EuMC), Nuremberg, Germany, 10–12 October 2017; pp. 196–199.

11. Mostafa, T.M.; Muharam, A.; Hattori, R. Wireless battery charging system for drones via capacitive power transfer. In Proceedings of the 2017 IEEE PELS Workshop on Emerging Technologies: Wireless Power Transfer (WoW), Chongqing, China, 20–22 May 2017; Volume 3, pp. 1–6.
12. Park, C.; Park, J.; Shin, Y.; Huh, S.; Kim, J.; Ahn, S. Separated Circular Capacitive Couplers for Rotational Misalignment of Drones. In Proceedings of the 2019 IEEE Wireless Power Transfer Conference (WPTC), London, UK, 18–21 June 2019; pp. 635–638.
13. Vincent, D.; Huynh, P.S.; Patnaik, L.; Williamson, S.S. Prospects of Capacitive Wireless Power Transfer (C-WPT) for Unmanned Aerial Vehicles. In Proceedings of the 2018 IEEE PELS Workshop on Emerging Technologies: Wireless Power Transfer (Wow), Montréal, QC, Canada, 3–7 June 2018; pp. 1–5.
14. Zou, L.J.; Hu, A.P.; Su, Y. A single-wire capacitive power transfer system with large coupling alignment tolerance. In Proceedings of the 2017 IEEE PELS Workshop on Emerging Technologies: Wireless Power Transfer (WoW), Chongqing, China, 20–22 May 2017; pp. 93–98.
15. Theodoridis, M.P. Effective capacitive power transfer. *IEEE Trans. Power Electron.* **2012**, *27*, 4906–4913. [CrossRef]
16. Mi, C. High power capacitive power transfer for electric vehicle charging applications. In Proceedings of the 2015 6th International Conference on Power Electronics Systems and Applications (PESA), Hong Kong, China, 15–17 December 2015; pp. 1–4.
17. Cao, C.; Wang, L.; Chen, B.; Harper, J.; Bohn, T.; Dobrzynski, D.; Hardy, K. Real-Time Modeling to Enable Hardware-in-the-Loop Simulation of Plug-In Electric Vehicle-Grid Interaction. In Proceedings of the 13th ASME/IEEE International Conference on Mechatronic and Embedded Systems and Applications; American Society of Mechanical Engineers, Cleveland, OH, USA, 6–9 August 2017; Volume 9, pp. 1–10.
18. Das, H.S.; Rahman, M.M.; Li, S.; Tan, C.W. Electric vehicles standards, charging infrastructure, and impact on grid integration: A technological review. *Renew. Sustain. Energy Rev.* **2020**, *120*, 109618. [CrossRef]
19. Wang, L.; Cao, C.; Chen, B. Grid-Tied single-phase Bi-directional PEV charging/discharging control. *SAE Int. J. Passeng. Cars-Electron. Electr. Syst.* **2016**, *9*, 275–285. [CrossRef]
20. Faria, R.; Moura, P.; Delgado, J.; de Almeida, A.T. Managing the Charging of Electrical Vehicles: Impacts on the Electrical Grid and on the Environment. *IEEE Intell. Transp. Syst. Mag.* **2014**, *6*, 54–65. [CrossRef]
21. Muharam, A.; Mostafa, T.M.; Nugroho, A.; Hapid, A.; Hattori, R. A Single-Wire Method of Coupling Interface in Capacitive Power Transfer for Electric Vehicle Wireless Charging System. In Proceedings of the 2018 International Conference on Sustainable Energy Engineering and Application (ICSEEA), Tangerang, Indonesia, 1–2 November 2018; pp. 39–43.
22. Lu, F.; Zhang, H.; Mi, C. A Two-Plate Capacitive Wireless Power Transfer System for Electric Vehicle Charging Applications. *IEEE Trans. Power Electron.* **2018**, *33*, 964–969. [CrossRef]
23. Zhang, H.; Lu, F.; Hofmann, H.; Liu, W.; Mi, C.C. Six-plate capacitive coupler to reduce electric field emission in large air-gap capacitive power transfer. *IEEE Trans. Power Electron.* **2018**, *33*, 665–675. [CrossRef]
24. Muharam, A.; Masuda, M.; Hattori, R.; Hapid, A. Compactly Assembled Transmitting and Receiving Modules with Shield for Capacitive Coupling Power Transfer System. In Proceedings of the 2019 IEEE PELS Workshop on Emerging Technologies: Wireless Power Transfer (WoW), London, UK, 18–21 June 2019; pp. 257–262.
25. Masuda, M. A high electric power supply to electric cars using the electric field resonance. *Furukawa Rev.* **2018**, *49*, 23–31.
26. Zhang, H.; Lu, F.; Hofmann, H.; Liu, W.; Mi, C.C. A 4-Plate Compact Capacitive Coupler Design and LCL-Compensated Topology for Capacitive Power Transfer in Electric Vehicle Charging Applications. *IEEE Trans. Power Electron.* **2016**, *31*, 1. [CrossRef]
27. Lee, J.-B.; Baek, J.-I.; Kim, J.-K. A New Zero-Voltage Switching Half-Bridge Converter With Reduced Primary Conduction and Snubber Losses in Wide-Input-Voltage Applications. *IEEE Trans. Power Electron.* **2018**, *33*, 10419–10427. [CrossRef]
28. Arteaga, J.M.; Aldhaher, S.; Kkelis, G.; Yates, D.C.; Mitcheson, P.D. Design of a 13.56 MHz IPT system optimised for dynamic wireless charging environments. In Proceedings of the 2016 IEEE 2nd Annual Southern Power Electronics Conference (SPEC), Auckland, New Zealand, 5–8 December 2016; pp. 1–6.
29. Narayanamoorthi, R.; Vimala Juliet, A.; Bharatiraja, C.; Padmanaban, S.; Leonowicz, Z.M. Class E power amplifier design and optimization for the capacitive coupled wireless power transfer system in biomedical implants. *Energies* **2017**, *10*, 1409. [CrossRef]

30. Choi, U.-G.; Yang, J.-R. A 120 W Class-E Power Module with an Adaptive Power Combiner for a 6.78 MHz Wireless Power Transfer System. *Energies* **2018**, *11*, 2083. [CrossRef]
31. Muharam, A.; Ahmad, S.; Hattori, R.; Obara, D.; Masuda, M.; Ismail, K.; Hapid, A. An Improved Ground Stability in Shielded Capacitive Wireless Power Transfer. In Proceedings of the 2019 International Conference on Sustainable Energy Engineering and Application (ICSEEA), Tangerang, Indonesia, 23–24 October 2019; pp. 1–5.
32. Bowick, C.; Blyler, J.; Ajluni, C. *RF Circuit Design*; John Wiley & Sons, Inc.: Hoboken, NJ, USA, 2008; ISBN 9780470405758.
33. Behagi, A. Resonant Circuits and Filters. In *RF And Microwave Circuit Design: A Design Approach Using (ADS)*; Techno Search: Ladera Ranch, CA, USA, 2015; pp. 1–68. ISBN 0890069735.
34. Masuda, M.; Kusunoki, M.; Obara, D.; Nakayama, Y.; Hamada, H.; Negami, S.; Kaizuka, K. Wireless power transfer via electric coupling. *Furukawa Rev.* **2013**, *44*, 33–38.
35. Choi, J.; Tsukiyama, D.; Tsuruda, Y.; Davila, J.M.R. High-Frequency, High-Power Resonant Inverter With eGaN FET for Wireless Power Transfer. *IEEE Trans. Power Electron.* **2018**, *33*, 1890–1896. [CrossRef]
36. International Commission on Non-Ionizing Radiation Protection (ICNIRP). Guidelines for Limiting Exposure to Electromagnetic Fields (100 kHz to 300 GHz). *Health Phys.* **2020**, *118*, 483–524. [CrossRef] [PubMed]
37. IEEE Standards Coordinating Committee 39. *IEEE Standard for Safety Levels with Respect to Human Exposure to Electric, Magnetic, and Electromagnetic Fields, 0 Hz to 300 GHz*; IEEE Std C95.1-2019 (Revision IEEE Std C95.1-2005/ Inc. IEEE Std C95.1-2019/Cor 1-2019); IEEE: Piscataway, NJ, USA, 2019; pp. 1–312.