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Harmonics Compensation by Using a Multi-Modular H-Bridge-Based Multilevel Converter

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Abstract: This paper presents an active power filter based on a seven-level cascade H-bridge where the main contribution is a control strategy that combines model-based predictive control, the voltage vectors of the converter output levels, the phase shift PWM technique, and suboptimal DC-link voltage control. The proposed scheme greatly simplified the overall control system, making it well suited to compensate the current harmonics distortion at the grid side, generated by nonlinear loads connected to the point of common coupling. In addition, the proposed method achieved a balancing of the capacitor voltages of the seven-level cascade H-bridge converter by using the minimum DC-link voltage sensors. This feature significantly reduced the control system complexity and provided a low computational burden. Experimental results confirmed the feasibility and effectiveness of the proposed controller.

Keywords: harmonics compensation; multilevel converter; multimodular APF

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1. Introduction

Currently, power quality issues play an increasingly important role in AC power distribution systems due to the complex electric scenario, where different kinds of dynamic loads such as power converters, AC motor drives, and distributed energy resources (DERs) are integrated. From a practical point of view, a power quality problem can be defined as the deviation of the magnitude and frequency from the ideal sinusoidal waveform [1,2]. These power quality problems have given rise to different developments, and these problems have been addressed in the literature from complementary aspects, depending on the type of compensation. Among these mitigation techniques used for power quality issues in the distribution system, it is possible to find the custom power devices (CPDs) based on the active power filter (APF), commonly used for reactive power compensation, harmonic mitigation, and balancing of source currents [3,4]. Additional devices such as the dynamic voltage restorer (DVR) are used to compensate unbalanced voltage disturbance [5,6], and unified power quality conditioners (UPQCs) are used to compensate both voltage and current quality problems [7,8].

Moreover, in power quality applications, regardless of the implemented compensation system, the voltage source converters (VSCs) are considered a fundamental element of the compensation systems [9,10]. A conventional two-level VSC has so far been the most widely used converter in APFs; however, it creates a poor harmonic profile, leading to additional power quality and loss issues [11,12]. In recent years, the multilevel converter (more than two levels) has drawn the attention of researchers, and the literature has reported the development of APFs based on a multilevel converter injecting current at the point of common coupling (PCC) in order to achieve the desired reactive power compensation with high-quality waveforms. Regarding the multilevel converter topology, the cascade H-bridge (CHB) is currently one of the greatest topologies due to its advantages, such as

the modular converter topology (which simplifies the increase in the number of levels of the converter), and it does not require a very large number of clamping diodes or flying capacitors. Due to these advantages, the CHB APF is now considered as a very competitive topology in the new generation of reactive power compensation devices [13,14]. Commonly, the APF based on the CHB multilevel converter is designed using IGBT power electrics devices, but recently, silicon carbide (SiC) MOSFET devices have gained the focus of researchers because these devices can reach high switching frequencies, far higher that what could be achieved with a multilevel converter based on IGBTs, exhibiting higher blocking voltage, lower on state resistance, and higher thermal conductivity, enabling better efficiency [15,16]. Nevertheless, for power quality applications using an active power filter, it is not enough to integrate fast switching devices. Rather, it is necessary to address this issue together with the control algorithm [17,18].

The control strategies implemented in the APF are the PID control techniques which need a large number of variables to be measured [19], the hysteresis control, which has a high band value, producing the greater propagation of low-order harmonic distortion and a low value [20], increasing switching losses, while model-based predictive control (MPC) is a nonlinear control technique applied to power converters [21,22], having some advantages such as fast dynamic response, the ability to handle multivariable systems [23], nonlinearities, and constraints. Some disadvantages are that it depends on the model of the system, and it uses a variable switching frequency, which causes the propagation of low-order harmonics in the output current that deteriorate the performance of the system [24]. On the other hand, the MPC applied to the APF based on seven-level cascade H-bridge converters uses the switching states, which correspond to a specific voltage level, which is normally a constant reference voltage [25], but having floating capacitors such as the DC-link, by which they are charged and discharged according to the polarity of the filter current, which generates ripples in the capacitor voltages. Therefore, there is an error propagation between the measured DC-link voltages with respect to their reference value [26,27].

The main contribution of this work is the implementation of an MPC technique that combines the selection of the optimal seven-level converter output voltage vectors (VVs) together with the phase-shifted PWM (PSPWM) approach. On the other hand, the proposed control strategy combines a suboptimal solution in order to achieve the DC-link voltage balance, simplifying the control structure and the experimental test bench.

In this regard, the proposed control method optimizes the prediction model using the estimates of the DC-link voltages in combination with the iterations of the control to obtain the sign of the output voltages of each CHB, thus avoiding using a constant reference voltage. In addition, a control is added that regulates the voltages of the DC-link capacitors to the reference values, minimizing the number of DC-link voltage controllers.

The proposed control technique was tested under different operating points, considering transient and steady-state conditions. The rest of the paper is organized as follows. The next section introduces the proposed multimodular APF topology. In the same section, the three-phase seven-level CHB converter scheme is analyzed, and the mathematical model of the APF based on the three-phase seven-level converter is extracted. Subsequently, the predictive model, the DC-link voltage controller, and the modulation strategy are presented in the same section. Section 3 describes the experimental test bench. In Section 4, the experimental results are shown, in which two figures of merit are used as a reference, the current tracking and harmonics compensation. Finally, in Section 5, the conclusions of the work are given.

2. Multimodular APF Model

Figure 1 shows the control scheme applied to the multimodular APF based on the 7-level 3-phase CHB multilevel converter. Note that each cell of the CHB has an independent DC-link and four switching devices based on the SiC-MOSFET semiconductors. The 7-level 3-phase converter topology is implemented by connecting three cells in series per phase.

Then, 36 firing signals, represented by $S^{\phi}_{xy} \in \{0,1\}$, are used to control each cell, ϕ being the phase ($\phi = a$, b, or c), x the cell number in each phase ($x = 1, 2, 3$), and y the switching device in each cell (y = 1, 2, 3, or 4). Table 1 shows a combination of the firing signals taking phase "a" as an example in order to generate 7 voltage levels at the output of the 7-level converter. A similar analysis can be extended to other phases considering allowable combinations and avoiding short circuits in the DC-link of each cell.

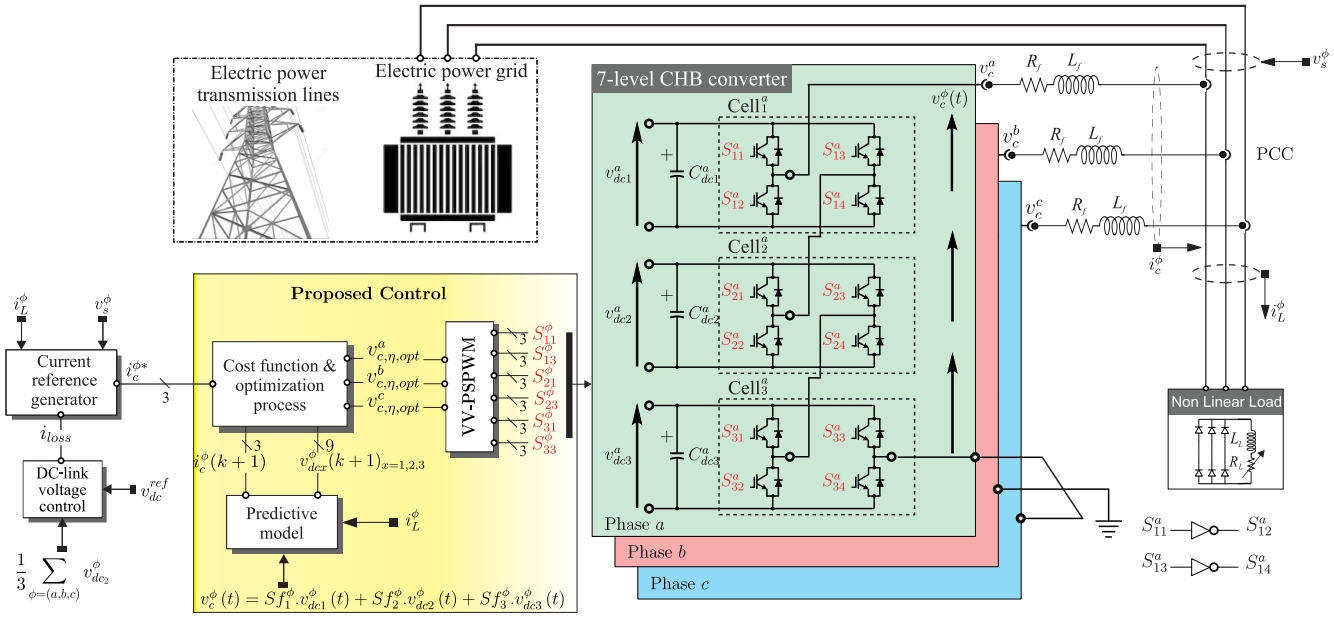

Figure 1. Proposed control scheme for the multimodular APF.

Table 1. Voltage vectors.

S^{ϕ}_{η}							
$\mathbf{Cell}^{\phi}_{1}$		$\mathbf{Cell}^{\phi}_{2}$		$\mathbf{Cell}^{\phi}_{3}$		η	$v^{\phi}_{c,\eta}$
S^{ϕ}_{11}	S^{ϕ}_{13}	S^{ϕ}_{21}	S^{ϕ}_{23}	S^{ϕ}_{31}	S^{ϕ}_{33}		
0	1	0	1	0	1	1	$-3{\cdot}v^{\phi}_{dc}$
0	1	0	1	0	0	2	$-2{\cdot}v^{\phi}_{dc}$
0	1	0	0	0	0	3	$-1{\cdot}v^{\phi}_{dc}$
0	0	0	0	0	0	4	$0{\cdot}v^{\phi}_{dc}$
1	0	0	0	0	0	5	$1{\cdot}v^{\phi}_{dc}$
1	0	1	0	0	0	6	$2{\cdot}v^{\phi}_{dc}$
1	0	1	0	1	0	7	$3{\cdot}v^{\phi}_{dc}$

To obtain an equation that describes the dynamics of the converter output voltage, the switching function of the CHB multilevel converters Sf_x is used. This is derived for each phase and H-bridge cell as:

$$Sf^{\phi}_{x} = S^{\phi}_{x1}.S^{\phi}_{x4} - S^{\phi}_{x2}.S^{\phi}_{x3} \tag{1}$$

The value of Sf^{ϕ}_{x} indicates the charging and discharging among the DC-link capacitors C^{ϕ}_{dc1}, C^{ϕ}_{dc2}, and C^{ϕ}_{dc3}. Supposing the current i^{ϕ}_{c} flows from the converter to the grid, then the capacitor C^{ϕ}_{dcx} is charging if $Sf^{\phi}_{x} = -1$, discharging if $Sf^{\phi}_{x} = 1$, and unchanged if $Sf^{\phi}_{x} = 0$. The output voltage of the multilevel converter depends on the switching function and the voltage in each of the DC-link capacitors and can be expressed as:

$$v^{\phi}_{c}(t) = Sf^{\phi}_{1}.v^{\phi}_{dc1}(t) + Sf^{\phi}_{2}.v^{\phi}_{dc2}(t) + Sf^{\phi}_{3}.v^{\phi}_{dc3}(t) \tag{2}$$

The values of v_{dc1}^{ϕ}, v_{dc2}^{ϕ}, and v_{dc3}^{ϕ} are the estimated voltages of each DC-link previously filtered. They may not be equal to their reference voltage due to the dynamics of the system.

According to Kirchhoff's law for the DC side and considering the ideal case ($R_{dc} = \infty$, where R_{dc} is a resistor that concentrates the overall losses in the DC side), the currents flowing into the electrical grid from capacitors C_{dc1}^{ϕ}, C_{dc2}^{ϕ}, and C_{dc3}^{ϕ}, whose capacitance values $C_{dcx}^{\phi} = C_{dc}$, can be expressed as:

$$i_{C_x}^{\phi}(t) = C_{dc}.\frac{d\left(v_{dc_x}^{\phi}\right)}{dt} = Sf_x^{\phi}.i_c^{\phi} \tag{3}$$

On the other hand, the proposed controller is based on the explicit APF mathematical model in order to calculate the effects of control actions over the evolution of the state variables. The dynamics of the system's model can be obtained by using Kirchhoff's circuit laws. Notice that the APF based on the CHB 7-level converter is connected at the PCC. Next, by applying Kirchhoff's laws for the AC side of the APF and using (2) and (3), assuming the currents flow from the converter to the electrical grid, the following equations in the state-space representation are obtained for each phase:

$$\begin{bmatrix} \dot{i_c^{\phi}}(t) \\ \dot{v_{dc1}^{\phi}}(t) \\ \dot{v_{dc2}^{\phi}}(t) \\ \dot{v_{dc3}^{\phi}}(t) \end{bmatrix} = \mathbb{F}.\begin{bmatrix} i_c^{\phi}(t) \\ v_{dc1}^{\phi}(t) \\ v_{dc2}^{\phi}(t) \\ v_{dc3}^{\phi}(t) \end{bmatrix} + \mathbb{G}.\begin{bmatrix} v_s^{\phi}(t) \\ 0 \\ 0 \\ 0 \end{bmatrix} \tag{4}$$

where $v_s^{\phi}(t)\ \forall\ \phi \in \{\ a, b, c\ \}$ are the grid voltages and $i_c^{\phi}(t)$ and $v_c^{\phi}(t)$ are the APF output currents and voltages, respectively. The matrices $\mathbb{F}$ and $\mathbb{G}$ are:

$$\mathbb{F} = \begin{bmatrix} -\frac{Rf}{Lf} & \frac{Sf_1^{\phi}}{Lf} & \frac{Sf_2^{\phi}}{Lf} & \frac{Sf_3^{\phi}}{Lf} \\ \frac{Sf_1^{\phi}}{C} & 0 & 0 & 0 \\ \frac{Sf_2^{\phi}}{C} & 0 & 0 & 0 \\ \frac{Sf_3^{\phi}}{C} & 0 & 0 & 0 \end{bmatrix} \tag{5}$$

$$\mathbb{G} = \begin{bmatrix} -\frac{1}{Lf} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix} \tag{6}$$

R_f being the parasitic (series) resistance of the inductive filter L_f connected between the output of the multilevel converter and the PCC.

3. Predictive Model

The predictive model can be obtained from (4) by using a forward-Euler discretization method. Euler's method is the most basic explicit method for numerical integration of ordinary differential equations and consequently carries a low computational burden, which benefits the experimental implementation [28–30]. The APF discrete-time model is given by:

$$\begin{bmatrix} \hat{i}_c^{\phi}(k+1) \\ \hat{v}_{dc1}^{\phi}(k+1) \\ \hat{v}_{dc2}^{\phi}(k+1) \\ \hat{v}_{dc3}^{\phi}(k+1) \end{bmatrix} = \mathbb{A}.\begin{bmatrix} i_c^{\phi}(k) \\ v_{dc1}^{\phi}(k) \\ v_{dc2}^{\phi}(k) \\ v_{dc3}^{\phi}(k) \end{bmatrix} + \mathbb{B}.\begin{bmatrix} v_s^{\phi}(k) \\ 0 \\ 0 \\ 0 \end{bmatrix} \tag{7}$$

where:

$$\mathbb{A} = \begin{bmatrix} \left(1 - \frac{R_f T_s}{L_f}\right) & \frac{T_s.Sf_1^{\phi}}{L_f} & \frac{T_s.Sf_2^{\phi}}{L_f} & \frac{T_s.Sf_3^{\phi}}{L_f} \\ \frac{T_s.Sf_1^{\phi}}{C} & 1 & 0 & 0 \\ \frac{T_s.Sf_2^{\phi}}{C} & 0 & 1 & 0 \\ \frac{T_s.Sf_3^{\phi}}{C} & 0 & 0 & 1 \end{bmatrix} \tag{8}$$

$$\mathbb{B} = \begin{bmatrix} -\frac{T_s}{Lf} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix} \tag{9}$$

T_s being the sampling time.

3.1. Current Reference Generation

The proposed controller requires the calculation of the reference currents in order to evaluate the cost function in (18). Figure 2 illustrates the block diagram of the current reference calculation based on synchronous reference frame (SRF) theory. As can be seen from Figure 2, the current reference generation block diagram requires the measurement of the capacitor voltages, load currents, and source voltages. The phase currents and voltages are represented in the $d-q-0$ subspace by using Park's transformation matrix:

$$\mathbb{T}_{dq} = \sqrt{\frac{2}{3}} \begin{bmatrix} \cos(\theta) & \cos(\theta - \frac{2\pi}{3}) & \cos(\theta + \frac{2\pi}{3}) \\ -\sin(\theta) & -\sin(\theta - \frac{2\pi}{3}) & -\sin(\theta - \frac{2\pi}{3}) \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \tag{10}$$

The use of a three-phase PLL is required to synchronize these signals with the source voltages. Due to the nonlinear loads, the components $d-q$ can be decomposed into two elements, one DC component $\bar{i}_{LdDC}$ associated with the 50 Hz fundamental frequency power and the other one $\tilde{i}_{Ld}$ associated with the harmonic frequencies. The currents in the d and q axes can be represented as the sum of their fundamental and harmonic components as follows:

$$\begin{aligned} i_{Ld} &= \bar{i}_{LdDC} + \tilde{i}_{Ld} \\ i_{Lq} &= \bar{i}_{Lq} + \tilde{i}_{Lq} \end{aligned} \tag{11}$$

The DC component of the current $\bar{i}_{LdDC}$ is separated using a digital second-order low-pass filter (LPF), as shown in the scheme of Figure 2. The reference currents in the time domain, based on the references i_{cd}^*, i_{cq}^*, and i_{c0}^*, are:

$$\begin{bmatrix} i_c^{\phi^*} \end{bmatrix} = [\mathbb{T}_{dq}]^{-1}. \begin{bmatrix} i_{cd}^* \\ i_{cq}^* \\ i_{c0}^* \end{bmatrix} \tag{12}$$

where:

$$i_{cd}^* = i_{Ld} - \bar{i}_{LdDC} - i_{loss} \tag{13}$$

$$i_{cq}^* = i_{Lq} \tag{14}$$

The term i_{loss} in (13) is the additional power needed to increase the average voltage across the DC-link capacitors and to balance the losses of the 7-level CHB converter associated with the switching states. This current i_{loss} is obtained by using a PI controller.

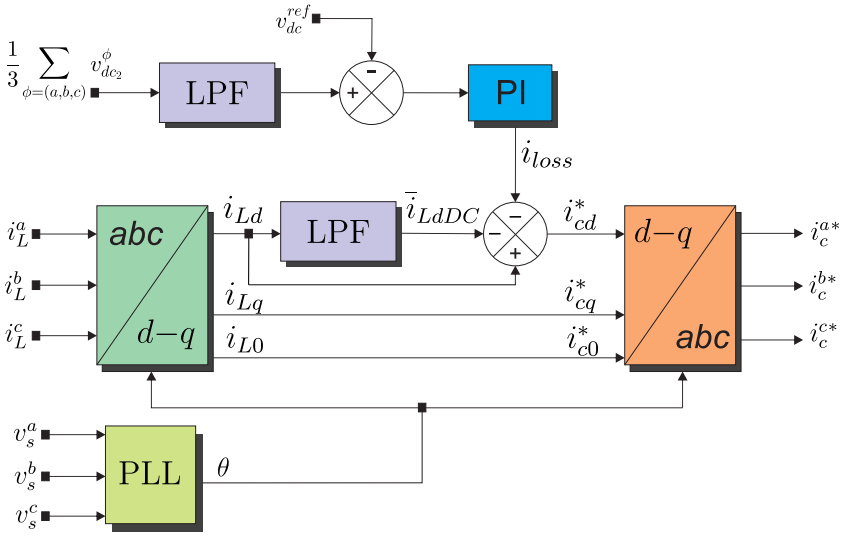

Figure 2. Current reference generation based on SRF theory including the DC-link voltage controller.

3.2. DC-Link Voltage Control

Depending on how the filter injects current into the electrical power grid, the DC-link capacitors release or absorb energy, causing a drop or increase, respectively, in the v_{dc}^{ϕ} voltage of the capacitors. On the other hand, semiconductor losses by switching and conduction also cause a reduction of the capacitor voltages. That is why a regulation system is needed that maintains the voltage levels at a certain average reference value. To regulate the average capacitor voltages to reference values in the CHB 7-level converter, a common methodology is based on the measurement of each capacitor voltage in order to evaluate the error to implement a PI controller in discrete-time [31,32]. This procedure represents an optimal solution to the capacitor voltage regulation process; however, it increases the complexity of the overall system, especially when considering the multilevel converter. A different approach is based on the modification of the cost function of predictive control, including a term that seeks to achieve the capacitor voltages' balance by applying an optimal switching function at each sampling period [33,34].

In this work, a suboptimal solution was proposed combining both approaches. The implemented DC-link voltage controller is shown in Figure 3. As can be seen from Figure 3, the voltage measurements performed made only in the middle cell. These capacitor voltages are used in the predictive model block to predict their voltage level, and an average of these measurements is used to calculate the voltage error applied to the PI control block, through an LPF. According to [35], an approximation to the proportional (kp) and integral (ki) gain values can be written as:

$$\begin{aligned} e_k^{\phi} &= v_{dc}^{ref} - v_{dc2}^{\phi} \\ i_{loss}^{\phi} &= i_{loss(k-1)} + kp.(e_k^{\phi} - e_{k-1}^{\phi}) + Tm_{pi}.ki.e_k^{\phi} \end{aligned} \tag{15}$$

$$i_{loss} = \frac{1}{3}\sum_{\phi=a,b,c} i_{loss}^{\phi} \tag{16}$$

$$\begin{aligned} k_p &= \frac{C_{dc}}{2.T_c} \\ k_i &= \frac{k_p}{2} \end{aligned} \tag{17}$$

where e_k^{ϕ} represents the error between the reference and the previously filtered measured voltages v_{dc2}^{ϕ}, then the loss current i_{loss} is calculated, $i_{loss(k-1)}$ being the loss current estimated in the previous instant, $e_{(k-1)}$ the voltage error calculated in the previous instant,

Tm_{pi} the PI controller actuation time, and finally, i_{loss}, which represents the sum of the loss currents of each phase with respect to the middle cell.

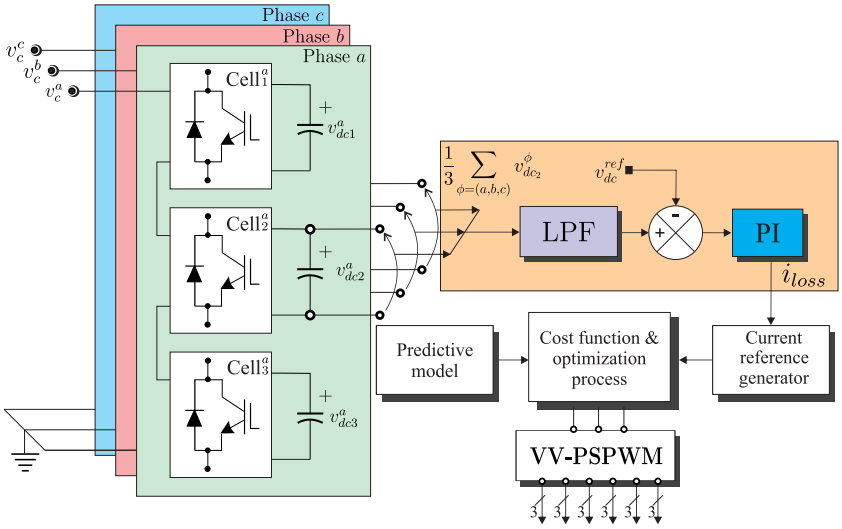

Figure 3. Block diagram of the DC-link voltage control scheme.

3.3. Cost Function and Optimization Process

The proposed controller was based on model-based predictive control to follow the current references and simultaneously achieve a balance in the capacitor voltages. The MPC was based on the optimization process in which a cost function is minimized. This cost function is defined as the difference between the reference values and the estimates obtained through the prediction model. In the three-phase control scheme, a general cost function is defined for each phase, which includes the reference current tracking error and the voltage tracking error for the capacitors, which are independently evaluated using the following equation:

$$g^{\phi} = \| \, i_c^{\phi^*} - \hat{i}_c^{\phi}(k+1) \, \|^2 + \lambda \| v_{dc}^{ref} - \hat{v}_{dc_2}^{\phi}(k+1) \|^2 \tag{18}$$

where λ is a weight factor in the optimization process.

Next, the optimization algorithm selects the optimum vector $S_{\eta,opt}^{\phi}$ for each firing signal of each cell by the evaluation and minimization of the predefined multi-objective cost function represented by (18). Algorithm 1 summarizes the optimization process.

3.4. Voltage Vectors' Phase-Shifted PWM Strategy

After selecting the optimal vector $S_{\eta,opt}^{\phi}$, which corresponds to an optimal voltage $v_{c,\eta,opt}^{\phi}$ given by (2), the classic solution is to apply this output voltage during one sampling period. However, the proposed method uses a modulation stage based on the phase-shifted pulse width modulation (PSPWM) approach. Three phase-shifted triangular carrier waves (with the same frequency and magnitude peak-to-peak) are needed to obtain the turn-on times of the firing signals of each cell. The phase-shift between the two adjacent carriers is $180^{\circ}/3$. By comparing one specific carrier wave $v_{cr,x}^{\phi}$ with a pair of inverted modulation signals v_{cont}^{ϕ} and $-v_{cont}^{\phi}$, we obtain the firing signals of s_{x1}^{ϕ} and s_{x3}^{ϕ}, as shown in Figure 4. Note that the carrier frequency is equal to the sampling frequency, and the modulation signals are normalized between -1 and 1. The modulated signals are associated with the optimal voltages as:

$$v_{cont}^{\phi} = \frac{v_{c,\eta,opt}^{\phi}}{3 v_{dc}^{ref}}. \tag{19}$$

Algorithm 1 Optimization algorithm.

Initialize $g^a_{opt} := \infty, g^b_{opt} := \infty, g^c_{opt} := \infty, \eta := 0$
Compute the APF current references (12).
while $\eta \leq 7$ **do**
  $S^{\phi}_{\eta} \leftarrow S^{\phi}_{xy}\ \forall\ x\ \&\ y = 1, 2, 3$
  Compute the output voltage of the multilevel converter (2).
  Calculate the APF prediction currents and voltage (4).
  Compute the cost function (18).
  if $g^a < g^a_{opt}$ **then**
    $g^a_{opt} \leftarrow g^a,\ S^a_{\eta,opt} \leftarrow S^a_{\eta}$
  end if
  if $g^b < g^b_{opt}$ **then**
    $g^b_{opt} \leftarrow g^b,\ S^b_{\eta,opt} \leftarrow S^b_{\eta}$
  end if
  if $g^c < g^c_{opt}$ **then**
    $g^c_{opt} \leftarrow g^c,\ S^c_{\eta,opt} \leftarrow S^c_{\eta}$
  end if
  $\eta := \eta + 1$
end while
Compute the modulation signals (19).
Obtain the turn-on times of the firing signals according to Figure 4.
Apply the firing signals.

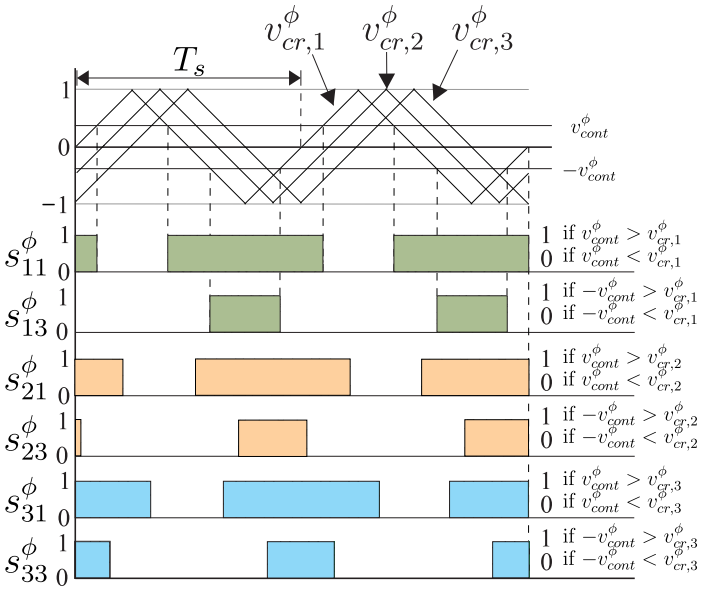

Figure 4. PSPWM waveform generation.

4. Experimental Test Bench

The multimodular APF built for experimental validation is shown in Figure 5. The test bench integrated three individual CHB cells per phase, interconnected in series. Control signals were conditioned in independent driver boards and were transmitted from the control board to the drivers by using fiber optics in order to avoid electromagnetic noises from the switching devices in the control signals. The control board was based on the dSPACE MicroLabBox multipurpose control system. The power semiconductor devices used were SiC-MOSFETs from Cree, CAS120M12BM2, with 120 A and 1200 V maximum drain–source current and drain–source voltage, respectively.

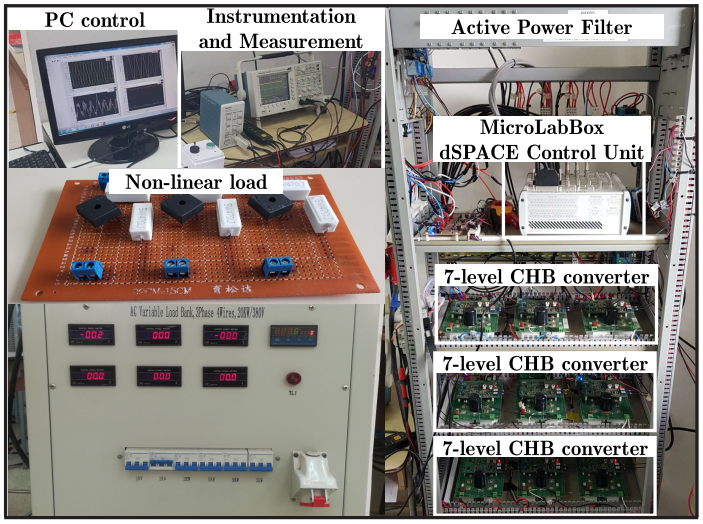

Figure 5. Experimental test bench.

In order to apply the proposed controller, analog phase voltages and currents were measured using a multimodular PCB. The analog signals were digitized by using the dSPACE MicroLabBox analog-to-digital converter (ADC) modules with 16 bit resolution. Figure 5 shows the current and voltage measurement boards designed to obtain the electrical variables necessary for the implementation of the control algorithms. The sampling frequency was 18 kHz, which was the same as the equivalent switching frequency, and the carrier frequency for PWM modulation was 1 kHz.

5. Experimental Validation

In order to verify the performance of the proposed APF, this section shows the experimental results considering v_s^{ϕ} =120 Vrms, v_{dc}^{ref} = 75 V, L_f = 10 mH. The nonlinear load was a three-phase rectifier. The DC side of the bridge rectifier was connected to an RL load with R_L = 100 Ω, 50 Ω, 25 Ω, and L_L = 114 mH, respectively. The capacitance of the DC-link in all DC cells (C_{dc}) was 20,000 µF. The defined cost function in (18) with λ = 0.02 was selected to evaluate the performance of the proposed controller, prioritizing the current tracking as the first control objective and the DC-link tracking voltage as the second objective.

5.1. Verification of the Harmonics Compensation

The harmonics compensation performance was tested by using a nonlinear load under different grid current conditions. The experimental results of the total harmonic distortion (THD) were obtained by using the data captured with the control desk software of the dSPACE MicroLabBox. Load currents (i_L), APF output currents (i_c), grid currents (i_s), as well as source voltages (v_s) and DC-link (V_{dc}) voltages were captured and analyzed. Figure 6 shows the THD level in the grid side before compensation considering three operating points R_L = 100 Ω, 50 Ω, and 25 Ω, respectively. Under these operating conditions, the THD of the currents at the grid side was 29.36%, 27.37%, and 28.33%, respectively. Once the APF was connected, the compensation process started. The output APF currents (i_c) were injected at the PCC in order to compensate the harmonics distortion at the grid side. According to the grid currents' evolution shown in Figure 6, after connecting the APF, currents at the grid side (i_s) quickly became sinusoidal. The THD level in the grid currents decreased to the values of 4.75%, 5.25%, and 6.6%, respectively, for each load impedance value. A significant improvement in terms of harmonic compensation was observed.

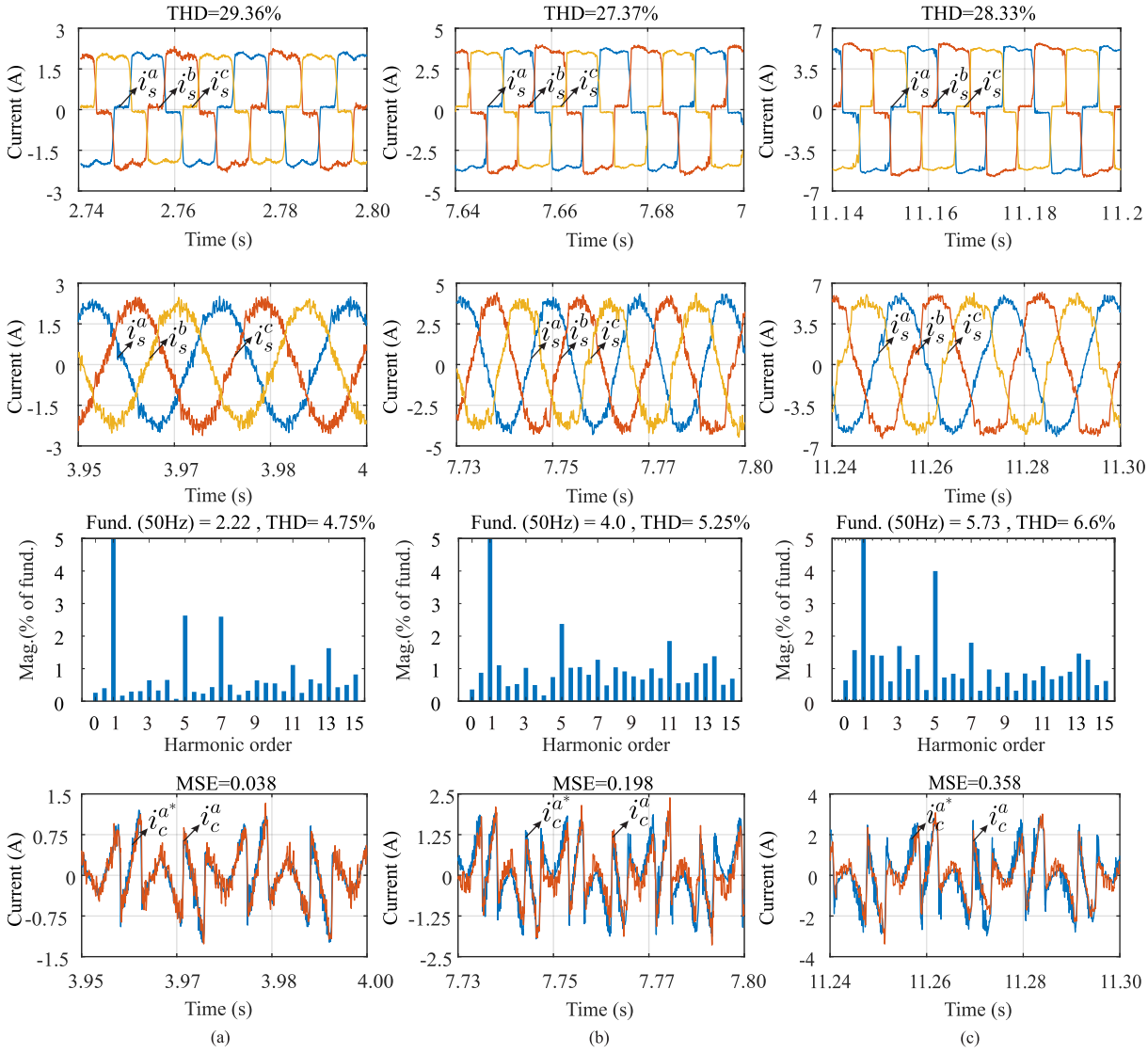

Figure 6. Experimental results of source current harmonics compensation at the grid side considering a nonlinear load and three operating points: (**a**) R_L = 100 Ω, (**b**) R_L = 50 Ω, and (**c**) R_L = 25 Ω.

To quantify the performance of the proposed MPC based on the PSPWM algorithm, the mean-squared error (MSE) between the reference currents calculated by (12) and the measured current captured by the ADC of the dSPACE MicroLabBox were used as the figure of merit. According to the results shown in Figure 6, the MSE increased as the load power increased, being able to quantify in 0.038A, 0.198A, and 0.358A, respectively. On the other hand, Figure 7a shows the source current evolution (i_s^a) at the grid side. It shows the distortions due to the high level of THD existing in the electrical grid due to the nonlinear load connected at the PCC. Once the APF was enabled, the current injection (i_c^a) at the PCC was produced by the APF in order to compensate the harmonics distortion of the source current, as shown in Figure 7b, where the CHB seven-level converter output voltage (v_c^a) is also shown. From Figure 7c, once the harmonics compensation process starts, a significant decrease can be observed in the THD level existing in the source current at the grid side (i_s^a).

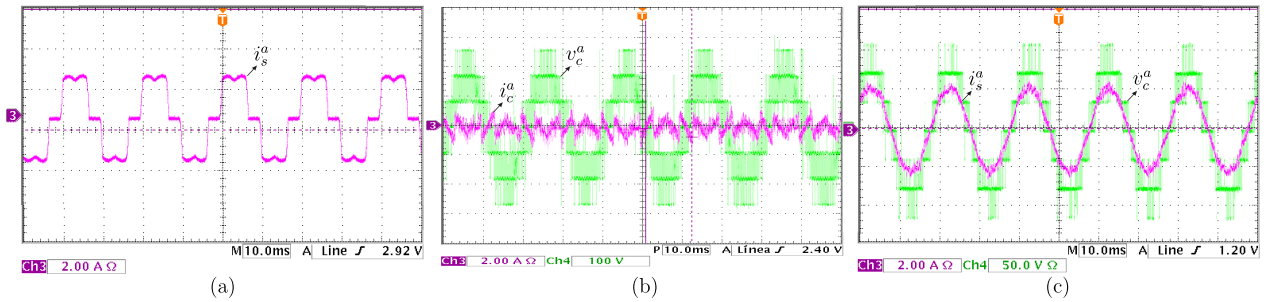

Figure 7. Steady operation of the APF (**a**) uncompensated source current, (**b**) compensated source current and filter output voltage, and (**c**) voltage and current APF output.

In order to analyze the APF behavior under dynamic conditions, a load resistance (R_L) variation from 150 Ω to 50 Ω was applied. Figure 8a presents the dynamic behavior of the APF current injection (i_c^a) at the PCC in order to produce the harmonics compensation at the grid side (i_s^a) where the measured grid current rapidly rose to the nominal value without oscillations that may affect the stability of the system. On the other hand, Figure 8b shows the dynamic behavior of the APF output voltage (v_c^a) produced by the load resistance variation. It can be seen how from the transient condition, the duty cycle of the APF output voltage was modified in order to generate a current compensation (i_c^a) with greater amplitude injected at the PCC, resulting in a compensated current at the grid side (i_s^a) with a low harmonic content, even instantaneously after the transient condition.

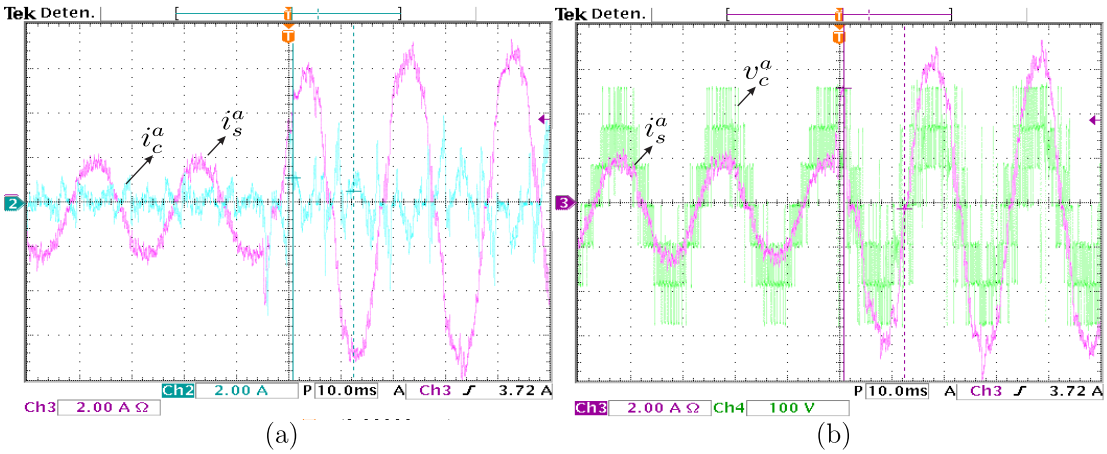

Figure 8. Transient behavior of the APF (**a**) current i_c^a and i_s^c for increased load and (**b**) current i_s^c and voltage v_c^a for instantaneous load resistance changes.

5.2. Verification of the DC-Link Voltage Control

In order to verify the effects of the DC-link voltage control under the transient condition, the APFs were intentionally disabled during the steady-state. After three seconds, the APF was suddenly connected, causing a transient in the DC-link voltages. Figure 9a shows the experimental waveforms of capacitor voltages under transient conditions. According to the experimental results, the PI control implemented on three cells was enough to achieve the stable behavior of the DC-link voltages. Once the APF was enabled, the capacitor voltages converged to their reference value. Figure 9b shows the harmonics compensation in the source current at the grid side when the APF was connected at the PCC. The experimental results demonstrated in Figures 6–9 confirmed the feasibility and effectiveness of the proposed controller.

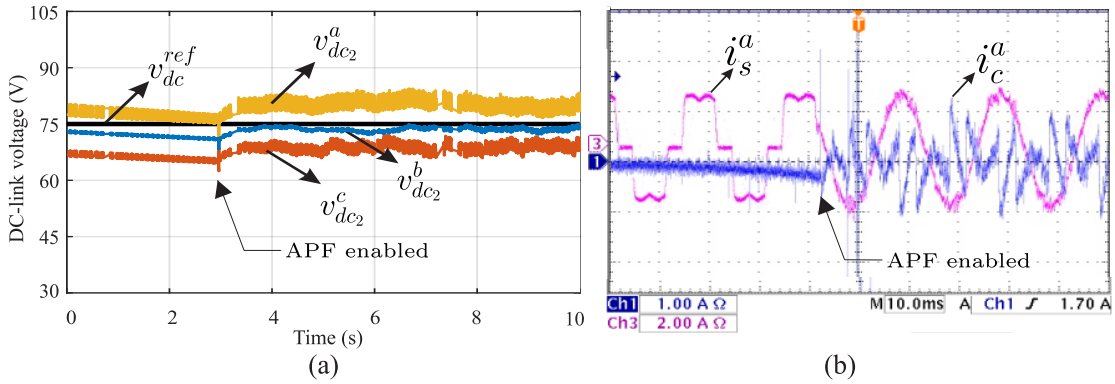

Figure 9. Transient behavior of the APF (**a**) DC-link voltage control performance and (**b**) source current harmonics compensation.

5.3. Verification of the Compensation for Unbalanced Voltages

Main currents may be unbalanced if nonlinear loads or AC source voltages are unbalanced. Figure 10a shows the measured phase voltage waveforms for the unbalanced grid voltages and nonlinear load conditions. The voltage amplitude unbalance was 20% for the experiment. Under these operating conditions, the active power filter operated properly, reducing the harmonic distortions at the grid side, as shown in Figure 10b.

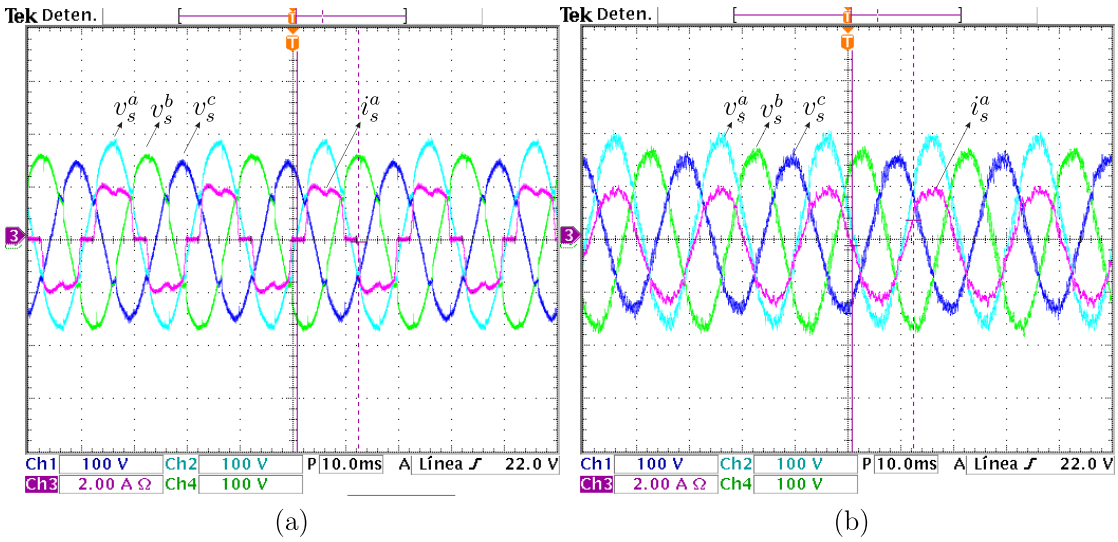

Figure 10. Unbalanced voltages (**a**) uncompensated by the source current and (**b**) compensated by the source current.

6. Conclusions

This paper presented the implementation of a multimodular H-bridge SiC-MOSFET-based APF using a simple and novel controller combining the concepts of model-based predictive control, voltage vector PSPWM, and suboptimal DC-link voltage control. The feasibility and effectiveness of the overall system was investigated and validated through experimental results. In this regard, the proposed system proved to be viable to compensate the current harmonics distortion at the grid side generated by nonlinear loads. The fifth and seventh harmonics originally present in the grid currents, with 27.30% of the THD value, were compensated after the interconnection of the APF at the PCC. The reduction of the THD of the grid currents from 27.30% to 4.75% proved the quality of the power system would be enhanced. This characteristic was evaluated under different operating points. The controller was found to be effective, and its validity was demonstrated based on the experimental results through the analysis of the MSE in the tracking reference currents obtained by the SRF theory, under both steady-state and dynamic conditions. From the

point of view of the harmonics compensation of the current at the grid side, the proposed algorithm showed a good dynamic response even under transient operating regimes and unbalanced voltages.

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Abbreviations

The following abbreviations were employed in this work:

AC	Alternating current
ADC	Analog-to-digital converter
APF	Active power filter
CHB	Cascade H-bridge
CPDs	Custom power devices
DC	Direct current
DERs	Distributed energy resources
DVR	Dynamic voltage restorer
IGBT	Isolated gate bipolar transistors
LPF	Low-pass filter
MOSFET	Metal–oxide–semiconductor field-effect transistor
MPC	Model predictive control
MSE	Mean-squared error
PCB	Printed circuit board
PCC	Predictive current control
PI	Proportional–integral
PLL	Phase-locked loop
PSPWM	Phase-shifted PWM
PWM	Pulse width modulation
SiC	Silicon carbide
SRF	Synchronous reference frame
THD	Total harmonic distortion
UPQC	Unified power quality conditioners
VSCs	Voltage source converters
VV	Voltage vectors

Nomenclature

ϕ	Phase of power grid a, b, and c
S_{xy}^{ϕ}	Firing signals
x	Corresponding cell number
y	Switching device in each cell

C	Capacitor
v_{dcx}^{ϕ}	Voltages measured in the DC-link
v_{c}^{ϕ}	Converter voltage output
$i_{C_x}^{\phi}$	Current estimation in the capacitor
i_{c}^{ϕ}	APF measured current
i_{L}^{ϕ}	Load measured current
i_{s}^{ϕ}	Power grid measured current
v_{s}^{ϕ}	Voltage measurement in the power grid
R_f	Filter resistance
L_f	Filter inductance
$\dot{i}_{c}^{\phi}(k+1)$	APF current prediction
$\dot{v}_{cx}^{\phi}(k+1)$	APF voltage prediction
T_s	Sample time
v_{dc}^{ref}	DC-link voltage reference
i_{Ld}	Active power load in synchronous frame
i_{Lq}	Reactive power load in synchronous frame
$\bar{i}_{LdDC}$	continuous component of i_{Ld}
$\tilde{i}_{Ld}$	alternating component of i_{Ld}
i_{cd*}	Active power reference in synchronous frame
i_{cq*}	Reactive power reference in synchronous frame
θ	Phase angle calculated by the PLL
i_{loss}	Estimation of the current required to charge the capacitors
T_{dq}	Transformation matrix a, b, c to $d-q$
T_{dq}^{-1}	Inverse transformation matrix $d-q$ to a, b, c
$i_{c}^{\phi^*}$	Reference current of phases a, b, and c.
e_{k}^{ϕ}	Error between the reference and measured voltages
e_{k-1}^{ϕ}	Voltage error calculated in the previous instant
i_{loss}^{a+b+c}	Sums of the loss currents of each phase
$i_{loss(k-1)}$	Loss current calculated in the previous instant
Tm_{pi}	PI controller actuation time
kp	PI proportional constant
ki	PI integral constant
$S_{\eta,opt}^{\phi}$	Optimum vector
$v_{c,\eta,opt}^{\phi}$	Optimal voltage
$v_{cr,x}^{\phi}$	Carrier wave
v_{cont}^{ϕ}	Modulation signals

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