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High-Gain High-Efficiency DC–DC Converter with Single-Core Parallel Operation Switched Inductors and Rectifier Voltage Multiplier Cell

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Abstract: This paper proposes a high step-up high-efficiency converter, comprised of an active switched coupled-inductor cell. The secondary windings are integrated into a rectifier voltage multiplier cell in a boost-flyback configuration, allowing the operation with high voltage gain with low switches duty cycle and low turn-ratios on the coupled-inductors. Both coupled-inductors are integrated into a single core due to the parallel operation of the switches. The leakage inductances of the coupled-inductors are used to mitigate the reverse recovery currents of the diodes, while regenerative clamp circuits are used to protect the switches from the voltage spikes caused by the leakage inductances. The operation of the converter is analyzed both quantitatively and qualitatively, and the achieved results are validated through experimentation of a 400 W prototype. A 97.1% CEC efficiency is also reported.

Keywords: high gain DC–DC converter; high efficiency; switched inductor; voltage multiplier cell



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1. Introduction

Currently, many applications require DC–DC low voltage (20–50 V) to high voltage (380–400 V) power conversion. In the context of sustainable energy generation, solar photovoltaic (PV) and fuel-cell (FC) are attractive alternative power sources in which power is generated at low voltage [1–4]. In electrical and hybrid vehicles, high voltage step-up is needed to convert the low voltage from the battery bank, FC or supercapacitors to the high voltage level required by the electric motors [5–7]. Other possible applications of high voltage converters are uninterruptible power supplies (UPS), high voltage light emitting diodes (LEDs), high intensity discharge (HID) lamps for vehicular headlights, among others [8–11].

The ideal boost converter can provide a high static voltage gain by operating with duty cycle near the unit. However, this generates elevated voltage stress on the semiconductor elements of the converter—which demands the use of high on-resistance semiconductors—and increases the reverse recovery current in the diodes resulting in higher losses. Moreover, the increased losses affect the static gain of the converter, resulting in decreased output voltage [12,13].

Many Switched-Inductor cell (SL)-based DC–DC converters have been proposed in the literature to achieve high voltage gain. In [2,9,14], DC–DC converters with high voltage gain were obtained by employing passive SL cells comprised of only diodes and inductors. However, this causes the main switches to suffer from high voltage stress, which demands the use of high on-resistance semiconductors. In [15,16], the Active Switched-Inductor cell (A-SL) is used, replacing the diodes with the dual active switches, which results in reduction of conduction losses due to decreased voltage stress. Moreover, as the switches

are in parallel, the current on each switch is halved, decreasing the losses. The A-SL cell can employ P-SL cells along with magnetic coupling techniques [15–18] to further increase the static voltage gain by using coupled-inductors with proper turn-ratios, without operating at extreme duty cycle values. In addition, by using high frequency switching, it is possible to employ compact magnetic cores and reduce the converter total weight and volume, making the use of magnetic coupling very attractive [1,3–5,11,15–27]. Furthermore, the magnetic element leakage inductance [28] can be used to mitigate the recovery current of the diodes.

DC–DC converters based on Voltage Multiplier Cells (VMCs)—which are arrangements of semiconductors, capacitors and inductors generally introduced after the main switch—are able to provide high voltage gain with low component count. VMCs are modular and can be cascaded or combined with other VMCs in order to improve voltage gain, add positive traits or mitigate negative characteristics of other voltage gain enhancing techniques. To further improve the voltage gain, coupled-inductors and built-in transformers can be employed simultaneously with or integrated to the VMCs [22–26,29,30]. This versatility, which allows combining the positive characteristics of different voltage lifting techniques, in addition to simple structures and ease of integration to any converter allows the use of VMCs in DC–DC converters for a multitude of applications.

Interleaved DC–DC converters are capable to achieve high voltage gain and present the beneficial features of reduced current ripples and current stress on the switches, due to the input current sharing between phases, while still maintaining good power density [25–27]. This arrangement, however, leads to an increased number of components with the same power rating of a single switch converter, as each phase of the interleaved converter operates alternately to each other.

To overcome the aforementioned disadvantages, this paper proposes a new high step-up, high efficiency VMC coupled switched-inductors based DC–DC converter. The coupled-inductors primary windings are inside an A-SL cell and the secondary windings are placed in series as the input of a rectifier VMC. The VMC output capacitors are placed in a boost-flyback configuration, which permits high voltage gain with small voltage stress across all components, allowing the use of low $R_{ds,on}$ semiconductors. Since both pairs of windings share the same operation modes, the magnetic components are integrated into a single core. Furthermore, the coupled-inductors leakage inductances are used to mitigate the diodes reverse current, further reducing conduction losses. To suppress voltage spikes on the switches, regenerative clamper circuits are used.

2. Proposed Converter Topology and Operation Analysis

The proposed converter is shown in Figure 1 and its main waveforms are shown in Figure 2, where:

- N_{p1} , N_{s1} , N_{p2} and N_{s2} are, respectively, the number of turns of the primary and the secondary windings of the first and the second coupled-inductor, where $\frac{N_{s1}}{N_{p1}} = \frac{N_{s2}}{N_{p2}} = n$;
- r_{w1} , r_{w2} are the resistances on the windings of the first and the second coupled-inductor, respectively;
- l_{lk1} , l_{lk2} are the leakage inductances of the first and the second coupled-inductor, respectively;
- L_{m1} and L_{m2} are the magnetizing inductances of the first and the second coupled-inductor, respectively;
- S_1 and S_2 are the switches;
- D_{o1} and D_{o2} are the output diodes;
- D_{cl1} and D_{cl2} are the clamper circuit diodes;
- C_{o1} , C_{o2} and C_{o3} are the output capacitors;
- C_{cl1} and C_{cl2} are the clamper circuit capacitors;
- C_{in} is the input capacitor.

Moreover, the converter operates at switching frequency f_s and duty cycle D . The converter main operation states for the continuous conduction mode (CCM) are shown in Figure 3 and described as follows:

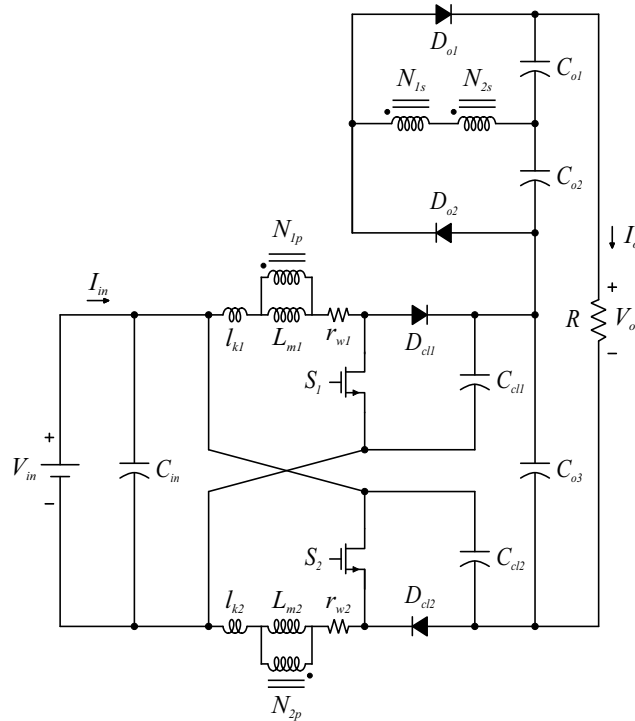


Figure 1. Equivalent circuit of the proposed converter.

2.1. State I [t₀ – t₁]

At t₀, switches S₁ and S₂ are turned on. The leakage inductances, l_{Lk1} and l_{Lk2} , are charged by capacitors C_{in} and C_{o2} , while the magnetizing inductances, L_{m1} and L_{m2} , are discharged with voltage $\frac{V_{Co2}}{2n}$. The difference between the currents on l_{Lk1} and l_{Lk2} and the current on L_{m1} and L_{m2} , respectively, flows through the primary windings of the coupled-inductors and through diode D_{o2} , decaying until it reaches zero. All the remaining diodes are reverse biased. This state ends when the leakage currents, i_{Lk1} and i_{Lk2} , become equal in value to the magnetizing currents, i_{Lm1} and i_{Lm2} . Although there is a formation of a resonant circuit between the leakage inductances, C_{in} and C_{o2} , this state is very brief as can be noted from Figure 2 and the currents on the components can be represented by a linear approximation as

$$i_{Lm1}(t) = -\frac{V_{Co2}}{2nL_{m1}}(t - t_0) + i_{Lm1}(t_0), \tag{1}$$

$$i_{Lk1}(t) = i_{S1}(t) = \frac{\left(\frac{V_{Co2}}{2n} + V_{in}\right)}{l_{Lk1}}(t - t_0) + i_{Lk1}(t_0), \tag{2}$$

$$i_{Do2}(t) = -\left[\frac{V_{in}}{nl_{Lk1}} + \frac{V_{Co2}}{2n^2}\left(\frac{1}{L_{m1}} + \frac{1}{l_{Lk1}}\right)\right](t - t_0) + \frac{i_{Lm1}(t_0)}{n} - \frac{i_{Lk1}(t_0)}{n}. \tag{3}$$

Due to the circuit symmetry, all equations pertaining to the first pair of windings are also valid for the second pair of windings. The equivalent circuit of the converter during this state is shown in Figure 3a.

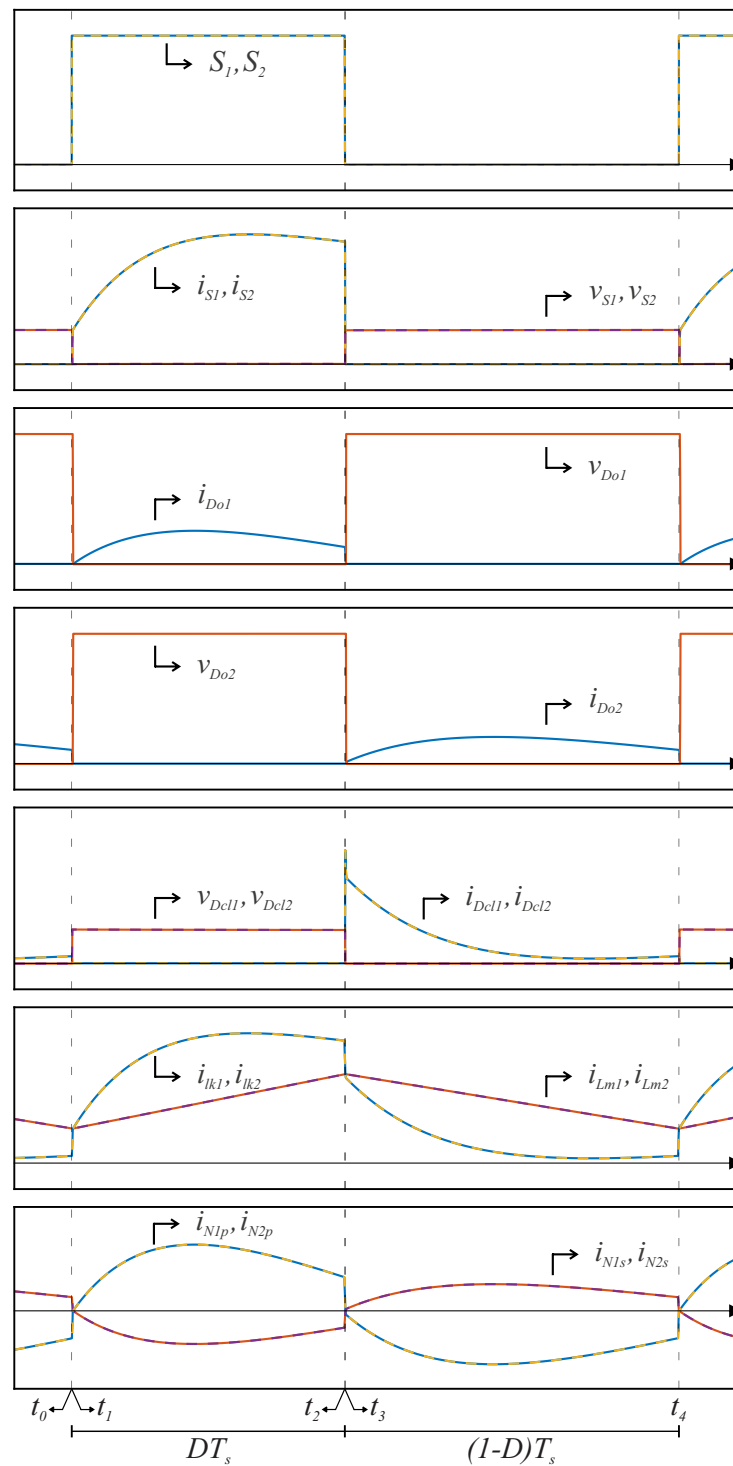


Figure 2. Converter main current and voltage waveforms during a switching cycle.

2.2. State II [$t_1 - t_2$]

Currents i_{lk1} and i_{lk2} values surpass i_{Lm1} and i_{Lm2} at instant t_1 , shown in Figure 3b. This causes the currents in both primary windings to change direction, which subsequently causes diode D_{01} to be forward biased and capacitor C_{01} to charge, while D_{02} becomes reverse biased. Due to D_{01} being forward biased, C_{01} is now in parallel with the secondary windings of the coupled-inductor, making L_{m1} and L_{m2} to be charged with voltage $\frac{V_{C01}}{2n}$ and, consequently, i_{lk1} and i_{lk2} are charged with voltage $V_{in} - \frac{V_{C01}}{2n}$. A resonant circuit is formed between i_{lk1} , i_{lk2} , C_{in} and C_{01} , leading to the appearance of high frequency sinusoidal

currents in these components and semiconductors. This state ends when S_1 and S_2 are commanded to turn off. This state can be described by the following Equations:

$$i_{Lm1}(t) = \frac{V_{Co1}}{2nL_{m1}}(t - t_1) + i_{Lm1}(t_1), \quad (4)$$

$$i_{lk1}(t) = i_{S1}(t) = \frac{V_{in} - \frac{V_{Co1}}{2n}}{\sqrt{r_{w1}^2 + (\omega_{d,II}l_{lk1})^2}} e^{-\alpha_{II}(t-t_1)} \sin(\omega_{d,II}(t - t_1)) + \frac{V_{Co1}}{2nL_{m1}}(t - t_1) + i_{Lm1}(t_1), \quad (5)$$

$$i_{Do1}(t) = \frac{V_{in} - \frac{V_{Co1}}{2n}}{n\sqrt{r_{w1}^2 + (\omega_{d,II}l_{lk1})^2}} e^{-\alpha_{II}(t-t_1)} \sin(\omega_{d,II}(t - t_1)), \quad (6)$$

where the equivalent elements regarding the resonant circuit during this state are:

$$R_{eqII} = r_{w1}, \quad (7)$$

$$L_{eqII} = l_{lk1}, \quad (8)$$

$$C_{eqII} = \frac{2n^2 C_{in} C_{o1}}{C_{in} + 4n^2 C_{o1}}. \quad (9)$$

Furthermore, the attenuation of the resonant circuit α_{II} is given by

$$\alpha_{eqII} = \frac{r_{eqII}}{2L_{eqII}}, \quad (10)$$

and the resonant frequency of the circuit is

$$\omega_{d,II} = \sqrt{\frac{1}{\sqrt{L_{eqII}C_{eqII}}} - \alpha_{II}^2}. \quad (11)$$

The equivalent circuit of the converter during this state can be seen in Figure 3b.

2.3. State III [$t_2 - t_3$]

At t_2 , both switches are turned off. Diodes D_{cl1} and D_{cl2} become forward biased and capacitors C_{cl1} , C_{cl2} and C_{o3} start to be charged. This causes l_{lk1} and l_{lk2} to start discharging with voltage $V_{in} - \frac{V_{Co1}}{2n} - V_{C_{cl1}}$, consequently leading their currents to decay. The diminishing currents on the leakage inductances cause the currents on the windings of the coupled-inductors and D_{o1} to decay as well. This stage ends when i_{lk1} and i_{lk2} become equal to i_{Lm1} and i_{Lm2} . Similarly to State I, there is the formation of a resonant circuit between the leakage inductances, C_{in} , C_{o1} and C_{o3} , but this state is very brief and the currents on these components and the semiconductors can be represented by linear approximations. Throughout this state, Equation (4) is still valid, while the leakage inductances and diode D_{o1} currents are given by:

$$i_{lk1}(t) = i_{D_{cl1}}(t) = \frac{V_{in} - \frac{V_{Co1}}{2n} - V_{C_{cl1}}}{l_{lk1}}(t - t_2) + i_{lk1}(t_2), \quad (12)$$

$$i_{Do1}(t) = \left[\frac{V_{in} - V_{C_{cl1}}}{nl_{lk1}} - \frac{V_{Co1}}{2n^2} \left(\frac{1}{L_{m1}} + \frac{1}{l_{lk1}} \right) \right] (t - t_2) - i_{Lm1}(t_2) + i_{Lk1}(t_2). \quad (13)$$

The converter equivalent circuit during this state is shown in Figure 3c

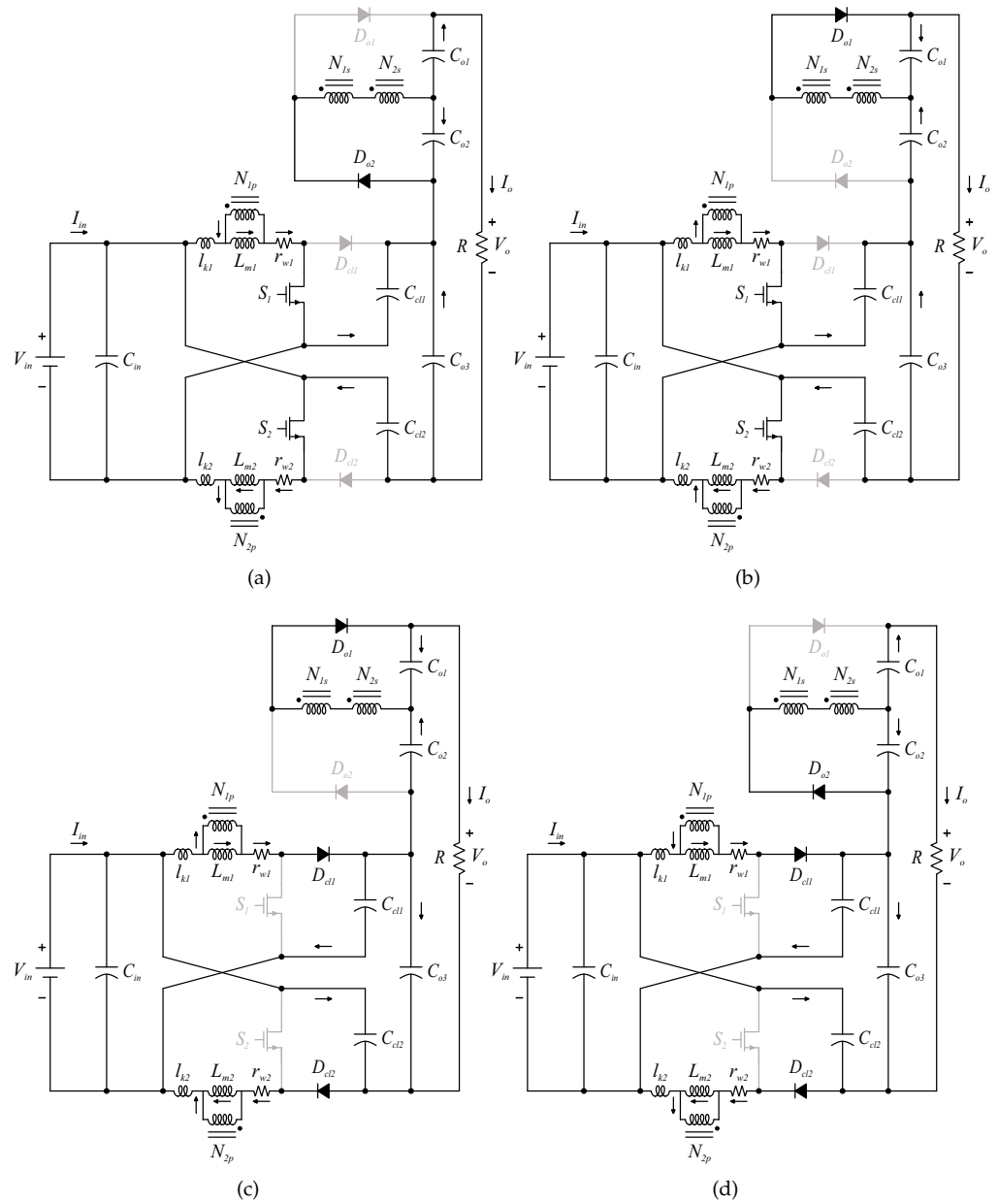


Figure 3. Topological states of the proposed converter. (a) State I, (b) State II, (c) State III, (d) State IV.

2.4. State IV [t3 – t4]

Currents i_{lk1} and i_{lk2} values become smaller than i_{m1} and i_{Lm2} at t_3 , which change the primary winding currents direction once more. This results in D_{o1} being reverse biased and D_{o2} to be forward biased. Consequently, C_{o2} is now in parallel with the secondary windings of the coupled-inductor, leading to L_{m1} and L_{m2} to be discharged with voltage $\frac{V_{Co2}}{2n}$, while l_{lk1} and l_{lk2} are discharged with voltage $V_{in} + \frac{V_{Co2}}{2n} - V_{ccl1}$. A resonant circuit is formed between l_{lk1} , l_{lk2} , C_{in} , C_{o2} and C_{o3} , leading to the appearance of high frequency sinusoidal currents in these components and semiconductors. This state ends when S_1 and S_2 are commanded to turn on at t_4 , restarting the cycle. The following equations can be used to describe this state:

$$i_{Lm1}(t) = -\frac{V_{Co2}}{2nL_{m1}}(t - t_3) + i_{Lm1}(t_3), \tag{14}$$

$$i_{lk1}(t) = i_{Dcl1}(t) = \frac{V_{in} + \frac{V_{Co2}}{2n} - V_{Ccl1}}{\sqrt{r_{w1}^2 + (\omega_{d,IV} l_{lk1})^2}} e^{-\alpha_{IV}(t-t_3)} \sin(\omega_{d,IV}(t-t_3)) - \frac{V_{Co2}}{2nL_{m1}}(t-t_3) + i_{Lm1}(t_3), \quad (15)$$

$$i_{Do2}(t) = \frac{V_{in} + \frac{V_{Co2}}{2n} - V_{Ccl1}}{n\sqrt{r_{w1}^2 + (\omega_{d,IV} l_{lk1})^2}} e^{-\alpha_{IV}(t-t_3)} \sin(\omega_{d,IV}(t-t_3)). \quad (16)$$

where

$$R_{eqIV} = r_{w1} + r_{w2}, \quad (17)$$

$$L_{eqIV} = l_{lk1} + l_{lk2}, \quad (18)$$

$$C_{eqIV} = \frac{n^2 C_{in} C_{o2} C_{o3}}{C_{in} + n^2 C_{o2} + C_{o3}}, \quad (19)$$

$$\alpha_{eqIV} = \frac{r_{eqIV}}{2L_{eqIV}}, \quad (20)$$

$$\omega_{d,IV} = \sqrt{\frac{1}{\sqrt{L_{eqIV} C_{eqIV}}}} - \alpha_{IV}^2. \quad (21)$$

The converter equivalent circuit during this State can be seen in Figure 3d.

3. Proposed Converter Steady-State Analysis

In order to facilitate the steady-state analysis of the proposed converter, the following assumptions are made:

- All components are ideal;
- The magnetizing inductances have the same value;
- $\frac{N_{s1}}{N_{p1}} = \frac{N_{s2}}{N_{p2}} = n$;
- The voltages across the capacitors are constant.

Since the leakage inductances influence is not represented, States I and III are not taken into consideration in the analyses made in this section, as these states are mainly characterized by the charge and discharge, respectively, of these inductances.

3.1. Voltage Stresses on the Capacitors

From Figure 3b, C_{in} is in parallel to the magnetizing inductances and the primary windings during State II, while C_{o1} is in parallel to the secondary windings, resulting in

$$V_{C_{o1}} = 2nV_{in}. \quad (22)$$

By applying the volt-second balance principle to the magnetizing inductances, it can be seen that during State IV

$$V_{C_{o2}} = 2n \frac{D}{1-D} V_{in}. \quad (23)$$

Moreover, applying the Kirchhoff's Voltage Law (KVL) to the lower loop of the circuit during State IV results in

$$V_{C_{o3}} = \frac{1+D}{1-D} V_{in} \quad (24)$$

The voltage across the clamper capacitors C_{cl1} and C_{cl2} can be found applying the KVL during State IV

$$V_{C_{cl1}} = V_{C_{cl2}} = \frac{1}{1-D} V_{in}, \quad (25)$$

3.2. Voltage Stresses on the Semiconductors

Since C_{cl1} and C_{cl2} are connected in parallel to S_1 and S_2 , respectively, during State IV, the voltage stress across the switches is given by Equation (25):

$$V_{S1} = V_{S2} = \frac{1}{(1-D)} V_{in}. \quad (26)$$

The output diodes D_{o1} and D_{o2} are subject to the sum of C_{o1} and C_{o2} voltages during States IV and II, respectively. Therefore, applying the KVL and using Equations (22) and (23) results in

$$V_{D_{o1}} = V_{D_{o2}} = \frac{2n}{(1-D)} V_{in}. \quad (27)$$

The clamber diodes D_{cl1} and D_{cl2} voltage stress can be obtained by applying the KVL during State II and using (25)

$$V_{D_{cl1}} = V_{D_{cl2}} = \frac{1}{(1-D)} V_{in}. \quad (28)$$

3.3. Voltage Gain

As can be seen from Figure 1, the output voltage V_o is given by the sum of the output capacitors voltages

$$V_o = V_{C_{o1}} + V_{C_{o2}} + V_{C_{o3}}. \quad (29)$$

The voltage gain G can be found by substituting Equations (22)–(24) into Equation (29), resulting in:

$$G = \frac{1 + 2n + D}{1 - D}. \quad (30)$$

Figure 4 shows the static gain versus duty cycle curves for different turn ratio values. As can be seen, it is possible to achieve very high static gain without need for high duty cycle values.

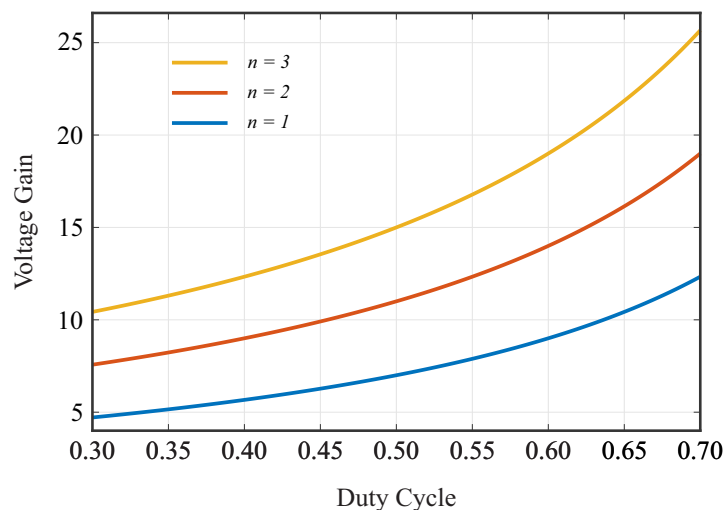


Figure 4. Duty cycle versus voltage gain curves under different turn-ratios.

3.4. Average Current Stresses

The average current through the magnetizing inductances and semiconductors in a switching cycle can be found by applying the ampere-second balance to the capacitors in Figure 1, resulting in

$$\bar{I}_{L_{m1}} = \bar{I}_{L_{m2}} = \frac{I_{in} + I_o}{2} = \frac{(G + 1)}{2} I_o, \quad (31)$$

$$\bar{I}_{D_{o1}} = \bar{I}_{D_{o2}} = \bar{I}_{D_{cl1}} = \bar{I}_{D_{cl2}} = I_o, \quad (32)$$

$$\bar{I}_{S1} = \bar{I}_{S2} = \frac{I_{in} - I_o}{2} = \frac{(G - 1)}{2} I_o, \quad (33)$$

3.5. Maximum Current Stresses

The maximum current on the magnetizing inductances is equal to its average value plus half of the total ripple. Therefore, utilizing Equations (4), (22) and (31) results in

$$\hat{I}_{L_{m1}} = \hat{I}_{L_{m2}} = \left[\frac{(G + 1)}{2} + \frac{RD}{2GL_m f_s} \right] I_o. \quad (34)$$

From Figure 2 and (14), the peak current on the clamper diodes occurs at t_3 and is equal to the magnetizing current at the same moment

$$\hat{I}_{D_{cl1}} = \hat{I}_{D_{cl2}} = \left[\frac{(G + 1)}{2} + \frac{RD}{2GL_m f_s} \right] I_o. \quad (35)$$

The maximum current on the diodes D_{o1} and D_{o2} can be found by not taking the attenuation during States II and IV into consideration. Since the average current on the output diodes is equal to the average output current (32), it means that

$$\frac{1}{T_s} \int_0^{DT_s} \hat{I}_{D_{o1}} \sin(\omega_{d,II} t) dt = I_o, \quad (36)$$

$$\frac{1}{T_s} \int_0^{(1-D)T_s} \hat{I}_{D_{o2}} \sin(\omega_{d,IV} t) dt = I_o, \quad (37)$$

where $T_s = \frac{1}{f_s}$ is the switching period. Thus, solving for the peak currents nets

$$\hat{I}_{D_{o1}} \approx \frac{\omega_{d,II} T_s}{1 - \cos(\omega_{d,II} D T_s)} I_o, \quad (38)$$

$$\hat{I}_{D_{o2}} \approx \frac{\omega_{d,IV} T_s}{1 - \cos(\omega_{d,IV} (1 - D) T_s)} I_o. \quad (39)$$

The maximum value of the currents on the switches is difficult to obtain from (4) due to the need to solve a transcendental equation. However, it is easy to note that the maximum value is lesser or equal than the sum of the maximum linear and sinusoidal parts of the equation. As such, by disregarding, it is possible to state that:

$$\hat{I}_{S1} = \hat{I}_{S2} \leq \hat{I}_{L_{m1}} + n \hat{I}_{D_{o1}}. \quad (40)$$

Substituting Equations (34) and (38) into Equation (41) results in

$$\hat{I}_{S1} = \hat{I}_{S2} \leq \left[\frac{(G + 1)}{2} + \frac{RD}{2GL_m f_s} + \frac{n \omega_{d,II} T_s}{1 - \cos(\omega_{d,II} D T_s)} \right] I_o. \quad (41)$$

4. Performance Comparison

Table 1 shows the performance comparison between the proposed converter and some recently published topologies using some relevant metrics, such as number of total used switches, diodes, capacitors and magnetic cores, the voltage stress on the semiconductors and maximum efficiency. All of the compared converters are non-isolated, high-gain, high-efficiency topologies with similar nominal power rating, employing magnetic coupling, a low number of components and employ two switches.

Table 1. Performance comparison between the proposed converter and other recently proposed topologies.

	No. of Comp.				Voltage Gain	Max. Voltage Stress		Efficiency	
	S	D	C	Cor.		Switches	Diodes	Max.	Full Load
Proposed	2	4	6	1	$\frac{1+2n+D}{1-D}$	$\frac{V_o}{1+2n+D}$	$\frac{2nV_o}{1+2n+D}$	97.3%	95.9%
[16]	2	2	2	1	$\frac{1+2nD+D}{1-D}$	$\frac{V_o}{1+2nD+D}$	$\frac{(2n+1)V_o}{1+2nD+D}$	95.9%	95.1%
[17]	2	3	3	1	$\frac{1+2nD+D}{1-D}$	$\frac{V_o}{1+2nD+D}$	$\frac{2nV_o}{1+2nD+D}$	96.4%	95.2%
[18]	2	5	5	2	$\frac{3+2n+D}{1-D}$	$\frac{V_o}{3+2n+D}$	$\frac{2nDV_o}{3+2n+D}$	94.0%	93.0%
[21]	2	2	3	1	$\frac{2+n}{1-D}$	$\frac{V_o}{2+n}$	$\frac{(n+1)V_o}{2+n}$	93.9%	93.3%
[22]	2	6	5	2	$\frac{2+nD}{1-D}$	$\frac{V_o}{2+nD}$	V_o	96.1%	95.9%
[24]	2	6	5	1	$\frac{1+2n}{1-D}$	$\frac{V_o}{1+2n}$	$\frac{nV_o}{1+2n}$	96.5%	95.5%
[26]	2	7	6	2	$\frac{1+5n}{1-D}$	$\frac{V_o}{1+5n}$	$\frac{2nV_o}{1+5n}$	98.0%	91.1%

The converters presented in [16,17] utilize the A-SL cell, substituting the normal inductors for coupled-inductors pairs to increase the voltage gain. Both topologies are very simple, employing a very low quantity of components. Since in both converters the coupled-inductors pairs are switched simultaneously, only one magnetic core is used. The low component count results in high voltage stress and the lack of an input filter results in very high current ripple in the input, which is detrimental to the lifespan of PV modules and fuel cells. Both converters also present low voltage gain when compared to most of the other converters shown.

In [18], a coupled-inductor A-SL converter is also proposed. This converter also employs a rectifier VMC in a boost-flyback configuration, which greatly improve the voltage gain of the converter when compared to [16,17], with the addition of only a few more components. This converter, however, employs two magnetic cores, increasing its volume and weight, and also presents very high input current ripple. Although the voltage stress on the switches and diodes is low, it presents comparatively low efficiency.

The converter proposed in [21] also has very low overall count of elements, using only one magnetic core, two diodes and three capacitors. However, it has one of the lowest voltage gains of all compared converters, which translates into higher voltage stresses on the semiconductor elements. Its voltage gain can be increased by changing the turn-ratio of the coupled-inductor or by cascading the used VMC, which, in turn, decreases the efficiency due to heightened conduction losses. Its maximum reported efficiency is also the lowest from all of the compared converters.

The converter presented in [22] uses its second switch in an active clamper circuit to achieve load-independent soft-switching. The converter voltage gain is low, however, and the voltage stresses between the diodes are not optimally distributed, resulting in several diodes presenting a maximum voltage equal to the output. The converter also presents two magnetic cores due to the interleaved nature of the switches operation. This converter presents high efficiency throughout the entire possible output power interval.

In [24], a soft switching boost-flyback converter with a rectifier VMC is presented. It presents a high voltage gain and efficiency, due to the use of the capacitors of the rectifier VMC and leakage inductances as resonant tanks, allowing for lossless turn-off of the diodes. Furthermore, the voltage stress on the semiconductor components are low and

well-distributed. The absence of an input filter allows for bidirectional currents in the input, which can be harmful to the input source.

An interleaved converter is presented in [26]. This converter features the highest voltage gain and the highest reported efficiency of all compared converters, while also presenting good voltage stress distribution between its semiconductor elements. However, this efficiency was reported at a low output power relative (10%) to the rated power of the converter. Moreover, it also features the highest number of components of all the presented converters.

The presented converter, therefore, shows promise as it achieves high voltage gain using low turn-ratios and duty cycles. It also employs an average number of components, whose voltage stresses are well distributed between them. The simultaneous operation of the switches permits the use of only one magnetic core and also decreases conduction losses due to the shared processing of power between them. Compared to [24], the proposed converter uses less diodes, and the added capacitor removes the high input current ripple, while maintaining the positive characteristics. This results in a high efficiency through all possible operation points.

5. Design Considerations

5.1. Semiconductors Design

The semiconductors can be chosen using Equations (26)–(28) for the maximum rated voltage, Equations (32) and (33) for the average current stress and Equations (35), (38), (39) and (41) for the peak current stress.

5.2. Coupled-Inductor Design

The turn-ratios can be chosen after the range of the duty cycle and the gain are set via

$$n = \frac{G(1-D)}{2(1+D)}. \quad (42)$$

However, as can be seen from Equations (35) and (41), the maximum current value on the clamper diodes and switches and, therefore, the RMS values of said currents increase along with the turn-ratios. Hence, using excessively high turn-ratios lead to high conduction losses and should be avoided.

The coupled-inductor magnetizing inductance is designed to have a current ripple, relatively to the average current, within the desired limits. The magnetizing currents ripple ΔI_{Lm1} and ΔI_{Lm2} are given by

$$\Delta I_{Lm1} = \Delta I_{Lm2} = 2(\hat{I}_{Lm1} - \bar{I}_{Lm1}). \quad (43)$$

Substituting Equations (31) and (34) into Equation (43) results in

$$\Delta I_{Lm1} = \Delta I_{Lm2} = \frac{V_{in}D}{L_{m1}f_s}, \quad (44)$$

To operate in the CCM, it is necessary that

$$\bar{I}_{Lm1} - \frac{\Delta I_{Lm1}}{2} > 0. \quad (45)$$

Substituting Equations (31) and (44) into Equation (45) results in

$$L_{m1} = L_{m2} > \frac{DR}{2G(G-1)f_s}. \quad (46)$$

5.3. Capacitor Design

The voltage rating of the capacitors can be chosen from Equations (22)–(25). The capacitance values of the output capacitors are designed to limit the voltage ripple within

the desired thresholds. During State IV, the output capacitor C_{o1} discharges into the load with current I_o . Thus, its charge variation during State IV can be given by

$$V_{C_{o1}} \Delta V_{C_{o1}} = \frac{(1-D)I_o}{f_s}. \quad (47)$$

Substituting Equations (22) and (30) into Equation (47) yields:

$$C_{o1} = \frac{(1+D+2n)}{2nRf_s(\Delta V_{C_{o1}}/V_{C_{o1}})}. \quad (48)$$

Similarly, output capacitors C_{o2} and C_{o3} discharge into the load during State II with current I_o ; therefore:

$$\Delta V_{C_{o2}} C_{o2} = \Delta V_{C_{o3}} C_{o3} = \frac{DI_o}{f_s}. \quad (49)$$

By substituting Equations (23) and (30) into Equation (49) it is possible to find

$$C_{o2} = \frac{(1+D+2n)}{2nRf_s(\Delta V_{C_{o2}}/V_{C_{o2}})}, \quad (50)$$

and substituting Equations (24) and (30) into Equation (49) results in

$$\Delta V_{C_{o3}} = \frac{(1+D+2n)}{2nRf_s(\Delta V_{C_{o2}}/V_{C_{o2}})}. \quad (51)$$

The charge variation in the input capacitor C_{in} during State IV is equal to the sum of the charge variation in C_{o2} reflected to the primary windings and C_{o3} , resulting in

$$C_{in} \Delta V_{in} = \frac{(2n(1-D)+1)I_o}{f_s}, \quad (52)$$

and with some manipulations, it is possible to find that

$$C_{in} = \frac{(2n(1-D)+1)G}{Rf_s(\Delta V_{in}/V_{in})}. \quad (53)$$

It must be noted that all the previously designed capacitors compose the resonant circuits in States II or IV and their capacitance values impact the resonance frequency. As such, it is important to reach a compromise between the need for low voltage ripple in the capacitors with the high frequency resonant currents which can reduce switching losses.

The clamping capacitors need to be large enough to absorb the energy stored in the leakage inductances after the switches are opened and are given by

$$C_{cl1} = C_{cl2} = \left(\frac{1+D}{\pi f_s} \right)^2 \frac{1}{l_{lk1} + l_{lk2}}. \quad (54)$$

6. Experimental Results

A prototype with rated power of 400 W was created and tested in order to validate the theoretical analyses performed previously. The experimental prototype is shown in Figure 5 and its design parameters and components are shown in Table 2.

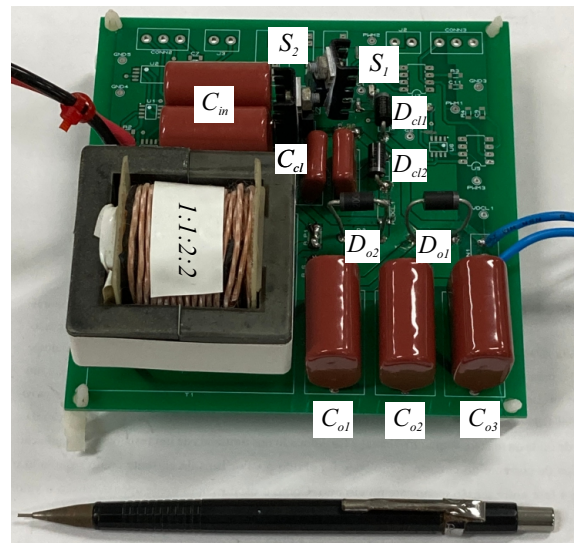


Figure 5. The assembled 400 W laboratory prototype.

Table 2. Operational parameters and components used on the prototype.

Parameter/Component	Value/Specification
Rated Power	400 W
Input Voltage	25–45 V
Output Voltage	400 V
Switching Frequency	100 kHz
Coupled-Inductor	Thornton NEE-55/28/21-496-IP12R $L_{m1} = L_{m2} = 76 \mu\text{H}$ 1:1:2:2
C_{in}	$2 \times 10 \mu\text{F}$
C_{o1}, C_{o2} and C_{o3}	10 μF
C_{cl1} and C_{cl2}	1 μF
S_1 and S_2	IPP110N20N3 G
D_{o1}, D_{o2}, D_{cl1} and D_{cl2}	STTH3R04

All waveforms measurements were performed using Yokogawa's DL850 Oscilloscope. The switches gate signals, input voltage and output voltage are shown in Figure 6. It can be seen that the converter is capable of high voltage gain, above ten times, while maintaining low duty cycle, around 0.45, in accordance to Equation (30)

The currents and drain-source voltages waveforms on both switches are shown in Figure 7. The voltage stress on the switches are much smaller than the output voltage, around 70 V, validating Equation (26). This makes possible employing low-voltage rating and, therefore, low $R_{DS,on}$ switches, decreasing the conduction losses.

From the output diodes waveforms, shown in Figure 8, it is possible to observe that the voltage stresses are lower than the output voltage. This, combined with the decaying currents, results in decreased switching losses. The use of ultrafast recovery diodes in the circuit causes the fast rise of current on the moment these diodes are forward biased, due to the forward recovery effect.

Similarly, from the clamper diodes waveforms, shown in Figure 9, it can be seen that the voltage stresses are as low as the voltage stresses on the switches, with reduced switching losses due to the naturally decaying current waveforms.

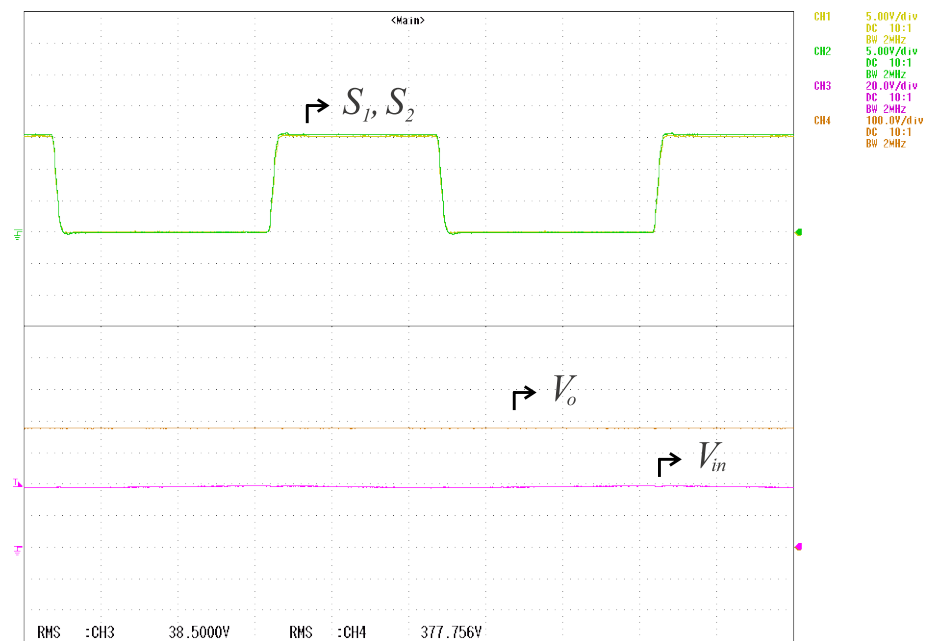


Figure 6. Top: switches gate signals v_{gs1} and v_{gs2} (5 V/div); bottom: input voltage v_{in} (20 V/div) and output voltage v_o (100 V/div).

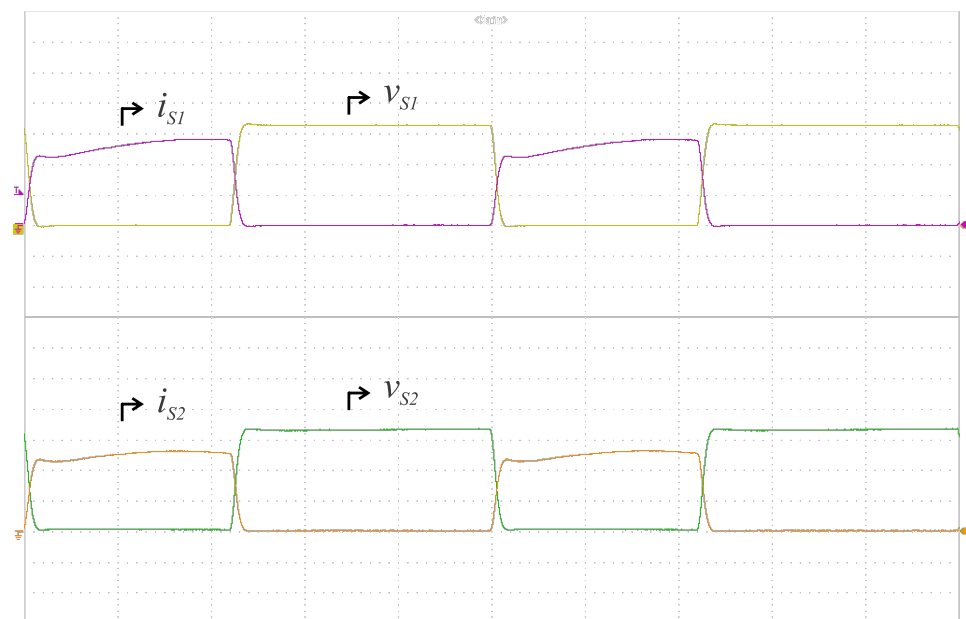


Figure 7. Top: switch S_1 voltage v_{S1} (20 V/div) and current i_{S1} (2 A/div); bottom: switch S_2 voltage v_{S2} (20 V/div) and current i_{S2} (2 A/div).

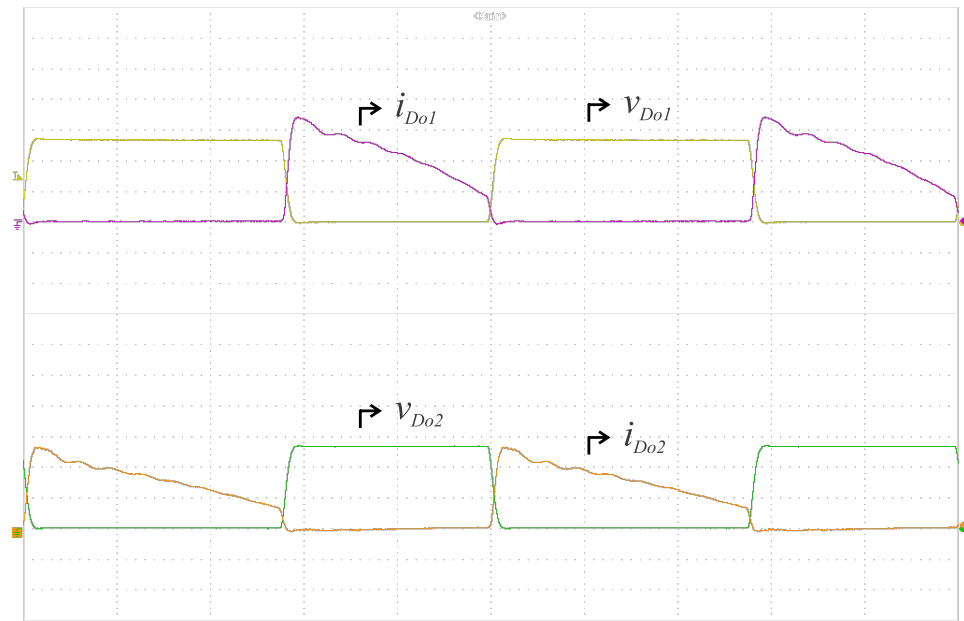


Figure 8. Top: diode D_{o1} voltage $v_{D_{o1}}$ (100 V/div) and current $i_{D_{o1}}$ (500 mA/div); bottom: diode D_{o2} voltage $v_{D_{o2}}$ (100 V/div) and current $i_{D_{o2}}$ (500 mA/div).

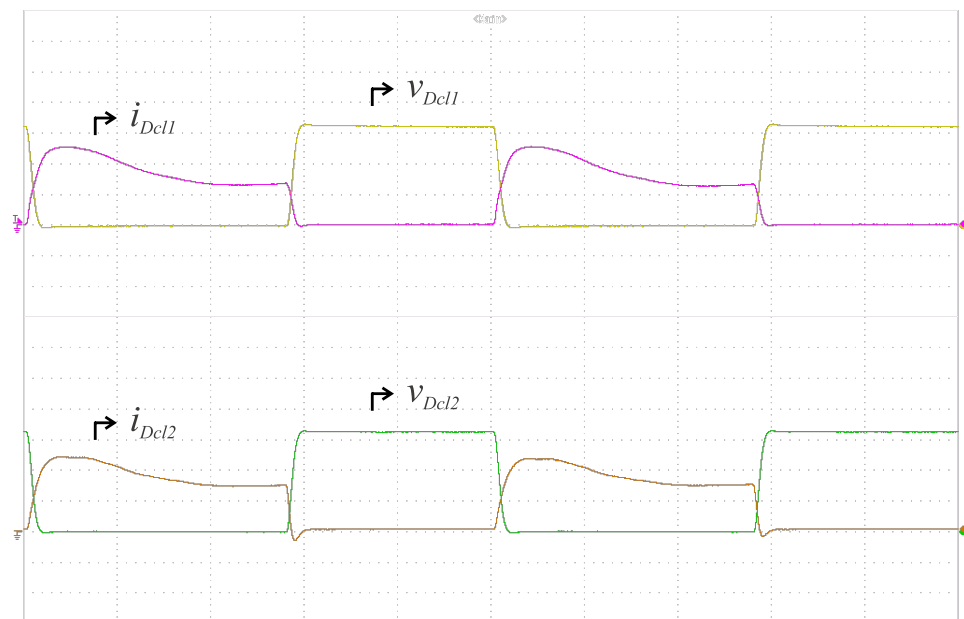


Figure 9. Top: diode D_{cl1} voltage $v_{D_{cl1}}$ (20 V/div) and current $i_{D_{cl1}}$ (500 mA/div); bottom: diode D_{cl2} voltage $v_{D_{cl2}}$ (20 V/div) and current $i_{D_{cl2}}$ (500 mA/div).

Finally, the currents on the magnetic components are shown in Figure 10. The magnetizing current shows that the converter is currently operating in the continuous conduction mode, while the leakage current shows the naturally decaying current waveform, which evidences the leakage inductances role in mitigating the diodes switching losses.

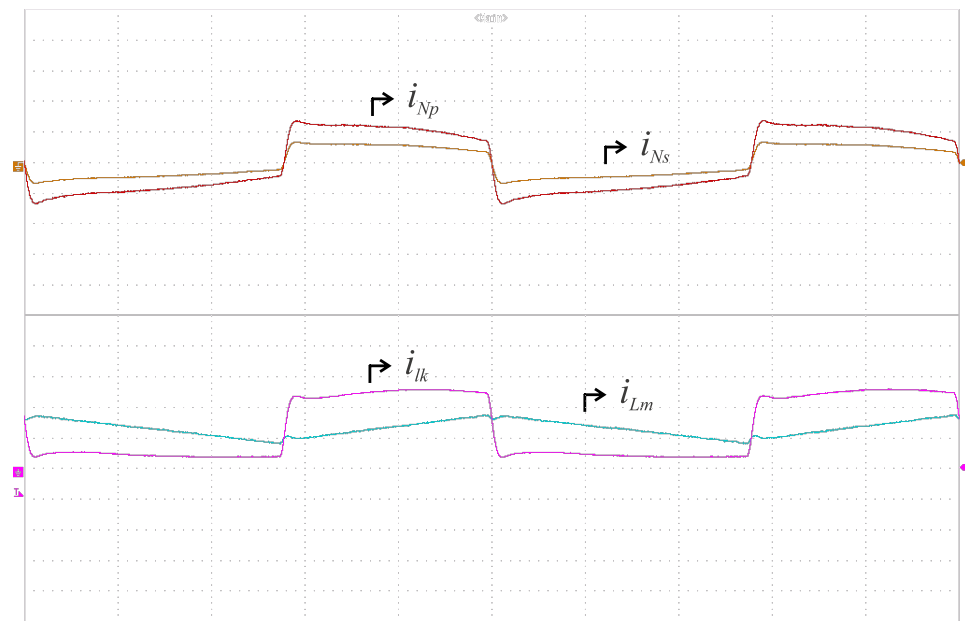


Figure 10. Top: primary winding N_{1p} current (2 A/div) and secondary winding N_{1s} (2 A/div); bottom: leakage inductance l_{k1} current (2 A/div) and magnetizing inductance L_{m1} current (2 A/div).

The efficiency of the proposed converter was measured using Yokogawa's WT1800 power analyzer in two different tests. In the first test, the converter is submitted to resistive loads of different power under a constant output voltage and duty cycle. In the second test, the load power and output voltage are constant while the duty cycle is changed. From the efficiency results, shown in Figure 11, the CEC efficiency is given by

$$\eta_{CEC} = 0.04\eta_{10\%} + 0.05\eta_{20\%} + 0.12\eta_{30\%} + 0.21\eta_{50\%} + 0.53\eta_{75\%} + 0.05\eta_{100\%} = 97.12\%. \quad (55)$$

where $\eta_{X\%}$ indicates the efficiency at $X\%$ of the nominal rated power.

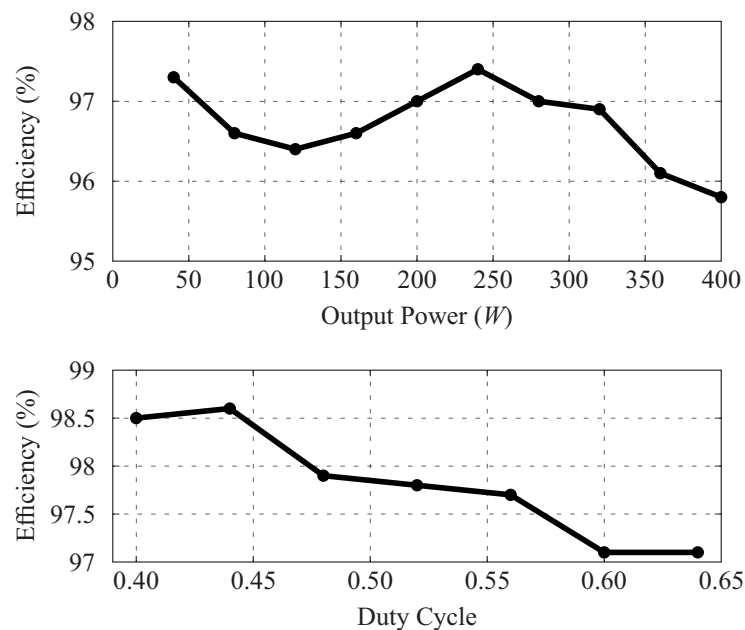


Figure 11. Efficiency tests results: different loads under constant duty cycle and 400 V output voltage, different duty cycle under constant 200 W and 400 V output voltage.

7. Conclusions

A new high-gain, high-efficiency converter utilizing active switched coupled-inductors and rectifier VMC techniques was proposed. By combining the AS-L cell with rectifier VMC techniques, the proposed converter is capable of achieving high voltage gain without high duty cycle and turn-ratios and low total component count. The use of coupled-inductor reduces the voltage stress on the switches, which enable the use of low $R_{ds,on}$ switches, decreasing losses. Furthermore, since the switches are switched simultaneously, the current through each switch is halved. This also permits the integration of both coupled-inductors into a single-core, reducing volume and weight. The coupled-inductors leakage inductances are utilized to reduce the reverse-recovery current losses, and their energy are recycled through the use of regenerative clamper circuits. A 400 W prototype was tested, validating the previously performed analyses and achieving high efficiency.

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