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Technical Limits of Passivity-Based Control Gains for a Single-Phase Voltage Source Inverter

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Abstract: Passivity-based control (PBC) seems to be predicted for the control algorithms in the voltage source inverters (VSI) for voltage backup systems. This paper presents limitations of the improved (IPBC) version of the PBC (directly measuring the output voltage) maximum voltage and current gains. In a microprocessor-controlled inverter, these depend on the PWM modulator dynamic properties, the switching frequency, the modulation index value (avoiding modulator saturation and enabling the rapid increase of the filter inductor current), and the parameters of the VSI output filter. A single switching period delay of the digital PWM modulator was considered in the theoretical calculations based on a discrete inverter model. The simulations for the standard nonlinear rectifier RC load enabled the initial adjustment of the IPBC border gains, which depended on the switching frequency. Some small harmonics oscillations of the output voltage were acceptable for the test rectifier RC load or dynamic load. However, oscillations of the inductor current increased the power losses in the coil core. Experimental verification of the simulation results using a laboratory VSI model is also presented.

Keywords: voltage source inverter; passivity-based control; control law; non-linear load

Citation: Rymarski, Z.; Bernacki, K. Technical Limits of Passivity-Based Control Gains for a Single-Phase Voltage Source Inverter. *Energies* **2021**, *14*, 4560. https://doi.org/10.3390/en14154560

Academic Editor: Woojin Choi

Received: 16 June 2021
Accepted: 22 July 2021
Published: 28 July 2021

1. Introduction

Passivity-based controls (PBC) were introduced into control algorithms more than 20 years ago. PCB is a method reminiscent of standard Lyapunov methods [1]. At first, it was used in electromechanical systems as an Interconnection and Damping Assignment Passivity-Based Control (IDA-PBC) [1,2]. More recently, different PBC versions are among the most promising control systems for voltage source inverters that work on-grid [3,4] or off-grid in AC voltage backup systems, single-phase voltage source inverters [5–9], or three-phase inverters [10–12].

AC voltage backup systems, e.g., uninterruptible power supplies (UPS), have requirements associated with the distortions of the output voltage for precisely defined loads [13–16]. All investigations should consider two basic standard loads—nonlinear rectifier RC with PF = 0.7 (PF is a product of the displacement factor and the distortion factor [17]) and the dynamic load. The component non-linear load values have been precisely defined elsewhere [13]. A VSI should reduce the value of the Total Harmonic Distortion (THD) coefficient of the output voltage (for Low Voltage < 1 kV, THD < 8%, harmonic amplitude maximum < 5%). This was a typical load for a UPS with an output power of less than 3 kW and is the subject of our research.

The undershoot, overshoot and settling time for a dynamic load change were 20–100% and 100–20% as defined in [13] for other VSI output voltage parameters. For a load step increase during the first switching period, the feedback loop does not work due to the delay of the PWM modulator—the output capacitor should contain a stored charge, and the step increase of the voltage would be forced on the output filter inductance. Step voltages that increase at the output sinusoidal voltage maximum point only have amplitudes of

(1–M)*V_{DC}, where M is the modulation index and V_{DC} is the input DC voltage of the inverter. We should force a rapid increase of the current through the filter coil (lower inductance values mean better control). In the case of a step load decrease (the worst case is at the voltage maximum), the output overvoltage depends on the capacity of the output capacitor and the instantaneous inductor current. The filter inductor works as the current source (the feedback has a one switching period delay) that forces the charge flow to the output filter capacitor for the switched-off load, which results in a voltage overshoot. The feedback works during the next switching period. The quality of the output voltage decreases for overly large filter inductances values, a capacitance that is too low (a large capacitance results in the reactive power in the output filter components, which causes excess power losses on the equivalent serial resistances of the inverter), and an excessive modulation index, which eliminates the possibility of a rapid increase of the filter inductor current.

In our opinion, the main problem with the PBC design stems from setting up the gain values (the "injected resistance" R_i for the inductor current control and the gain K_v of the output voltage error in the improved PBC-IPBC versions) when considering the technical possibilities of a digitally controlled inverter. Higher gains correspond to higher rates of theoretical error convergence; however, a real system with a control loop begins to oscillate. A basic theoretical analysis of the root locus of the characteristic polynomial of a closed-loop system showed that a positive sum of the injected resistance R_i and the equivalent serial resistance of the inverter and a positive voltage error gain K_v [5,10] was required for the convergence to zero of the tracking errors and maintaining the stability of a system. While the real parts of these poles in a continuous model are theoretically always negative in the s-plane [12], the nonzero imaginary parts in the restricted gain ranges also caused oscillations. Simulations of a VSI with discrete control and experimental verification for a standard nonlinear rectifier RC load proved that increasing IPBC gains from zero initially resulted in a reduction of the output voltage THD coefficient. In the short-range of the IPBC gains, THD was almost the same and additional increases of the R_i and K_v gains increased the THD oscillations of the output voltage [9,12]. R_i and K_v values (their product) always merit consideration. Authors of previous publications tried to determine the upper limitations of the controller gains. A reduction of the injected resistance without considering K_v in [5] was insufficient in our experiments with an IPBC, which was based on the idea of an IDA-PBC control law presented in [10]. Ideas presented in [5] comparing the limited carrier slope in a PWM modulator with the derivative of the control voltage (this derivative should not be faster than the carrier slope in the modulator) were further developed in this paper. We did not consider the carrier slope, but rather the maximum speed of the output PWM modulator voltage increase/decrease (the derivative of the control voltage). A wider discussion of this problem that considered the output voltage error gain K_v was presented in [12]. This paper focuses on the dependence of the maximum allowable gains on the switching frequency of an inverter that was not focused yet. The theoretical analysis, results of MATLAB-Simulink simulations, and experimental VSI model measurements results (controlled with an STM32F407VG microprocessor) were examined at three switching frequencies (12,800 Hz, 25,600 Hz, and 51,800 Hz).

The authors sought to create a control law readily utilized by an engineer-designer of a voltage source off-grid inverter. There are many approaches to the nonlinear modeling of an inverter. The simple linear approach treats the whole inverter plant as an LC filter and one switching period delay in series [9,18–20]. The PWM modulation scheme requires dead time implementation between switching on the transistors from the same bridge leg [19,20]. The dead time causes a step decrease of the output voltage when the load current crosses a zero value. This can be treated as nonlinear [21]. However, new switching devices require a short dead time (<500 ns, and was the problem with the "current tail" for older technology IGBTs). The serial resistance and inductance of the filter coils vary and depend on the switching frequency, the coil current, and temperature [22–24], which is important for the cheap iron-powder coil core materials. For the alloy powder materials

such as Super MSS (Micrometals), this was less important [23,24]. Some approaches for describing the nonlinearity of the coils in the output filter have been reported [25]. We could neglect these nonlinearities for the alloy-powder material, for a constant switching frequency, and the coil current changes around to the operating point.

When creating an inverter model, we usually approximate the PWM modulator as a linear function of the input voltage. We were mindful that when we solved the state equations, the output voltage was an exponential function of the switching on time. We approximated this function with the linear function proposed many years ago [26,27]. Using a double Fourier transform to describe the nonlinear switching function of a converter in the steady-state of an inverter was possible [28]. One approach for analyzing a PWM using the double Fourier transform was initially reported nearly 50 years ago [29,30]. The small-signal models can be compared with the nonlinear model of a switching power electronic converter using the black-box identification method, called the Hammerstein model. In this model, the nonlinear static and linear dynamic characteristics can be considered separately to create an identification model of a power electronic system. The Hammerstein model consists of a static nonlinearity followed by a linear and time-invariable model [31].

The authors used a continuous linearized model [9,18–20] with a delay in the PWM modulator in this discussion of the switching frequency influence on the design of an IPBC controller. The discrete control law, which has six coefficients (three of the products of the coefficients and the mutually shifted reference voltages can be presented in the form of the initially calculated look-up tables) is easily implemented in the microprocessor-based controller of a VSI.

Section 2 presents the fundamentals of the PBC controller design and its difference control law. Section 3 contains the calculations that enabled us to determine the border values of the PBC gains above which the oscillations of the output voltage existed due to the technical limits of the inverter and the switching frequency. Section 4 presents the simulations of the VSI operating with the nonlinear rectifier load (according to [13]), the most representative kind of load for the device tests (<3 kW) for the different switching frequencies and different parameters of an inverter filter. Section 5 includes a discussion of the simulation results. Section 6 gives the experimental verification of the simulations from Section 4. Section 7 discusses the experimental verification results and the differences in the values of the border PBC gains in simulations and a real inverter (different scaling of the input variables).

2. Fundamentals of PBC Controller Design

Figure 1 presents the schematic of a multi-input-single-output (MISO) controller in which the load current is treated as an independent disturbance (e.g., [10,32]). While this helps eliminate the load impedance in the control law, feedback from the output voltage to the load current disappears. In some cases, this simplification significantly changes the locus of the characteristic equation poles for a closed-loop system [19]. We used the inductor current and output voltage as the state variables, the load current as a disturbance, and the delay, T_s, as the modulator model.

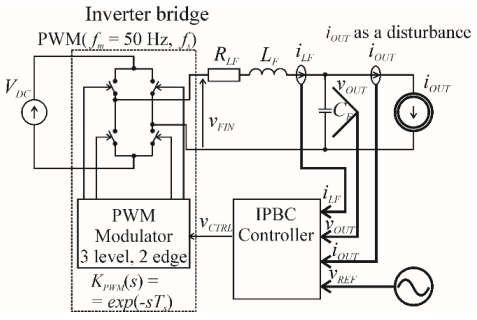


Figure 1. Simplified concept of a MISO control in inverters.

A PBC is based on the concept that when the supplied energy in a system exceeds the stored energy, the system is passive. The energy in an inverter is stored in two non-dissipative components—the filter coil and the filter capacitor. The energy stored in a system Equation (1) is described by the Hamiltonian function $H(x)$ (in some papers [5], $H(x)$ is called a Lyapunov function).

$$H(x) = \frac{1}{2}(L_F {i_{LF}}^2 + C_F {v_{OUT}}^2) \tag{1}$$

That explains why we used the products of Equation (2), $L_F i_{LF}$ and $C_F v_{OUT}$, as the state variables (for the other control systems, we used i_{LF} and v_{OUT} as state variables).

$$\mathbf{x} = \begin{bmatrix} L_F i_{LF} & C_F v_{OUT} \end{bmatrix}^T \tag{2}$$

The error vector **e** is defined Equation (3) where i_{LFref} and v_{OUTref} are the reference values (i_{LFref} is calculated, v_{OUTref} is assigned).

$$\mathbf{e} = \begin{bmatrix} L_F(i_{LF} - i_{LFref}) \\ C_F(v_{OUT} - v_{OUTref}) \end{bmatrix} \tag{3}$$

The stored energy of the error values comes from Equation (4).

$$H(\mathbf{e}) = \frac{1}{2}(L_F(i_{LF} - i_{LFref})^2 + C_F(v_{OUT} - v_{OUTref})^2) \tag{4}$$

The equilibrium of a closed-loop system is asymptotically stable [2] and achieved when $H(\mathbf{e})$ minimizes (5) in $\mathbf{x} = \mathrm{x}_{ref}$.

$$\left.\frac{\partial H(\mathbf{e})}{\partial \mathbf{x}}\right|_{\mathbf{x}=\mathbf{x}_{ref}} = 0, \quad \left.\frac{\partial^2 H(\mathbf{e})}{\partial \mathbf{x}^2}\right|_{\mathbf{x}=\mathbf{x}_{ref}} > 0 \tag{5}$$

The system is passive when the energy $H(\mathbf{e})$ of the error decreases with time; therefore, if the time derivative, $H(\mathbf{e})$, is negative in Equation (6),

$$\frac{\mathrm{d}H(\mathbf{e})}{\mathrm{d}t} < 0 \tag{6}$$

Equation (7) describes a closed-loop system [10].

$$\dot{\mathbf{e}} = [\mathbf{J} - (\mathbf{R} + \mathbf{R}_a)]\mathbf{P}^{-1}\mathbf{e}, \ \mathbf{P} = \begin{bmatrix} L_F & 0 \\ 0 & C_F \end{bmatrix}, \ \mathbf{P}^{-1} = \begin{bmatrix} 1/L_F & 0 \\ 0 & 1/C_F \end{bmatrix}, \ \mathbf{P}^{-1}\mathbf{e} = \partial H(\mathbf{e})/\partial \mathbf{e} \tag{7}$$

where the interconnection matrix, **J**, and the damping matrix, **R**, are defined as Equation (8).

$$\mathbf{J} = \begin{bmatrix} 0 & -1 \\ 1 & 0 \end{bmatrix}, \ \mathbf{R} = \begin{bmatrix} R_{LF} & 0 \\ 0 & 0 \end{bmatrix} \tag{8}$$

$\mathbf{R}_a$ (the PBC controller) is the matrix of the injected damping, R_i is the gain of the current error, and K_v is the conductive gain of the voltage error in Equation (9).

$$\mathbf{R}_a = \begin{bmatrix} R_i & 0 \\ 0 & K_v \end{bmatrix} \tag{9}$$

Equation (10) describes an open-loop system where $m(t - T_s)$ is a delayed control function (the delay of the PWM modulator) from the previous switching period.

$$\dot{\mathbf{x}} = [\mathbf{J} - \mathbf{R}]\mathbf{P}^{-1}\mathbf{x} + \begin{bmatrix} V_{DC} \\ 0 \end{bmatrix} m(t - T_s) + \begin{bmatrix} 0 \\ -1 \end{bmatrix} i_{OUT} \tag{10}$$

To obtain the control law (11), we subtracted (7) from Equation (10):

$$\begin{bmatrix} m(t-T_s)V_{DC} \\ 0 \end{bmatrix} = \begin{bmatrix} L_F di_{LFref}/dt \\ C_F dv_{OUTref}/dt \end{bmatrix} + \begin{bmatrix} (R_{LF}+R_i)i_{LFref} + v_{OUTref} \\ -i_{LFref} + K_v v_{OUTref} \end{bmatrix} - \begin{bmatrix} R_i i_{LF} \\ K_v v_{OUT} \end{bmatrix} + \begin{bmatrix} 0 \\ 1 \end{bmatrix} i_{OUT} \quad (11)$$

Hence, we have the equation of the control law Equation (12) with Equation (13).

$$v_{CTRL}(t-T_s) = L_F di_{LFref}/dt + (R_{LF}+R_i)i_{LFref} + v_{OUTref} - R_i i_{LF} \quad (12)$$

$$i_{LFref} = C_F dv_{OUTref}/dt - K_v(v_{OUT} - v_{OUTref}) + i_{OUT} \quad (13)$$

A difference control law that considers the T_s delay of the modulator is Equation (14) with Equations (15) and (16)—we have to predict state variables for the $k+1$ switching period.

$$v_{CTRL}(k) = L_F \frac{i_{LFref}(k+1) - i_{LFref}(k)}{T_s} + (R_{LF}+R_i)i_{LFref}(k+1) + v_{OUTref}(k+1) - R_i i_{LF}(k+1) \quad (14)$$

$$i_{LFref}(k) = C_F \frac{v_{OUTref}(k) - v_{OUTref}(k-1)}{T_s} + K_v[v_{OUTref}(k) - v_{OUT}(k)] + i_{OUT}(k) \quad (15)$$

$$i_{LFref}(k+1) = C_F \frac{v_{OUTref}(k+1) - v_{OUTref}(k)}{T_s} + K_v[v_{OUTref}(k+1) - v_{OUT}(k+1)] + i_{OUT}(k+1) \quad (16)$$

3. The Influence of the Switching Frequency and Output Filter Parameters on the Border IPBC Gains

Using the inverter state Equations (17) and (18) is the simplest way to predict the $v_{OUT}(k+1)$, $i_{LF}(k+1)$ and, finally, to calculate $i_{OUT}(k+1)$. The presented calculation is based only on a discrete model of an inverter [18–20].

$$v_{OUT}(k+1) = \varphi_{11} v_{OUT}(k) + \varphi_{12} i_{LF}(k) + \varphi_{13} i_{OUT}(k) + g_{11} v_{CTRL}(k) \quad (17)$$

$$i_{LF}(k+1) = \varphi_{21} v_{OUT}(k) + \varphi_{22} i_{LF}(k) + \varphi_{23} i_{OUT}(k) + g_{21} v_{CTRL}(k) \quad (18)$$

where the coefficients are presented in Equation (19):

$$\begin{aligned} &\xi_{Fe} = 0.5\frac{R_{LFe}}{\omega_{F0} L_{Fe}},\ \omega_{F0} = \frac{1}{\sqrt{L_F C_F}}, \\ &C_A = \cos(\omega_{F0} T_s)\exp(-\xi_{Fe}\omega_{F0} T_s), \\ &S_A = \sin(\omega_{F0} T_s)\exp(-\xi_{Fe}\omega_{F0} T_s), \\ &\phi_{11} = C_A + \xi_{Fe} S_A,\ \phi_{12} = \frac{1}{\omega_{F0} C_F} S_A, \\ &\varphi_{13} = -\frac{1}{\omega_{F0} C_F} S_A - (1 - C_A - \xi_{Fe} S_A) R_{LFe}, \\ &\phi_{21} = -\frac{1}{\omega_{F0} L_{Fe}} S_A,\ \phi_{22} = C_A - \xi_{Fe} S_A, \\ &\phi_{23} = 1 - C_A - \xi_{Fe} S_A, \\ &\varphi_{31} = 0,\ \varphi_{32} = 0,\ \varphi_{33} = 1, \\ &C_G = \cos(\omega_{F0} T_s/2)\exp(-\xi_{Fe}\omega_{F0} T_s/2), \\ &S_G = \sin(\omega_{F0} T_s/2)\exp(-\xi_{Fe}\omega_{F0} T_s/2), \\ &g_{11} = \omega_{F0} T_s S_G, g_{21} = \frac{1}{L_{Fe}} T_s (C_G - \xi_{Fe} S_G),\ g_{31} = 0 \end{aligned} \quad (19)$$

The output current in the next switching period, $i_{OUT}(k+1)$, was readily calculated as the difference between the inductor current and the output filter capacitor current in Equations (20) and (21).

$$i_{OUT}(k+1) = i_{LF}(k+1) - C_F \frac{v_{OUT}(k+1) - v_{OUT}(k)}{T_s} \quad (20)$$

$$\begin{aligned} i_{OUT}(k+1) = {} & [\varphi_{21} - \tfrac{C_F}{T_s}(\varphi_{11} - 1)] v_{OUT}(k) + (\varphi_{22} - \tfrac{C_F}{T_s}\varphi_{12}) i_{LF}(k) + \\ & + (\varphi_{23} - \tfrac{C_F}{T_s}\varphi_{13}) i_{OUT}(k) + (g_{21} - \tfrac{C_F}{T_s} g_{11}) v_{CTRL}(k) \end{aligned} \quad (21)$$

The reference inductor current in the next switching period was calculated using the state space Equation (22).

$$\begin{array}{l} i_{LFref}(k+1) = (\frac{C_F}{T_s} + K_v)v_{OUTref}(k+1) - \frac{C_F}{T_s}v_{OUTref}(k) - \\ +[\varphi_{21} - (\frac{C_F}{T_s} + K_v)\varphi_{11} + \frac{C_F}{T_s}]v_{OUT}(k) + [\varphi_{22} - (\frac{C_F}{T_s} + K_v)\varphi_{12}]i_{LF}(k) + \\ +[\varphi_{23} - (\frac{C_F}{T_s} + K_v)\varphi_{13}]i_{OUT}(k) + [g_{21} - (\frac{C_F}{T_s} + K_v)g_{11}]v_{CTRL}(k) \end{array} \quad (22)$$

The predicted increase of the reference inductor current in the next switching period is described with Equation (23).

$$\begin{array}{l} i_{LFref}(k+1) - i_{LFref}(k) = (\frac{C_F}{T_s} + K_v)v_{OUTref}(k+1) - (2\frac{C_F}{T_s} + K_v)v_{OUTref}(k) + \frac{C_F}{T_s}v_{OUTref}(k-1) \\ +[\varphi_{21} - (\frac{C_F}{T_s} + K_v)\varphi_{11} + \frac{C_F}{T_s} + K_v]v_{OUT}(k) + [\varphi_{22} - (\frac{C_F}{T_s} + K_v)\varphi_{12}]i_{LF}(k) + \\ [\varphi_{23} - (\frac{C_F}{T_s} + K_v)\varphi_{13} - 1]i_{OUT}(k) + [g_{21} - (\frac{C_F}{T_s} + K_v)g_{11}]v_{CTRL}(k) \end{array} \quad (23)$$

The difference control law of the IPBC of a single-phase inverter, which considers the delay of the PWM discrete modulator is expressed by Equation (24).

$$\begin{array}{l} v_{CTRL}(k) = A_{VREF1}v_{OUTref}(k+1) + A_{VREF2}v_{OUTref}(k) + A_{VREF3}v_{OUTref}(k-1) + \\ +A_{VOUT4}v_{OUT}(k) + A_{ILF5}i_{LF}(k) + A_{IOUT6}i_{OUT}(k) \end{array} \quad (24)$$

where Equation (25):

$$\begin{array}{l} R_e = \frac{L_F}{T_s} + R_{LF} + R_i,\ K_e = \frac{C_F}{T_s} + K_v \\ A_{VREF1} = \frac{(R_eK_e+1)}{1+R_eK_eg_{11}-(\frac{L_F}{T_s}+R_{LF})g_{21}}, \\ A_{VREF2} = \frac{-\frac{C_F}{T_s}R_e-\frac{L_F}{T_s}K_e}{1+R_eK_eg_{11}-(\frac{L_F}{T_s}+R_{LF})g_{21}}, \\ A_{VREF3} = \frac{\frac{1}{\omega_{F0}{}^2T_s{}^2}}{1+R_eK_eg_{11}-(\frac{L_F}{T_s}+R_{LF})g_{21}}, \\ A_{VOUT4} = \frac{-R_eK_e\varphi_{11}+(\frac{L_F}{T_s}+R_{LF})\varphi_{21}+\frac{C_F}{T_s}R_e+\frac{L_F}{T_s}K_e-\frac{1}{\omega_{F0}{}^2T_s{}^2}}{1+R_eK_eg_{11}-(\frac{L_F}{T_s}+R_{LF})g_{21}} \\ A_{ILF5}\frac{-R_eK_e\varphi_{12}+(\frac{L_F}{T_s}+R_{LF})\varphi_{22}}{1+R_eK_eg_{11}-(\frac{L_F}{T_s}+R_{LF})g_{21}}, \\ A_{IOUT6} = \frac{-R_eK_e\varphi_{13}+(\frac{L_F}{T_s}+R_{LF})\varphi_{23}-\frac{L_F}{T_s}}{1+R_eK_eg_{11}-(\frac{L_F}{T_s}+R_{LF})g_{21}} \end{array} \quad (25)$$

However, we can use the reference voltage shifted by one switching period and the final discrete control law used is Equation (26).

$$\begin{array}{l} v_{CTRL}(k) = A_{VREF1}v_{OUTref}(k) + A_{VREF2}v_{OUTref}(k-1) + A_{VREF3}v_{OUTref}(k-2) + \\ +A_{VOUT4}v_{OUT}(k) + A_{ILF5}i_{LF}(k) + A_{IOUT6}i_{OUT}(k) \end{array} \quad (26)$$

The calculated values of the variables in the next switching period might be inaccurate because we use the discretized model of the inverter directly [18–20]. More exact results were obtained when we would estimate the state variables at the next sampling instant using the full order state observer [33,34]. We would use the same state equations but would sum them with the gain matrix of the estimator multiplied by the difference between the measured and estimated system output variable (the output voltage). However, the complexity of the calculations is difficult to use in practice, though additional simulations showed that the simplified approach was satisfactory.

The basic frequency of the closed-loop system oscillations was caused by the higher speed (derivative) of the control voltage increase than the speed (derivative) of the PWM modulator control voltage change. The restrictions of the PBC gains depend on the maximum speed (derivative) of the PWM modulator control voltage increase. The maximum

increase speed of the v_{CTRL} voltage in Equation (27) cannot be faster than the maximum increase speed of the PWM modulator control voltage.

$$\begin{array}{l}\frac{v_{CTRL}(k)-v_{CTRL}(k-1)}{T_s} \approx (A_{VREF1}+A_{VREF2}+A_{VREF3})\frac{\Delta v_{OUTref}}{T_s}+\\ +A_{VOUT4}(\frac{v_{OUT}(k)-v_{OUT}(k-1)}{T_s})+A_{ILF5}(\frac{i_{LF}(k)-i_{LF}(k-1)}{T_s})+A_{IOUT6}(\frac{i_{OUT}(k)-i_{OUT}(k-1)}{T_s})\end{array} \quad (27)$$

The maximum increase speed of the sinusoidal reference voltage, v_{OUTref} is expressed using Equations (28) and (29), where M is a modulation index.

$$\left.\frac{d(MV_{DC}\sin(2\pi 50t))}{dt}\right|_{\max} = MV_{DC}2\pi 50 \quad (28)$$

$$\begin{array}{l}\left.\frac{v_{OUTref}(k+1)-v_{OUTref}(k)}{T_s}\right|_{\max} \approx \left.\frac{v_{OUTref}(k)-v_{OUTref}(k-1)}{T_s}\right|_{\max}\\ \approx \left.\frac{v_{OUTref}(k-1)-v_{OUTref}(k-2)}{T_s}\right|_{\max} \approx \left.\frac{\Delta v_{OUTref}}{T_s}\right|_{\max} = MV_{DC}2\pi 50\end{array} \quad (29)$$

The maximum speed of the output voltage increase will occur for a step load decrease to zero for the maximum control voltage when the filter inductor operates like the voltage source i_{LF} and loads the charge to the output capacitor C_F. For this calculation, we approximated the inductor current as constant during one switching period in this case Equation (30). We did not consider a short circuit of the inverter output.

$$\begin{array}{l}\left.\frac{v_{OUT}(k)-v_{OUT}(k-1)}{T_s}\right|_{\max} = \left.\frac{\Delta v_{OUT}}{T_s}\right|_{\max} \approx \left.\frac{i_{LF}(k)}{C_F}\right|_{\max}, -\frac{V_{DC}}{L_F}T_s < i_{LF}(k) < \frac{V_{DC}}{L_F}T_s,\\ -\frac{V_{DC}}{L_F C_F}T_s < \left.\frac{\Delta v_{OUT}}{T_s}\right|_{\max,\min} < \frac{V_{DC}}{L_F C_F}T_s\end{array} \quad (30)$$

The maximum speed of the increase/decrease of the inductor current occurred for the zero crossing of the output voltage Equation (31).

$$\frac{i_{LF}(k)-i_{LF}(k-1)}{T_s} = \frac{\Delta i_{LF}}{T_s}, -\frac{V_{DC}}{L_F} < \left.\frac{\Delta i_{LF}}{T_s}\right|_{\max,\min} < \frac{V_{DC}}{L_F} \quad (31)$$

The maximum increase/decrease of the output current caused by the control action can be equal to the difference/sum of the inductor current increase and the output capacitor current increase/decrease (Equation (32)). We did not consider a short circuit of the inverter output when the changes of the output voltage and the current were much higher and depended on the parasitic resistance of the capacitor. The value obtained from Equation (33) is only indicative.

$$\frac{i_{OUT}(k)-i_{OUT}(k-1)}{T_s} = \frac{\Delta i_{OUT}}{T_s} = \frac{\Delta i_{LF} \mp \Delta v_{OUT}C_F/T_s}{T_s} = \frac{\Delta i_{LF}}{T_s} \mp \frac{\Delta v_{OUT}}{{T_s}^2}C_F \quad (32)$$

$$0 < \left.\frac{\Delta i_{OUT}}{T_s}\right|_{\max,\min} < 2\frac{V_{DC}}{L_F} \quad (33)$$

It should be noted the assumed maximum values of the increases of the voltages and currents only appeared in specific cases of the dynamic load change, e.g., when the current to the load was cut off by the rectifier diode for a rectifier RC load. This is the standard [13] load for UPS systems up to 3 kW. We calculated the maximum value of $(\Delta v_{CTRL}/T_s)_{\max}$ using Equations (27)–(33). The speed (derivative) of the voltage increase in a three-level PWM modulator is expressed by Equation (34).

$$\frac{d(\frac{t}{T_s}V_{DC})}{dt} = \frac{V_{DC}}{T_s}, \text{ where } 0 < t < T_s \quad (34)$$

The final indicative inequality that should be maintained to avoid oscillations is shown in Equation (35).

$$\frac{dv_{CTRL}}{dt} < \frac{V_{DC}}{T_s}, \frac{v_{CTRL}(k) - v_{CTRL}(k-1)}{T_s} < \frac{V_{DC}}{T_s} \quad (35)$$

The simulations shown in Figure 2a–c (for L_F = 1 mH, C_F = 50 µF, R_{LF} = 1 Ω, and M = 0.5) for three switching frequencies (12,800, 25,600 and 51,200 Hz) help estimate the border values (below the control voltage oscillations) of the voltage gain K_v (Figure 2d) as a function of the current gain R_i. R_{LF} equals the serial equivalent resistance of the inverter when power losses in the inverter are considered [22–24].

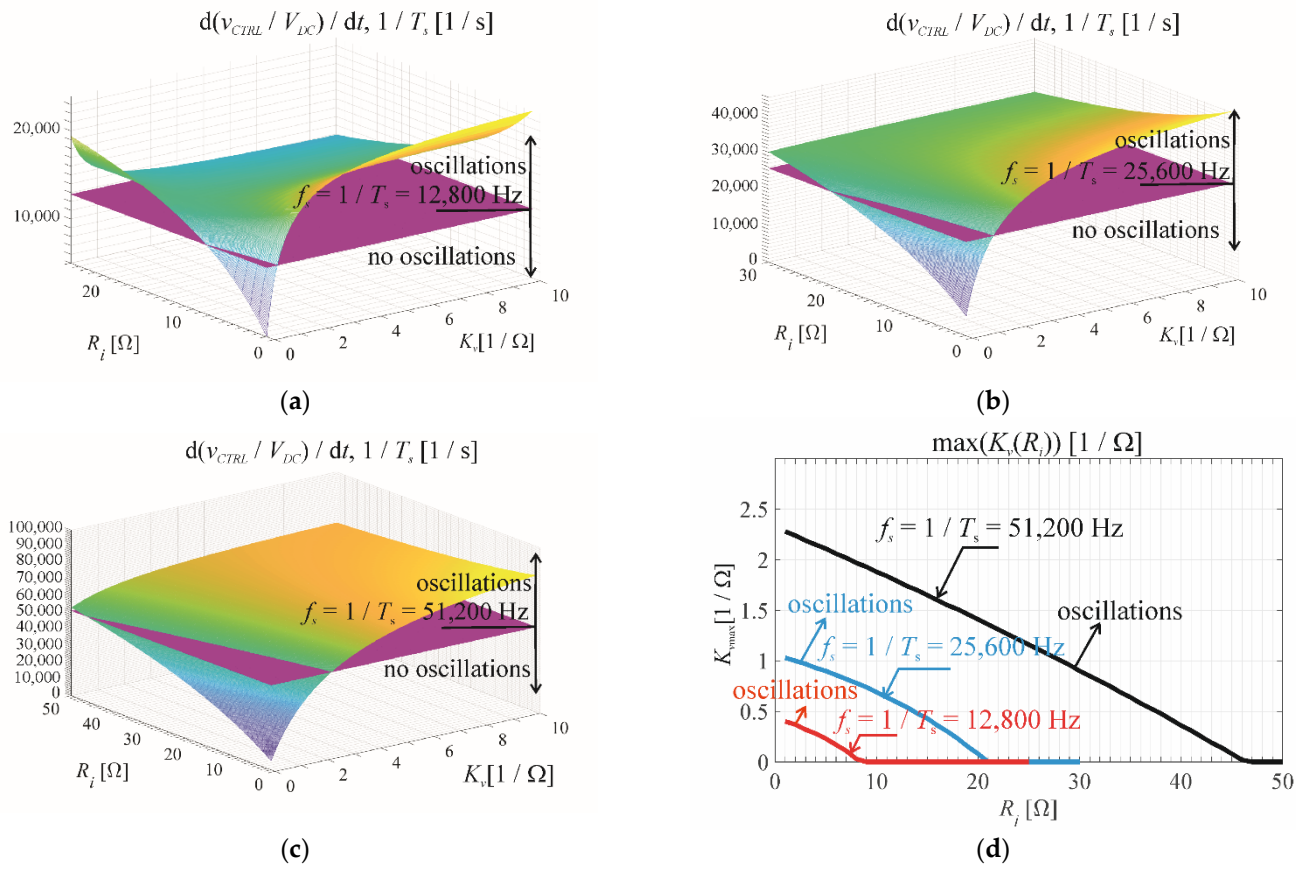


Figure 2. Determining the border gains (**d**) of the IPBC controller for different switching frequencies (12,800 (**a**), 25,600 (**b**), and 51,200 Hz (**c**)) when L_F = 1 mH, C_F = 50 µF, R_{LF} = 1 Ω, and M = 0.5.

The border values of the IPBC gains depended on the parameters of the output filter. Figure 3a–d show the border gain dependence as a function of the filter inductance, L_F = 0.5–2 mH, for C_F = 50 µF, R_{LF} = 1 Ω, M = 0.5, and f_s = 25,600 Hz.

Figure 4 illustrates how the border gains depend on filter capacitances C_F = 10–100 µF for L_F = 1 mH, R_{LF} = 1 Ω, M = 0.5, and f_s = 25,600 Hz.

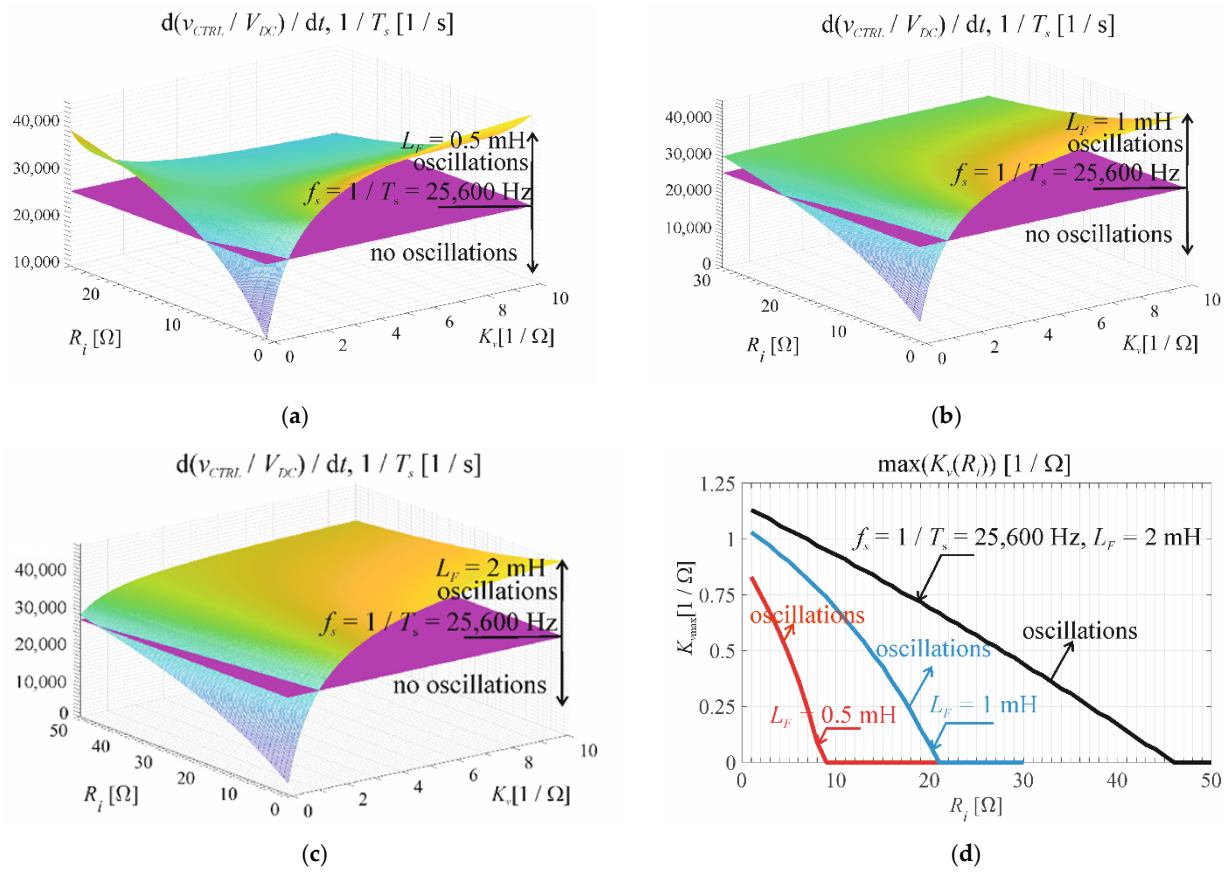


Figure 3. Determining the border gains (**d**) of the IPBC controller for a constant switching frequency f_s = 25,600 Hz and different inductances L_F (0.5 (**a**), 1.0 (**b**), 2 mH (**c**)) when C_F = 50 µF, R_{LF} = 1 Ω, and M = 0.5.

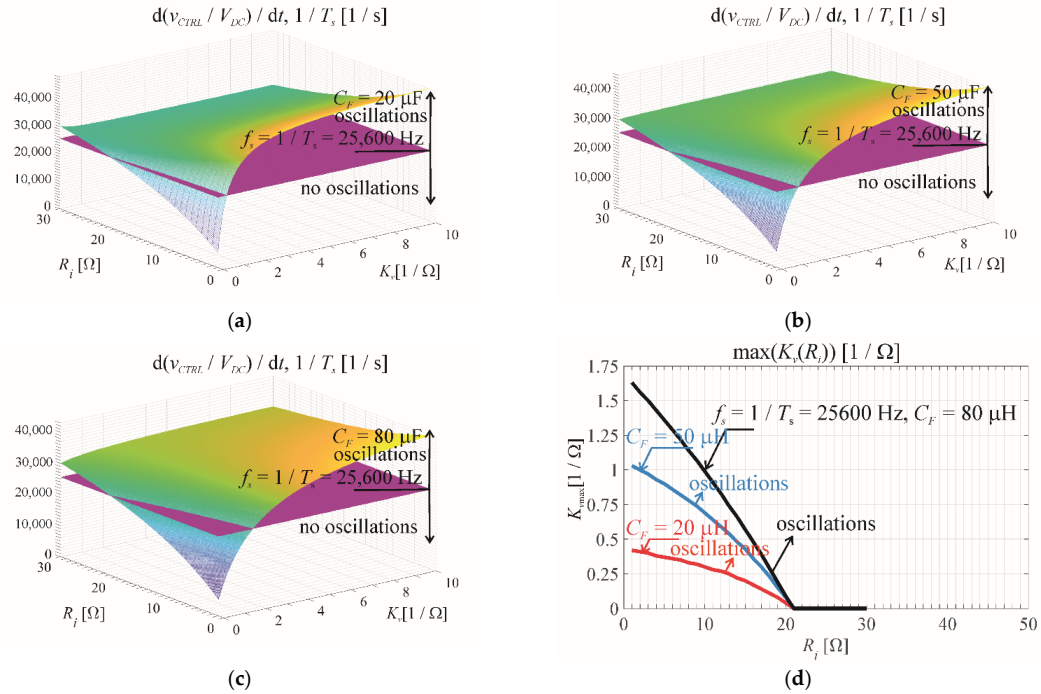


Figure 4. Determining the border gains (**d**) of the IPBC controller at different capacitances C_F (20 (**a**), 50 (**b**), and 80 µF (**c**)), for L_F = 1 mH, R_{LF} = 1 Ω, M = 0.5, and f_s = 25,600 Hz.

The dependence of the maximum IPBC gains on the switching frequency, the output filter inductor, and the output filter capacitor are presented in Figures 2–4. Higher inductor and capacitor values correspond to higher PBC border gains. The assumed values of the possible changes of the inductor current, output current, and output voltage were only indicative.

4. Simulations of a VSI with an IPBC for a Nonlinear Rectifier RC Load

The simulations in MATLAB 2020b should determine initially identified areas of IPBC gains without control voltage oscillations (Figures 5a,b and 6a). The standard nonlinear rectifier RC load (PF = 0.7) was selected based on the results reported in [13]. However, gains over the border values, which caused some oscillations of the control voltage (Figure 6b), resulted in lower distortions of the output voltage (lower THD).

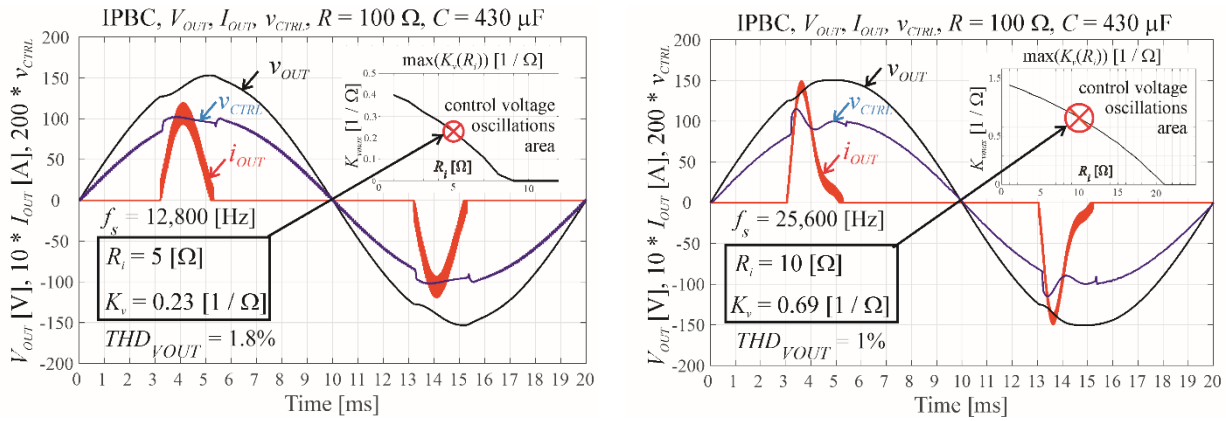


Figure 5. Border values for the rectifier RC load gains (C_F = 50 μF, L_F = 1 mH, R_{LF} = 1 Ω, and M = 0.5, load: R = 100 Ω, C = 430 μF) for (**a**) f_s = 12,800 Hz and (**b**) f_s = 25,600 Hz.

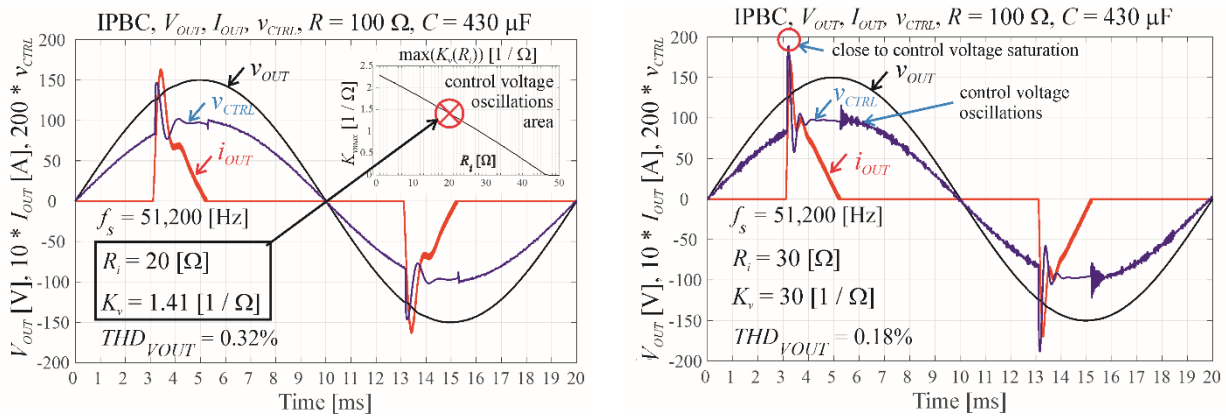


Figure 6. The border values of the gains (**a**) and the gains over the border values (**b**) of the output voltage, which resulted in a control voltage saturation for the rectifier RC load (f_s = 51,200 Hz, C_F = 50 μF, L_F = 1 mH, R_{LF} = 1 Ω, and M = 0.5, load: R = 100 Ω and C = 430 μF).

In simulations and the experimental inverter, the first scheme of a three-level double edge PWM modulation was used [19,20,22] in which the frequency of the bridge transistor switches is a double $2f_s$ switching (control) frequency f_s. Some small additional power losses [35] occurred when we allowed small oscillations of the inductor current. The power losses in the magnetic material of the filter coil core (neglecting so-called excess power losses) are shown presented as (36) where k_1 is the coefficient of the hysteresis losses and

k_2 is the coefficient of the eddy current losses and the flux density is a linear function of the magnetizing current. We used a Super-MSS (Sendust) alloy-powder (soft magnetic material) core [36,37] (MS 184075-2) for which the hysteresis power losses were much lower than the eddy current losses ($k_1 << k_2 f_n$).

$$P_{losses} = \sum_{n=1}^{n=\infty} {I_{LFhn\max}}^2 (k_1 f_n + k_2 {f_n}^2) = \sum_{n=1}^{n=\infty} {I_{LFhn\max}}^2 (k_1 + k_2 f_n) f_n \approx \sum_{n=1}^{n=\infty} k_2 {I_{LFhn\max}}^2 {f_n}^2 \quad (36)$$

Increasing the IPBC gains yielded the minimum THD_{VOUT} of the output voltage by allowing some oscillations of the inductor current, and we decreased the power efficiency (Table 1).

$$\Delta P_{losses}[\%] = 100 \frac{P_{osc} - P_{border}}{P_{border}}[\%] \approx 100 \left(\frac{\sum_{n=1}^{n=\infty} {I_{LFhn\max osc}}^2 {f_n}^2}{\sum_{n=1}^{n=\infty} {I_{LFhn border}}^2 {f_n}^2} - 1 \right)[\%] \quad (37)$$

$$\Delta P_{losses}[\%] \approx 100 \left(\frac{{I_{LFh1\max osc}}^2 \sum_{n=1}^{n=\infty} \frac{{I_{LFhn\max osc}}^2}{{I_{LFh1\max osc}}^2} n^2}{{I_{LFh1\max border}}^2 \sum_{n=1}^{n=\infty} \frac{{I_{LFhn\max border}}^2}{{I_{LFh1\max border}}^2} n^2} - 1 \right)\% \quad (38)$$

Table 1. Simulation results: Comparison of the inverter output voltage parameters with the three switching frequencies for the border gains and above the border gains for a nonlinear rectifier RC load (three-level, double edge, the first scheme PWM modulation); C_F = 50 µF, L_F = 1 mH, R_{LF} = 1 Ω, and M = 0.5; RC load: R = 100 Ω, C = 430 µF, dynamic loads (500 | | 50)/500 Ω.

Switching Frequency, R_i [Ω], K_v [1/Ω]		**THD_{VOUT} (Rectifier RC Load, R = 50 Ω, C = 430 µF)**	**Power Losses Increase ΔP_{losses}**	**Overvoltage after the Step Load Decrease (500 | | 50)/500 Ω**
12,800 [Hz], R_i = 5, K_v = 0.23	Border gains	1.8%	-	2.71%
25,600 [Hz], R_i = 10, K_v = 0.69	Border gains	1.0%	-	1.81%
51,200 [Hz], R_i = 20, K_v = 1.41	Border gains	0.32%	-	0.94%
51,200 Hz, R_i = 30, K_v = 30 (oscillations begin)	The values over the border gains	0.18%	negligible	0.77%

However, when the border gain values were R_i = 20 and K_v = 1.41 and for gains, R_i = 30 and K_v = 30 that resulted in oscillations for f_s = 51,200 Hz, the theoretical relative increase of the power losses in the magnetic material was negligible (in the experimental inverter, the increase in the power losses was much higher).

5. Discussion of the Simulation Results

An analysis of the simulation results showed the following:

1. For the frequencies analyzed (12,800, 25,600, and 51,200 Hz), it was important to consider the delay of the PWM modulator in the control law. Even the simplest prediction of the variables in the next switching period using the discrete state space equations allowed an estimation of the PBC border gains to lower distortions of the inverter output voltage and a better dynamic load change response.
2. Basic PBC theory does not enable the limits of the PBC gains to be found. For positive gains, a system is always theoretically stable [9]. The technical properties of an inverter control system cause the restrictions. Below the border gains of the PBC, there are no output voltage oscillations. The border gains are calculated based on the assumption that the increase of the control voltage should not be faster than the possible increase of the PWM modulator voltage (V_{DC} voltage in one switching period T_s).

3. Additional gain increases over the border values causes oscillations of the output voltage and the inductor current and output voltage distortions. It is possible to find the maximum gains of the PBC for the minimum of the output voltage THD.
4. A lower modulation index, M, is preferable—it is a $(1–M)V_{DC}$ margin of voltage that forces an inductor current increase. However, low values of M will not be used in a practical design because we always allow for the potential of full input voltage (M close to unity).
5. A lower M helps avoid saturation of the PWM modulator (Figure 6b) for higher controller gains.
6. The oscillations of the inductor current slightly increase the power losses in the inductor core.
7. The results shown in Table 1 confirm the preference for using a higher switching frequency. However, we should not forget about potential technical problems. In one switching period, we count up to a value that equals the PWM comparator frequency divided by the switching frequency. In the experimental work, we used an STM32F407VG microprocessor with an 84 MHz frequency in the PWM modulator. Using f_s = 51,200 Hz (1024 switching time periods per fundamental period), we obtained the maximum counted value per switching period of ≈1640 (the amplitude of the sinusoidal reference waveform was 820). The resolution, $1/820 = 1.2 \times 10^{-3}$, was insufficient for the generated sinusoidal waveform close to π because the change of $1 - \sin(2\pi \times (256 - 1)/1024) = 1.8825 \times 10^{-5}$, was lower than the resolution. It caused the width of some (in our case 16) neighboring PWM pulses of the reference waveform close to $\pi/2$ or $3\pi/2$ to be the same; however, in this case, the additional distortions were ignored (ΔTHD = 0.051%). Therefore, f_s = 51,200 Hz was assigned as the highest switching frequency for the STM32F407VG microprocessor control.

6. Experimental Verification

The experimental inverter parameters (Figure 7): three-level, double edge, the first modulation scheme PWM [19,20,22], f_s = 51,200 Hz, C_F = 50 µF, L_F = 1 mH, R_{LF} = 1 Ω, M = 0.5, RC load: R = 50 Ω, C = 430 µF, dynamic load (500||50)/500 Ω). R_{LF} is a series equivalent resistance of the inverter and was measured [24] for a filter coil with the core: Super-MSS™–Sendust (MS), MS-184075-2, μ = 75, A_L = 169, and l_e = 0.10743 m [36]. A STM32F407VG (32 bit, 168 MHz) microprocessor controlled the inverter. The border gains, R_i and K_v, were selected experimentally and therefore were not directly compared to the theoretical gains because they were multiplied by the output voltage and current scaling factors.

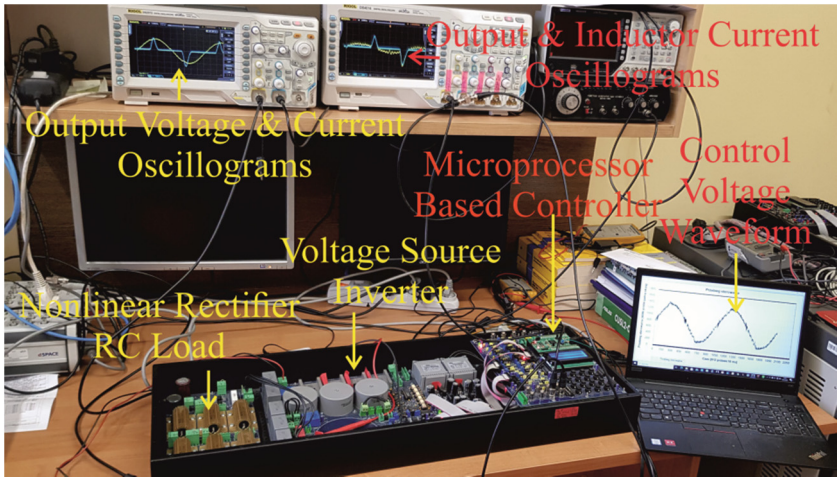
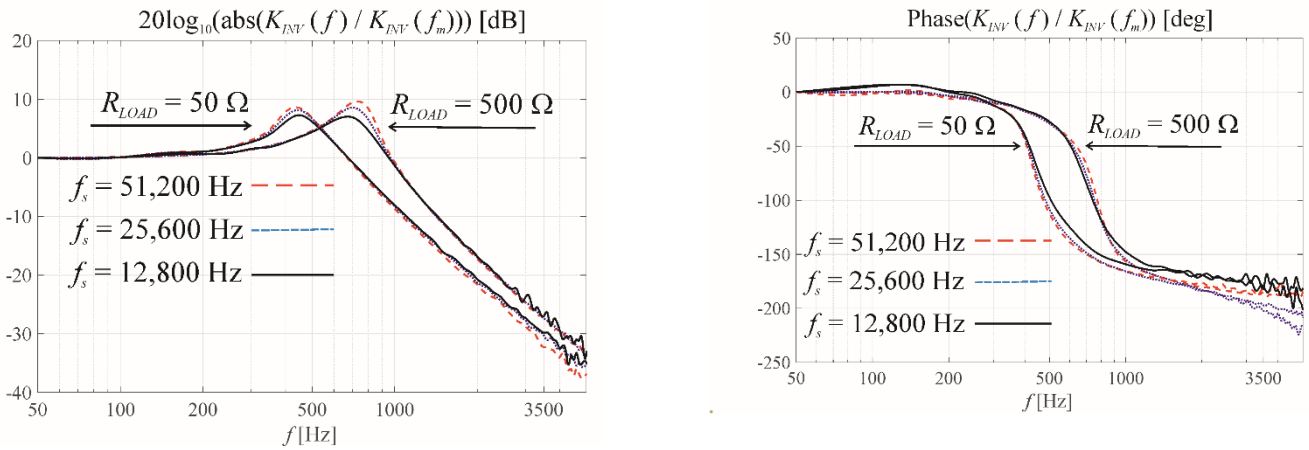


Figure 7. Experimental laboratory inverter.

Figure 8 shows the Bode plots of the plant (the inverter with PWM modulator). The Bode plots were measured for the relative amplitude values of the sinusoidal waveforms and phases for frequencies ranging from 100 Hz to 5000 Hz relative to the fundamental frequency (50 Hz) waveform in the input of the PWM modulator and the fundamental frequency waveform of the output voltage of the inverter. A relative measurement was required because the modulator input uses modulator units (the maximum amplitude equaled 820 units for f_S = 51,200 Hz, 1640 for f_S = 25,600 Hz, and 3280 for f_S = 12,800 Hz), and the output voltage uses volts. This dimensionless measurement is precisely described in [22–24]. Figure 8 also shows that the switching frequency for the coil with the Super-MSS core did not significantly influence the Bode plots of the inverter.



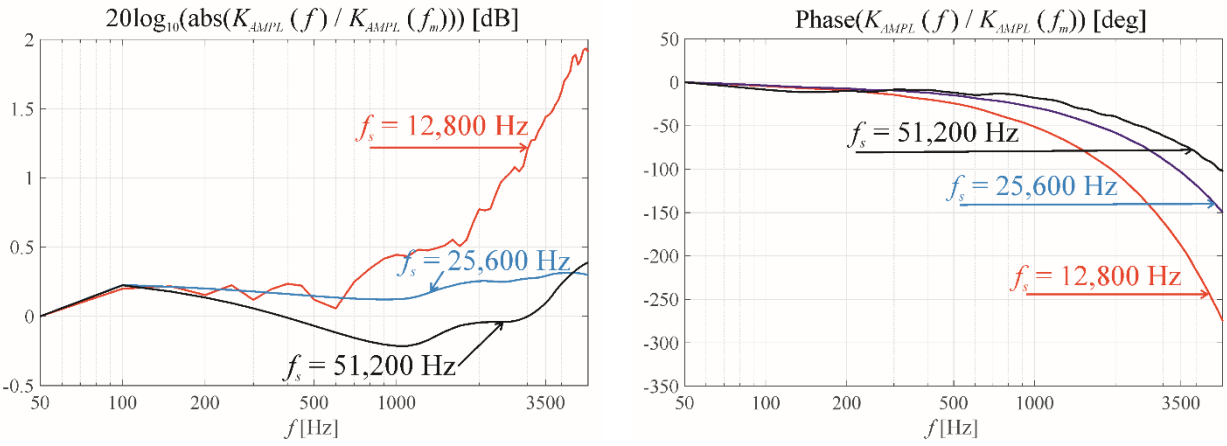
(**a**) (**b**)

Figure 8. Bode magnitude (**a**) and phase (**b**) plots for f_S = 12,800 Hz, 25,600 Hz, and 51,200 Hz, and two loads—50 and 500 Ω.

The other components of the experimental model were the measurement traces (including an Analog-to-Digital Conversion—ADC) of the output voltage, output current, and coil current. All traces were similar except for the sensors that ensured galvanic isolation (isolated amplifier ISO 124P in the output voltage trace and LA-25NP current transducers in the output current and the inductor current traces). Both sensors had a much higher bandwidth than the plant and the rest of the measurement trace (ISO 124P has a small-signal bandwidth of 50 kHz and a slew rate of 2 V/µs, and LA-25 NP has a bandwidth of 150 kHz). Therefore, the dynamic characteristics (the magnitude and the phase) of the output voltage measurement trace should represent all three traces up to 5000 Hz. Figure 9a,b give the Bode plots of the output voltage measurement trace (including the galvanic isolation and ADC).

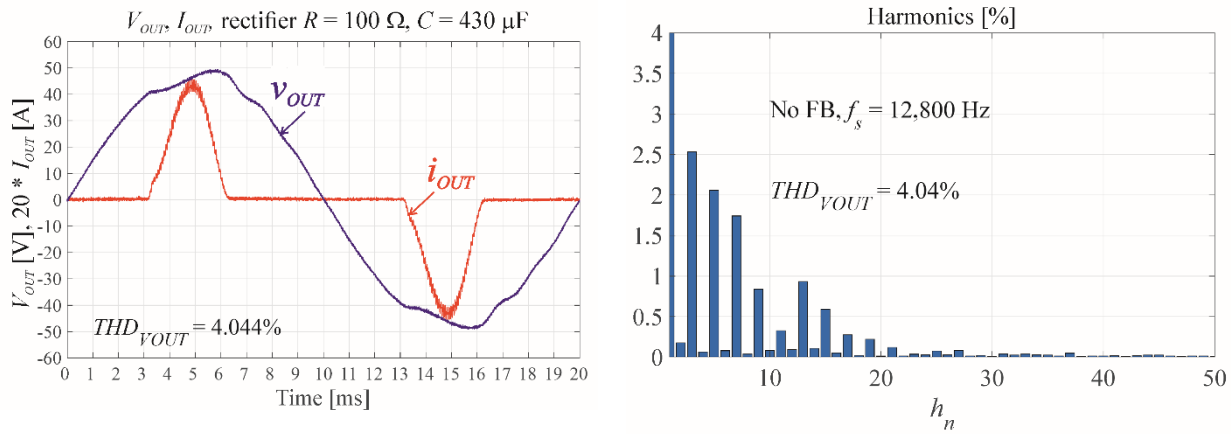
The relative magnitude of the traces was approximately 0 dB (from −0.25 dB to 0.4 dB for f_S = 25,600 Hz, and 51,200 Hz), and the phase-shifted. We can approximate the magnitude and the phase plots with the simple delay $2T_s$ (two switching periods). It seemed that output voltage damping 40 dB/decade over the resonant frequency (712 Hz) sufficiently maintained the phase margin of the loop. There were no additional low pass filters (except for the antialiasing filters). However, for gains over the border values, the oscillations could have come from a phase delay of the entire loop; a higher switching frequency corresponds to a smaller loop delay and higher frequency oscillations. The amplification of the voltage trace was adjusted so that for the output nominal amplitude of the output voltage fundamental harmonic for the 50 Ω load, we could read 3000 units of the ADC (it ranged from −4095–+4095). This was treated as the voltage scale ratio equal to unity. For the 50 Ω load resistance, which was assumed as nominal, we adjusted the amplification of this current trace to get 2000 units from the ADC reading. Therefore, the output current scaling ratio was (3000/2000)/50 = 0.03. For the small output capacitor (1 µF), the same adjustment procedure was performed for the inductor current trace to obtain

the same current scaling ratio of 0.03. It was important to adjust the voltage and current scaling factors carefully because they were multiplied by the PBC controller gains. In the simulations, the voltage and current scaling factors were simply $1/V_{DC}$ for the maximum amplitude of the reference waveform equal to 1. For the experimental inverter, the reference amplitudes were 3280, 1640, and 820 for the 12,800 Hz, 25,600 Hz, and 51,200 Hz switching frequencies, respectively. In all cases, we used 3000 units for the voltage and 2000 units for currents as nominal ADC values. Therefore, to compare the simulation and the experiment, the experimentally assigned gains were multiplied by r(12,800 Hz) = 3000/3280 = 0.915, r(25,600 Hz) = 3000/1640 = 1.829, and r(51,200 Hz) = 3000/820 = 3.659 for 12,800, 25,600, and 51,200 Hz. The recalculated gains were assigned as $R_i' = r^*R_i$ and $K_v' = r^*K_v$. Figures 10–14 present the results of the PBC control for the border gains and the values above them.



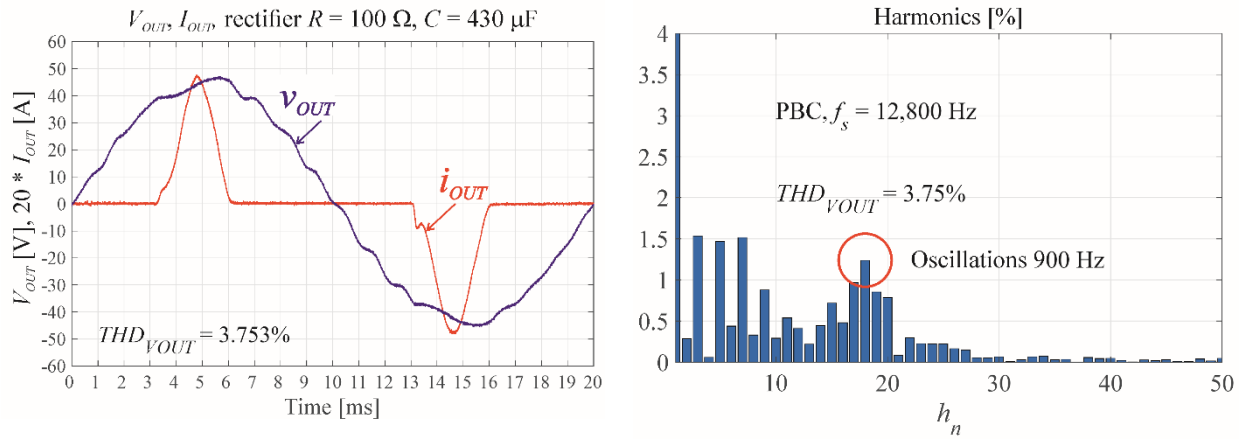
(**a**) (**b**)

Figure 9. Bode magnitude and phase plots of the output voltage measurement trace for f_s = 12,800 Hz, 25,600 Hz, and 51,200 Hz: (**a**) Magnitude; (**b**) Phase.



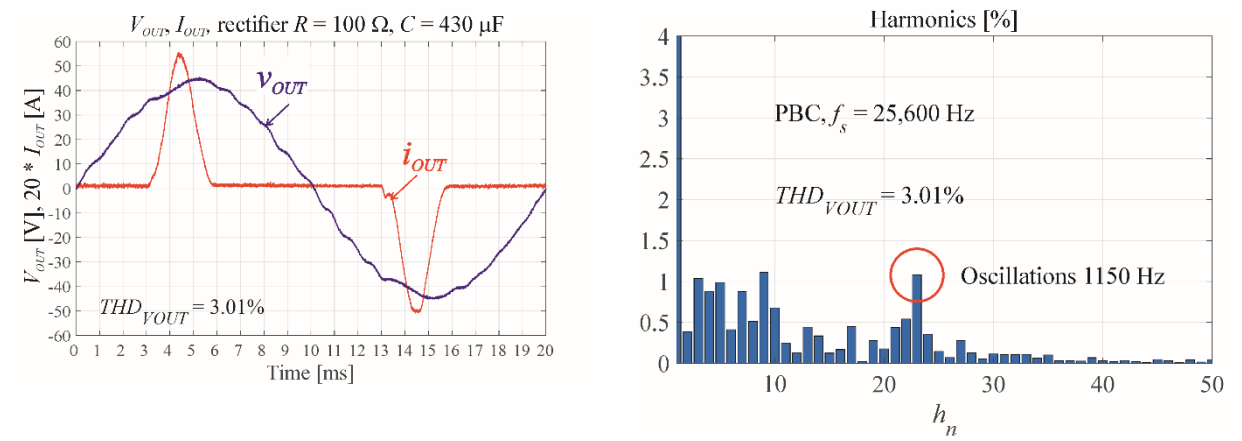
(**a**) (**b**)

Figure 10. (**a**) The output voltage and current; (**b**) The harmonics analysis of the output voltage without the feedback loop for f_s = 12,800 Hz (RC load: R = 100 Ω, C = 430 μF).



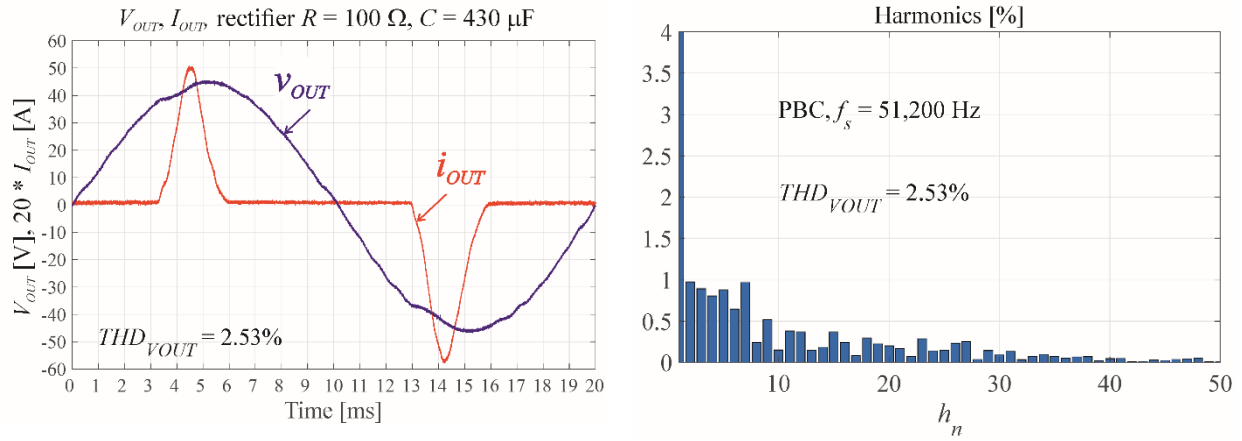
(**a**) (**b**)

Figure 11. (**a**) The output voltage and current; (**b**) The harmonics analysis of the output voltage for the PBC with experimentally adjusted border gains (R_i = 2, K_v = 0.2, R_i' = 1.83, K_v' = 0.183) for f_s = 12,800 Hz (RC load: R = 100 Ω, C = 430 μF); (**a**, **b**) Harmonics analysis of the output voltage.



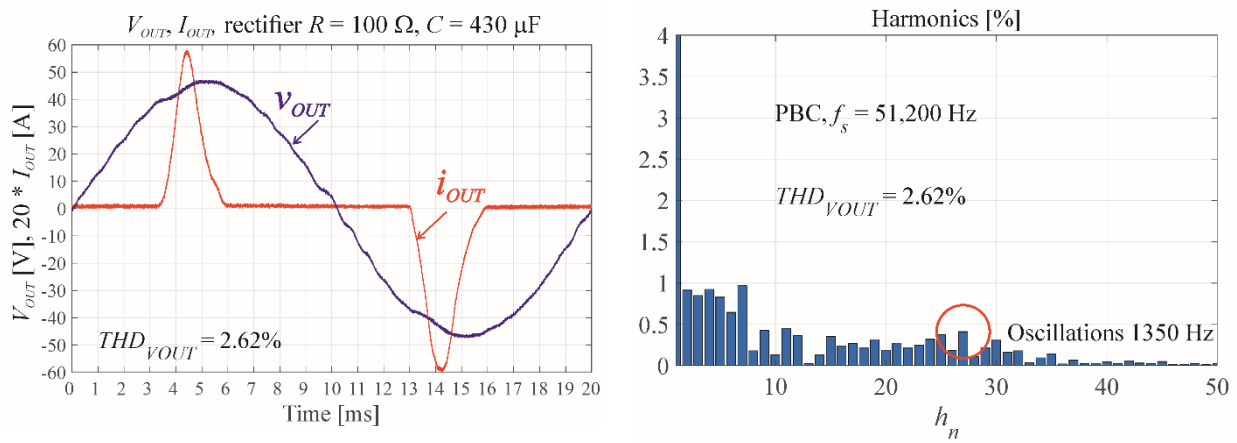
(**a**) (**b**)

Figure 12. (**a**) The output voltage and current; (**b**) The harmonics analysis for the PBC with the experimentally adjusted border gains (R_i = 3, K_v = 0.5, R_i' = 5.49, K_v' = 0.92) for f_s = 25,600 Hz (RC load: R = 50 Ω, C = 430 μF).



(**a**) (**b**)

Figure 13. (**a**) The output voltage and current; (**b**) The harmonics analysis for the PBC with the experimentally adjusted border gains (R_i = 3, K_v = 0.5, R_i' = 10.98, K_v' = 1.83) for f_s = 51,200 Hz (RC load: R = 100 Ω, C = 430 μF).



(**a**) (**b**)

Figure 14. (**a**) The output voltage and current; (**b**) The harmonics analysis of the output voltage for the PBC with gain values that exceeded the experimentally adjusted border gains (R_i = 3, K_v = 0.7, R_i' = 10.98, K_v' = 2.56) for f_s = 51,200 Hz (RC load: R = 100 Ω, C = 430 μF).

7. Discussion of the Experimental Results

The recalculated (R_i', K_v') experimental border gains differed from those previously appointed theoretically: R_i = 5, K_v = 0.23 vs. R_i' = 1.83, K_v' = 0.183 for 12,800 Hz, R_i = 10, K_v = 0.69 vs. R_i' = 5.49, K_v' = 0.92 for 25,600 Hz and R_i = 20, K_v = 1.41 vs. R_i' = 10.98, K_v' = 1.83 for 51,200 Hz. Figure 15 presents the recalculated values of the border gains R_i', K_v', which closely approximated the theoretically appointed border gain curves. Higher switching frequencies led to better compatibility of theory and measurements.

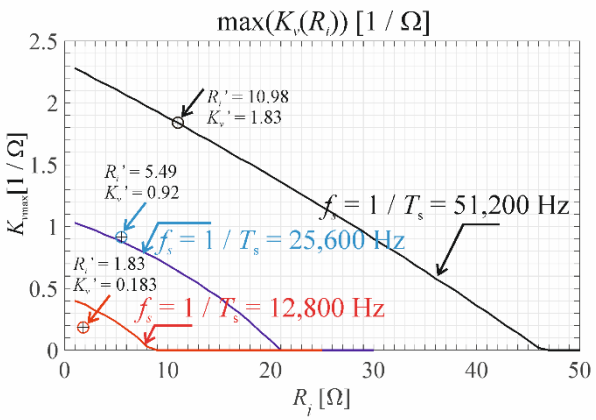


Figure 15. The recalculated values of the border gains R_i', K_v' for the experimental model vs. the theoretically appointed border curves.

The theoretical results were perfect. The experimental inverter had voltage and current measurement traces from which the Bode plots (Figure 9a,b) approximated as a delay of about $2T_s$ [24]. Higher switching frequencies led to better agreement between simulation and experimental results (Table 2). Lower measurement trace delays ($2T_s$; Figure 9) resulted in higher possible gains and lower output voltage distortions. However, the 40 dB/decade damping of the plant (inverter) above 700 Hz (in the presented experimental model) should maintain a safe phase margin. The linearization of the inverter model at higher switching frequencies resulted in a lower error because there was a more precise linear approximation of the exponential function (used in the discrete model [19,20]) for shorter switching periods. Measurement trace delays led to lower gain oscillation values (above the border values) than in simulations. At higher switching frequencies, the oscillation frequencies increased (the measuring trace delays decreased with switching frequency)—900 Hz for

f_s = 12,800 Hz, 1150 Hz for f_s = 25,600 Hz, and 1350 Hz for f_s = 51,200 Hz. The power loss increases in the core of the coil between two sets of gains R_i = 3, K_v = 0.5, R_i' = 10.98, K_v' = 1.83 (close to the border values) and R_i = 3, K_v = 0.7, R_i' = 10.98, K_v' = 1.83 above the border values was 18.6%.

Table 2. Experimental results: Comparison of the parameters of the inverters output voltage with C_F = 50 µF, L_F = 1 mH, R_{LF} = 1 Ω, M = 0.5, RC load: R = 100 Ω, C = 430 µF, dynamic loads (500||50)/500 Ω).

Switching Frequency, Gains: R_i [Ω], K_v [1/Ω]		**THD_{VOUT} (Rectifier RC Load, R = 50 Ω, C = 430 µF)**	**Power Losses Increase ΔP_{losses}**	**Overvoltage for the Step Load Decrease (500||50)/500 Ω**
12800 [Hz], R_i = 2, K_v = 0.2 R_i' = 1.83, K_v' = 0.183	Border gains	3.753%	-	6%
25600 [Hz], R_i = 3, K_v = 0.5 R_i' = 5.49, K_v' = 0.92	Border gains	3.01%	-	5.5%
51200 [Hz], R_i = 3, K_v = 0.5 R_i' = 10.98, K_v' = 1.83	Border gains	2.53%	-	5%
51200 Hz, R_i = 3, K_v = 0.7 R_i' = 10.98, K_v' = 2.56	Above the border values	2.62%	18.6%	3.5%

The IPBC controller design should begin by calculating the border curve from simulations for the particular parameters of the inverter and the chosen switching frequency (Figures 2d, 3d and 4d). Then we should appoint the recalculated gains R_i', K_v' on or below the border curve. We physically adjust the output voltage amplifiers to obtain the assigned value (in units) ADC_V of the ADC for the amplitude of the nominal voltage. After such an operation, we assign a unity gain in the voltage amplification trace (in our example ADC_V = 3000 for the nominal output voltage amplitude). We adjusted the output current amplifiers to obtain the assigned value (in units) ADC_I of the ADC (in our example ADC_I = 2000) for the amplitude of the output current for the nominal resistive R_{NOM} load. For the lowest possible output capacitor, we proceeded the same way for the inductor current. The scaling ratios of voltage and currents were s_v = 1, $s_I = (ADC_V/ADC_I)/R_{NOM}$ (in our example s_I = 0.03). These scaling factors were implemented in the inverter control software. For the PWM comparator input frequency f_{PWM} (in our example, f_{PWM} = 84 MHz) and the switching frequency f_s (in our example, 12,800, 25,600, and 51,200 Hz), we determined the maximum amplitude of the reference waveform f_{PWM}/f_s (in our example, it was 3280, 1640, or 820). That meant we should use the recalculation factor $r = ADC_V/(f_{PWM}/f_s)$ (for us, it was r(12800 Hz) = 0.915, r(25600 Hz) = 1.829, and r(51200 Hz) = 3.658 for f_s = 12800, 25,600 and 51,200 Hz). If we chose the recalculated PBC gains R_i', K_v' from the border curve, we can calculate the PBC gains that we have to use in the inverter software $R_i = R_i'/r$, $K_v = K_v'/r$.

8. Conclusions

The paper presents the basic reasons for restricting PBC controller gains. Previously reported basic theoretical considerations showed that positive PBC gains have no limitations and the poles of the characteristic equation of the closed-loop system were always in the left half of the *s*-plane. However, the first limitation is the control signal speed increase above the possible speed of the increase in a PWM double edge, three-level modulator. The second limitation was modulator signal saturation. This limitation could be relaxed for the tolerably lower inductance of the output filter coil or the lower modulation index [12]. The third limitation came from delays in the measurement traces (depending on the design) and in the same PWM modulator (it is always one switching period). The delay of the PWM modulator was considered in the control law using the state space equations to predict the state variables of a discrete, linearized inverter model. A more sophisticated solution involves using a Luenberger state observer; however, the final equations were extremely complex, and theoretical results showed that the use of simple state space equations sufficed. Higher switching frequencies resulted in higher PBC controller gains and lower output voltage distortions. The simulations and the experimental model had different

scaling coefficients of the voltage and currents. That explains why the border gains of the controller in the simulations and the directly adjusted gains (R_i, K_v) in the experimental model were different. However, after recalculation of the adjusted experimental model border gains with the scaling factors that differed significantly from simulation results, the recalculated gains (R_i', K_v') closely approximated the theoretical border curves (Figure 15). The most general conclusion drawn in the paper stems from the possibility of using higher PBC gains for higher switching frequencies, and better reduces output voltage distortions for standard linear and nonlinear loads.

Author Contributions: Conceptualization, Z.R. and K.B.; methodology, Z.R. and K.B.; software, Z.R.; validation, Z.R. and K.B.; formal analysis, Z.R. and K.B.; investigation, Z.R. and K.B.; resources, Z.R. and K.B.; writing—original draft preparation, Z.R.; writing—review and editing, Z.R. and K.B.; visualization, Z.R.; supervision, Z.R.; project administration, Z.R. and K.B.; funding acquisition, Z.R. and K.B. All authors have read and agreed to the published version of the manuscript.

Funding: The authors were supported by a pro-quality grant of the Rector of the Silesian University of Technology, Zbigniew Rymarski, grant number: 02/140/RGJ21/0013 and Krzysztof Bernacki 02/140/RGJ21/0011. This research was partially supported by the Polish Ministry of Education and Science funding for statutory activities (BK/RAU11/2021).

Institutional Review Board Statement: Not applicable.

Informed Consent Statement: Not applicable.

Conflicts of Interest: The authors declare no conflict of interest.

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