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New Nine-Level Cascade Multilevel Inverter with a Minimum Number of Switches for PV Systems

Ali Abedaljabar Al-Samawi [1,2,*] and Hafedh Trabelsi [1]

[1] Department of Electrical Engineering, Computer and Embedded Systems Laboratory (CES-Lab), National Engineering School of Sfax (ENIS), Sfax University, Sfax 3038, Tunisia
[2] Department of Electronic and Communications Engineering, College of Engineering, Al-Muthanna University, Samawah 66001, Iraq
* Correspondence: aliasamaw@mu.edu.iq

Abstract: To support the grid system with high power quality from photovoltaics (PVs) and reduce the partial shading condition (PSC) effect of the PV system, as well as the mismatch power issue, in this study, we present a simple single-phase, nine-level cascade inverter architecture for photovoltaic (PV) systems with a minimum number of power components and passive parts. This reduction in the number of switches decreases the switching losses and the number of driving circuits, which causes a reduction in the complexity of the control circuit and hence reduces the cost and size. The suggested inverter shows a lower output voltage total harmonic distortion (THD) and unity power factor. In addition, this inverter's control and switching techniques are far simpler than those of recently published designs. To evaluate the performance of the proposed inverter, we performed a comparison of the cascaded multilevel inverter (CMLI) topology, which required recent cascade topologies with the same nine voltage levels. The comparison depends on parameters such as the number of components (diode and capacitors) and the number of active switches in the inverter, in addition to total harmonic distortion. MATLAB/Simulink models for a grid-tied solar system PV application driven by the proposed nine-level inverter were built for design and validation.

Keywords: nine-level inverter; cascade multilevel inverter; PV system; minimize the number of switches; new single-phase inverter; THD

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1. Introduction

As a result of the rapid growth in the world's energy demand, many fossil fuels have been burned, which has had a negative effect on the environment. Solar, wind, and geothermal energy are just a few examples of the many renewable resources. Photovoltaic (PV) cells are commonly employed for solar energy conversion into electrical energy [1–3]. Systems for solar energy conversion include converters and a control unit that regulates the amount of power that PV cells can produce. To optimize the potential of PV cells, the front-end stage DC/DC must be adapted to power variation and increase efficiency [2,3].

Three-level converters were the first multilevel converters attempted in 1975 [4]. A multilevel inverter is connected with a PV system for the power system [5–9], followed by several other multilevel inverter (MLI) topologies [6–68].

MLIs can be categorized in to three main groups depending on the number of DC sources used in their topology: neutral-point diode-clamped (NPC), flying capacitor (FC), and cascaded H-bridge (CHB) [12–15] are the most common topologies in the industry to date. However, cascaded multilevel inverters (CMLI) are more suitable for photovoltaic applications because each PV array is a separate DC source [5]. A cascaded MLI arrangement is used for most studies [23–35]. Maximum power point tracker (MPPT) techniques with a DC/DC converter [36,37] are used to obtain high power and improve the efficiency of the PV system.

An MPPT is used to track the maximum power point following changes in the irradiation or temperature. Independent MPPT controllers are used with PV panel strings on individual DC links to solve the problem of a partial shading condition (PSC) of panels in PV arrays due to shading caused by static and moving objects, such as trees, buildings, birds, cumulative dust on panels, or clouds. Researchers have discussed solutions to the problem of a partial shading condition, which decreases output power and contributes to problems caused by hot spots, which ultimately result in malfunction of shaded modules [38–40].

Reference [38] shows a PV system connected to an array with a DC/DC boost converter to control its terminal voltage by adding a bypass diode in parallel with each PV module, thus avoiding hotspot phenomena; however, this approach causes multiple peaks in the power of the PV array, limiting the application of MPPT techniques and leaving researchers to focus on identifying novel techniques. Other studies have shown that this problem can be solved using multi-PV arrays with an interleaved boost converter (IBC) to reduce the ripple current, improve the power quality, adjust the DC-link voltage, and allow for the use of an independent MPPT control for each PV array to obtain high output power and increased efficiency [39].

Reference [40] showcases the use of a cascaded multilevel inverter to enhance the power quality of grid-connected PV systems under partial shading using individual panels or a small string on a separate DC link with an independent MPPT controller. Therefore, among the main types of multilevel inverters, a cascaded multilevel inverter (CMLI) (multisource) is most suitable for photovoltaic applications because each PV array is a separate DC source [5].

MLIs, on the other hand, are based on the idea of synthesizing a stepped voltage waveform using multiple DC sources and multiple low-power-rated semiconductor switches to achieve higher levels of power generation. Various energy sources, such as PV panels, batteries, fuel cells, and capacitors, can be used as multiple-input DC sources. When multiple DC sources are combined to produce a high-voltage output, power switches are controlled by algorithms [13–15]. For example, multilevel inverter (MLI) topologies are used in grid-connected renewable energy systems (RES) as an advanced power converter topology. Current MLI trends emphasize decreasing the number of switches and gate driver circuits to improve the power quality and fault tolerance, making the system more cost-effective for grid-connected renewable energy sources [5–10].

Modern power systems use MLIs because of their low total harmonic distortion (THD) and electromagnetic interference, as well as their ability to enhance power quality and rating demands. Compared to conventional two-level inverters, which use high switching frequency pulse width modulation (PWM), an MLI has several advantages [13–16]. One of the essential advantages of a multilevel inverter is the small size of the filter and its low cost compared with a two-level inverter. A multilevel inverter reduces total harmonic distortion (THD) compared to two-level inverters by using multiple DC sources. Other advantages include lower switching frequency, low cost, higher switching speed, and lower-voltage switches than those typically required in two-level inverters, resulting in lower switching losses, high-voltage generation, low levels of electromagnetic interference (EMI), and good power quality [5].

To increase the power quality and dynamic performance of demanding systems, multilevel inverters are currently considered an industrial solution [5]. Due to their low THD output waveform and limited device rating, MLIs make excellent high-voltage devices [42]. Solar PV applications, wind turbine systems, and fuel cells can be integrated with multilevel converters [3,5–10]. PWM control algorithms used with MLIs significantly impact their efficiency, power ratings, and applications [15]. Over the past few decades, several studies have proposed various MLI topologies with a reduced number of switches [18–35,51–65].

However, the development of new multilevel inverters is still influenced by current trends, resulting in alterations of the built-in structure. The authors of previous studies have proposed seven-level inverters and other multilevel topologies [42–49]. For example, a

conventional CMLI was reduced by three switches, resulting in a seven-level MLI with nine switches [42], achieving low THD and promising results. It was found that the seven-level MLI eliminated an additional two controls compared to the prior layout [43,44]. A topology with six switches and three DC sources resulted in seven levels, and another multilevel topology [45–47] with just five switches and four DC sources also resulted in a seven-level MLI topology [48]. Researchers have also discussed multilevel inverters with three sources seven switches, and seven levels [51]. As a result of the reduced THD and the smaller number of gate circuits required to drive the switches, the topology switch design has undergone a considerable shift in recent years.

The simplicity of CMLI is highlighted by attempts to create five-level systems with eight switches, seven-level systems with twelve switches, nine-level systems with sixteen switches, etc., with conventional cascade topology [5,17]. However, increasing the number of levels also necessitates an increased number of switches, contradicting the claim that CMLI is simple approach. Therefore, the primary goal of the present study was to determine how to reduce the intricacy of the circuit through the concept of "switch minimization". After investigating the topologies of existing seven-level systems, we reduced the number of switches from 12 to 9, then to 7 and, finally, to 6.

The proposed architecture involves five switches for seven levels, representing the maximum reduction in the number of switches with the aim of reducing complexity [17]. As a result of this change, the new MLI configuration comprises five switches, a seven-level topology [47], and four DC input sources to afford a seven-level output. The more switches we utilize, the more expensive it is to design a circuit. No PWM is required for verification of circuit validity.

The pulse width modulation (PWM) technique is associated with benefits such as ease of implementation, improved performance, and limited loss of power in the switching devices [49]. The tree main types of level-shifted pulse width modulation (LS-PWM) are phase disposition (PD), phase opposition disposition (POD), and alternative phase opposition disposition (APOD). In general, phase disposition (PD) is appropriate for reducing the THD of cascade multilevel inverters [5,17]. We used multicarrier PD simulations to evaluate performance of the circuit.

2. Materials and Methods

2.1. Conventional Nine-Level Cascade Topology

In the traditional CMLI shown in Figure 1, four H-bridge units, each with four switches, are used with four DC voltage sources to provide 16 switches. m = (n + 2)/2, where n is the number of switches in the setup. + Vdc, −Vdc, and zero are outputs from each bridge. Stepped nine-level staircase waveforms are generated by cascading four bridges [5,12–16,48,50].

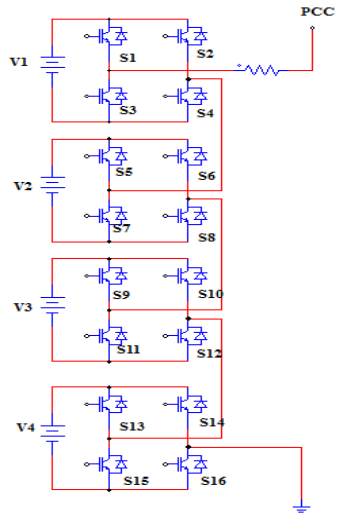

Figure 1. Traditional nine-level cascade inverter [50].

2.2. Other Topologies

The existing topology involves a total of 7 levels and 7 switches, as depicted in Figure 2. Three DC sources, one H bridge with four switches, and three more switches are used to produce nine stepped levels for positive and negative half cycles in the architecture depicted in Figure 2 [51].

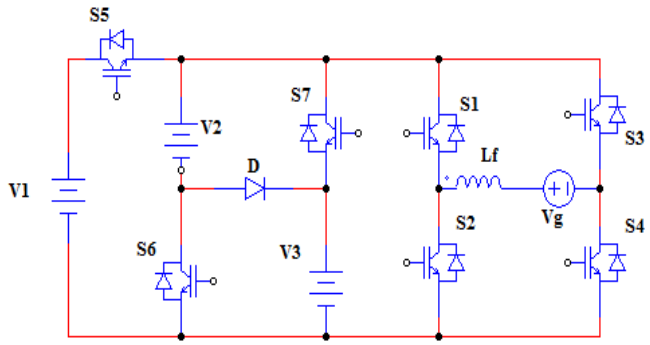

Figure 2. Seven-switch, seven-level topology [51].

Figure 3 depicts a topology with nine levels, nine switches, two capacitors, and two diodes [52]. The only H bridge in the topology is used primarily for polarity transitions. To generate the levels, at least four switches are active in a given state.

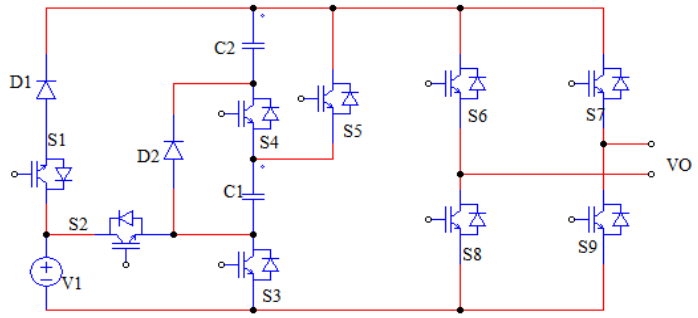

Figure 3. Nine-switch, nine-level topology [52].

The cascaded multilevel inverter produces a 9-level topology [53] with a reduced number of switches (10) and four DC sources, as shown in Figure 4.

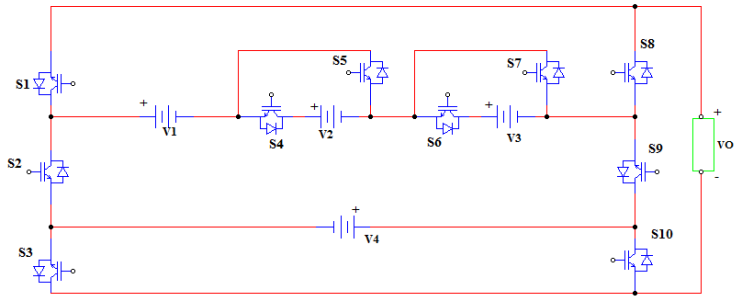

Figure 4. Ten-switch, nine-level topology [53].

Figure 5 depicts the nine-level inverter under investigation [54]. It includes a DC voltage source (representing the output of the DC–DC converter fed by solar panels PV applications), a capacitor, and eight switches (Si, i = 1... 8), two of which are bidirectional (S2 and S5). Switches S1 and S4, which connect the DC link to the inverter's positive output terminal, operate in a complementary manner, with only one of them at a given time. The

inverter's negative output terminal is connected to the capacitor via switches S3 and S6, which work similarly. There is a complementary relationship between the DC link and the four switches of the capacitor.

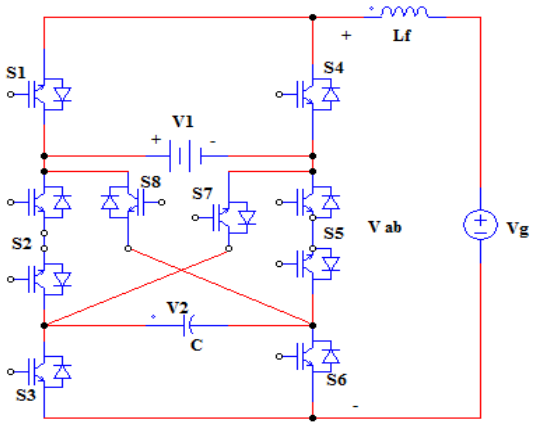

Figure 5. Eight–ten-switch, 9-level topology [54].

The new multilevel topology has 9 levels and 10 unidirectional switches, as shown in Figure 6 [55]. The number of components was reduced, and MLI topology was developed to generate all conceivable output voltage combinations of DC input levels. Cascading the proposed inverter causes a positive output voltage level. The entire bridge inverter is connected in series with the proposed unit to change the polarity and produce output waveforms with positive and negative output voltage levels. It is possible to run the MLI at two different switching frequencies. The proposed architecture was evaluated with a trinary sequence DC source to provide a higher output voltage level with a minimal DC source count compared to other arrangements of DC sources, such as symmetric, natural, and binary arrangements.

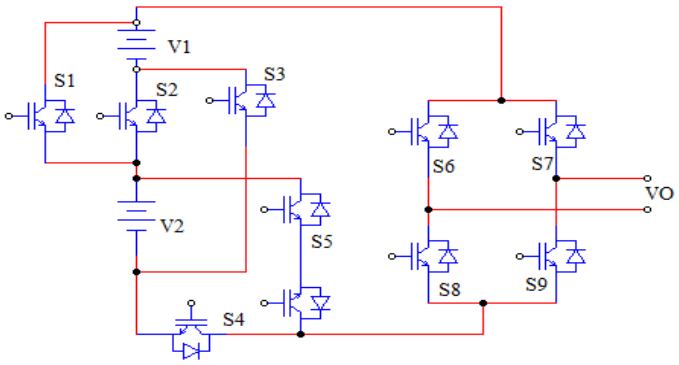

Figure 6. Nine-ten-switch, 9-level topology [55].

The number of switches was reduced to obtain a nine-level cascaded transformer multilevel inverter. When using cascaded transformers and multilevel inverters, the proposed topology requires only one DC source to supply a local load or grid with all the power it needs. Batteries, solar panels, fuel cells, and similar power sources can serve as DC sources. Figure 7 [56] depicts the proposed topology, including four legs, each with two unidirectional switches (8 switches). In each transformer, two separate legs are connected to each of the two arms. Additionally, the secondary side of two adjacent transformers must be symmetrical.

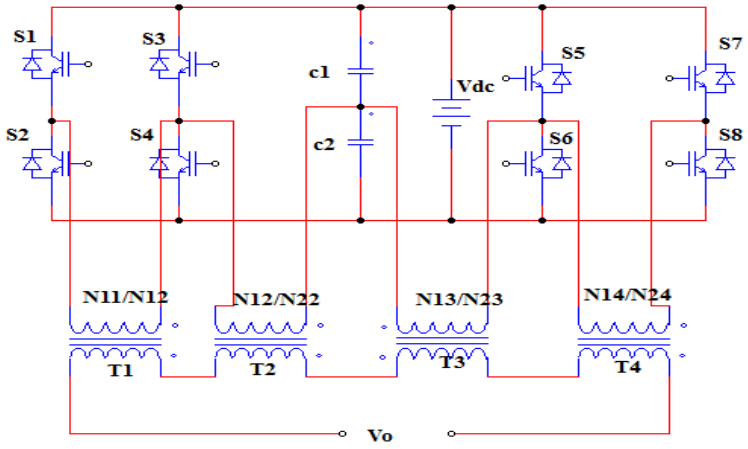

Figure 7. Eight-switch, nine-level topology [56].

The proposed multilevel topology with nine levels, nine switches, four capacitors, and three diodes is shown in Figure 8 [57]. A single-phase MLI based on a switchable capacitor network with the voltage gain of 4 is proposed. It only uses nine switches and three diodes to achieve a nine-level function, resulting in a common control ratio for each level. A multicarrier PWM technique is used to operate the proposed inverter in various states. In the interest of avoiding the employment of high-voltage semiconductor devices, we conducted a theoretical analysis, which revealed that the voltages across the switches and diodes are all lower than the maximum output voltage, reducing the total conduction and switching losses. We considered the merits and disadvantages of several SC-based boost MLIs when evaluating the qualities mentioned above. We verified the viability of the proposed design by conducting tests with a 1 kVA inverter prototype, MLIs can also be applied to three-phase systems to obtain higher voltages between lines. Therefore, they can be used for various applications, including renewable generation systems. A boost-type DC–AC power converter with high-voltage gain and low-voltage stresses is desired while minimizing the switch count and employing a single DC source.

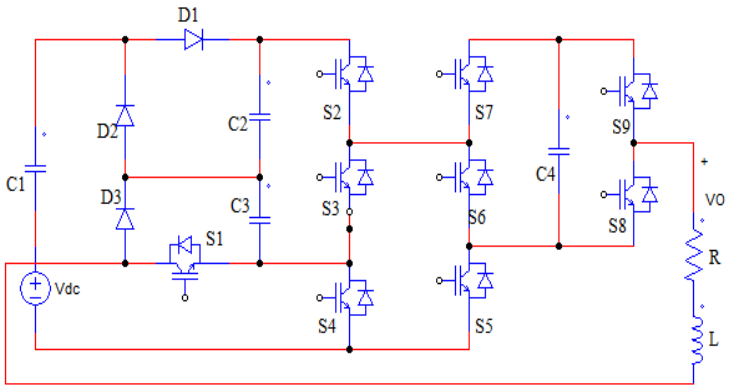

Figure 8. Nine-switch, nine-level topology [57].

The new multilevel topology involves nine levels with twelve switches and four capacitors, as shown in Figure 9. The hybrid nine-level inverter (H9ISPC) described in [58] is shown in Figure 9, with an input voltage source (V1), three capacitors (C1–C4), and twelve switches (S1–S12). The voltage of each capacitor is naturally maintained by the H9ISPC, which generates a nine-level bus voltage with fewer components than typical nine-level inverters. Designed for step-down operation, the circuit is shown below. Capacitors can be regarded as constant voltage sources because they maintain a constant voltage. The H9ISPC can be used as a step-up inverter by rearranging the capacitors and voltage sources. Floating power sources can replace either the C1 or C2 capacitors or the C3 or C4 capacitors,

depending on your preference. Double boosting is achieved in the first instance, whereas quadruple boosting is achieved in the second instance. Quadruple boosting circuits is the topic of this research. Figure 2 in [58] depicts the circuit topology of the inverter under consideration. The switched capacitor cells could be increased to obtain an inverter with more levels and a higher step-up ratio, as shown in [58]. Figure 3a in [58] depicts a 9 + 4x (x = 1, 2,...)-level extended circuit topology. For every additional switched capacitor cell (x), four switches and one capacitor are required. The bus voltage is (4 + 2x)Vin in amplitude, and the number of switches in the circuit is represented by 9 + 8y (y = 1, 2,...), as shown in Figure 3b in [58], where y is the number of additional switched capacitor cells. Three switches and a capacitor make up each cell. The bus voltage has an amplitude of (4 + 4y) Vin.

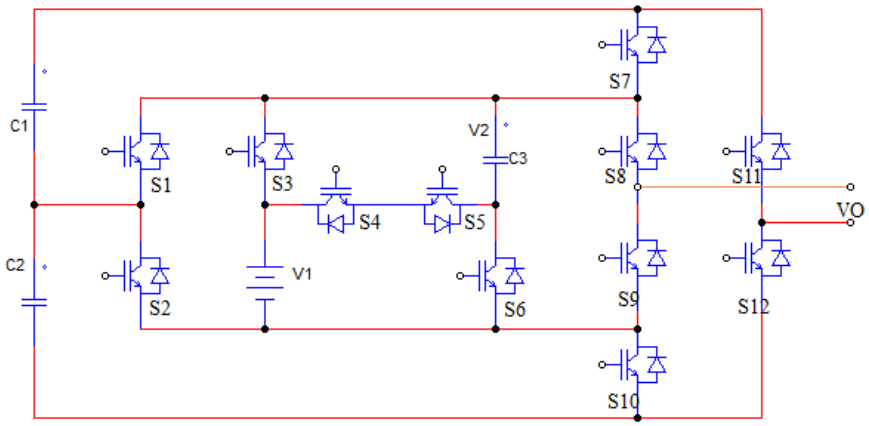

Figure 9. 12-switch, 9-level topology [58].

Figure 10 depicts a nine-level topology with eight switches, three capacitors, and three diodes [59]. The 9LSCI proposed in this study features quadruple boost, fewer components, self-balancing voltage, and inductive-load capability features. A backend H bridge is unnecessary in the proposed topology, as it uses only eight switches. Comparisons of the proposed design to other topologies show its strengths from various perspectives. An experimental prototype was built using the multicarrier PD PWM approach as a final step.

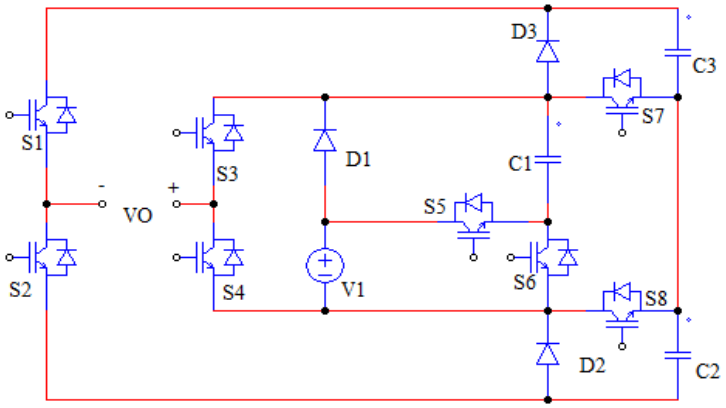

Figure 10. Eight-switch, nine-level topology [59].

Figure 11 depicts a topology with nine levels, nine switches, two capacitors, and two diodes [60]. The proposed 9L-SCMLI design was simulated using the MATLAB/SIMULINK software package to estimate its performance. The simulations showed that the multilayer voltage output of the designed converter is satisfactory, with minimal harmonic distortions. This architecture can be applied to high-voltage and medium-power applications. Various switching sequences were tested, and the resulting output voltages were

recorded and graphed several times. Furthermore, the proposed design was compared with other converters.

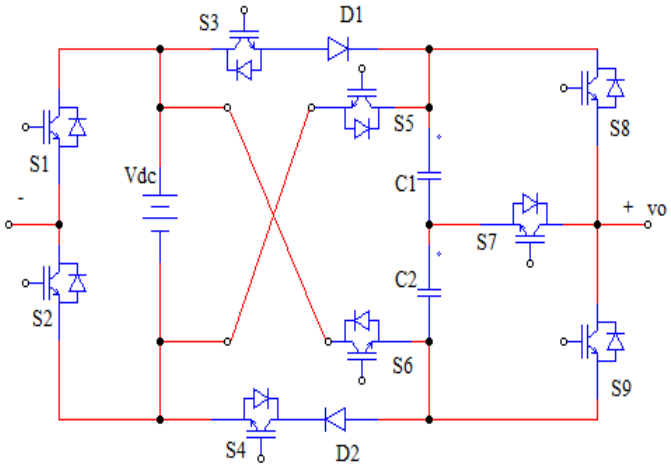

Figure 11. Nine-switch, nine-level topology [60].

The new multilevel topology involves nine levels, nine switches, and three capacitors, as shown in Figure 12. There are 10 switching devices (S1, S2,... S10) and body diodes (D1, D2,... D10) in the proposed single-phase, nine-level hybrid multilevel inverter, as shown in Figure 2 [61]. The topology can provide an output voltage waveform with a nine-level gradation using fewer switching devices. The cascading connection of three pieces creates this configuration. First, there are two L.F. switches. As mentioned in Section 2, CT2 LI has become a popular topology in recent years. Section 3 comprises a standard H bridge and F.C. (Ca). Sections 1 and 2 are connected by a single DC power supply and two DC link capacitors (Cd1 and Cd2). The A and N output terminals are wired to a single-phase R.L. load. It is possible to keep the voltage across the F.C. at a constant level by leveraging the redundant switching states accessible in Section 3. Assuming that the switching devices operate correctly, the suggested design creates an output voltage with a step size of Vdc/4, ranging from Vdc to + Vdc.

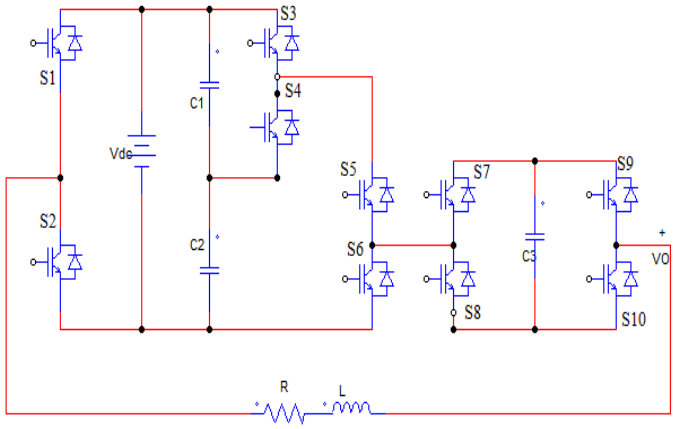

Figure 12. Ten-switch, nine-level topology [61].

Custom power devices have been increasingly important in the fight against power quality (P.Q.) problems. D-STATCOM plays a crucial role in eliminating harmonics and managing the real reactive power flows of electric power systems. As a result, one of the primary goals of this study was to compare the P.Q. of two unique power control algorithms. The focus of both techniques was to improve P.Q. for an SPV-fed cascaded NMLI (nine-level multi-level inverter) system. The implementation of D-STATCOM at the

point of common coupling justifies the increase in P.Q. Future research on multiple MLI topologies is expected to benefit from the SPV model provided here. In rural locations, solar-powered controllers could be designed to feed non-linear loads in a manner that is both efficient and affordable. The new topology involves nine levels with two dc source (PV system), eight switches and two transformers, as depicted in Figure 13 [62].

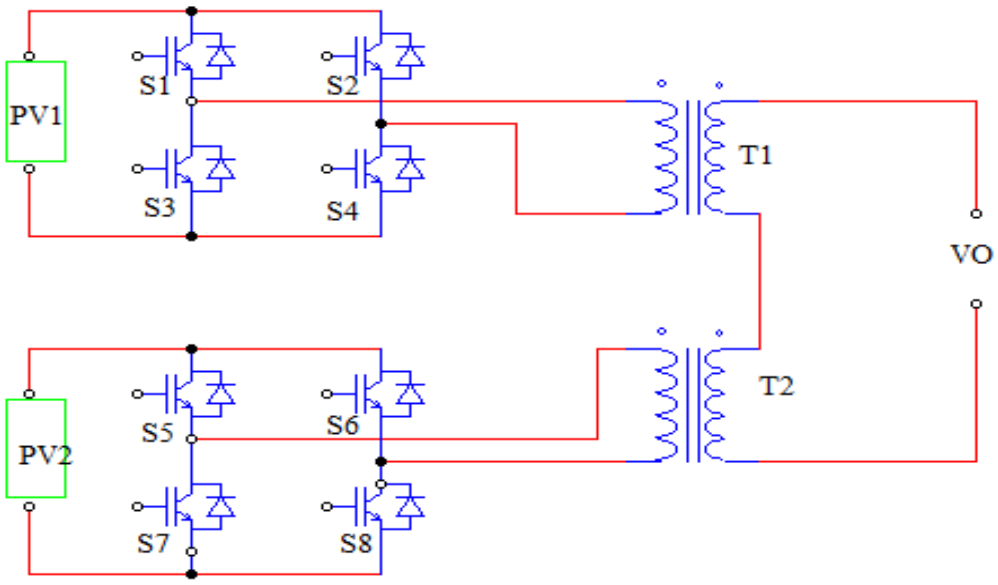

Figure 13. Eight-switch, nine-level topology [62].

Figure 14 depicts a nine-level switching capacitor MLI in single-phase mode proposed in [63]. The suggested topology involved boosted voltage and self-balanced capacitor voltage to control the switch states and generate various voltage levels [64]. Three capacitors (C1, C2, and C3), ten switches (S1 to S10), and a single input voltage source make up each phase. Low-voltage stress between the switches and capacitors, limited to Vdc, is an advantage of this architecture. The proposed circuit generates all possible voltage levels (0, 0.5 Vdc, Vdc, 1.5 Vdc, and 2 Vdc).

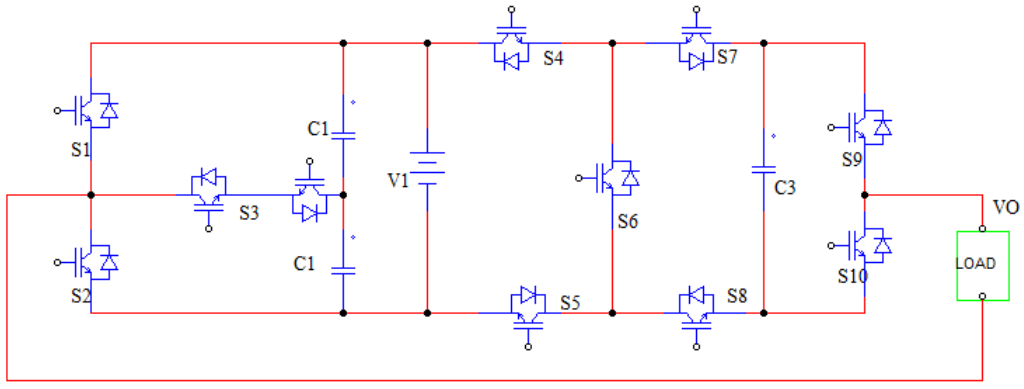

Figure 14. Ten-switch, nine-level topology [63].

Figure 15 depicts a nine-level multilevel inverter based on a T-type switched capacitor module with a reduced number of switches (S1–S10) and a single DC source with four capacitors and two diodes [64].

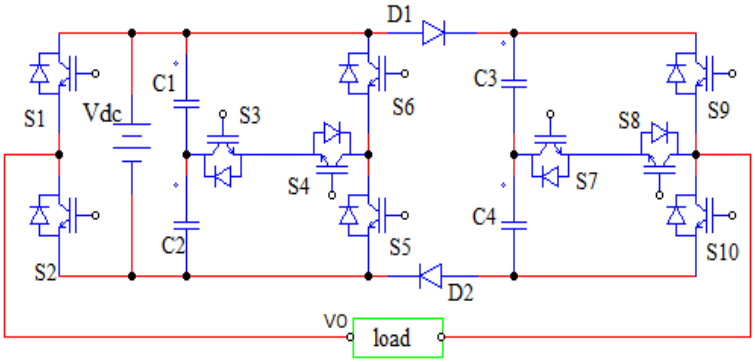

Figure 15. Ten-switch, nine-level topology [64].

Jafar Siahbalaee [65] compared a conventional multilevel inverter with a novel cascaded multilevel inverter to showcase several new cascaded topologies (NCTs) with nine levels, four DC sources, and multiple switches in each cascaded topology, as well as other indices. The cascaded nine-level topologies reviewed in [65] included an NCT with 11 switches, an NCT with 12 switches, and NCT with 13 switches, an NCT 8 switches, an NCT with 10 switches, an NCT with 11 switches, an NCT 8 switches, and NCT 10 switches, and an NCT with 10 switches.

In this paper, proposed nine-level has a reduced number of power switches (seven), with four separate DC sources, as shown in Figure 16. We compared the proposed topology with the conventional nine-level cascade topology, as well as the abovementioned topologies presented in fourteen literature reviews. The proposed nine-level inverter achieves superior performance relative to that of the topology shown in Figure 2, which has the same number of the switches but fewer levels (seven). In addition, the proposed inverter has a simple structure and simple switching states.

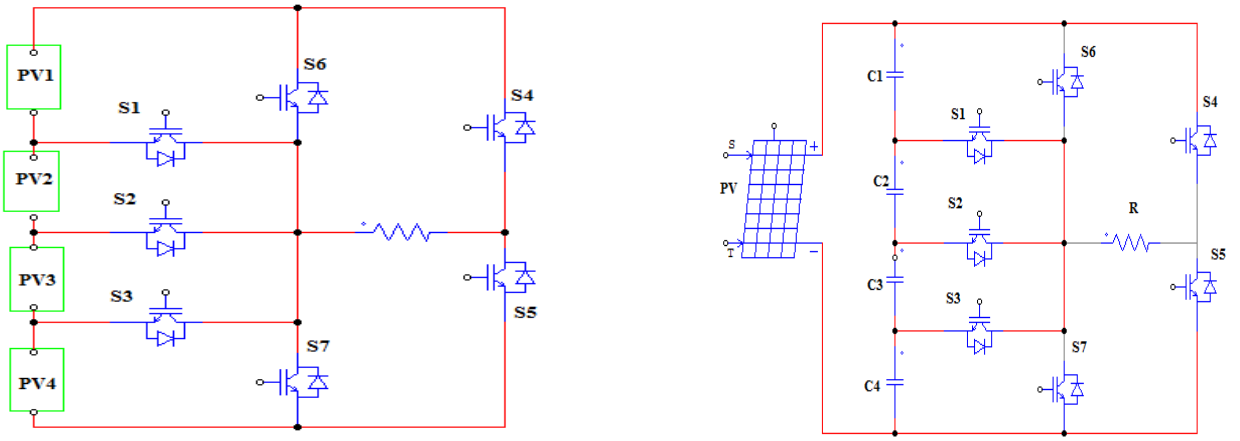

Figure 16. Nine-level, seven-switch proposed topology (**a**) based on four series of DC sources and (**b**) on a single DC source and four capacitors.

3. Proposed Inverter

The proposed nine-level MLI with seven switch and four independent DC sources is shown in Figure 16. Compared to traditional and existing topologies, this design is the simplest.

The number of output voltage levels for the proposed topology can be expressed as m = (2 × n + 1), where m = the number of the output voltage levels, and n = the number of DC sources.

The number of switches in the proposed cascaded multilevel inverter relative to conventional cascaded multilevel inverters can be determined by the following equation:

$$S_{proposed} = \left(m + \frac{S_{Conventional}}{n} + 1\right) \div 2 \quad (1)$$

where S = the number of switches.

The pulse-producing circuit topology of the proposed inverter differs from traditional designs so that it can generate a unique pulse pattern that triggers the switches at the appropriate moment. The output waveform is warped if switches S1, S2, and S3 are not all unidirectional. The circuit is compact and easy to operate thanks as a result of having fewer switches than traditional inverters. Because the proposed nine-level MLI uses only four DC sources, all sources are used, resulting in a reduction in switching losses. Furthermore, the proposed topology does not use an H bridge, and polarity reversal is accomplished with only two switches. Table 1 shows the switching states and output voltages for the proposed topology.

Table 1. Switching states and output voltages for the proposed inverter.

Level	S_1	S_2	S_3	S_4	S_5	S_6	S_7	Output Voltage
1	0	0	1	0	1	0	0	Vdc
2	0	1	0	0	1	0	0	2 Vdc
3	1	0	0	0	1	0	0	3 Vdc
4	0	0	0	0	1	1	0	4 Vdc
5	0	0	0	0	0	0	0	0
6	1	0	0	1	0	0	0	−Vdc
7	0	1	0	1	0	0	0	−2 Vdc
8	0	0	1	1	0	0	0	−3 Vdc
9	0	0	0	1	0	0	1	−4 Vdc

The positive operational modes necessary to produce each of the nine states presented in Table 1 are demonstrated in Figure 17a–d, and the negative-signal operating modes necessary to produce the same nine states are depicted in Figure 18a–d. These operational sequences show that the proposed topology synthesizes DC voltage sources according to a simple principle to reduce the stress voltage across the active switch and produce an appropriate amount of voltage without the need for complexity to control the pulses generated by the switches.

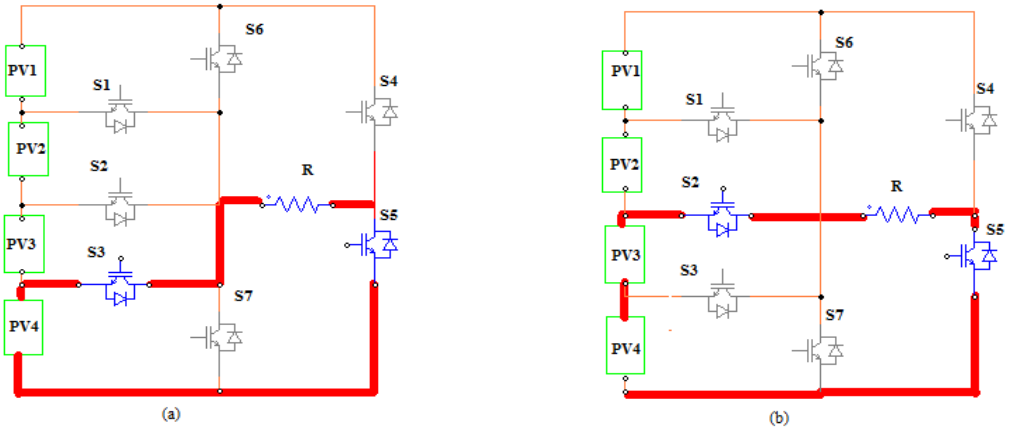

Figure 17. *Cont.*

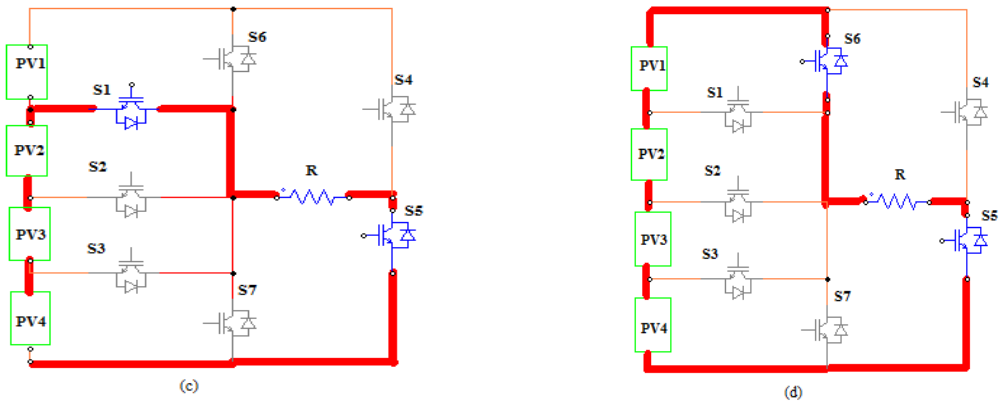

Figure 17. Positive sequences for synthesizing the nine-level output voltage. (**a**) output voltage = Vdc; (**b**) output voltage= 2 Vdc; (**c**) output voltage = 3 Vdc; (**d**) output voltage = 4 Vdc.

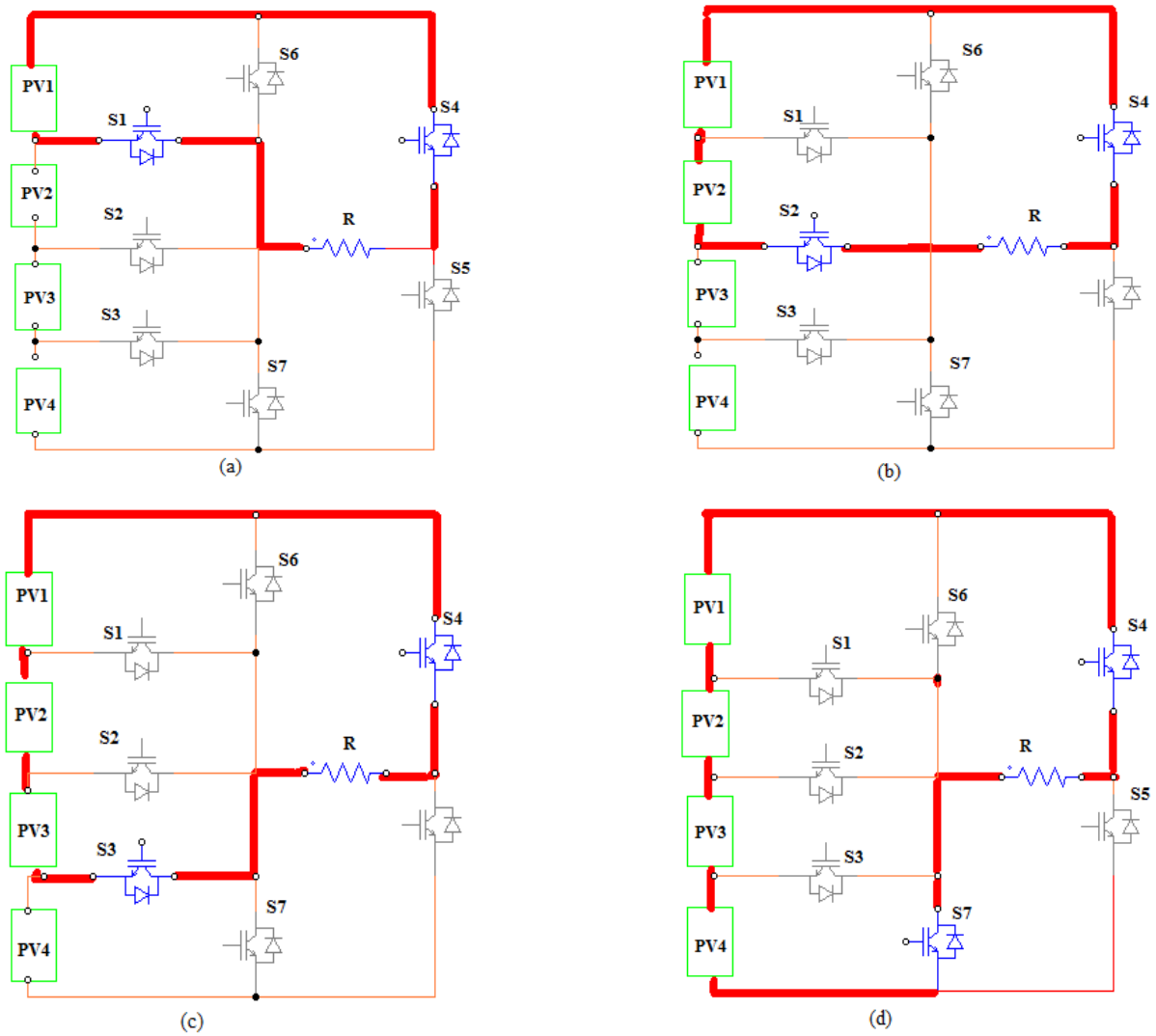

Figure 18. Negative sequences for synthesizing the nine-level output voltage. (**a**) output voltage = −Vdc; (**b**) output voltage = −2Vdc; (**c**) output voltage = −3Vdc; (**d**) output voltage = −4 Vdc.

PV System and DC/DC Converter with MPPT Techology

To improve the performance of the PV system and obtain high power, the PV panel is combined with a DC/DC converter with MPPT technology, which play an important

role in PV applications with respect to increasing the output voltage of the PV module. The implementation of an MPPT controller is the main advantage a DC/DC converter irradiation change. Therefore, a DC/DC boost converter with MPPT technology was used in this work to provide the optimum voltage for the proposed MLI and produce the maximum power from the PV array via the modified incremental conductance MPPT technique. Incremental conductance (In Cond) is among the most widely used traditional MPPT methods and involves the use of a variable step size [37].

Figure 19 shows a simulation diagram for a nine-level multilevel inverter with seven switches and a PV group. Figure 20 shows a simulation diagram of a PV group, which includes a PV system and a boost converter with MPPT technology.

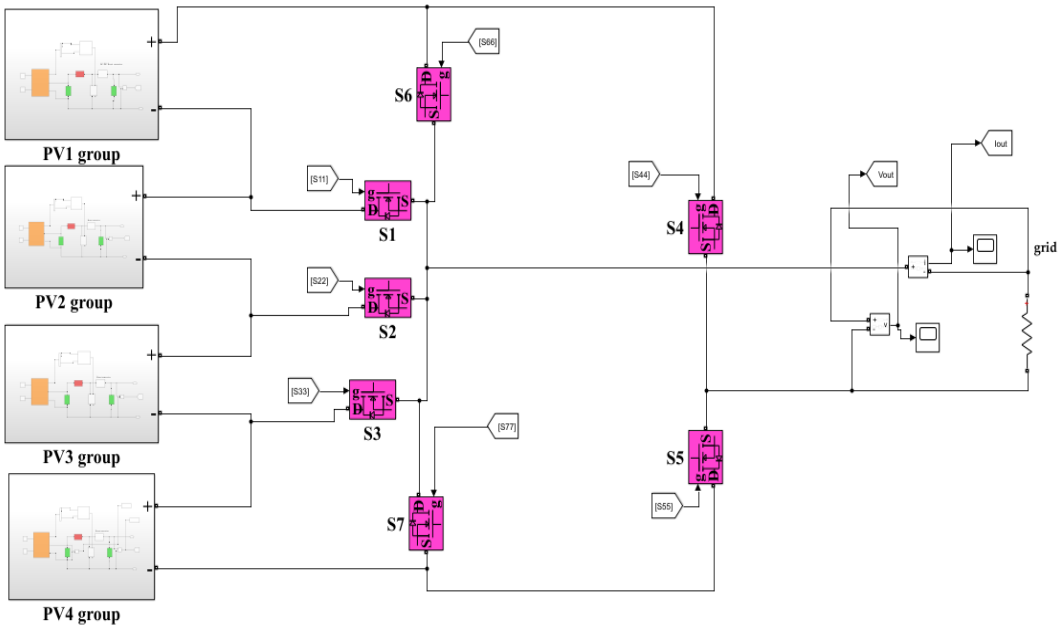

Figure 19. Simulation diagram of the proposed nine-level, seven-switch topology.

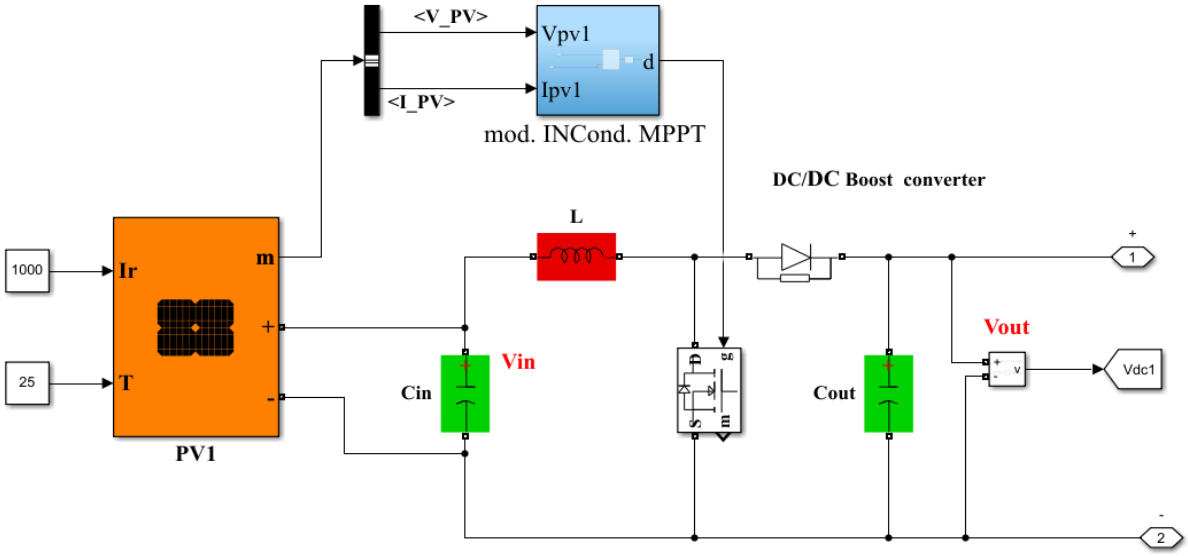

Figure 20. Simulation diagram (PV group) of a PV system with a boost converter.

In the DC/DC boost converter Figure 20, the duty cycle (d), input inductor (L), and output capacitor (C_{out}) can be obtained using the following formulas [66,67].

$$V_{out} = \left(\frac{1}{1-d}\right) V_{in} \tag{2}$$

$$L = \frac{V_{in}\, d\, T_S}{2\, \Delta I_L} \tag{3}$$

$$C_{out} = \frac{V_{out}\, T_S\, d}{2\, R\, \Delta V_{out}} \tag{4}$$

where (V_{out}) and (V_{in}) are the output and input of boost converter, respectively; (T_s) is the switching period; ΔI_L is the inductor ripple current (3–5%), ΔV_{out} is the ripple value in the capacitor; and R is the output load resistance of the boost converter. In this design, the four required boost converters use the parameters listed in Table 2. Figure 21 shows the V-I and P-V characteristics (PV group) of a PV system with a boost converter and reduced power due to a change in irradiance under the effect of a partial shading condition.

Table 2. PV panel specifications and parameters of the simulated system with boost converters.

Parameter	Value
Kyocera KC200GT PV solar panel	2 Series × 10 Parallel
Maximum power	200 W
Open-circuit voltage (Voc)	32.9 V
Short-circuit current (Isc)	8.21 A
Voltage at maximum power point (Vmp)	26.3 V
Current at maximum power point (Imp)	7.61 A
Inductor (L)	0.1 mH
Output capacitance (C_{out})	3000 µF
Duty ratio (d)	0.5
Vin boost converter	52 V
Vout boost converter	100 V

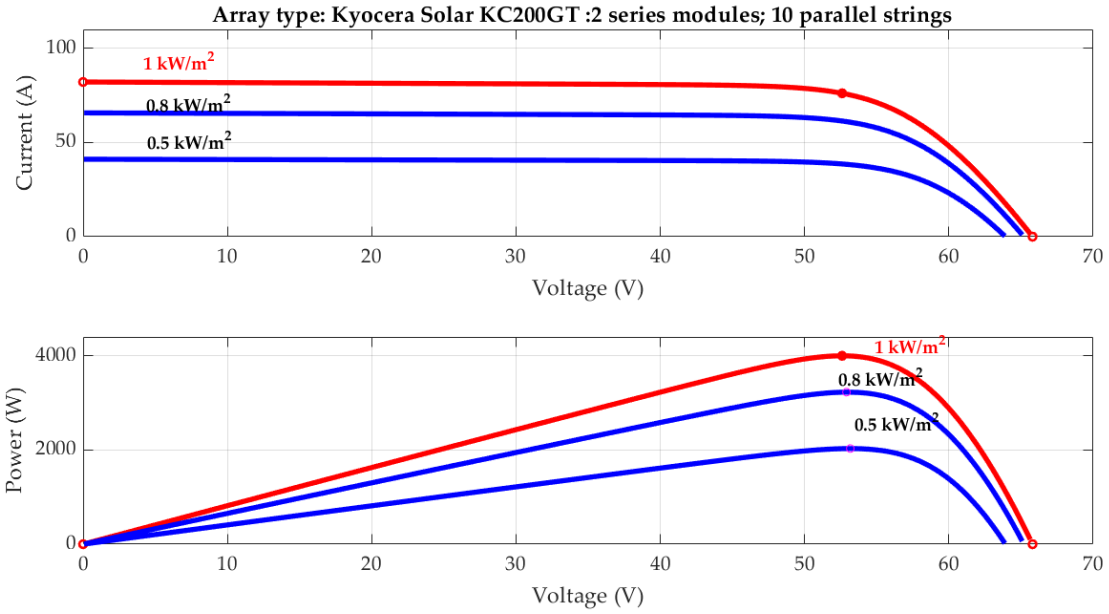

Figure 21. V-I and P-V characteristics of the PV system under PSC.

4. Control Strategy

4.1. Inverter Control

Cascaded multilevel topology works as a (DC to AC) converter when transferring electrical power to the grid. The control of the proposed topology is divided into two parts: the output current and voltage control for the inverter and independent MPP tracking in each cell. We compared the output voltage from each PV boost converter with MPPT against a reference voltage. The sum of the result was compared with voltage and current feedback. Control is accomplished with a phase-locked loop (PLL) control technique and a PI controller, as shown in Figure 22. The most important part of the control process is phase-disposition PWM (PD-PWM), which generates pulse signals for each switch (S1–S7) and will be discussed in detail in the next section [51,68].

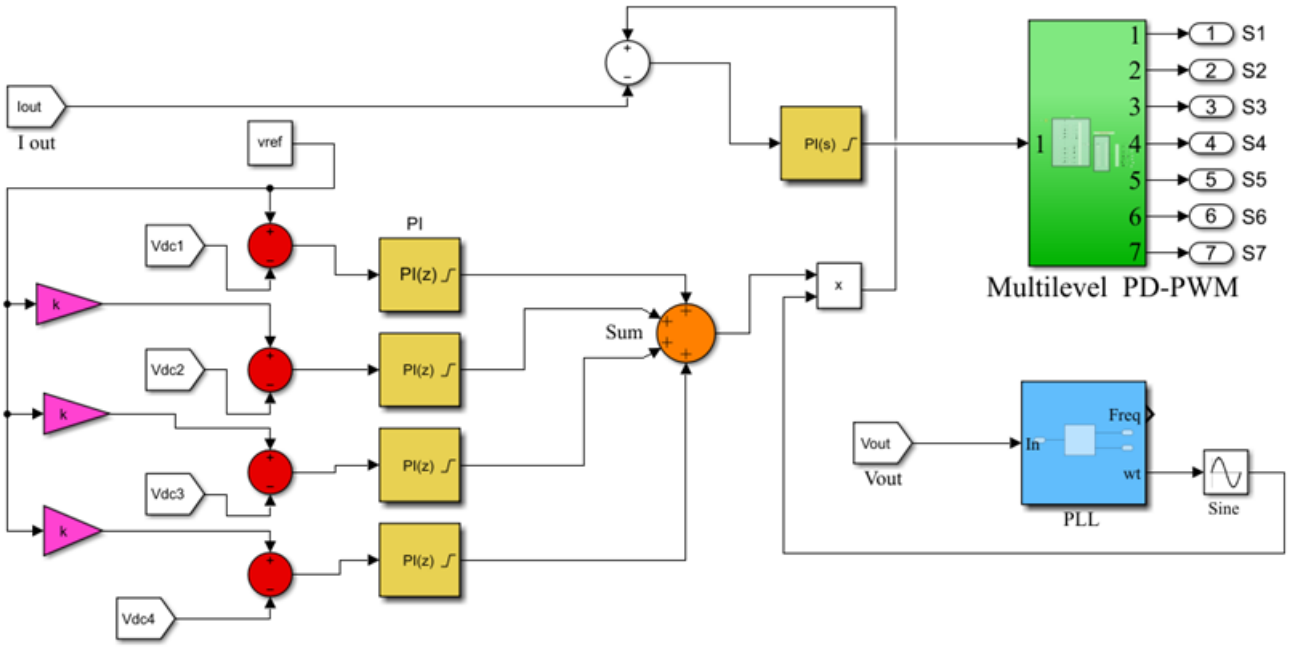

Figure 22. Simulation diagram of a cascaded multilevel control approach.

4.2. Phase Disposition PWM

Pulse generation is necessary for the nine-level output. There will always be a need to determine which PWM best suits the new topology. The THD value of CHB MLIs can be significantly reduced to the minimum possible percentage by employing phase disposition (PD) [17]. Power switches can be activated by comparing pulses generated by carrier-shifted signals to a sinusoidal wave. In PD-PWM, the magnitude and phase angle of the carrier signals shifted above and below zero are the same. This method provides superior harmonics performance with a higher modulation index than previous methods. With multilayer inverters, this modulation method is ideal. Table 1 shows the switching states for each switch, as well as the output voltages for the proposed inverter. Figure 23a shows a simulation diagram of the voltage waveform corresponding to the carrier signals generated by the phase-disposition PWM technique. Figure 23b depicts the eight carrier signals that are needed to modulate the reference signal using the phase-disposition PWM technique. Figure 23c shows the pulse signals for each switch (S1–S7).

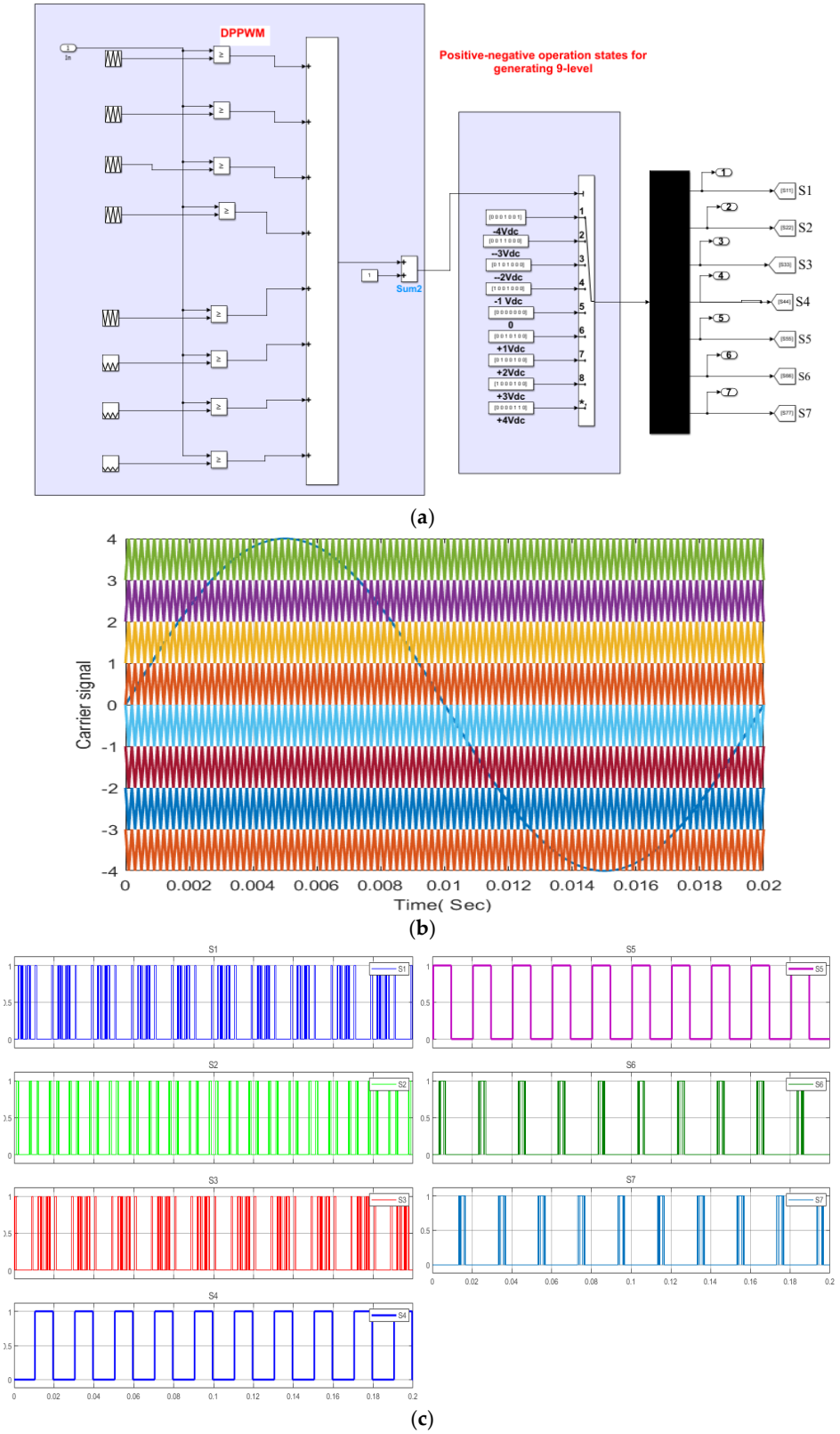

Figure 23. Phase-disposition PWM for seven switches with nine levels. (**a**) Simulation diagram of DPPWM, (**b**) carrier signals with the reference signal, and (**c**) pulse signals for seven-switch (S1 to S7) of the proposed nine-level MLI.

5. Simulation Results

The simulation was carried out using MATLAB/Simulink. Table 1 explains the switching mechanism of the proposed inverter. The output PV groups (DC sources) are Vdc1 = Vdc2 = Vdc3 = Vdc4 = 100 V, which functioned as symmetric sources to validate the nine-level output voltage inverter, as shown in Figure 24. An inverter circuit with a maximum output voltage of 400 volts, four DC voltage sources, and seven switches was investigated. In the first case, the simulation was carried out under resistive load with R = 10 Ω, as illustrated in Figures 25–27.

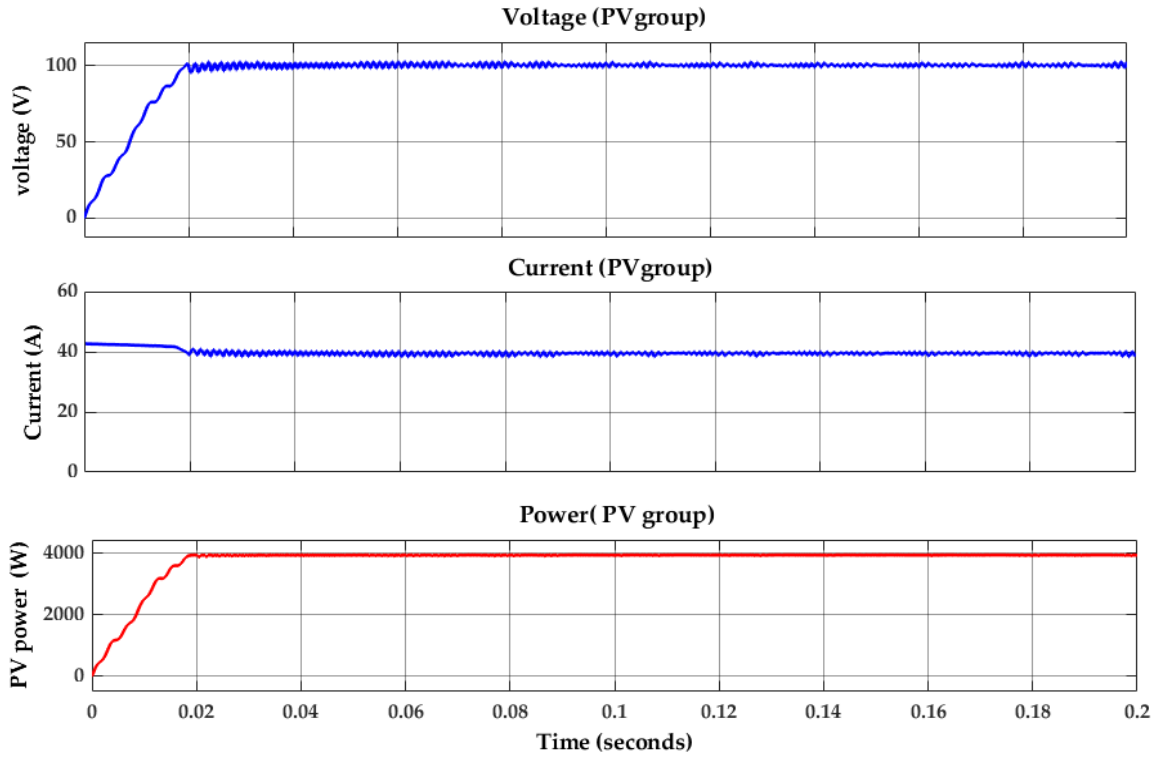

Figure 24. Output voltage, current, and power of each PV group.

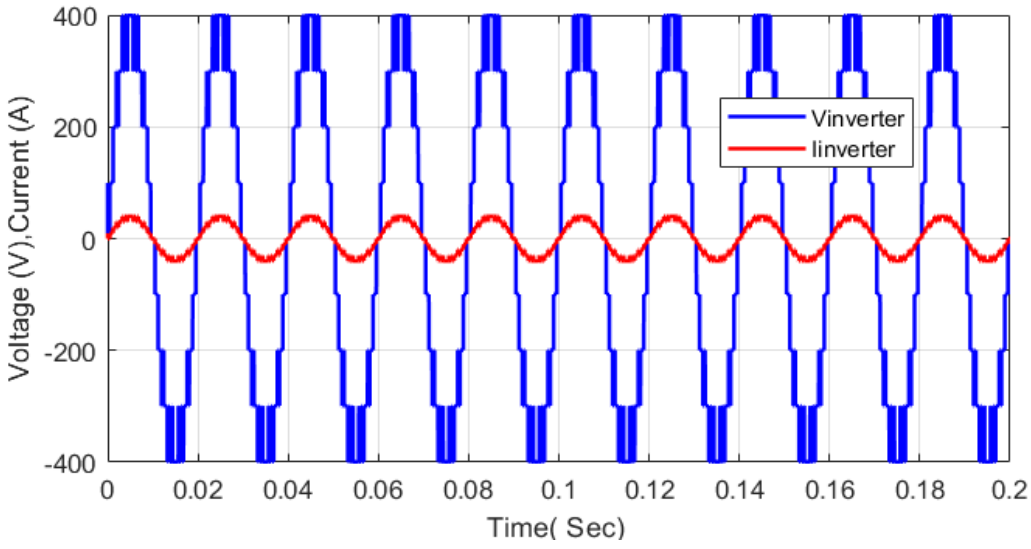

Figure 25. Nine-level output voltage of the proposed topology.

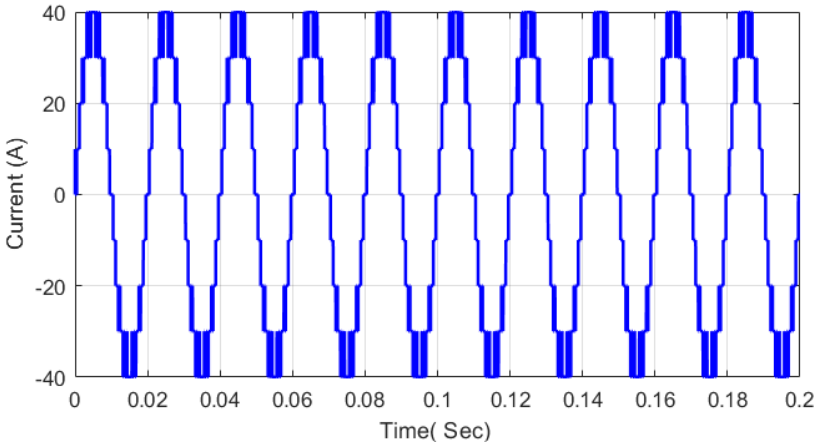

Figure 26. An output current of the proposed topology.

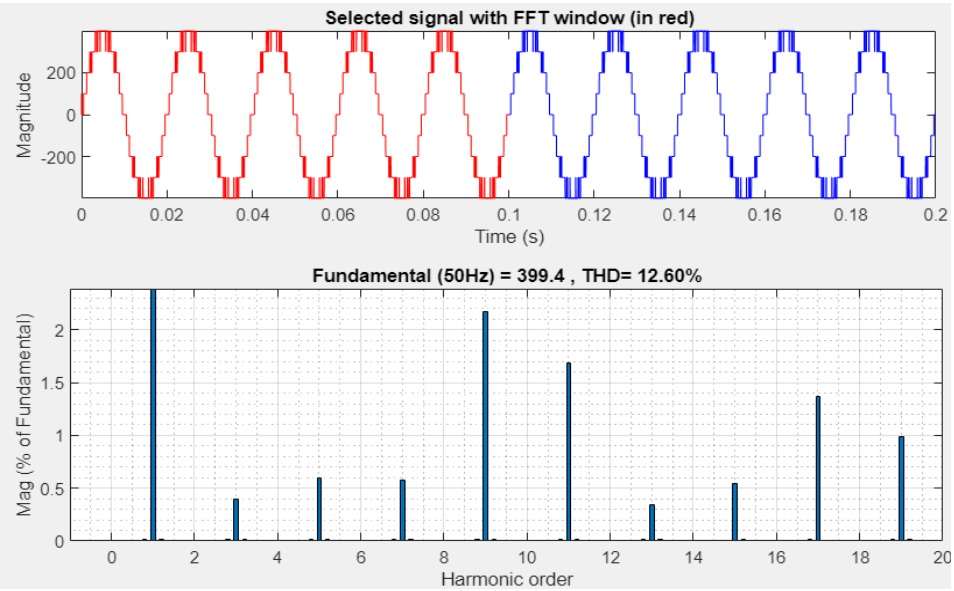

Figure 27. FFT spectrum of the output voltage before filtering.

Figure 25 depicts the output voltage of the proposed inverter. The output voltage comprises nine levels according to the switching state present in Table 1. The stair voltage is obtained according to m = 4 × n + 1 = 4 × 4 + 1 = 9. The difference between the proposed inverter with 7 switches and 4 DC sources and a conventional nine-level cascade topology with 16 switches and 4 DC sources can be determined with Equation (1): $S_{proposed} = \left(9 + \frac{16}{4} + 1\right) \div 2 = 7$.

The proposed inverter uses all DC sources to achieve all nine levels, in contrast with some topologies presented in the literature with four DC sources and seven levels [48], which implies that there is a redundant source.

The load current waveforms and harmonic content at nine levels are demonstrated in Figures 26 and 27. Figure 26 shows that the load current resembles sine wave, which proves the advantage of the proposed inverter. In contrast, Figure 27 demonstrates the THD spectrum of the nine-level output. The results discussed above and shown in Figures 25–27 were obtained before LC filtering.

In the second simulation scenario, the proposed inverter was connected to an LC filter with C = 15 µF and L = 50 µH; the simulation results are shown in Figures 28 and 29, including the nine-level inverter output voltage, load current, and harmonic spectra. The

proposed inverter can use any switching method for multilevel inverters, such as the multilevel carrier-based PD-PWM method used in this study.

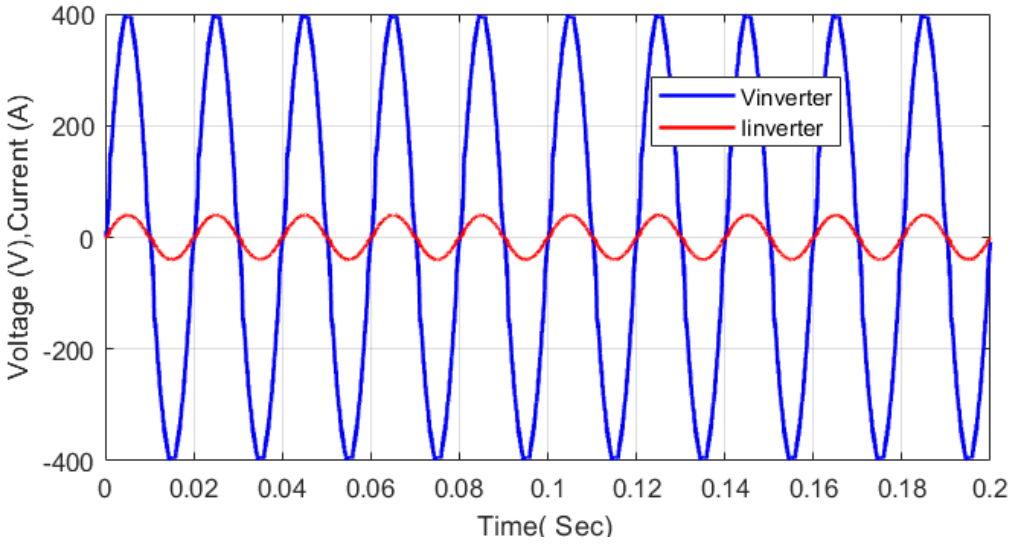

Figure 28. Output voltage and current of the proposed topology after minimal filtering.

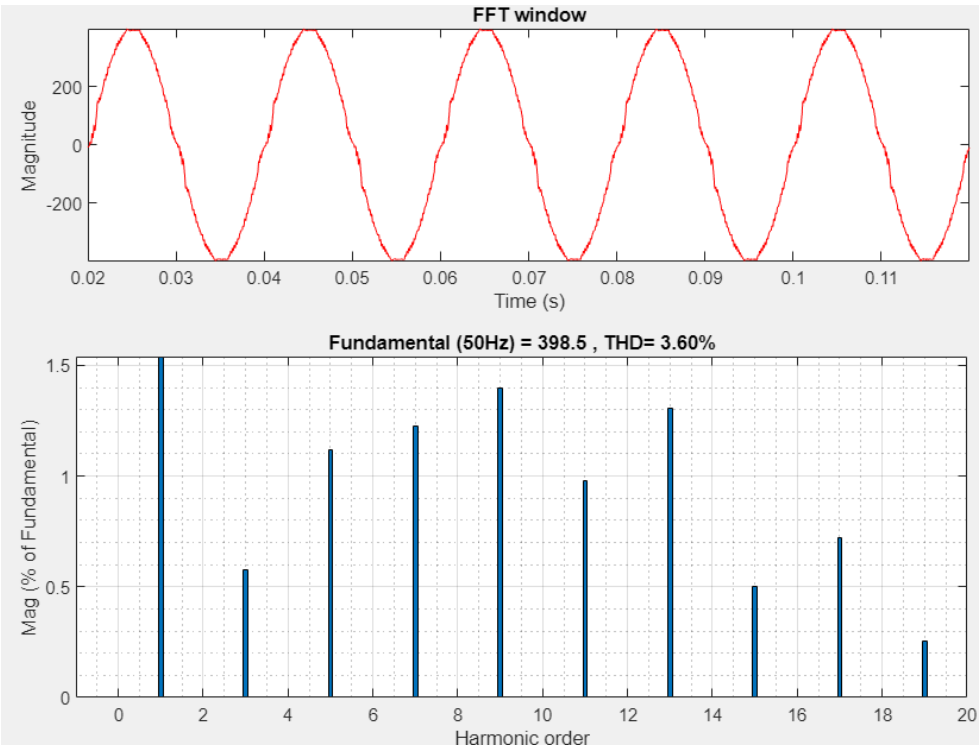

Figure 29. FFT spectrum of the output voltage after filtering.

In the second simulation scenario, as a load, an inverter's output is linked in series to an R–L branch with R = 10 Ω and L = 1 mH. Figure 30 shows the nine-level inverter output voltage and load current on the same axes. The output load current resembles a sine wave and presents with the same phase shift without DC offset. The proposed symmetric multilevel inverter was proven valid and effective through simulation and theoretical analysis.

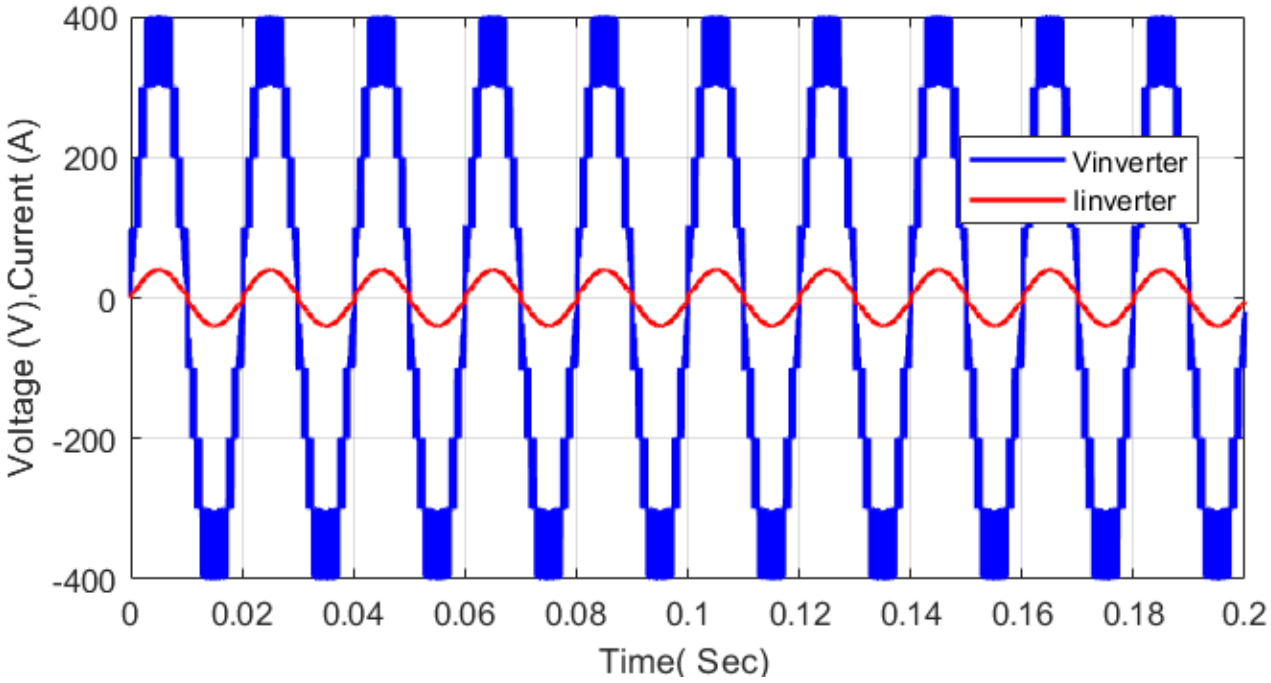

Figure 30. Output voltage and current of the proposed topology with R = 10 Ω and L = 1 mH.

Asymmetrical power sources under partial shading condition (PSC) results in a reduction of PV 1 from 1000 to 500 W/m^2 (P = 2 KW) and PV 4 from 1000 to 800 W/m^2 (P = 3.2 KW), with no change in PV2 and PV3 (4 KW). The current and voltage of a symmetrical power supply are shown in Figures 25 and 26, and those of an asymmetrical power supply are shown in Figures 31 and 32. Under PSC, 27.8% of power is lost, and the THD changes by 13.11, as shown in Figure 33.

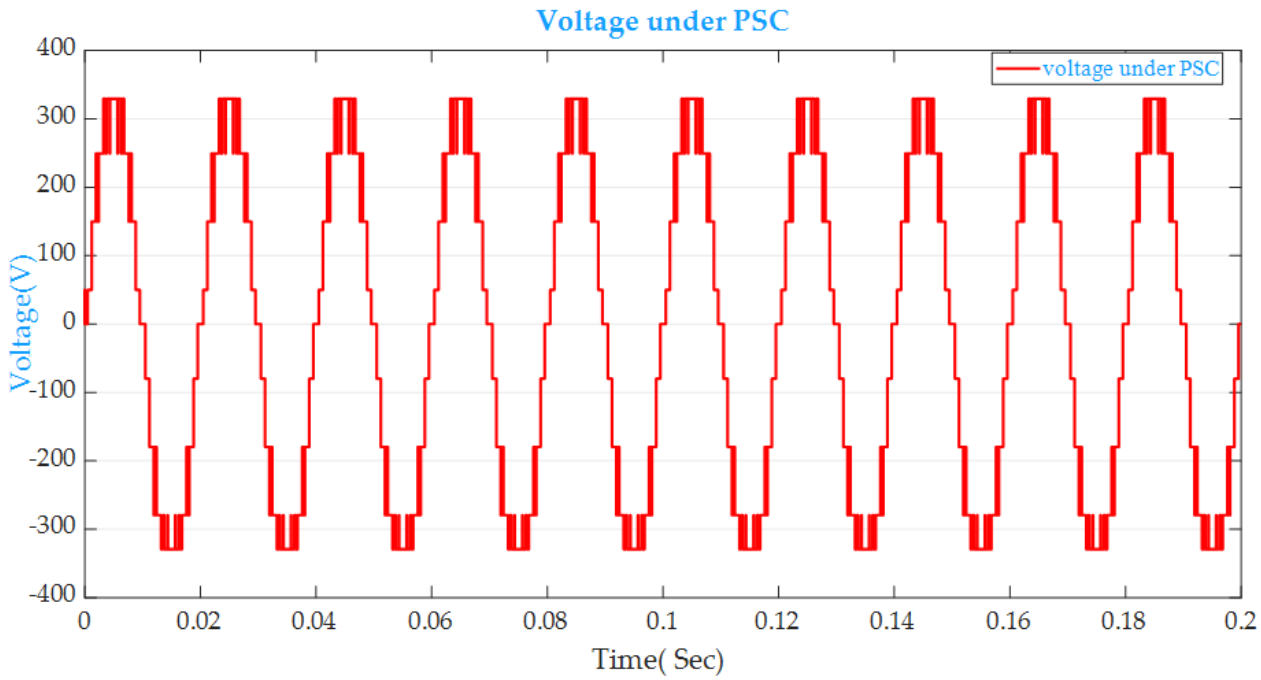

Figure 31. Output voltage of the proposed topology under PCS.

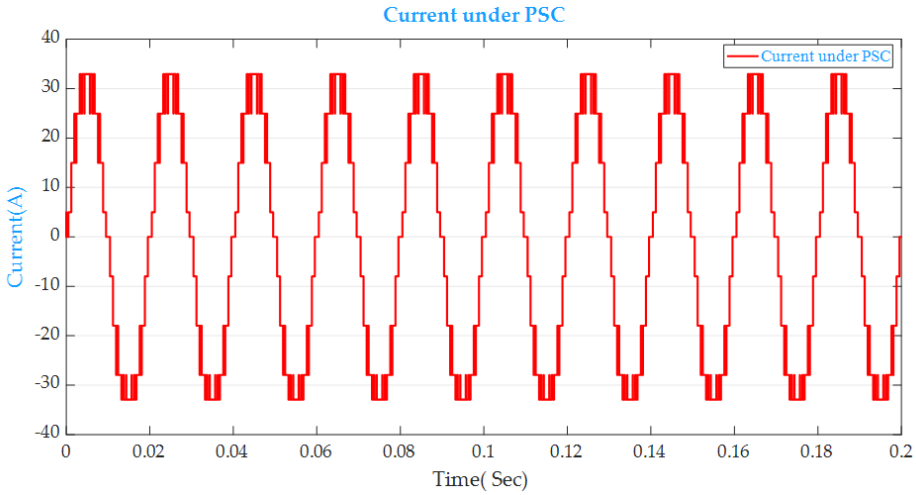

Figure 32. Output current of the proposed topology under PCS.

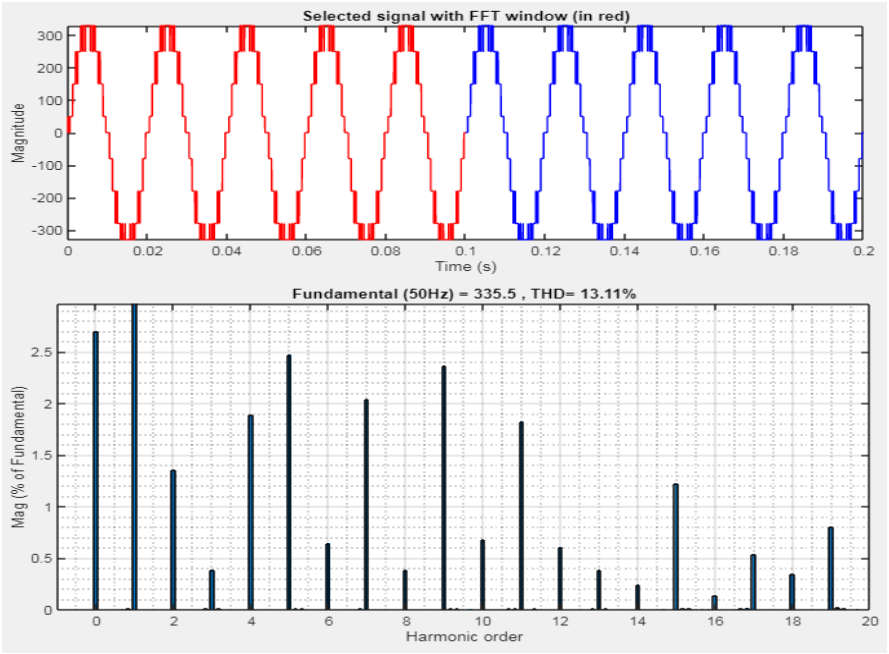

Figure 33. FFT spectrum of the output voltage under PSC.

This power loss percentage is satisfactory compared with the power losses of traditional PV systems due to PSC, which are considerably high and may surpass 70% of the total generated power [39].

6. Comparisons with Related Work

A new cascade multilevel inverter was proposed in this work and compared to a standard cascaded inverter and other novel inverters proposed in [49–61]. The proposed design uses fewer switches and relevant gate driver circuits without redundant DC sources to provide a nine-level output voltage. Table 3 compares the proposed inverter with another inverter in terms of the number of levels (N level), the number of switches (N switch), the number of diodes (N diode), the number of capacitors (N capacitor), the percentage of total harmonic distortion of the voltage before filtering (THD 1) and the percentage of total harmonic distortion after minimal filtering (THD2). The proposed structure reduces the installation space and cost, in addition to simplifying the control technique.

Table 3. Comparison of the proposed MLI topology with other topologies.

Reference	Figure	N Level	N Switch	N Diode	N Capacitor	N Source	THD%1	THD%2
[50]	Figure 1	9	16	-	-	4	13.63	6.53
[51]	Figure 2	7	7	1	-	3	24.35	3.43
[52]	Figure 3	9	9	2	2	1	-	3.13
[53]	Figure 4	9	10	-	-	4	12.66	-
[54]	Figure 5	9	8	-	1	1	-	1.73
[55]	Figure 6	9	9	-	-	2	13.51	1.12
[56]	Figure 7	9	8	-	2	1	14.23	1.19
[57]	Figure 8	9	9	3	4	1	16.7	2.2
[58]	Figure 9	9	12	-	4	1	17.3	0.33
[59]	Figure 10	9	8	3	3	1	-	1.8
[60]	Figure 11	9	9	2	2	1	15.63	7.82
[61]	Figure 12	9	10	-	3	1	16.73	-
[62]	Figure 13	9	8	-	-	2	11.43	1.45
[63]	Figure 14	9	10	-	3	1	12.46	-
[64]	Figure 15	9	10	2	4	1	12.15	-
Proposed	Figure 16a	9	7	-	-	4	12.6	3.60
Proposed	Figure 16b	9	7	-	4	1	12.6	3.60

7. Conclusions

In this paper, we presented a nine-level CMLI with only seven switches developed and introduced by modeling the circuitry in Matlab/Simulink simulation and achieving a clear stepped nine-level waveform. The PD-PWM strategy was used to investigate the proposed topology. The new design is straightforward in appearance and a reduced number of components compared to standard symmetric and asymmetric topologies. The proposed nine-level multilevel inverter decreases the THD to an acceptable value of 12.6% compared to the topologies represented in the literature. The suggested MLI can be applied to three-phase power systems to increase line-to-line voltages. Thus, the proposed power inverter offers a novel solution for a wide range of applications, such as renewable energy generation systems that require high voltage gain and low voltage stresses while maintaining low switch counts and using a single DC source for DC–AC power conversion. In particular, photovoltaic (PV) systems require many separate PV panels in an array to obtain high power. The effect of a partial shading condition (PSC) can result in mismatched power between panels. Under PSC, the power loss amounts to 27.8% of the total generated power, with a reduction in THD of 13.11, which is a satisfactory result compared with the power losses sustained in traditional PV systems due to PSC, which are extraordinarily high and can surpass 70% of the total generated power. The proposed topology is outperforms in all other designs presented in the literature to date.

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