Control System Development for the Three-Ports ANPC Converter

Silvio Antonio Teston [1,2] [iD]**, Kaio Vinicius Vilerá** [2] [iD]**, Marcello Mezaroba** [3] [iD]
and Cassiano Rech [2,*] [iD]

1   Department of Physical Facilities, Federal University of Fronteira Sul, Chapecó-SC 89802-112, Brazil;
    silvioteston@gmail.com
2   Power Electronics and Control Research Group (GEPOC), Federal University of Santa Maria,
    Santa Maria-RS 97105-900, Brazil; kaiovilera@gmail.com
3   Electric Power Processing Group, Santa Catarina State University, Joinville-SC 89219-710, Brazil;
    marcello.mezaroba@udesc.br
*   Correspondence: rech.cassiano@gmail.com; Tel.: +55-55-3220-9590

Abstract: This paper proposes a control system for the single-phase Three-Ports Active Neutral-Point-Clamped (ANPC-3P) converter, which can inject a sinusoidal current into the grid, balance the neutral point voltage, and regulate the energy storage system (ESS) current with reduced low-frequency ripple. Despite other applications, ANPC-3P inverter can be used in grid-tied renewable generation to allow the simultaneous connection of a photovoltaic (PV) energy source and an ESS to the AC grid. The ESS is connected directly to the inverter circuit without any auxiliary DC-DC converter, but due to the DC bus pulsed power, it can be subjected to low-frequency current ripple. This undesired current ripple is difficult to filter and can lead to shorter battery life. A control system based on well-known controllers is analyzed and designed. Theoretical analysis is validated experimentally using a single-phase 1-kW prototype.

Keywords: active neutral-point-clamped (ANPC) converter; control system; distributed power generation; energy storage; integrated secondary DC port; low-frequency current ripple

1. Introduction

The insertion of renewable generation in the electrical grid arises some problems related to the undetermined availability of these sources [1]. In this sense, the energy mix must be planned and diversified to improve the reliability and resilience of the electrical system. The integration of energy storage systems (ESSs) is shown as an option to allow greater penetration of renewable generation [1–5]. Furthermore, the integration of ESSs in the power grid allows the addition of auxiliary services and increases the possibilities of power dispatch, as illustrated in Figure 1, which provides an overview of the main functions of the ESS.

Considering an electrical system with distributed generation (DG), the connection of a renewable energy source integrated with an ESS can be performed in different ways as presented in Figure 2. Each connection type might be interesting for a certain ESS power and/or voltage range. Besides, the design requirements and the technology of the storage system have a significant impact on the choice of the connection type.
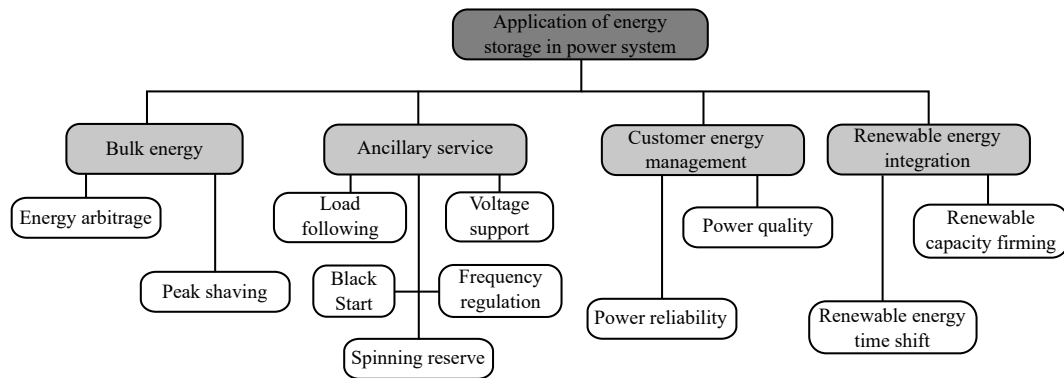
Figure 1. Overview of the main applications of energy storage systems (ESSs) [6].
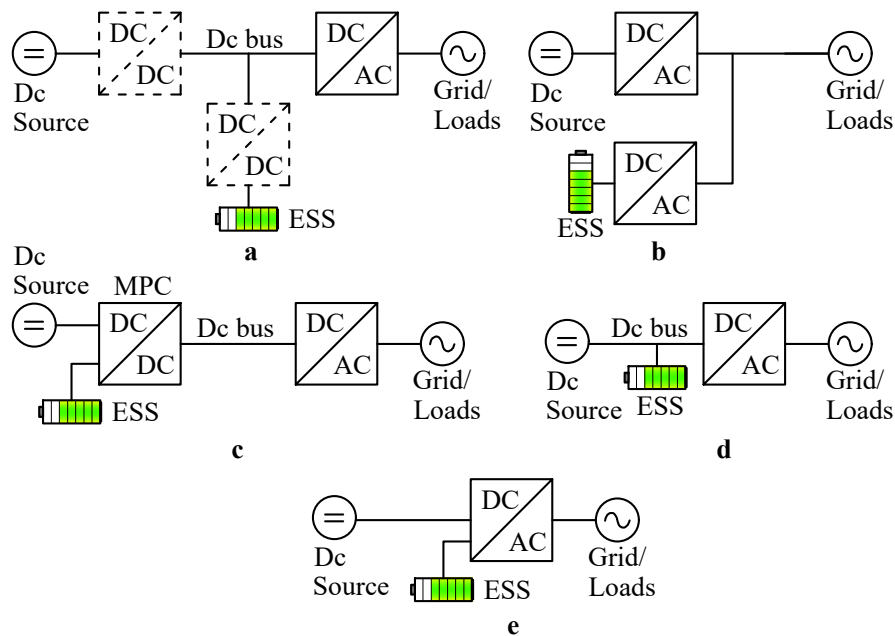

Figure 2. Main configurations for connecting the energy storage system (ESS). (**a**) Connection to the DC bus of the inverter through a bidirectional DC-DC converter; (**b**) Connection to the AC bus through a dedicated inverter; (**c**) Connection using a DC-DC multiport converter (MPC); (**d**) Direct connection to the DC bus; and (**e**) Direct connection to the inverter topology.

The most used types for ESS connection are shown in Figure 2a [7,8] and Figure 2b [9,10]. The static converters allow bidirectional power flow for ESS charge and discharge, adapting the voltage and current at the connection point. In general, these forms of connection have a larger number of converters (and power elements) but they give the greatest design flexibility–choice of topology, voltage and current levels, passive filters, and so forth. The connection type shown in Figure 2c uses multiport DC-DC converters (MPC) [11]. They are particularly interesting for low power applications (<1 kW). In Figure 2d the ESS is connected directly to the DC bus of the power inverter [12–14]. As the main advantage, this form of connection allows the use of a single DC-AC converter to process the power of the generation system and to control the charge and discharge of the ESS. On the other hand, this configuration could present a complex modulation strategy [15]. In the connection shown in Figure 2e, the ESS is connected directly to the inverter circuit. In this type of connection, the ESS is not directly connected to the DC bus, but other favorable connection points are used. The ESS integration in the quasi-Z-source inverter (qZSI) is proposed in References [16,17], in which the degree of freedom of the shoot-through state is explored. On the other hand, qZSI allows the integration of only one type of ESS per inverter. The flying-capacitor inverter is also reported in the literature with the floating capacitors replaced by floating ESSs [18]. Due to the need to control the state of charge (SOC) of each

ESS independently, the voltages of the floating ESSs can be different, adding considerable complexity to the modulation and control systems. For high power applications (megawatts), an option also explored in the literature is the integration of ESSs in the modular multi-level converter (MMC) [19].

The ANPC-3P inverter, proposed in Reference [20], allows an ESS to be directly connected to the inverter topology. Figure 3 shows the ANPC-3P inverter in a single-phase grid-connected application and it details how the ESS connection can be performed. This is achieved by exploring the various redundant switching states of the ANPC inverter. In Reference [20], the study focused on analyzing the topology and a basic control system was presented only to demonstrate the operation of the inverter. The AC output is similar to the NPC/ANPC inverter and classical control strategies can be used to obtain a sinusoidal current with low total harmonic distortion (THD).
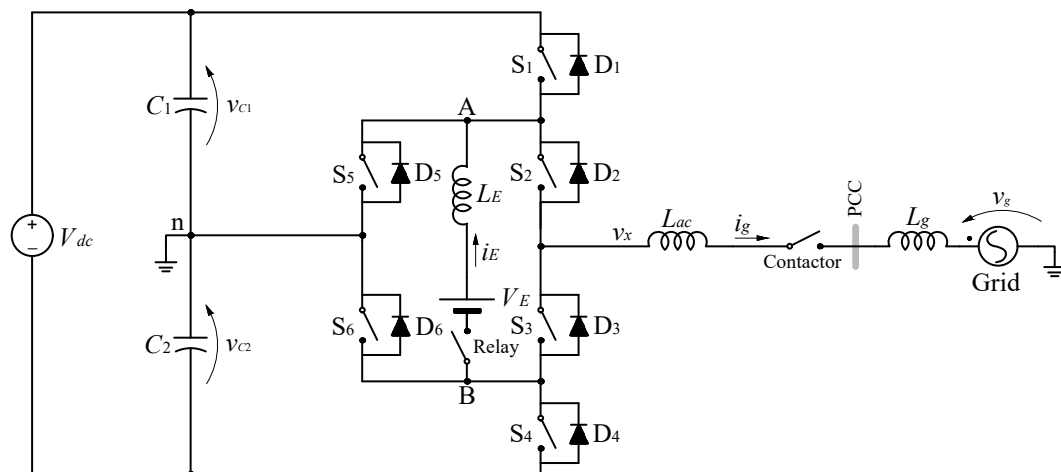

Figure 3. Three-Ports Active Neutral- Point-Clamped (ANPC-3P) topology in a grid-tied application.

Pulsed power is inherently present in the DC bus of single-phase inverters, resulting in low-frequency voltage ripple. In the single-phase ANPC-3P inverter, these voltage ripples affect the ESS battery current causing a low-frequency current ripple, which is undesirable since it is difficult to filter and it can rise the temperature of the batteries if not properly handled [21]. Possible solutions for this problem are the increase of the DC bus capacitance or the use of a control system capable of compensating these low-frequency ripples.

In Reference [22], the low frequency current ripple issue was analyzed and a control strategy based on the proportional-integral controller (PI) associated to a feedforward (FF) action was proposed. The FF control action was derived and, ideally, allowed the low frequency ripple to be completely compensated. However, the FF action has no feedback and non-idealities of the plant may result in partial compensation of the low frequency ripple.

Therefore, the main contribution of this paper is to propose and experimentally validate a complete control system for the ANPC-3P in a grid-tied application. This paper proposes the inclusion of a resonant controller in the secondary DC port control loop to compensate the low-frequency ripple in the battery current. The problem of neutral point voltage balancing is also considered. Two distinct control actions are used for this purpose.

This paper is organized as follows: Section 2 presents a review of the ANPC-3P topology; Section 3 is dedicated to the control system analysis and design; and Section 4 presents and discusses the experimental results of the proposed control strategy.

2. Description of the ANPC-3P Inverter

The ANPC inverter was originally proposed to address the problem of unequal losses distribution of the NPC inverter [23]. With this topology it is possible to increase the power capacity of the inverter while maintaining the same semiconductor devices. The ANPC-3P inverter is based on the ANPC

topology, but the main objective is not to improve the losses distribution among the semiconductor devices. On the other hand, the main purpose is to allow the connection of an ESS directly to the inverter leg through a secondary DC port (v_{AB}) [20].

The switching states of the ANPC-3P inverter are shown in Table 1. There are seven redundant states to generate zero level at v_x (AC port), besides the P and N states that generate $+V_{dc}/2$ and $-V_{dc}/2$ at v_x, respectively. In the secondary DC port, five states generate zero level; P and 0L1 generate $+V_{dc}/2$ by using the capacitor voltage C_1, while N and 0U1 generate $+V_{dc}/2$ by using the capacitor voltage C_2. Thus, during the zero-level generation in v_x, it is possible to impose the voltage levels $V_{dc}/2$ or zero in v_{AB}. Therefore, by properly selecting the duration of each voltage level, it is possible to control the electrical parameters of a circuit connected between nodes A and B.

Table 1. Switching states of the three-level ANPC-3P voltage source inverter.

| State | Switches | | | | | | v_x | v_{AB} |
	S_1	S_2	S_3	S_4	S_5	S_6		
P	1	1	0	0	0	1	$V_{dc}/2$	$V_{dc}/2$
0U4	0	1	1	0	1	0	0	0
0U3	0	1	0	0	1	1	0	0
0U1	0	1	0	1	1	0	0	$V_{dc}/2$
0UL	0	1	1	0	1	1	0	0
0L1	1	0	1	0	0	1	0	$V_{dc}/2$
0L3	0	0	1	0	1	1	0	0
0L4	0	1	1	0	0	1	0	0
N	0	0	1	1	1	0	$-V_{dc}/2$	$V_{dc}/2$

Figure 4 shows typical ANPC-3P waveforms and provides a better understanding of how the voltage levels are generated in the AC and DC ports. It is worth noting that the modulation of the secondary DC port occurs during the application of the zero level in v_x.
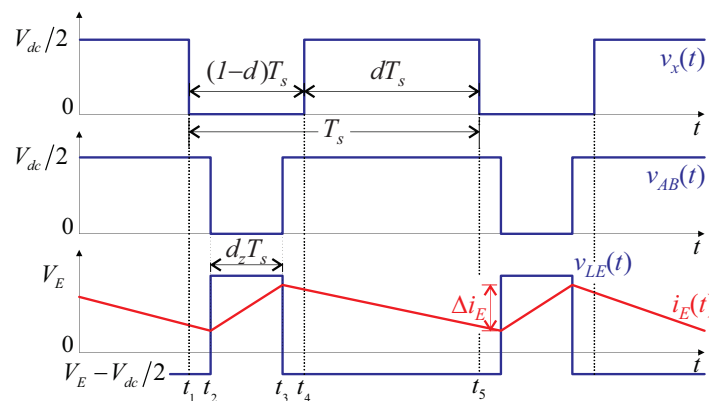

Figure 4. Waveforms detailing the modulation of the ANPC-3P power ports.

The duty ratio d_z is related to the duration of the zero level in v_{AB}, that is, the duration of the positive voltage pulse across L_E. From steady-state analysis of the circuitry of Figure 3 and considering the waveforms shown in Figure 4, the duty ratio d_z can be calculated by the volt-second balance of the inductor L_E:

$$d_z = 1 - \frac{V_E}{V_{dc}/2}. \tag{1}$$

To maintain a constant average current i_E, one can adjust the value of d_z. As stated in (1), d_z depends on V_E and V_{dc}. If V_{dc} is constant, d_z is adjusted according to the ESS voltage. Considering that the modulation of the secondary DC port occurs during the application of zero voltage level in the AC port, the upper limit of d_z is given by $1 - d_{max}$. A second limit must be established to ensure that

the inductor voltage has two polarities, so that the volt-second balance can be achieved. Therefore, V_E cannot be greater than $V_{dc}/2$. With these considerations, a range of values for V_E can be defined:

$$V_p < V_E < V_{dc}/2, \tag{2}$$

where V_p is the peak value of the average voltage synthesized by the AC port when d reaches its maximum value ($d_{\max}$).

Initially, the voltage range defined in (2) may seem a disadvantage since it is necessary to accommodate for the ESS voltage variation due its SOC. To better understand the impact of the ESS voltage variation, a comparison of the ANPC-3P topology with a configuration that uses the AC bus connection, shown in Figure 2b, is presented. The compared configuration consists of a dedicated NPC inverter for connecting the ESS to the grid, and the ESS is connected to the DC bus of this inverter. Hypothetically, when the ESS is completely discharged the voltage $V_{dc}/2$ is equal to the grid peak voltage, that is, the amplitude modulation index ($m_a = V_p/(V_{dc}/2)$) is unitary. However, when the ESS is fully charged, the voltage V_{dc} increases and m_a presents a minimum value $m_{a,min}$. This can be better understood by looking at Figure 5a. This range of V_{dc} is required due to the voltage variation caused by the ESS SOC. Furthermore, considering the ANPC-3P inverter case, the DC bus operates with constant and maximum voltage V_{dc} regardless of the ESS SOC. According to (2), the inverter cannot operate with m_a close to one. The DC bus voltage must be increased to allow ESS SOC variation. This causes the inverter to operate with $m_a = m_{a,nom}$ below unity. According to Figure 5b, values between $m_{a,nom}$ and 1.0 can be chosen to adjust the duty ratio d_z, as defined in (1), to react to the variations of the ESS voltage. As a result, the DC bus voltage of the inverters in this comparison is approximately the same [20]. To simplify the analysis, voltage drops in the filtering elements were not considered in this comparison.
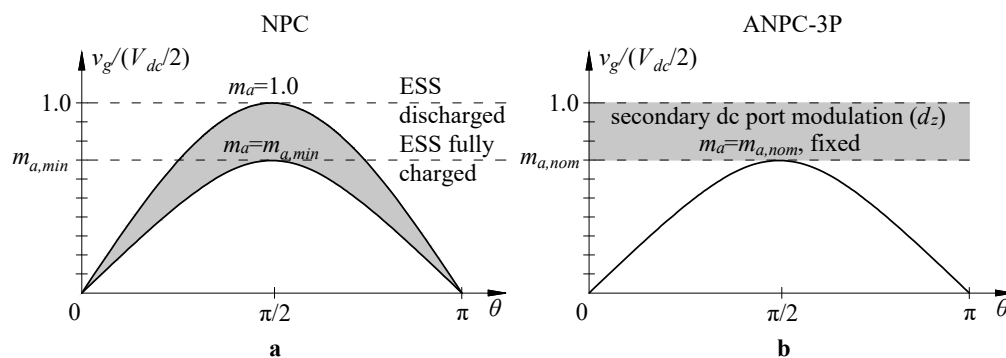

Figure 5. Modulation regions considering ESS state of charge (SOC) variation: (**a**) dedicated NPC inverter and (**b**) ANPC-3P inverter.

Modulation

The modulation scheme presented in this paper is based on the modulation proposed in Reference [20]. Three blocks are used to generate the gate signals for the six switches ($v_{gS1} - v_{gS6}$), as shown in Figure 6. The first block receives two carrier signals (v_{tri+} and v_{tri-}) in phase opposition disposition (POD) and signals $v_{m,ac}$ and $v_{m,dc}$, which are the modulating signals of the AC port and secondary DC port, respectively. This block is responsible for comparing the modulating signals with the carriers and for generating the signals b_p, b_n and b_z, which are sent to the second block and contain information about the voltage levels that must be generated on both power ports. When b_p is high, level $+V_{dc}/2$ must be generated in v_x ($V_{dc}/2$ is imposed in v_{AB}). Signal b_n high indicates that $-V_{dc}/2$ must be generated in v_x ($V_{dc}/2$ is imposed in v_{AB}). Lastly, b_z high requests a zero level in v_x and v_{AB} simultaneously. When all the three signals are low, level zero is applied in v_x and level $V_{dc}/2$ in v_{AB}. The second block selects the appropriate switching state considering the signals computed by the first

block and the available redundant switching states. The third block generates the gate signals for the six switches, including the appropriate dead times.
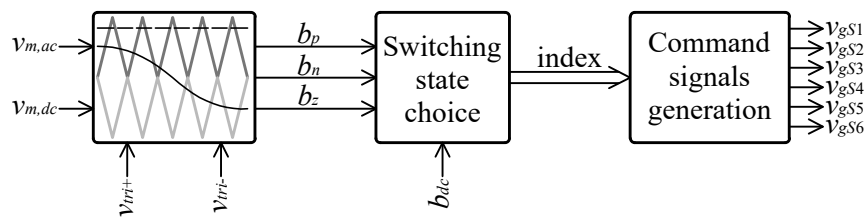

Figure 6. Modulation block diagram [20,22].

The ANPC-3P inverter has some redundant states and it is necessary to define how they are used. For example, states 0U3, 0U4, 0UL, 0L3, and 0L4 perform the same function considering the levels applied to the power ports. However, each state affects semiconductor devices differently. With the exception of 0UL, the other states have a single internal semiconductor device (S_2, S_3, S_5 and S_6) turned off and may not allow parallelism of the upper (S_2–S_5), lower (S_3–S_6), left (S_5–S_6) and right (S_2–S_3) current paths. On the other hand, state 0UL allows the currents to flow through the four current paths. According to Reference [24], the use of 0UL results in a simple modulation system and a small increase in the efficiency of the inverter. Thus, in this paper, only the 0UL state is used to generate the zero level simultaneously on the DC and AC ports.

States 0U1 and 0L1 play a special role in helping to balance the neutral-point voltage. Theses switching states are redundant and depending on which switching state is employed, a different effect is produced on the neutral-point potential. Therefore, by properly selecting these states, the neutral-point potential can be conveniently increased or decreased. A controller is responsible for selecting these states and this is covered in the next section.

3. Control System

The control system of the grid-tied single-phase ANPC-3P inverter is responsible for controlling the grid current (i_g) and the ESS current and to keep the DC bus voltages balanced. The control system is composed of two subsystems—one for the AC port and the other for the ESS. Figure 7 shows a block diagram of the proposed control system. The AC port control strategy is shown at the top (red color), and it is composed of a resonant controller (RES), aiming the grid current control, and a proportional controller, responsible for assisting in balancing the DC bus. There is also a band-stop filter (BSF) used to reject the grid frequency component from $\delta(t)$. At the bottom (blue color), the complete ESS current control system consists of a PI (proportional-integral) controller, responsible for regulating the DC value of the ESS current, and a resonant action responsible for compensating the low-frequency ripple of the dc bus capacitors. There is also a hysteresis controller responsible for assisting in balancing the DC bus voltages by using the current i_E.

The supervisory system shown in Figure 7 is responsible for monitoring the various variables involved in the operation of the grid-connected inverter and, by acting on the controller references, it defines the desired power at each port of the inverter. This supervisory system makes pre-programmed decisions to achieve certain objectives, which could be any of those ancillary services shown in Figure 1. However, in this paper, the supervisory block is only responsible for calculating the grid voltage angle (θ) and for adjusting the references of the controllers to perform some pre-programmed experiments. Details of the supervisory system are not presented in this paper.
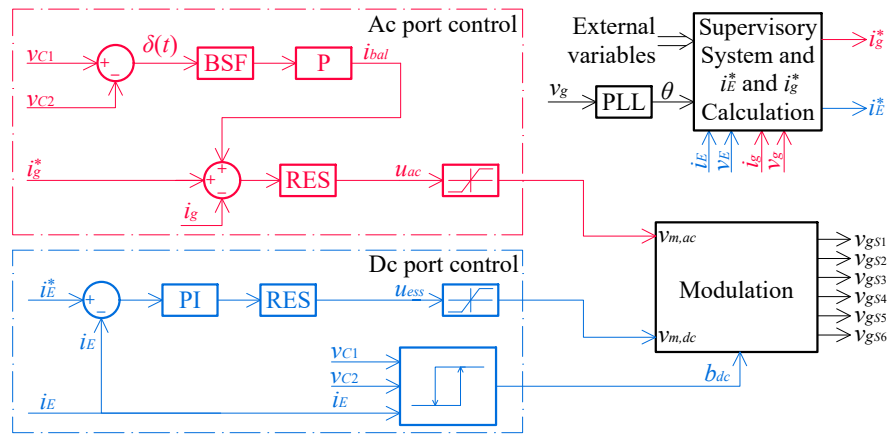
Figure 7. Control system block diagram. The control subsystems of the secondary DC and AC ports are represented in blue and red colors, respectively.

Firstly, the AC power port control and the neutral point balancing system are presented. Afterward, the proposed controllers for the ESS current are described.

Table 2 presents the main design parameters.

Table 2. Main parameters.

Parameter	Value
Output AC power (P_o)	1 kW
ESS power (P_E)	1 kW
Dc bus voltage (V_{dc})	720 V
Dc bus capacitance ($C_1 = C_2$)	500 µF
ESS voltage (V_E)	23 × 12 V VRLA batteries
ESS internal resistance (R_E)	0.5 Ω
Ac voltage (V_{ac})	127 V rms
Ac filter inductor (L_{ac})	6 mH ($R_s = 0.3$ Ω)
ESS filter (L_E)	8 mH ($R_{LE} = 0.5$ Ω)
Ac frequency (f_{ac})	60 Hz
Carrier frequency (f_c)	10.26 kHz
Amplitude modulation index (m_a)	0.5

3.1. Ac Port Control System

A resonant controller is used to control the current injected into the grid. Considering the grid voltage source as an infinite bus, the model of the AC port of the inverter connected to the grid can be given by:

$$G_{iac}(s) = \frac{I_g(s)}{D(s)} = \frac{V_{dc}/2}{L_{ac}s + R_{ac}},$$　　　　(3)

where R_{ac} is the series resistance of the filtering inductor.

The resonant controller transfer function is given by:

$$C_{res}(s) = k_r \frac{s^2 + 2\omega_z\zeta_z s + \omega_z^2}{s^2 + 2\omega_p\zeta_p s + \omega_p^2}.$$　　　　(4)

The pair of conjugated complex poles is allocated in the frequency f_{ac} ($\omega_p = 2\pi f_{ac}$) with a damping ratio of 0.001 (ζ_p). The zero pair is allocated a decade below the crossover frequency with a damping ratio of $\zeta_z = 0.7$. Finally, the k_r gain is adjusted to result in a 1 kHz gain crossover frequency (approximately one decade below the switching frequency).

3.2. Neutral Point Balancing

When the ESS current is non-zero, it can help with the neutral point balancing. This can be achieved by the proper selection of states 0U1 and 0L1. These states are redundant in terms of the output voltages since they generate zero level in v_x and $V_{dc}/2$ in v_{AB}. However, each state has a different impact on the DC bus capacitors, which is opposite to each other. Table 3 presents the logic to select 0U1 and 0L1 considering the C_1 and C_2 voltages and i_E polarity. For example, if $i_E > 0$ and $v_{C1} > v_{C2}$, state 0U1 is selected. This state causes current i_E to flow into C_2 through its positive pole. Consequently, C_2 is charged and the DC bus voltages tend to balance. On the other hand, if $i_E < 0$ and $v_{C1} > v_{C2}$, state 0L1 should be used. This state causes current i_E to flow through C_1 exiting from its positive pole. In this way, C_1 is discharged aiming the equalization of the DC bus voltages. A simple way to use these states to help balancing the neutral point is to add a controller based on Table 3. However, when i_E is zero its ripple causes a random selection of 0U1 and 0L1. To avoid this problem, a hysteresis band equal to the peak-to-peak battery current ripple is added to the feedback signal i_E.

Table 3. Logic for selecting the states 0U1 and 0L1.

$b_I = (i_E > 0)$	$b_V = (v_{C1} > v_{C2})$	$b_{dc} = b_I \oplus b_V$	State
0	0	0	0U1
0	1	1	0L1
1	0	1	0L1
1	1	0	0U1

As can be seen from Figure 4, states 0U1 and 0L1 can be imposed during two intervals of the switching cycle: $t_1 - t_2$ and $t_3 - t_4$. In this study, sampling is performed once in each complete switching cycle. Therefore, only one switching state is used during both time intervals.

When $i_E = 0$ or the ESS is disconnected from the inverter, it may be desirable to keep the inverter in operation and thus a mechanism to balance the DC bus voltages is required. For three-phase inverters, redundant switching states are available to synthesize a determined line voltage and, since they cause opposite impact on the DC bus voltages, these states are usually used to balance the neutral point [25–28]. Single-phase NPC/ANPC full-bridge inverters also have these redundant switching states. However, single-phase NPC/ANPC half-bridge inverters have no such redundant states and another approach should be considered. Depending on the application, a front-end converter, which is often used for other purposes, can also be used to balance the neutral point. Some works propose the use of a dedicated balancing circuit [29,30]. Another technique is the insertion of a DC signal into the modulating signal of the AC port [31] or into the current reference [32].

During the positive semicycle of the synthesized AC output voltage of the inverter, the power is delivered by capacitor C_1. During the negative semicycle, capacitor C_2 performs this function. In normal operation, the power delivered in the positive semicycle must be equal to that of the negative semicycle so that the current i_g are equal in both semicycles and the DC current is zero [32,33]. In practice, due to small discrepancies in the inverter or instrumentation errors, it is expected that a DC component will appear in the grid current and that will cause the DC bus capacitors voltages to become unbalanced. This unwanted DC component can be compensated by a control system. In this sense, the inclusion of a control loop capable of compensating for differences in the average voltages of the DC bus capacitors is proposed. This control action (i_{bal}) is summed with the grid current reference (i_g^*).

The transfer function between the voltage in the capacitor C_2 and current i_g is ideally given by:

$$G_{C2i}(s) = \frac{V_{C2}(s)}{I_g(s)} = \frac{V_{g,pk}/(V_{dc}/2)}{\pi C s},$$

$$(5)$$

where $C = C_1 = C_2$ and $V_{g,pk}$ is the peak voltage at PCC (Point of Common Coupling), which is the point where the inverter is connected to the utility grid.

A simple proportional compensator is proposed to generate the balancing current i_{bal}. The gain was adjusted to result in a crossover frequency of 6 Hz and phase margin of 90°. This corresponds to a settling time of approximately 100 ms.

The error signal $\delta(t)$ can be extracted from the DC bus capacitors voltages using:

$$\delta(t) = v_{C1}(t) - v_{C2}(t). \tag{6}$$

This signal presents ripple mainly in the grid frequency. To improve the compensator performance, one can add a band-stop filter (BSF) to the error signal. As a result, the compensator only acts at the DC value of $\delta(t)$. Without the BSF filter, the compensator could interfere with the grid reference current and lead to steady state errors. In this paper, a second order BSF filter was designed with a center frequency of 60 Hz and a 20 Hz stop band.

3.3. ESS Control System

The current control of the ESS is composed of the cascade association of PI and resonant controllers. The PI compensator is responsible for ensuring zero steady-state error for step inputs and for adjusting the transient response. A resonant control action is responsible for compensating the low frequency current ripple.

Initially, to design the PI controller, the control-to-output transfer function of the secondary DC port is needed, which is given by:

$$G_{iE}(s) = \frac{I_E(s)}{V_{m,dc}(s)} = -\frac{V_{dc}/(2L_E)}{s + R_s/L_E}, \tag{7}$$

where the resistance R_s is the sum of all series resistances, such as the inductor resistance (R_{LE}) and the ESS internal resistance (R_E), and so forth. The PI controller transfer function is:

$$C_{pi}(s) = k_p \frac{s + 1/T_i}{s}, \tag{8}$$

where T_i is the integral time constant and k_p is the proportional gain.

A response in the order of a few milliseconds and with minimum overshoot for the current i_E is desirable. The zero of the controller is placed to cancel the plant pole, that is, $T_i = L_E/Rs$. Thus, the closed-loop system can be approximated by a first order system, and the proportional gain can be defined as:

$$k_p = -\frac{2L_E}{T_p V_{dc}}, \tag{9}$$

where T_p is the time constant of the resulting closed-loop first order system. Considering the parameters shown in Table 2 and $T_p = 0.5$ ms, the resulting controller gains are: $k_p = -0.04444$ and $T_i = 0.008$ s. These gains correspond to a crossover frequency equal to 318 Hz and phase margin of 90 degrees.

The design of the resonant compensator was carried out similarly to that presented for the AC current control. Signal $\delta(t)$ has a dominant frequency at 60 Hz. In this way, b_{dc} also changes its logic level at the same frequency. However, the ESS current is also affected when the $v_{m,ac}$ polarity changes. Therefore, the low-frequency ripple in the ESS current is twice the grid frequency. Considering (4), the pair of conjugated complex poles is allocated in the frequency $2f_{ac}$ ($\omega_p = 2\pi 2f_{ac}$) with a damping ratio of 0.001 (ζ_p). The zero pair is allocated at the same frequency $\omega_z = \omega_p$ but with a damping ratio of $\zeta_z = 0.7$ and the gain k_r is set to 1 to keep the PI response unchanged at lower frequencies. The complete transfer function of i_E controller is given by:

$$C_{iE}(s) = \left(k_p \frac{s + 1/T_i}{s}\right) \left(k_r \frac{s^2 + 2\omega_z \zeta_z s + \omega_z^2}{s^2 + 2\omega_p \zeta_p s + \omega_p^2}\right). \tag{10}$$

Figure 8 presents the root locus and the Bode diagram for the ESS current control loop. As can be seen, the inclusion of the resonant controller causes a little change in the crossover frequency and the phase margin becomes 62.3 degrees.
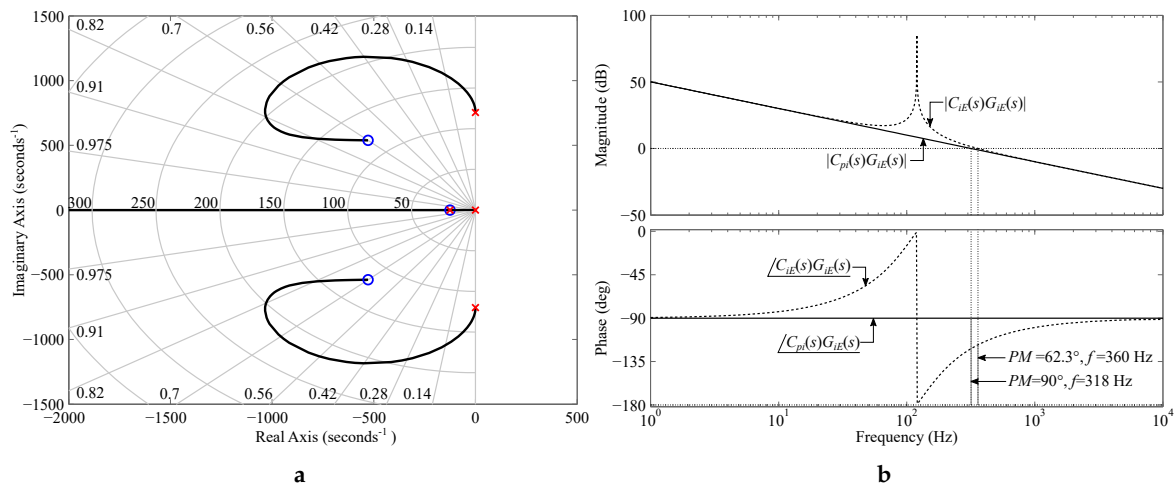

Figure 8. (**a**) Root locus of the open-loop transfer function $C_{iE}(s)G_{iE}(s)$. (**b**) Bode diagram of the open-loop transfer function considering only a PI controller and a PI+resonant control action.

4. Experimental Results and Discussions

The ANPC-3P inverter was designed according to the specifications listed in Table 2. The experimental setup is shown in Figure 9. The modulation and control systems described in this study were implemented in the dSPACE MicroLabBox 1202 platform. The inverter is composed of six IGBTs IRGP50B60PD1. The current transducers are LEM LA-25NP and the voltage measurement boards were designed based on HCNR201 optocouplers. The experiments were conducted with the DC bus connected to a DC power supply. The ESS consists of 23 valve-regulated lead acid (VRLA) batteries of 12 V and 7 Ah. The battery charging current is limited to −2 A.
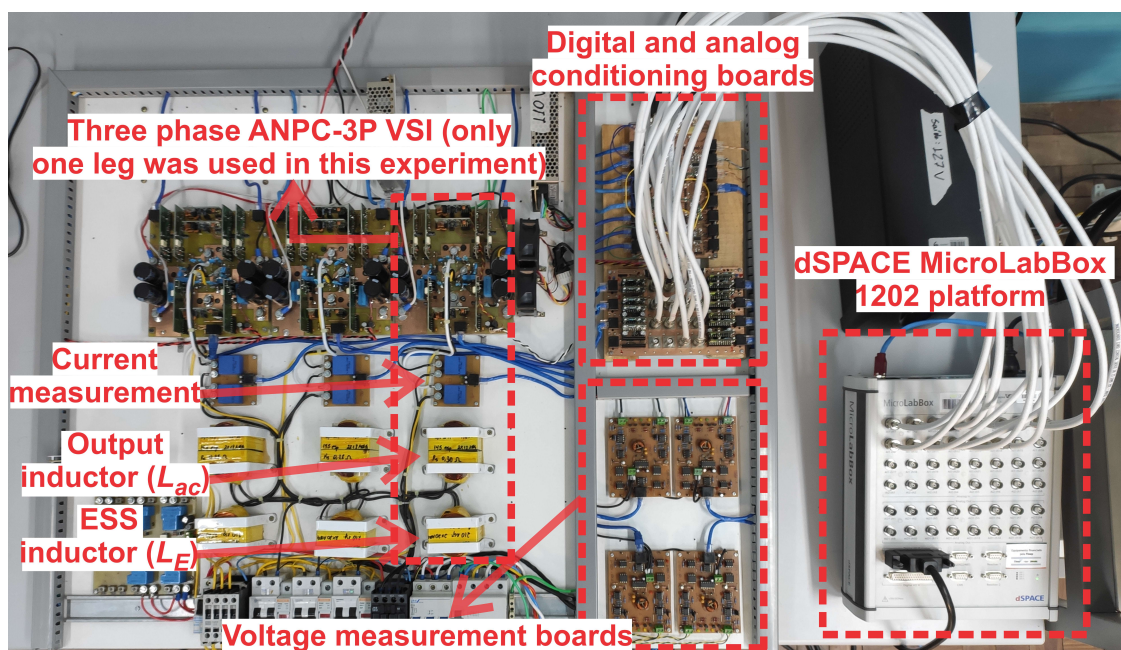

Figure 9. Picture of the experimental setup.

Figure 10 shows experimental results when the resonant control action is turned on and off in the i_E control loop. The experiments begin with the resonant controller off. It can be seen that there is 120 Hz ripple in the current i_E. Considering the time reference of the oscilloscope trigger, in $t \approx -100$ ms the resonant control action is turned on. After the transient produced by the inclusion of the controller, the current i_E presents mostly high frequency ripple. Considering the Figure 10a, in $t = 0$ ms a discharging step of 3.33 A is performed on the ESS. After this moment, the ESS provides approximately the full power injected into the grid. Additionally, the step in the ESS current i_E does not cause significant disturbance to the current i_g and the voltages across the DC bus capacitors remain balanced. It is also noted that the switch-off of the resonant controller during discharge mode in $t \approx 100$ ms has little visible effect. In Figure 10b, in $t = 0$ ms, a charging step of -2 A was performed on the ESS. The current injected into the grid was reduced to keep the nominal power (1 kW) processed by the inverter. In charging mode, at $t \approx 100$ ms the resonant controller is turned off and a significant 120 Hz ripple appears in i_E. In ESS recharge mode, resonant compensator reduces the current ripple of i_E by approximately 0.5 A peak-to-peak.
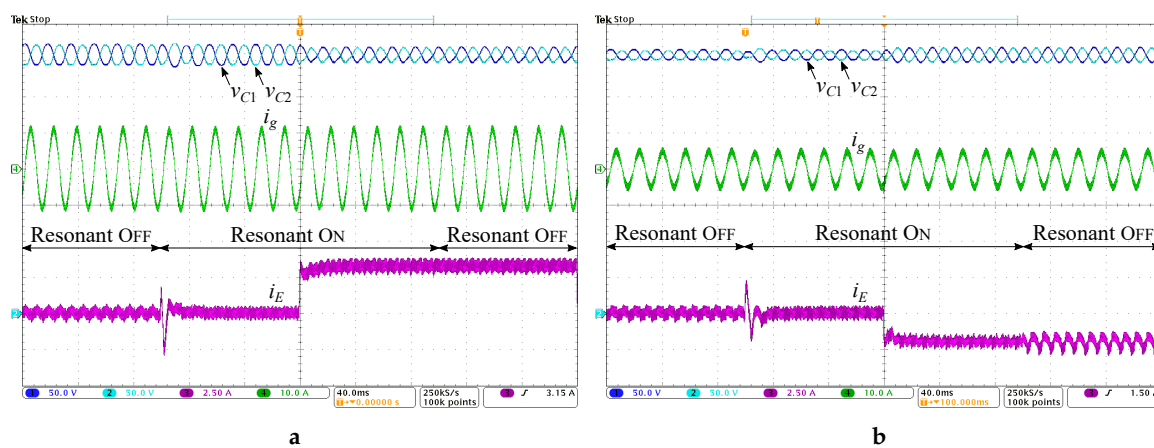

Figure 10. Experimental results showing the effect of the resonant control action and step responses of i_E. (**a**) i_E step response for the ESS commutation from floating to discharging mode. (**b**) i_E step response for the ESS commutation from floating to charging mode.

Figure 11 shows experimental results when current steps are applied on both power ports to verify dynamic performance. In these experiments, the resonant controller of i_E is kept on. In Figure 11a the power injected into the grid is always positive. At the time reference of the oscilloscope trigger, in $t = 0$ ms the power injected into the grid is increased. After, in $t \approx 100$ ms, the ESS starts to discharge with partial power compensating the power reduction of the main dc source. In $t \approx 200$ ms grid power is reduced and it is fully supplied by the ESS (V_{dc} power is near zero). Afterward, in $t \approx 300$ ms, ESS goes to recharge mode and the power injected into the grid is kept positive and constant. It can be noted that the proposed control system can maintain controlled currents and quickly reject disturbances.

In Figure 11b an experiment is shown in which the grid is charging the ESS for a certain period. At the time reference of the oscilloscope trigger, in $t = 0$ ms the ESS is switched to charging mode. The power injected into the grid is positive and constant, that is, the DC bus provides power for both the grid and the ESS. Approximately at $t \approx 100$ ms, power is drawn from the grid to supply the ESS power demand. In photovoltaic applications this condition can occur at night and/or when energy is cheaper. Then, in $t \approx 200$ ms power is injected into the grid again. Finally, in $t \approx 300$ ms the ESS returns to its initial state (floating).
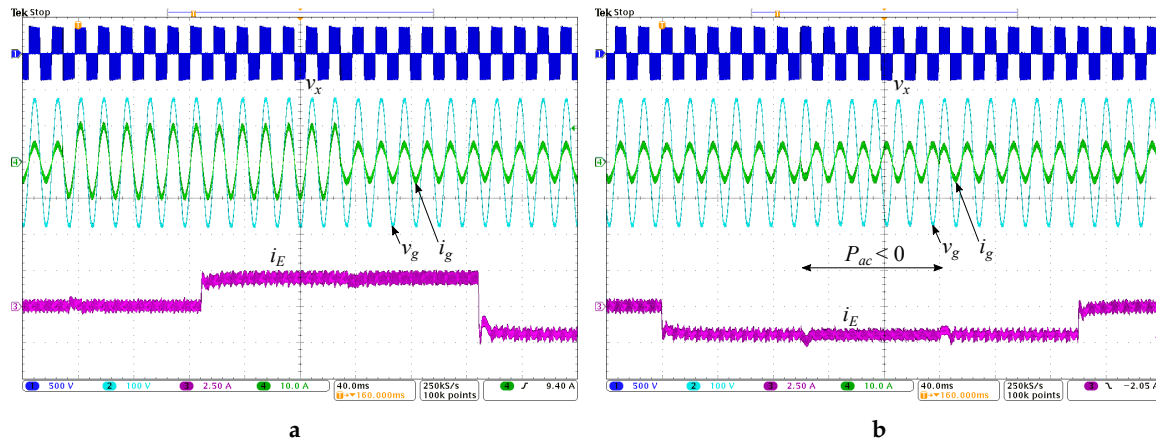
Figure 11. Experimental results showing the step responses of currents i_E and i_g under different operating modes. (**a**) $P_{ac} > 0$ and ESS in floating, charging, and discharging modes. (**b**) ESS under floating and charging modes with $P_{ac} > 0$ and ESS under charging mode with the grid supplying its power ($P_{ac} < 0$).

As shown in the experimental results, current steps performed in one power port caused a slight disturbance in the current of the other port. The modulation and the control systems of each port are independent. These disturbances occur because both ports are connected to the same DC bus. Thus, a step on one port causes disturbances in the DC bus voltages that are reflected to the other port.

During the experiments, measurements focusing on the quality of the current injected into the grid were taken. A Yokogawa WT1800 precision power meter was used to perform the measurements. When the rated current of the inverter was applied, the DC component injected into the grid was below 10 mA. The THDi was approximately 5% considering the rated AC current. The measuring equipment was configured to calculate up to the 500th harmonic (30 kHz).

5. Conclusions

The ANPC-3P topology proves to be an interesting option for grid-tied distributed generation applications, mainly when the inclusion of energy storage systems is required. A detailed analysis of the control system for this topology is presented in this paper. Special attention should be given to the control strategy of the ESS current. In addition to the ripple of the DC bus voltages caused by the pulsed behavior of AC power, there is the possibility of applying the voltage from either pole of the DC bus in v_{AB}. Depending on how the DC bus pole is selected, current i_E may present random disturbances that are more difficult to compensate. In this study, the inclusion of the i_E hysteresis function when calculating b_{dc} proved to be crucial for the correct functioning of the resonant compensator.

The experimental results demonstrate that the designed control system is capable of injecting a sinusoidal current into the grid, balance the neutral point voltage and regulate the ESS current with reduced low-frequency ripple. Both power ports of the inverter have been subjected to different operating modes, typical of grid-tied renewable generation, including the reverse power mode, in which the ESS is charged from the utility grid.

6. Patents

There is a patent application filing with the Instituto Nacional de Propriedade Intelectual—INPI (Brazil) under number BR 10 2018 015664-0.

Author Contributions: Conceptualization, S.A.T., K.V.V., M.M. and C.R.; methodology, S.A.T., K.V.V., M.M. and C.R.; software, K.V.V.; validation, S.A.T., K.V.V., M.M. and C.R.; formal analysis, S.A.T., K.V.V., M.M. and C.R.; writing–original draft preparation, S.A.T. and K.V.V.; writing–review and editing, S.A.T., K.V.V., M.M. and C.R.; supervision, C.R.; project administration, C.R.; funding acquisition, C.R. All authors have read and agreed to the published version of the manuscript.

Conflicts of Interest: The authors declare no conflict of interest. The funders had no role in the design of the study; in the collection, analyses, or interpretation of data; in the writing of the manuscript, or in the decision to publish the results.

References

1. Vazquez, S.; Lukic, S.M.; Galvan, E.; Franquelo, L.G.; Carrasco, J.M. Energy Storage Systems for Transport and Grid Applications. *IEEE Trans. Ind. Electron.* **2010**, *57*, 3881–3895. [CrossRef]

2. Tummuru, N.R.; Mishra, M.K.; Srinivas, S. Dynamic Energy Management of Renewable Grid Integrated Hybrid Energy Storage System. *IEEE Trans. Ind. Electron.* **2015**, *62*, 7728–7737. [CrossRef]

3. Abdelrazek, S.A.; Kamalasadan, S. Integrated PV Capacity Firming and Energy Time Shift Battery Energy Storage Management Using Energy-Oriented Optimization. *IEEE Trans. Ind. Appl.* **2016**, *52*, 2607–2617. [CrossRef]

4. Hou, R.; Nguyen, T.T.; Kim, H.M.; Song, H.; Qu, Y. An Energy-Based Control Strategy for Battery Energy Storage Systems: A Case Study on Microgrid Applications. *Energies* **2017**, *10*, 215. [CrossRef]

5. Faisal, M.; Hannan, M.A.; Ker, P.J.; Hussain, A.; Mansor, M.B.; Blaabjerg, F. Review of Energy Storage System Technologies in Microgrid Applications: Issues and Challenges. *IEEE Access* **2018**, *6*, 35143–35164. [CrossRef]

6. Palizban, O.; Kauhaniemi, K. Energy storage systems in modern grids—Matrix of technologies and applications. *J. Energy Storage* **2016**, *6*, 248–259. [CrossRef]

7. Riffonneau, Y.; Bacha, S.; Barruel, F.; Ploix, S. Optimal Power Flow Management for Grid Connected PV Systems With Batteries. *IEEE Trans. Sustain. Energy* **2011**, *2*, 309–320. [CrossRef]

8. Sun, K.; Zhang, L.; Xing, Y.; Guerrero, J.M. A Distributed Control Strategy Based on DC Bus Signaling for Modular Photovoltaic Generation Systems With Battery Energy Storage. *IEEE Trans. Power Electron.* **2011**, *26*, 3032–3045. [CrossRef]

9. Wang, C.; Nehrir, M. Power Management of a Stand-Alone Wind/Photovoltaic/Fuel Cell Energy System. *IEEE Trans. Energy Convers.* **2008**, *23*, 957–967. [CrossRef]

10. Abeywardana, D.B.W.; Hredzak, B.; Agelidis, V.G. Single-Phase Grid-Connected LiFePO$_4$ Battery—Supercapacitor Hybrid Energy Storage System With Interleaved Boost Inverter. *IEEE Trans. Power Electron.* **2015**, *30*, 5591–5604. [CrossRef]

11. Bhattacharjee, A.K.; Kutkut, N.; Batarseh, I. Review of Multiport Converters for Solar and Energy Storage Integration. *IEEE Trans. Power Electron.* **2019**, *34*, 1431–1445. [CrossRef]

12. Jayasinghe, S.D.G.; Vilathgamuwa, D.M.; Madawala, U.K. Diode-Clamped Three-Level Inverter-Based Battery/Supercapacitor Direct Integration Scheme for Renewable Energy Systems. *IEEE Trans. Power Electron.* **2011**, *26*, 3720–3729. [CrossRef]

13. Vechiu, I.; Etxeberria, A.; Camblong, H.; Vinassa, J.M. Three-level Neutral Point Clamped Inverter Interface for flow battery/supercapacitor Energy Storage System used for microgrids. In Proceedings of the 2nd IEEE PES International Conference and Exhibition on Innovative Smart Grid Technologies, Manchester, UK, 5–7 December 2011; pp. 1–6.

14. Teymour, H.R.; Sutanto, D.; Muttaqi, K.M.; Ciufo, P. Solar PV and Battery Storage Integration using a New Configuration of a Three-Level NPC Inverter With Advanced Control Strategy. *IEEE Trans. Energy Convers.* **2014**, *29*, 354–365.

15. Tabart, Q.; Vechiu, I.; Etxeberria, A.; Bacha, S. Hybrid Energy Storage System Microgrids Integration for Power Quality Improvement Using Four-Leg Three-Level NPC Inverter and Second-Order Sliding Mode Control. *IEEE Trans. Ind. Electron.* **2018**, *65*, 424–435. [CrossRef]

16. Cintron-Rivera, J.G.; Li, Y.; Jiang, S.; Peng, F.Z. Quasi-Z-Source inverter with energy storage for Photovoltaic power generation systems. In Proceedings of the Twenty-Sixth Annual IEEE Applied Power Electronics Conference and Exposition (APEC), Fort Worth, TX, USA, 6–11 March 2011; pp. 401–406.

17. Ge, B.; Abu-Rub, H.; Peng, F.Z.; Lei, Q.; de Almeida, A.T.; Ferreira, F.J.T.E.; Sun, D.; Liu, Y. An Energy-Stored Quasi-Z-Source Inverter for Application to Photovoltaic Power System. *IEEE Trans. Ind. Electron.* **2013**, *60*, 4468–4481. [CrossRef]

18. Vilathgamuwa, D.M.; Jayasinghe, S.D.G.; Madawala, U.K. Battery clamped three-level inverter for renewable energy systems. In Proceedings of the IECON 2011 37th Annual Conference of the IEEE Industrial Electronics Society, Melbourne, VIC, Australia, 7–10 November 2011; pp. 3105–3110.

19. Vasiladiotis, M.; Rufer, A. Analysis and Control of Modular Multilevel Converters With Integrated Battery Energy Storage. *IEEE Trans. Power Electron.* **2015**, *30*, 163–175. [CrossRef]

20. Teston, S.A.; Mezaroba, M.; Rech, C. ANPC Inverter With Integrated Secondary Bidirectional Dc Port for ESS Connection. *IEEE Trans. Ind. Appl.* **2019**, *55*, 7358–7367. [CrossRef]

21. Bala, S.; Tengner, T.; Rosenfeld, P.; Delince, F. The effect of low frequency current ripple on the performance of a Lithium Iron Phosphate (LFP) battery energy storage system. In Proceedings of the 2012 IEEE Energy Conversion Congress and Exposition (ECCE), Raleigh, NC, USA, 15–20 September 2012 .

22. Teston, S.A.; Vilerá, K.V.; Mezaroba, M.; Rech, C. Feedforward Compensation of the ESS Low-Frequency Current Ripple in the Three-Ports ANPC Converter. In Proceedings of the 2019 IEEE 15th Brazilian Power Electronics Conference and 5th IEEE Southern Power Electronics Conference (COBEP/SPEC), Santos, Brazil, 1–4 December 2019.

23. Bruckner, T.; Bernet, S.; Guldner, H. The active NPC converter and its loss-balancing control. *IEEE Trans. Ind. Electron.* **2005**, *52*, 855–868. [CrossRef]

24. Jiao, Y.; Lee, F.C. New Modulation Scheme for Three-Level Active Neutral-Point-Clamped Converter With Loss and Stress Reduction. *IEEE Trans. Ind. Electron.* **2015**, *62*, 5468–5479. [CrossRef]

25. Celanovic, N.; Boroyevich, D. A comprehensive study of neutral-point voltage balancing problem in three-level neutral-point-clamped voltage source PWM inverters. *IEEE Trans. Power Electron.* **2000**, *15*, 242–249. [CrossRef]

26. Wang, C.; Li, Y. Analysis and Calculation of Zero-Sequence Voltage Considering Neutral-Point Potential Balancing in Three-Level NPC Converters. *IEEE Trans. Ind. Electron.* **2010**, *57*, 2262–2271. [CrossRef]

27. Vilerá, K.V.; Rech, C.; Teston, S.A. Analysis of Neutral-Point Voltage Balancing in Three-Ports Active Neutral-Point-Clamped Converter. In Proceedings of the 2019 IEEE 15th Brazilian Power Electronics Conference and 5th IEEE Southern Power Electronics Conference (COBEP/SPEC), Santos, Brazil, 1–4 December 2019.

28. Zhang, Y.; Hu, C.; Wang, Q.; Zhou, Y.; Sun, Y. Neutral-Point Potential Balancing Control Strategy for Three-Level ANPC Converter Using SHEPWM Scheme. *Energies* **2019**, *12*, 4328. [CrossRef]

29. Sano, K.; Fujita, H. Voltage-Balancing Circuit Based on a Resonant Switched-Capacitor Converter for Multilevel Inverters. *IEEE Trans. Ind. Appl.* **2008**, *44*, 1768–1776. [CrossRef]

30. Luo, S.; Wu, F.; Zhao, K. Modified Single-Carrier Multilevel SPWM and Online Efficiency Enhancement for Single-Phase Asymmetrical NPC Grid-Connected Inverter. *IEEE Trans. Ind. Inf.* **2020**, *16*, 3157–3167. [CrossRef]

31. Newton, C.; Sumner, M. Neutral point control for multi-level inverters: Theory, design and operational limitations. In Proceedings of the 1997 IEEE Industry Applications Conference Thirty-Second IAS Annual Meeting, New Orleans, LA, USA, 5–9 October 1997.

32. Barater, D.; Concari, C.; Buticchi, G.; Gurpinar, E.; De, D.; Castellazzi, A. Performance Evaluation of a Three-Level ANPC Photovoltaic Grid-Connected Inverter With 650-V SiC Devices and Optimized PWM. *IEEE Trans. Ind. Appl.* **2016**, *52*, 2475–2485. [CrossRef]

33. Teymour, H.R.; Sutanto, D.; Muttaqi, K.M.; Ciufo, P. A Novel Modulation Technique and a New Balancing Control Strategy for a Single-Phase Five-Level ANPC Converter. *IEEE Trans. Ind. Appl.* **2015**, *51*, 1215–1227. [CrossRef]