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Design and Development of Non-Isolated Modified SEPIC DC-DC Converter Topology for High-Step-Up Applications: Investigation and Hardware Implementation

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Abstract: A new non-isolated modified SEPIC front-end dc-dc converter for the low power system is proposed in this paper, and this converter is the next level of the traditional SEPIC converter with additional devices, such as two diodes and splitting of the output capacitor into two equal parts. The circuit topology proposed in this paper is formulated by combining the boost structure with the traditional SEPIC converter. Therefore, the proposed converter has the benefit of the SEPIC converter, such as continuous input current. The proposed circuit structure also improves the features, such as high voltage gain and high conversion efficiency. The converter comprises one MOSFET switch, one coupled inductor, three diodes, and two capacitors, including the output capacitor. The converter effectively recovers the leakage energy of the coupled inductor through the passive clamp circuit. The operation of the proposed converter is explained in continuous conduction mode (CCM) and discontinuous conduction mode (DCM). The required voltage gain of the converter can be acquired by adjusting the coupled inductor turn's ratio along with the additional devices at less duty cycle of the switch. The simulation of the proposed converter under CCM is carried out, and an experimental prototype of 100 W, 25 V/200 V is made, and the experimental outcomes are presented to validate the theoretical discussions of the proposed converter. The operating performance of the proposed converter is compared with the converters discussed in the literature. The proposed converter can be extended by connecting voltage multiplier (VM) cell circuits to get the ultra-high voltage gain.

Keywords: clamp circuit; coupled inductor; high voltage gain; SEPIC converter; voltage stress

1. Introduction

The demand for high voltage gain dc-dc converters is increased in many real-time power electronics applications in renewable energy systems. High voltage gain dc-dc converters play a significant role in renewable energy-based systems, and this is due to the sources like individual solar photovoltaic (PV) panels, fuel cells, etc. that produce a low output voltage in the range of 20–40 V, and it has to be stepped up to 200–400 V for standalone systems or grid-tied systems with high efficiency, power quality, and the reliability. Traditional boost converters are used for the abovementioned purpose,

however, due to the limitations caused by the parasitic elements, the voltage gain cannot be increased by more than six-fold in real-time. Adjusting the duty cycle of the switch nearby one which leads to high current ripples, large magnetic components and reverse recovery issues on the semiconductor devices [1–3]. The abovementioned problems are reduced by connecting converters such as SEPIC, Zeta, Cuk, and Landsman converters. Various advanced converter topologies were introduced by researchers incorporating boosting methods such as voltage-doubler, voltage lift, voltage multiplier (VM) cells, coupled inductors, cascaded circuits, etc. These converters have their own demerits, which has motivated researchers to propose a new converter topology. The authors of [4,5] proposed a modified SEPIC converter topology to improve the voltage gain of a converter for renewable energy applications. However, the conversion efficiency of the modified SEPIC converter is less than 90% under full load conditions. In addition, the voltage stress of the semiconductor switch is equal to the output voltage of the converter. The author of [6] presented a version of the Cuk converter modified by incorporating multiple numbers of voltage lift switched inductor circuits to improve the voltage gain. However, the number of components such as inductors, diodes and capacitors are higher compared to the other converter topologies, which ultimately reduces the conversion efficiency. The author of [7,8] also presented a modified version of the Cuk converter, which comprises a conventional Cuk converter along with VM cell circuits to increase the voltage gain of the converter for renewable energy applications. However, the conversion of the efficiency of the converter is less than 90% due to the large number of components needed. The author of [9] introduced a modified Zeta converter by connecting two switches along with the passive clamp circuit to reduce the voltage stress of the switch. However, the conversion efficiency of the converter is only in the range of 85–88%. The author of [10] introduced a modified version of the Landsman converter by connecting switch reactive circuitry, which includes two diodes, one capacitor, and one inductor to improve the voltage gain the converter. However, the converter produces a negative polarity output which is suitable for very few applications. The converters discussed above comprise coupled inductors along with boosting methods such as VM cells, voltage lift, etc. to increase the voltage gain.

Among the various boosting techniques, the converter with the coupled inductor is an effective method to boost the conversion voltage of the converter, which avoids large part counts [11–13]. The key objective of this technique is to get the required voltage gain by adjusting the turn ratio of the coupled inductor without connecting a large number of components. This technique also helps to achieve a high conversion efficiency due to the lower part count. Due to various merits, the conventional SEPIC converter is provided with the coupled inductor to increase the voltage gain [14–18]. However, the converters with the coupled inductor have problems such as two magnetic circuits with a few extra components which are used to increase the voltage gain, but which may damage the power density of the converters [19–21], and the necessity of clamp circuits to recover the energy leaked by the coupled inductor which further increases the losses in the converter [22]. However, the optimal design of the coupled inductor can reduce the leakage inductance, and subsequently, the requirement of a clamp circuit, which improves the converter efficiency. Another converter topology called flyback converters have limited components, and can achieve the required voltage gain. However, it is only suitable for low power applications because large size transformers have high dc magnetization currents, which ultimately increases the power losses under CCM. As discussed earlier, many researchers are focused on developing a high-gain converter using concepts such as coupled-inductor, switched-capacitor/inductor, VM cells, etc. [23–26], but many switched-cells are utilized to get the required voltage gain with low voltage stress of the switch in many practical conditions. The converter derived with the concept called Z-source and quasi Z-source utilizes many components, and it can achieve the required voltage gain with a reduced starting inrush current. However, due to the many components, the power losses are higher than with other converters [27,28]. The authors of [29] proposed a converter with different types of clamp circuit to reduce the voltage spikes of the MOSFET switch. However, the converter efficiency is low under full-load conditions due to its passive clamp structure. The converter with voltage lift concept is presented in [30], but the

conversion efficiency is reduced due to the large part count. The authors of [31] presented a converter topology with the switched-inductor and switched-capacitor concept. The voltage gain of the presented converter is high, however, the converter requires a large number of devices, which makes the converter complex. The authors of [32] proposed a converter with a coupled inductor and voltage-doubler circuit to increase the voltage gain, however, an additional MOSFET switch is used as an active clamp circuit to reduce the voltage stress of the main MOSFET switch. The authors of [33] have investigated electromagnetic interference (EMI) mitigation techniques to reduce the EMI impact on dc-dc converters. After thorough investigations, it is always desired that the power converters be designed with a smaller number of components. This lower number of components may be an important design factor as it leads to a simple, compact, efficient power converter with less cost. Among the various available methods, utilizing a coupled inductor is a better method to improve the voltage gain to the desired level with a lower number of components. The voltage gain can be improved by increasing the coupled inductor turn ratio without adding a high number of components, and therefore, the power loss can be reduced, and hence the efficiency can be improved [34–36].

From the above discussions, it is clear that the converters discussed in the literature have positive features such as high voltage gain and continuous input current, but the large number of device components makes their converter circuits more complex. In addition, most of the converters are designed with a coupled inductor and advanced boosting techniques, and also provided with the active clamp circuit to reduce the voltage stress, which reduces the converter efficiency even further. Therefore, the proposed converter is designed with the coupled inductor without any advanced boosting techniques to get the required voltage gain with fewer losses in low power and high-power applications. The proposed converter is derived from the traditional SEPIC converter along with the concept of a coupled inductor, and less additional components compared to the conventional SEPIC converter [37]. The voltage spikes across the MOSFET switch is reduced by connecting resistor-capacitor-diode (RCD) clamp circuit, which enables the researchers to select the MOSFET switch with low on-state resistance which leads to effective and efficient design. The theoretical analysis of the proposed converter and experimental results are presented to validate the performance of the converter. The major contributions of the paper are as follows:

- The converter is basically derived from the traditional SEPIC converter with an additional diode to increase the voltage gain of the converter.
- The converter is provided with the traditional RCD clamp circuit to reduce the voltage stress of the MOSFET switch.
- Performance comparison and design guidelines of the proposed converter is discussed in detail.
- The mathematical equations of the output voltage under ideal and practical conditions are discussed for better insight.
- Finally, the circuit structure with an active clamp circuit is also proposed in this paper as a future extension.

The organization of the paper as follows: Section 2 discusses the system configuration and operation of the proposed converter in CCM, DCM, and BCM. The steady-state analysis of the proposed converter in addition to the voltage and current stresses of various devices is discussed in Section 3, and design guidelines and performance comparison are carried out in Section 4. Section 5 discusses the simulation and experimental results of the proposed converter in CCM operation. The paper is concluded in Section 6.

2. System Configuration

Figure 1a depicts the structure of the proposed converter and Figure 1b shows the equivalent circuit of the proposed converter. In Figure 1b, the variables of the proposed converter are illustrated, in which, the current through the MOSFET switch is represented as I_{ds}, the current the primary and secondary of the coupled inductor is represented as I_{Lp} and I_{Ls}, respectively, the leakage current of

the coupled inductor is represented as I_{Llk}, the current through the diodes, such as D_1, D_2, and D_3 are represented as I_{D1}, I_{D2}, and I_{D3}, the voltage stress of MOSFET is denoted as V_{ds}, and the load current is represented as I_{out}. The operating principle of the proposed converter in CCM and DCM is illustrated, and the operation in boundary conduction mode (BCM) is also briefly introduced. The proposed converter in this paper resembles the basic SEPIC converter with two additional diodes and splitting the output capacitor into two equal capacitors.

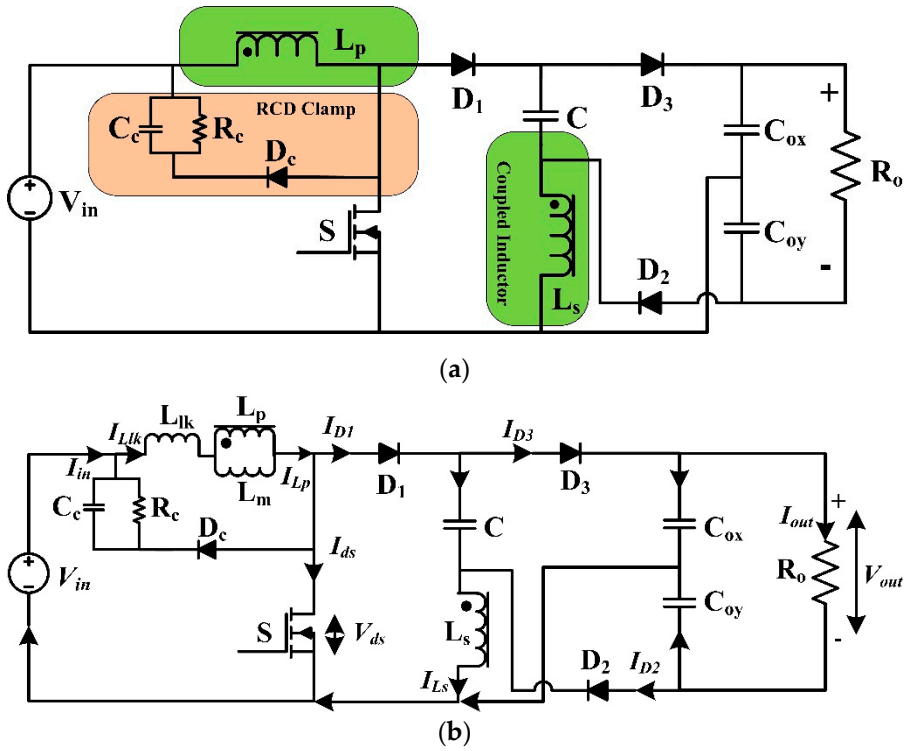


Figure 1. System configuration; (**a**) Circuit structure of the proposed converter, (**b**) Equivalent circuit of the proposed converter.

2.1. CCM Operation

It is noticed from Figure 1 that the converter topology does not need an isolated drive circuit for the MOSFET, which results in less cost. Besides, the capacitor, C, is connected in series with the coupled inductor, which stops the dc current flow in the coupled inductor and hence avoids saturation. Several assumptions are made to analyze the converter operation, which can be given as follows: (i) Diodes and MOSFET are considered as ideal devices, (ii) the value of the capacitors are large enough to produce ripple-free voltage, and (iii) the effects of leakage inductance are negligible, and the coupled inductor is modelled as an ideal transformer with a turns ratio T_2/T_1. The theoretical waveform of the proposed converter in CCM operation is illustrated in Figure 2. The operating modes are split into three modes for better understanding:

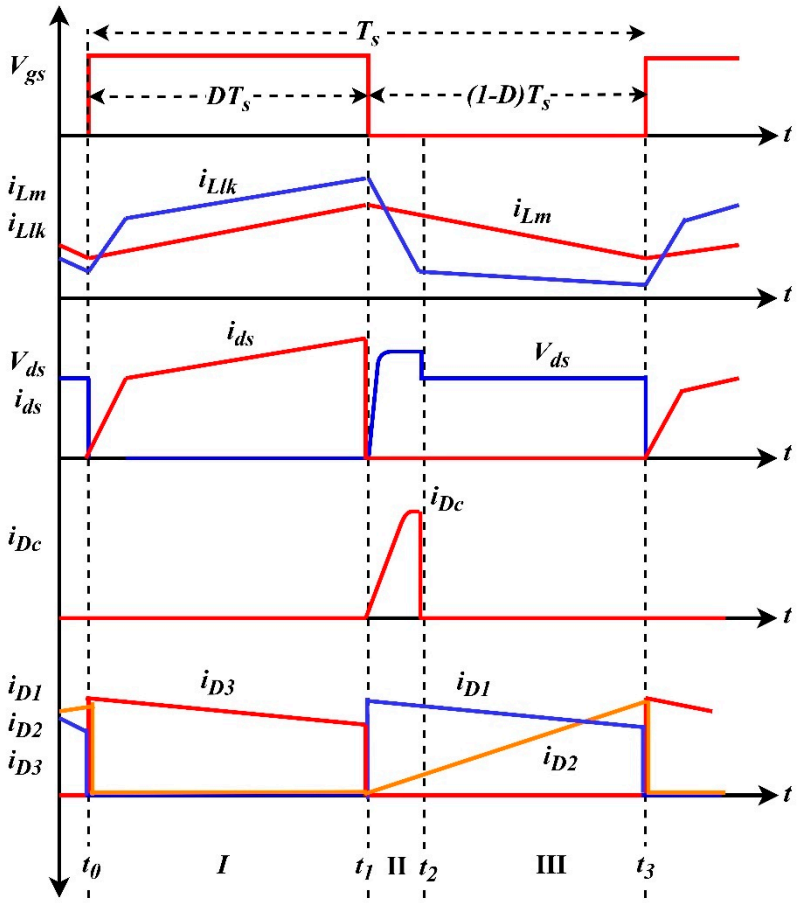


Figure 2. Theoretical waveform of the proposed converter during CCM.

Mode-1 ($t - t_1$): AT $t = t_0$, the MOSFET switch is ON, the diodes D_1, D_2 are reverse biased and the diode D_3 is forward biased. During this mode, the capacitor C delivers energy to the load along with the secondary side of the coupled inductor. The output capacitors such as C_{ox}, C_{oy} gets charged during this period. The magnetizing current reaches its maximum value at the end of this mode. The voltage across the magnetizing inductor L_m is equal to the input source voltage, V_{in}, and this mode ends at $t = t_1$. The current directions are depicted in Figure 3a.

Mode-2 ($t_1 - t_2$): AT $t = t_1$, the MOSFET switch is OFF, the diodes D_2 and D_3 are reverse biased and the diode D_1 is forward biased. During this mode, the leakage energy delivered by the coupled inductor is recovered using the RCD clamp circuit, and the voltage stress across the switch can be reduced. The diode, D_1, provides the path for the magnetizing current, and the output capacitors, C_{ox}, and C_{oy} delivers the required power to the load. This mode is very short, and this mode ends at $t = t_2$. The current directions are depicted in Figure 3b.

Mode-3 ($t_2 - t_3$): AT $t = t_1$, the MOSFET switch is turned off, the diodes D_1, D_2 are forward biased and the diode D_3 is reverse biased, which provides the path for the magnetizing current. During this mode, the output capacitors such as C_{ox}, C_{oy} delivers power to the load. At $t = t_3$, when the switch is turned on again, this mode ends. The current directions are depicted in Figure 3c.

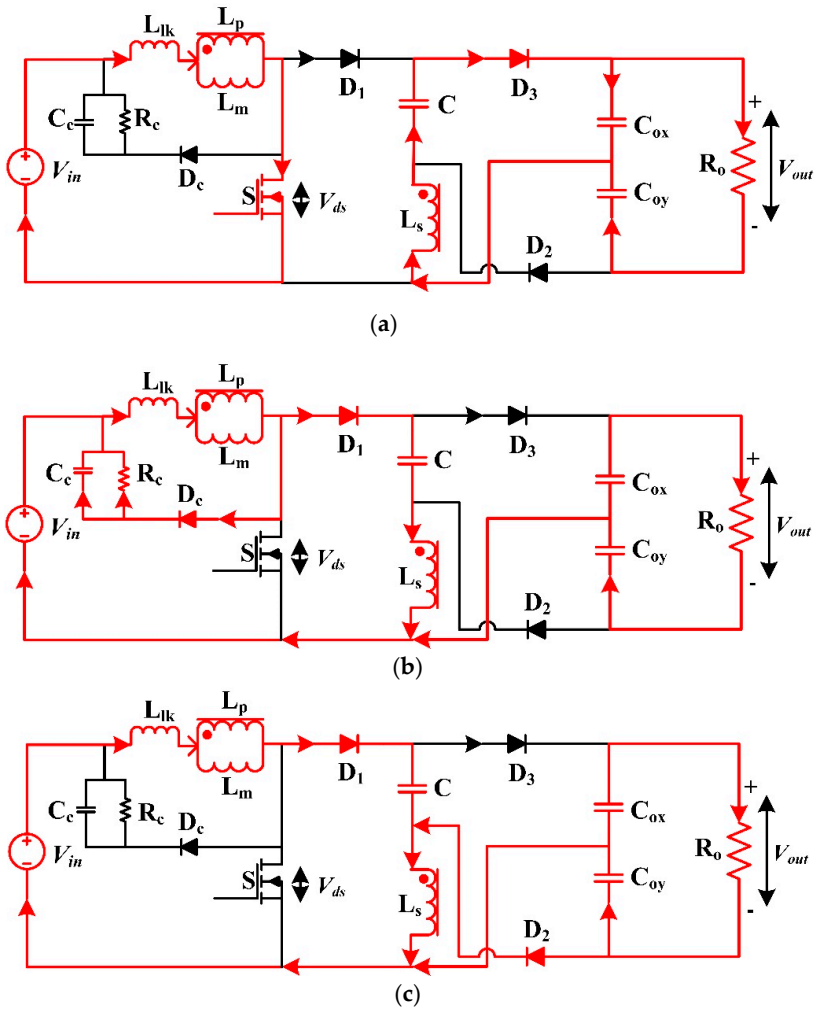


Figure 3. Modes of operation; (**a**) Mode-1, (**b**) Mode-2, (**c**) Mode-3.

2.2. DCM Operation

Similar to CCM operation, the DCM has three modes of operation, and the operation of the converter in DCM during the first two modes are similar to CCM. The key waveform of the proposed converter under DCM operation is shown in Figure 4. The current path of the third operating mode of the proposed converter is shown in Figure 5.

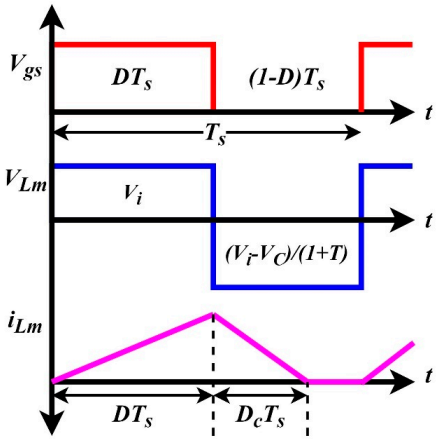


Figure 4. Theoretical waveform of the proposed converter during DCM.

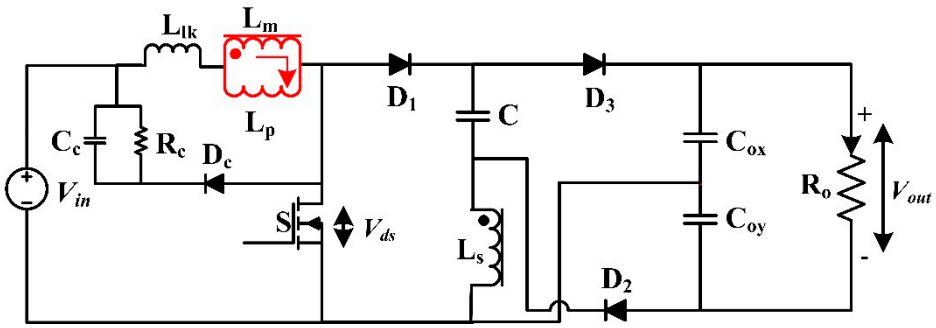


Figure 5. Third operating mode of the converter under DCM operation.

During the third mode of converter operation, the diodes such as D_1, D_2, and D_3 are reverse biased and the MOSFET switch is already in OFF state. The magnetizing current of the primary of the coupled inductor is circulated, as shown in Figure 5. At the end of this mode, the MOSFET switch is turned ON again and the cycle repeats. Practically, the converters are not allowed to operate in DCM operation due to its features such as discontinuous current, and low conversion efficiency. Moreover, the converter voltage gain is load dependent during DCM operation. Therefore, the converter under DCM operation is not recommended for any applications.

3. Steady-State Analysis of the Proposed Converter

The steady-state analysis of the proposed converter is analyzed in this section of the paper. For the investigation, the converter operation during one switching period is considered. For ease of analysis, the effect of the parasitic elements of the components is neglected to derive the expression for the static voltage gain of the proposed converter in this section. Later, the effects of parasitic elements of various components are discussed. The operation of the proposed converter is very short during Mode-2, and therefore, the converter operation during Mode-2 is not considered for steady-state analysis.

During Mode-1 (from Figure 3a), the voltage across the magnetizing inductor of the coupled inductor (V_{Lm}) is equal to the input source voltage (V_{in}), as presented in Equation (1):

$$V_{L_m}^{I} = V_{in} \tag{1}$$

During Mode-3 (from Figure 3c), the expression for the voltage across the magnetizing inductor is derived by applying Kirchhoff's voltage law (KVL) and is given in Equation (2):

$$V_{L_m}^{III} = \frac{V_{in} - V_C}{1 + T} \tag{2}$$

By using the voltage-second balance principle over one switching period of the converter, the following condition is derived:

$$DV_i + \frac{(1 - D)(V_{in} - V_C)}{1 + T} = 0 \tag{3}$$

where, the turns ratio of the coupled inductor, $T = T_2/T_1$, and the voltage across the coupling capacitor, C is as follows:

$$V_C = \frac{1 + TD}{1 - D} V_{in} \tag{4}$$

Since the output capacitor is split into two halves, the voltage across the two capacitors such as V_{Cox} and V_{Coy} needs to be derived during the converter operation. By applying KVL during Mode-1, the voltage across the capacitor, C_{ox} is obtained as:

$$V_{C_{ox}} = V_C + TV_{in} = \frac{(1+T)V_{in}}{1-D} \tag{5}$$

Similarly, by using KVL during Mode-3, the voltage across the capacitor, C_{oy} is derived as:

$$V_{C_{oy}} = \frac{V_{in}DT}{1-D} \tag{6}$$

The voltage across the capacitor can supply the converter load. Therefore, the output voltage (V_o) of the proposed converter is equal to the sum of the voltage across the capacitors, such as V_{Cox} and V_{Coy}, and is given in Equation (7):

$$V_{out} = V_{C_{ox}} + V_{C_{oy}} = \frac{(1+T)V_{in} + V_{in}DT}{1-D} \tag{7}$$

The static voltage gain, M of the proposed converter is derived from Equation (8) as follows:

$$M_{CCM} = \frac{V_{out}}{V_{in}} = \frac{1+T+DT}{1-D} \tag{8}$$

The voltage gain of the proposed converter for various values of turn's ratio of the coupled inductor is depicted in Figure 6. From Figure 6, it is observed that the voltage gain can be increased by increasing the turn ratio.

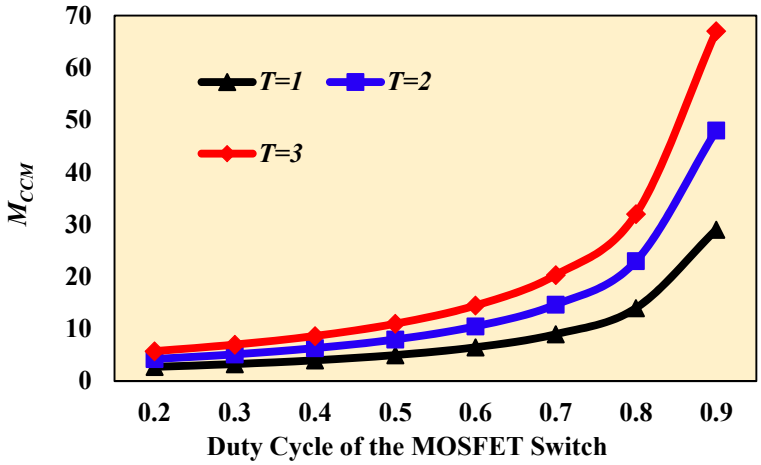


Figure 6. Voltage gain of the proposed converter for various turn ratios.

The converter proposed in this paper may also operate in BCM when the magnetizing current of the coupled inductor, i_{Lm} reaches zero during the next switching period. Figure 7 depicts the key waveform for the magnetizing voltage and its respective current. The converter enters into BCM due to reasons such as the value of L_m is a small or less loading condition or switching frequency, f_s is low. From Figure 7, the expression for the magnetizing inductor current ripple and the average value of the magnetizing inductor current are derived as follows:

$$\Delta i_{L_m} = \frac{V_i DT_s}{L_m} \tag{9}$$

$$\langle i_{L_m} \rangle = \frac{\Delta i_{L_m}}{2} = \frac{V_{in} D T_s}{2 L_m} \tag{10}$$

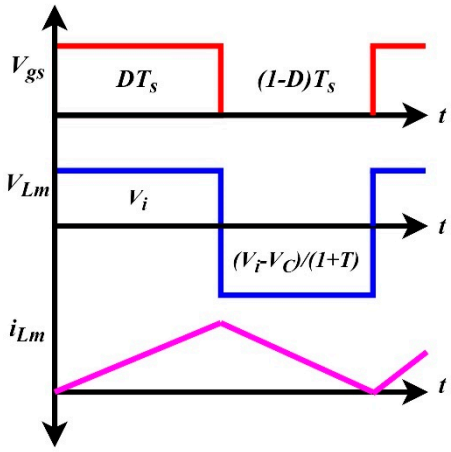


Figure 7. Voltage and current waveform during BCM.

Due to the series-connected capacitor with the secondary winding of the coupled inductor, the primary side and secondary side average values of the current is equal to zero. Therefore, by applying Kirchhoff's current law, the average value of the input current is derived as follows:

$$\langle i_i \rangle = \left\langle i_{L_m} \right\rangle \tag{11}$$

By neglecting the effect of parasitic elements of the components, the output power of the converter is assumed to equal to the input power:

$$V_{in} I_{in} = V_{out} I_{out} \tag{12}$$

Substitute Equation (8) and Equations (10)–(11) in Equation (12) and Equation (12) is modified as follows:

$$\frac{V_{in} D T_s}{2 L_m} = \frac{1 + T + DT}{1 - D} I_{out(boundary)} \tag{13}$$

From Equation (13), the boundary value of the output current ($I_{o(boundary)}$) and the normalized boundary value of the output current are simplified as follows:

$$I_{out(boundary)} = \frac{D(1-D)^2 V_{out}}{2 L_m f_s (1 + T + TD)^2} \tag{14}$$

$$\frac{I_{out(boundary)}}{\frac{V_{out}}{2 L_m f_s}} = \frac{D(1-D)^2}{(1 + T + TD)^2} \tag{15}$$

From Equation (14), the expression for the magnetizing inductance is derived and presented in Equation (16). This is the minimum value of the magnetizing inductance (L_m) to maintain the converter operation in CCM, and the converter goes to DCM operation if the value of L_m is small. In addition, the boundary value of the output load resistance is given in Equation (17):

$$L_m \geq \frac{D(1-D)^2 V_{out}}{2 I_{0ut(boundary)} f_s (1 + T + TD)^2} \tag{16}$$

$$R_{o(boundary)} = \frac{2f_s L_m (1 + T + TD)^2}{D(1-D)^2} \tag{17}$$

As discussed earlier, the converter goes to DCM operation if the value of load resistance is small, as presented in Equation (17). The plot between the normalized boundary output current and the duty cycle of the switch for various turns ratio of the coupled inductor is illustrated in Figure 8. It is observed from Figure 8 that the CCM operating region of the converter can be increased by increasing the turn's ratio. As discussed earlier, the converter enters into DCM operation if it crosses the boundary, as shown in Figure 8. When the converter in DCM operation, the average value of the inductor magnetizing current is derived as follows:

$$\langle i_{L_m} \rangle = \frac{\Delta i_{L_m}(D + D_c)}{2} = \frac{V_{in} D(D + D_c) T_s}{2L_m} \tag{18}$$

where, $D_c T_s$ is the time to reach zero value from the maximum value by the magnetizing inductor current.

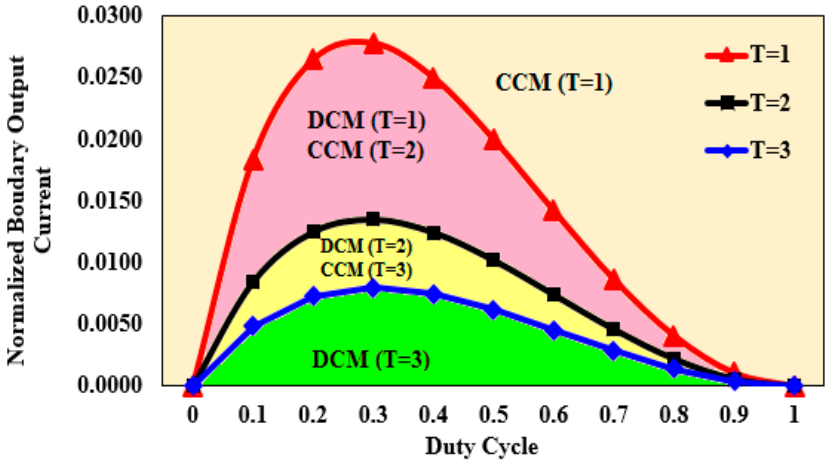


Figure 8. Normalized boundary output current of the converter for various turns ratio.

Equation (19) is derived from Equations (11) and (12) for obtaining the expression for the duty cycle of the switch during DCM operation:

$$\frac{V_{in}^2 D(D + D_c)}{2f_s L_m} = \frac{V_{out}^2}{R_o} \tag{19}$$

By applying the volt-second balance principle as similar to Equation (3), the following expression is derived:

$$DV_{in} + \frac{D_c(V_{in} - V_C)}{1 + T} = 0 \tag{20}$$

From Equations (3), (4) and (20), the voltage gain of the proposed converter under DCM operation is obtained as follows:

$$M_{DCM} = \frac{V_{out}}{V_{in}} = \frac{(1+T)}{D_c}\left(\frac{TD(1-D) + (1+TD)D_c}{1-D}\right) = \sqrt{\frac{D(D + D_c)}{2\tau_s}} \tag{21}$$

where, the normalized time constant is represented as τ_s and is presented in Equation (22). In addition, the expression for the duty cycle D_c is derived as follows:

$$\tau_s = \frac{L_m}{R_o T_s} \tag{22}$$

$$D_c = \frac{D(1+T)V_{in}}{V_{out} - V_{in}(1+T)} \tag{23}$$

From Equation (21), it is observed that the voltage gain of the proposed converter during DCM operation is load-dependent, and usually, the converter under DCM is not preferable for any practical applications.

Voltage Stress and Current Stress of MOSFET and Diodes

Apply KVL in Figure 2c to derive the voltage stress of the MOSFET switch during Mode-3 of CCM operation. The MOSFET voltage stress is derived as follows:

$$V_{ds} = V_{in} - V_{L_m}^{III} = V_{in} - \frac{(V_{in} - V_C)}{1+T} = \frac{V_{in}}{1-D} = \frac{V_{out}}{1+T+TD} \tag{24}$$

From Equation (24), it is noticed that the voltage stress of the MOSFET switch is very much less than the output voltage of the converter. The switching power loss of the MOSFET switch is derived as follows, in which the intrinsic capacitance of the MOSFET switch is represented as C_s:

$$P_{sw} = f_s C_s V_{ds}^2 = f_s C_s \frac{V_{in}^2}{(1-D)^2} \tag{25}$$

From Equation (25), it is noticed that the switching loss of the proposed converter is less than the conventional SEPIC converter. Besides, it enables the researcher to select the low voltage rating MOSFET switch with low on-state resistance ($r_{ds\text{-}on}$) for the switching operation, which further reduces the conduction loss and hence the efficiency. The voltage stress of the diodes, such as V_{D1}, V_{D2}, and $V_{D3,}$ is derived as follows:

$$V_{D_1} = \frac{1+T}{1-D} V_{in} \tag{26}$$

$$V_{D_2} = V_{D_3} = \frac{TV_{in}}{1-D} \tag{27}$$

The average value of MOSFET current is equal to the average value of the magnetizing inductor current. In addition, the average value of magnetizing inductor current is equal to the average value of the input current, and this is due to the average value of the primary side inductor current is equal to zero. By considering all these facts, the current stress of the MOSFET switch is derived and is given in Equation (29):

$$\langle I_{ds} \rangle = \langle I_{L_m} \rangle = \langle I_{in} \rangle = \frac{1+TD}{1-D} I_{out} \tag{28}$$

$$I_{ds} = \frac{(1+TD)}{D(1-D)} I_{out} \tag{29}$$

The current stress of all the diodes is derived as follows:

$$I_{D_2} = I_{D_3} = I_{out}/D \tag{30}$$

$$I_{D_1} = I_{out}/(1-D) \tag{31}$$

From the above discussions, it is noticed that the voltage stress across the switch and diodes is lower than half of the output voltage of the proposed converter. Therefore, the switch with low on-state resistance has been selected for the proposed converter resulting in less conduction loss with high conversion efficiency.

4. Design Guidelines and Performance Comparison of the Proposed Converter

4.1. Design Guidelines

The specifications of the proposed converter are presented in Table 1 and based on the specifications; an experimental prototype is made to validate the performance of the proposed converter.

Table 1. Electrical specification of the proposed converter.

S. No.	Parameters	Range
1	Input voltage range, V_{in}	20–30 V
2	Output voltage, V_{out}	200 V
3	Output power, P_{out}	100 W
4	Switching frequency, F_s	50 kHz
5	Voltage ripple	<1%
6	Coupled inductor turns ratio, T	2
7	Inductances, L_m and L_{lk}	200 µH, 2 µH
8	Capacitance, C	10 µF
9	Capacitance, C_{ox} and C_{oy}	22 µF
10	Clamp resistance, R_c	3.3 kΩ
11	Clamp capacitance, C_c	6 nF

From Equation (8), the minimum and maximum value of the duty cycle of the switch as follows:

$$D_{min} = 1 - \left[\frac{(1 + T + TD)V_{i,max}}{V_0}\right] = 0.4 \tag{32}$$

$$D_{max} = 1 - \left[\frac{(1 + T + TD)V_{i,min}}{V_0}\right] = 0.6 \tag{33}$$

The optimal value of the duty cycle is 0.5, and therefore the proposed converter is switched at 0.5 duty cycle for the optimal duty cycle. From Equation (24), the voltage stress of the MOSFET switch is equal to 50 V, and the value of the maximum current stress of the switch is calculated as follows:

$$I_{ds,max} = \frac{(1 + TD_{max})}{D_{max}(1 - D_{max})}[I_{out}] = 4.58 \text{ A} \tag{34}$$

Based on the above discussions, the voltage and current rating of the MOSFET should be more than 50 V and 4.58 A, and therefore, a MOSFET IRFB4410 with 100 V, and 96 A rating is selected for the proposed converter. The minimum value of the magnetizing inductance is calculated by substituting the minimum value of the duty cycle of the switch in Equation (16), and is presented in Equation (35). If the value of the magnetizing inductance is less than the value calculated using Equation (35), the converter operation goes to DCM:

$$L_m \geq \frac{0.4(1 - 0.4)^2 \times 200}{2 \times 0.5 \times 50000 \times (1 + 2 + (2 * 0.4))^2} = 39.58 \text{ µH} \tag{35}$$

By using Equation (35), the minimum value of the magnetizing inductance is calculated and is found equal to 39.58 µH. The value is selected as 200 µH to maintain the converter operation in CCM. Finally, the coupled inductor is designed with EI33 ferrite core by considering the values T = 2, and L_m = 200 µH for the CCM operation. Similarly, the voltage stress of the diodes such as V_{D1}, V_{D2}, and V_{D3} is calculated using Equations (26) and (27) and is equal to 150 V, 100 V, and 100 V, respectively. In addition, the current stress of the diodes such as I_{D1}, I_{D2}, and I_{D3} is calculated using Equations (30) and (31), and is equal to 1 A, 1 A, and 1 A, respectively. By considering all the facts, a Schottky diode

(MUR820) with rating 200 V, 8 A, has been selected for the converter operation. The value of the output capacitor (C_o) is calculated using Equation (36), and is given below:

$$C_0 = \frac{(1 - D_{max})I_{0ut}}{f_s \Delta V_C} = \frac{(1 - 0.6) \times 0.5}{50000 \times 1.1} = 3.63\ \mu\text{F} \tag{36}$$

In the proposed converter, the output capacitor is split into two equal parts, and the output capacitance, such as C_{ox} and C_{oy} is equal to 20 µF. Therefore, the output capacitors such as C_{ox} and C_{oy} are selected as 22 µF, 250 V (electrolytic type) each. The minimum value of the capacitor, C, can be calculated using Equation (16):

$$C_{min} \geq \frac{I_{0ut}}{f_s \Delta V_C} = \frac{0.5}{50000 \times 1.1} = 9.09\ \mu\text{F} \tag{37}$$

The value of the coupling capacitor, C, is calculated as 9.09 µF, and for ripple-free operation, 10 µF, 250 V electrolytic capacitor has been selected. The values of the resistor and the capacitor in the RCD clamp is selected based on the literature [38,39]. In the proposed converter, the peak voltage of the MOSFET switch is clamped, which should satisfy the following equation:

$$V_{dss} > V_{in} + V_{C_c} \tag{38}$$

where, the breakdown voltage of the MOSFET switch is represented as V_{dss}, and the voltage across the clamp capacitor, $C_{c,}$ is represented as V_{Cc}. The voltage ripple in the clamp capacitor voltage is negligible by selecting a large value for the clamp capacitor, i.e., $C_c > T_s/R_c$, where T_s is switching period, and the clamp resistance is represented as R_c. This breakdown voltage increases until the power dissipated the clamp resistor, P_{Rc} is equal to the average leakage inductance power transfer, P_{Llk}:

$$P_{L_{lk}} = \frac{W_{L_{lk}}}{T_s} = P_{R_c} = 1.63 \times 10^{-6} \times 50 \times 10^3 = 81.92\ \text{mW} \tag{39}$$

$$W_{L_{lk}} = \frac{1}{2} L_{lk} I_{ds}^2 = 1.63\ \mu\text{J} \tag{40}$$

The voltage across the clamp resistance during the off period of the switch must satisfy the following equation:

$$V_{R_c} = V_{C_c} = \vartheta \times V_{ds,max} - V_{in} = (0.8 \times 50) - 25 = 15\ \text{V} \tag{41}$$

where, ϑ is voltage security constant and is usually equal to 0.8–0.95. Moreover, now, the expression for the clamp resistance and the clamp capacitance is derived as follows:

$$R_c = \frac{V_{R_c}^2}{P_{L_{lk}}} = \frac{15^2}{81.92 \times 10^{-3}} \cong 3.3\ \text{k}\Omega \tag{42}$$

$$C_c > T_s/R_c \cong 6\ \text{nF} \tag{43}$$

4.2. Performance Comparisons

The converter proposed in this paper is compared with the traditional SEPIC dc-dc converter with the coupled inductor [23]. In addition, the voltage gain of various converters is plotted in Figure 9. The performance comparison is also presented in Table 2. As seen in Figure 9, the voltage gain of the proposed converter is higher than the traditional SEPIC converter proposed in [23] by adding an extra two diodes and one capacitor with the traditional one. In addition, as seen in Table 2, the voltage stress of the switch in the proposed converter is much less than the conventional converter when the turn's ratio of the coupled inductor is higher than one, which also helps to select the MOSFET switch with

low $r_{ds\text{-}on}$. This helps the converter to achieve high conversion efficiency by minimizing the switching and conduction losses.

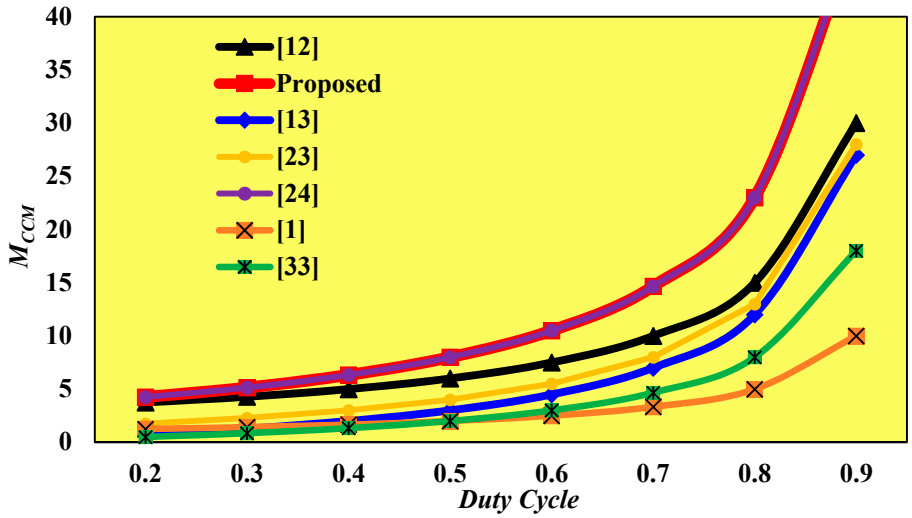


Figure 9. Voltage gain comparison among various converters.

Table 2. Performance comparison of the proposed converter with other topologies.

Ref.	Year	M	V_{ds}	I_{ds}	Input Current Ripple	No. of Components					N_{total}	Rating
						CI	D	C	S	L		
Proposed	-	$\frac{1+T+TD}{1-D}$	$\frac{V_in}{1-D}$	$\frac{(1+TD)}{D(1-D)}I_{out}$	Low	1	4	4	1	-	10	100
[1]	2019	$\frac{1}{1-D}$	$\frac{V_{in}}{1-D}$	$\frac{D}{(1-D)}I_{out}$	High	1	1	3	1	-	6	60
[12]	2013	$\frac{1+T}{1-D}$	$\frac{V_{in}}{1-D}$	-	Medium	1	4	5	1	1	12	500
[13]	2003	$\frac{D(1+T)}{1-D}$	$\frac{V_{in}}{1-D}$	-	High	1	2	3	2	-	8	36
[23]	2010	$\frac{TD}{1-D}$	V_{out}	$\frac{(1+T)}{(1-D)}I_{out}$	High	1	2	4	1	1	9	200
[24]	2013	$\frac{1+T+TD}{1-D}$	$\frac{V_{in}}{1-D}$	-	Low	1	5	6	1	-	13	150
[40]	2018	$\frac{T+2+D}{1-D}$	$\frac{V_{in}}{1-D}$	$\left(\frac{2(T+1)}{D}+\frac{2D+3}{1-D}\right)I_{out}$	Low	1	5	7	1	1	15	200
[41]	2017	$\frac{1+T+TD}{(1-D)^2}$	$\frac{V_{in}}{1-D}$	-	Medium	2	5	6	1	1	14	150
[42]	2018	$\frac{2+T+D}{1-D}$	$\frac{V_{in}}{1-D}$	$\left(\frac{2T}{D}+1\right)I_{out}$	Low	1	4	6	1	1	13	100
[43]	2019	$\frac{D}{(1-D)^2}$	V_{out}	-	Medium	-	3	4	1	3	11	100

N_{total}—Total number of components, CI—Coupled inductor, D—Diode, L—Inductor, S—Switch, C—Capacitor.

The proposed converter is also compared with the other converter topologies, which is employed with the coupled inductors. However, the converters with a high-boosting technique such as VM cells, voltage lift, quadratic boost, cascaded connections are not considered for the comparison. To have a fair performance comparison, the converter with two winding coupled inductor with a single MOSFET switch is taken into account. Therefore, the proposed converter is compared with nine other converter topologies in terms of voltage gain, a number of components, and voltage stress of the switch.

From Table 2, it is witnessed that the proposed converter holds a better position in terms of a device count, MOSFET voltage stress, and the voltage gain when compared to other converters except the converter presented in [24]. The voltage gain of the proposed converter and the converter proposed in [24] is similar; however, the proposed converter has one diode and one capacitor less in number. Moreover, the voltage gain is four times better than the traditional coupled inductor based SEPIC converter.

4.3. Efficiency and Power Loss Analysis

The analysis of the converter efficiency is discussed in this section of the paper. The equivalent circuit of the proposed converter, including the internal resistance of each component is illustrated in Figure 10, in which, r_{L_p} and r_{L_s} are the coupled inductor's primary and secondary Equivalent Series Resistance (ESR), respectively. Similarly, the internal resistance of the diodes are denoted as r_{D_c}, r_{D_1}, r_{D_2}, and r_{D_3} and its respective forward voltage drop is represented as V_{FD_c}, V_{FD_1}, V_{FD_2}, and V_{FD_3}. The conducting duration of the clamp diode is very less, and therefore, the effect of the clamp diode parasitic element and the voltage drop is neglected in this paper. The on-state resistance of the MOSFET switch is represented as r_{ds}.

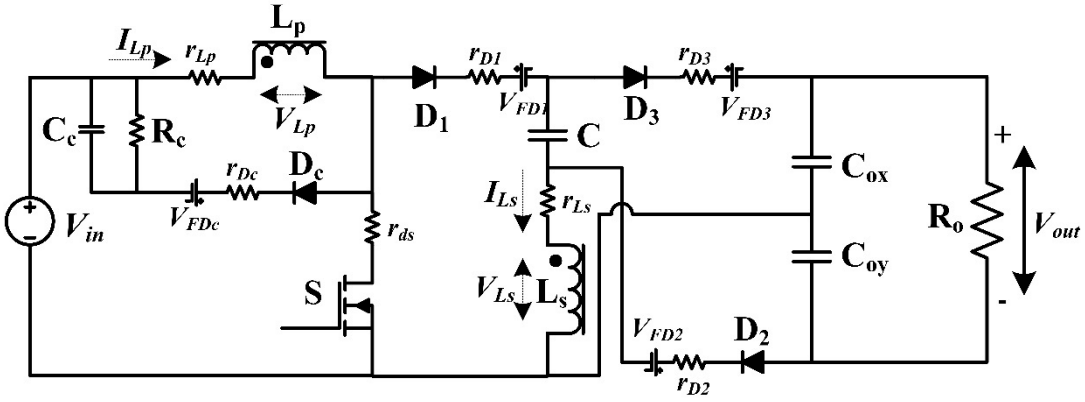


Figure 10. Proposed converter with ESR of MOSFET, coupled inductor, switch and diode voltage drops.

The voltage equation of two sides of the coupled inductor by considering the parasitic elements in nonconducting and conducting states are given as follows:

$$\left.\begin{array}{c} V_{L_p} = V_{in} - I_{L_p}\left(r_{L_p} + r_{ds}\right) \\ V_{L_s} = V_C + V_{C_{ox}} - I_{L_s}\left(r_{L_s} + r_{D_3}\right) - V_{FD_3} - V_{out} + V_{C_{oy}} \end{array}\right\} \text{ON State} \tag{44}$$

$$\left.\begin{array}{c} V_{L_p} = V_{in} - I_{L_p}\left(r_{L_p} + r_{L_s} + r_{D_1}\right) - V_{FD_1} - V_C \\ V_{L_s} = -V_C - V_{C_{ox}} - I_{L_s}\left(r_{L_s} + + r_{D_2}\right) - V_{FD_2} + V_{out} + V_{C_{oy}} \end{array}\right\} \text{OFF State} \tag{45}$$

The output voltage of the proposed converter is derived by applying the volt-second balance principle by considering the components voltage drop and is presented as follows:

$$V_{out} = \frac{V_{in}(1 + T + DT)}{1 - D} - \left[Ar_{L_p} + Br_{L_s} + Cr_{ds} + Er_{D_1} + Fr_{D_2} + Gr_{D_3}\right] \tag{46}$$

where, $A = \frac{V_{in}(1+TD)^2}{R_o(D(1-D))^2}$, $B = \frac{DV_{in}}{R_o}$, $C = \frac{V_{in}(1+TD)}{R_oD(1-D)}((1-D) + 1 + D(2-D))$, $E = \frac{V_{in}}{R_o(1-D)}\left(D^2 + V_{D_1}\right)$, $F = \frac{V_{in}}{R_oD}\left(D^2 + V_{D_1}\right)$, and $G = \frac{V_{in}}{R_oD}\left((1-D) + V_{D_3}\right)$. From above all equation, it is worth noticing that the voltage drop of the MOSFET switch is high as compared to diodes and the voltage drop of the diode, D_3 and the secondary of the coupled inductor is less at 50% duty cycle. The converter efficiency and the output voltage gain are affected by the switching loss of the MOSFET and the conduction loss of the various components. The expression for the converter efficiency is given in Equation (47). The efficiency of the proposed converter is analyzed by calculating the power losses of the circuit elements. The converter efficiency is calculated as follows:

$$\eta = \frac{P_{out}}{P_{out} + P_{loss}} = \frac{P_{out}}{P_o + P^S_{loss} + P^C_{loss} + P^{CI}_{loss} + P^D_{loss}} \tag{47}$$

where, P_{out} is the output power of the converter, P^{S}_{loss} is the loss due to the MOSFET switch, P^{C}_{loss} is the loss due to the capacitors, P^{CI}_{loss} is the loss due to the coupled inductor, and P^{D}_{loss} is the loss due to the diodes. The MOSFET power loss is equal to the sum of the switching loss ($P^{S}_{SW-loss}$) and the conduction loss (P^{S}_{c-loss}) and the expression is given as follows:

$$P^{S}_{loss} = P^{S}_{SW-loss} + P^{S}_{c-loss} = \frac{1}{2} V_{ds} I_{ds} \left(t_f + t_r\right) f_s + r_{ds} I^{2}_{ds} \tag{48}$$

where, t_f and t_r are falling and rising time of the MOSFET switch and the switching frequency is represented as f_s. From above all equations, the expression for the power losses of the MOSFET switch is given as follows:

$$P^{S}_{SW-loss} = \frac{1}{2} \frac{V_{in}}{1-D} \times \frac{V_{out}(1+TD)}{R_o(1-D)} \left(t_f + t_r\right) f_s \tag{49}$$

$$P^{S}_{c-loss} = r_{ds} \times \left[\frac{V_{out}(1+TD)}{R_o(1-D)}\right]^2 \tag{50}$$

The expression to calculate the loss of each diode, capacitors, and the coupled inductor are as follows:

$$P^{D}_{loss} = V_F \times \langle I_D \rangle + \left(r_D \times {I_{D(rms)}}^2\right) \tag{51}$$

$$P^{C}_{loss} = r_C \times {I_{C(rms)}}^2 \tag{52}$$

$$P^{CI}_{loss} = r_L \times {I_{L(rms)}}^2 \tag{53}$$

where V_F is the forward voltage drop of the diode, r_D is the ESR of the diode, r_C is the ESR of the capacitors, and the r_L is the ESR of the coupled inductor.

5. Results and Further Discussion

To validate the theoretical analysis of the proposed converter, the converter is first simulated and also verified with the experimental results in further sub-sections. The simulations and experimentations were carried-out by considering the various parameters listed in Table 1.

5.1. Simulation Results

To validate the performance of the proposed converter, the simulations are carried out using MATLAB/Simulink software, and various simulation waveforms are illustrated in Figure 12. The simulation is carried out at full load condition. To get the required voltage gain, the duty cycle of the MOSFET switch of adjusted to 0.5. The load resistance, R_0 is selected as 400 Ω, 2 A. The electrical specifications of the proposed converter, the values of capacitance and the coupled inductor inductances are listed in Table 1.

The gate-source voltage and the voltage stress of the MOSFET switch are shown in Figure 12a, and from Figure 12a, it is noticed that during Mode-2, the maximum voltage stress is about 60 V, and during Mode-3, the maximum voltage stress about 50 V, as discussed earlier. The remaining 10 V is clamped using the RCD clamp circuit, and the voltage stress across the clamp diode (V_{Dc}) is shown in Figure 12c. The maximum current stress of the MOSFET switch at a 0.5 duty cycle is calculated using Equation (29), and is equal to 4 A. The same can be noticed from Figure 12b. During the OFF time of the MOSFET switch, the voltage stress of the clamp diode is equal to the voltage stress of the MOSFET switch. Figure 12d illustrates the current waveforms of the diode D_1 and the diode, D_c. It is observed from Figure 12d that the current stress of the diode, I_{D1} is equal to 1 A and the same can be calculated using Equation (31). It is also noticed that the clamp diode clamps the leakage energy during mode-2 and the current stress of the clamp diode, I_{Dc} is observed as 0.78 A. The voltage stress of the diodes such as V_{D1}, V_{D2}, and V_{D3} are calculated using Equations (26) and (27), and is equal to 150 V, 100 V, and 100 V, respectively. The same can be observed in waveforms, as depicted in

Figure 12e,f. The average value of the current stress of the diodes, such as I_{D2} and $I_{D3,}$ is calculated using Equation (30), and is equal to 1 A and 1 A, respectively. The same can be observed in waveforms, as depicted in Figure 12g. The voltage across the capacitors such as V_C, V_{Cox}, and V_{Coy}, and calculated using Equations (4)–(6), and is equal to 100 V, 150 V, and 50 V, respectively. The same can be observed in Figure 12h. The output voltage, V_{out} of the proposed converter is equal to the sum of the voltage across the capacitors, V_{Cox} and V_{Coy}, and is equal to 200 V. The same can be observed in Figure 12i for the input voltage, V_{in} is equal to 25 V. All the simulation waveforms are in good agreement with the theoretical discussions, as presented in Section 2 of this paper. Therefore, the performance of the proposed converter is validated using simulations.

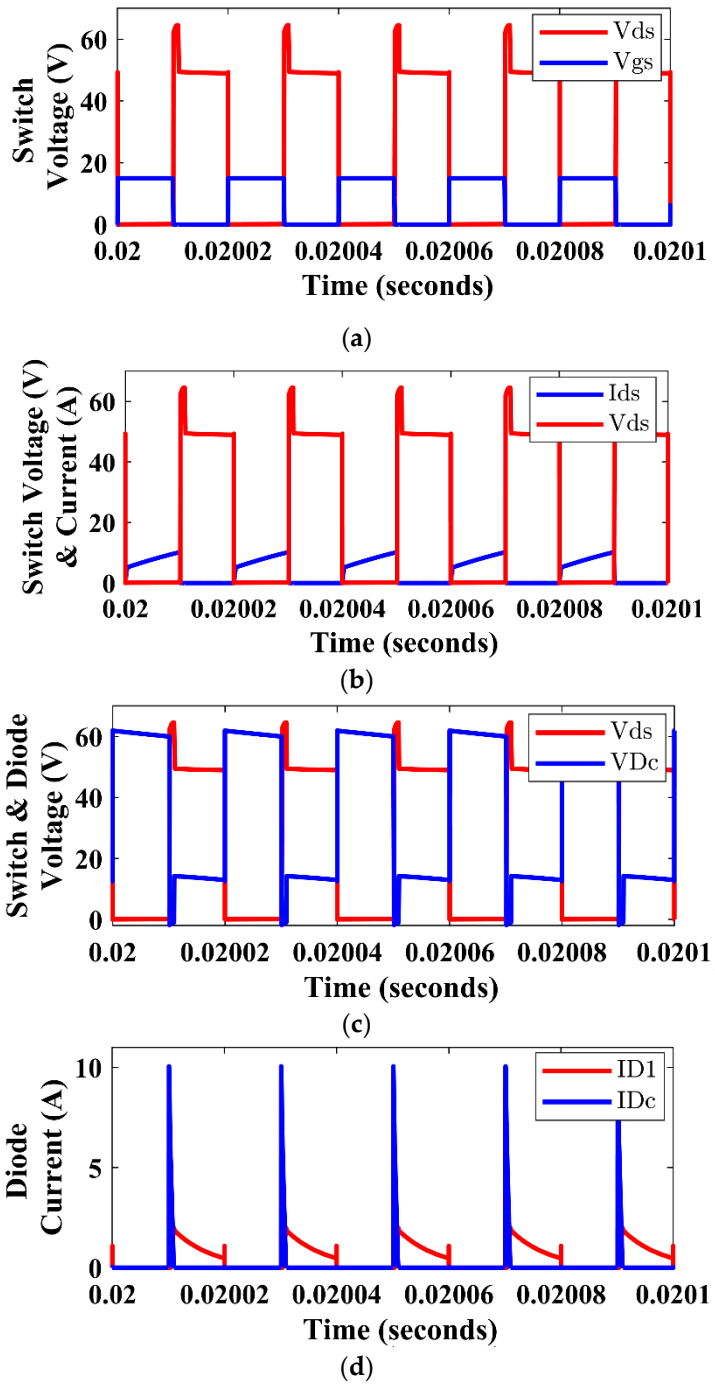
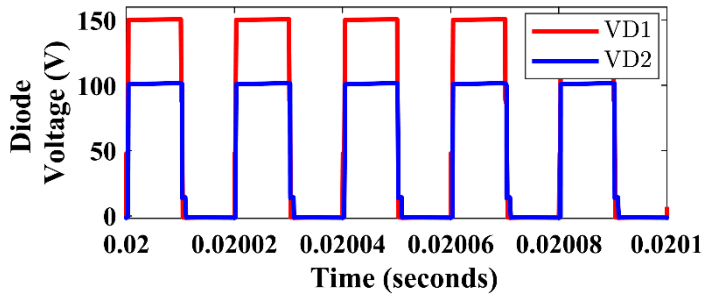
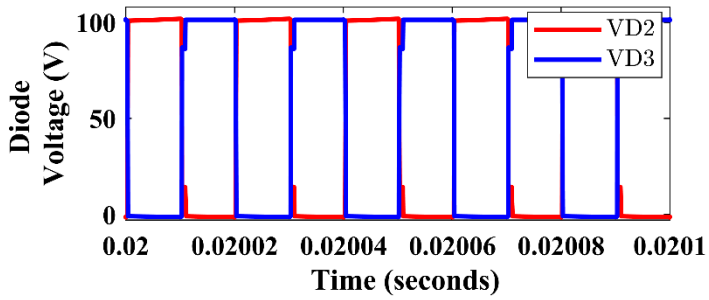


Figure 11. *Cont.*



(e)



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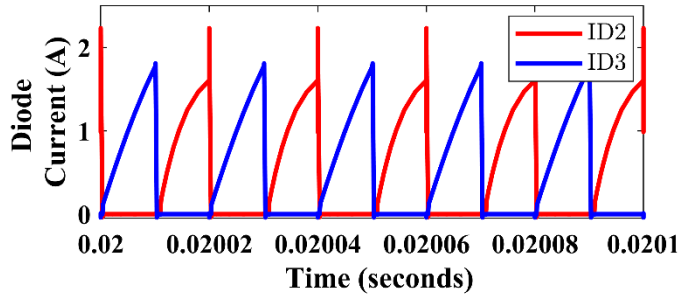
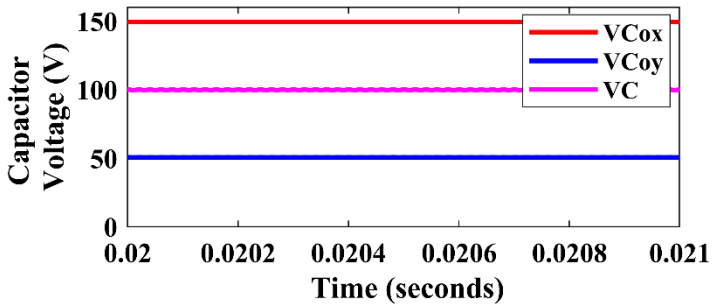


(g)



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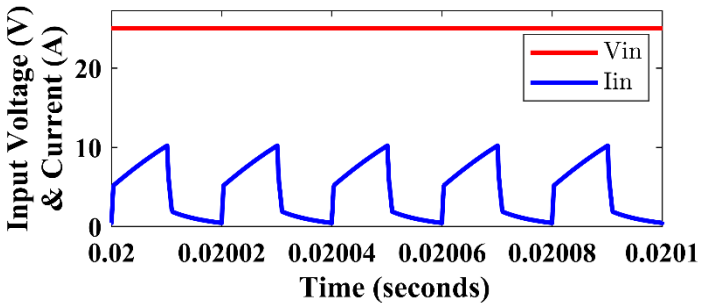

(i)

Figure 12. *Cont.*

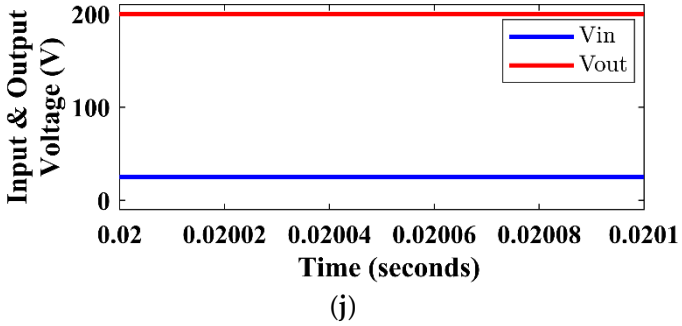

Figure 12. Simulation waveforms of the proposed converter under full load condition: (**a**) Vds vs. Vgs, (**b**) Vds vs. Ids, (**c**) Vds vs. VDc, (**d**) ID1 vs. IDc, (**e**) VD1 vs. VD2, (**f**) VD2 vs. VD3, (**g**) ID2 vs. ID3, (**h**) VC vs. VCox vs. VCoy, (**i**) Vin vs. Iin, (**j**) Vin vs. Vout.

5.2. Hardware Results

As per earlier discussions, and specification, a 100 W, 200 V/0.5 A, an experimental prototype of the proposed converter is fabricated, and tested in the laboratory environment to validate the performance experimentally. The duty cycle of the switch is kept at 0.5 to get the required output voltage at $T = 2$, and $V_{in} = 20$ V. Table 3 shows various components of the proposed converter and its specifications. Figure 13 depicts the experimental prototype.

Table 3. Components and its specifications of the proposed converter.

S. No.	Component	Type/Range	Quantity
1	MOSFET, S	IRFB4410, 100 V, 96 A, 8 mΩ	1
2	Diode, D_1, D_2, D_3, and D_c	MUR820, 200 V, 8 A	4
3	Capacitors, C_{ox} and C_{oy}	22 µF, 250 V, Electrolytic type	2
4	Capacitor, C	10 µF, 250 V, Electrolytic type	1
5	Coupled inductor	L_m = 200 µH, L_{lk} = 2 µH T = 2, EI33 core	1
6	Clamp resistor, R_c	3.3 kΩ	1
7	Clamp Capacitance, C_c	6nF, 100 V	1
8	MOSFET driver	TLP250	1

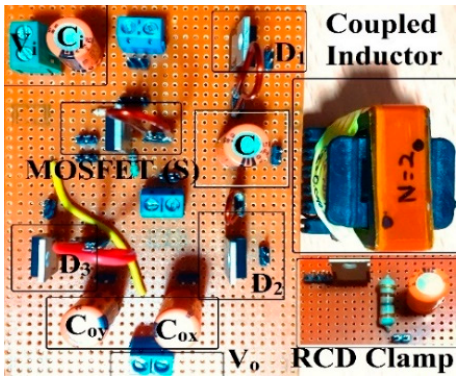

Figure 13. Experimental prototype of the proposed converter.

Figure 14 illustrates the experimental waveforms under full load conditions. The waveforms for gate-source voltage (V_{gs}) and the voltage stress of the MOSFET switch is illustrated in Figure 14a. The gate-source voltage is produced using the MSP430FR2355 Texas Instruments development board, and this PWM pulse is isolated and MOSFET driven with the help of TLP250 MOSFET/IGBT gate driver IC. The voltage sensor, LV-55-P, senses the output voltage of the proposed dc-dc converter,

and this feedback is processed through MATLAB/Simulink for effective closed-loop operation of the converter. By assuming a 1% output ripple voltage, the capacitance of the output capacitors V_{Cox} and V_{Coy} are selected. From Figure 14a, it is noticed that the voltage stress of the MOSFET switch is about 60 V and the leakage energy of the coupled inductor is effectively clamped using the passive RCD clamp circuit. Figure 14b shows the waveform of the voltage stress and current stress of the MOSFET switch. The current stress of the MOSFET switch is observed as 4.56 A and voltage stress is observed as 60 V, which almost satisfies the theoretical values. Besides, it is also noticed that the MOSFET switch is operated at zero-voltage switching condition, which minimizes the switching losses of the MOSFET. The waveform of the voltage across the clamp diode is depicted in Figure 14c. From Figure 14c, it is observed that the clamp diode effectively clamps the leakage energy during Mode-2 of the converter operation and the voltage stress of the clamp diode is similar to the voltage stress of the MOSFET switch. The waveforms for the current stress of the clamp diode, $i_{Dc,}$ and the current stress of the diode, D_1 is depicted in Figure 14d. It is noticed that the clamp diode clamps the leakage energy of the coupled inductor during Mode-2 and the current stress of the clamp diode is observed as 0.75 A. Similarly, the current stress of the diode, D_1 is observed as 1.05 A. The voltage stress of the various diodes is depicted in Figure 14e,f. As per the earlier discussions, the maximum voltage stress of the diodes such as V_{D1}, V_{D2}, and V_{D3} is equal to 150 V, 100 V, and 100 V, respectively. The same can be noticed from Figure 14e,f, and the voltage stress is somewhat deviated from the actual due to the parasitic elements of the diodes. The current stress of the diodes, such as i_{D2} and $i_{D3,}$ is illustrated in Figure 14g. By using Equations (30) and (31), the average current stress of the diodes such as i_{D2}, and i_{D3} are equal to 1 A, and 1 A, respectively, and the same can be noticed from Figure 14g. The maximum voltage across the capacitors such as V_C, V_{Cox}, and V_{Coy} is equal to 100 V, 150 V, and 50 V, respectively. From Figure 14h, it is observed that the voltage across the capacitors is equal to 98 V, 146 V, and 51 V, respectively, and this deviation is due to the parasitic elements of the capacitors. The input source current, $i_{i,}$ and the input source voltage are illustrated in Figure 14i, and from Figure 14i, it is observed that the source current is continuous throughout the operating period of the converter when the converter is operated at CCM operation, which proves the theoretical discussion. The waveforms of the input source, V_{in}, and the output voltage, V_{out} of the proposed converter is illustrated in Figure 14j. The input source voltage is kept constant at 25 V, and the output voltage of the converter is observed as 199 V from Figure 14j. It is also noted that as per the electrical specifications, the proposed converter can deliver the required voltage gain of 8 at the duty cycle of 50%.

It is noticed from various waveforms that the proposed converter is employed with the passive RCD clamp circuit in the primary of the coupled inductor to reduce the leakage inductance effect and to prevent the MOSFET switch from the voltage spikes/oscillations. To highlight the usage of the clamp circuit, the waveform for the voltage stress of the MOSFET switch with and without the clamp circuit is illustrated in Figure 15. It is observed from Figure 15 that the maximum magnitude of the switch voltage spike is greater than 100 V, and is lesser than the output voltage of the converter without the RCD clamp circuit.

At the same time, the maximum magnitude of the switch voltage spike is less than 60 V and is lower than the output voltage of the converter with the RCD clamp circuit. It is concluded that the passive RCD circuit effectively clamps the voltage spikes and helps to maintain less voltage stress of the MOSFET switch.

From the above discussions and various waveforms, it is concluded that the proposed converter is performing as per the theoretical analysis and the simulation results, and the performance of the proposed converter is better than the converter presented in the literature. The power losses in the proposed converter are analyzed by neglecting the switching losses since the MOSFET switch operates at the zero-voltage-switching condition. Moreover, the diode reverse-recovery losses are omitted due to the consideration of the coupled inductor leakage inductance. Thus, the overall losses of the proposed converter include conduction losses and the coupled inductor losses. The power loss distribution of the proposed converter is presented in Table 4.

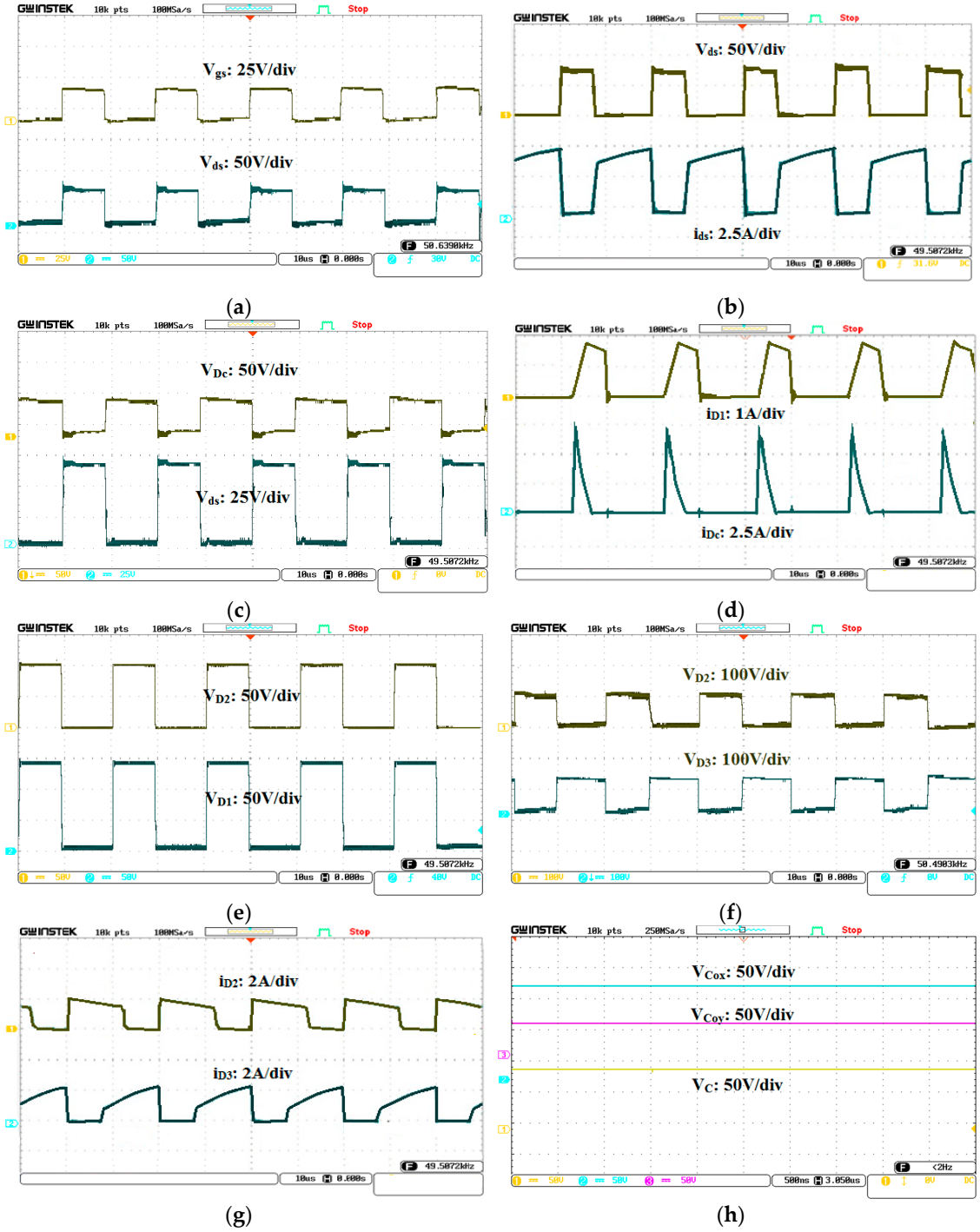

Figure 14. *Cont.*

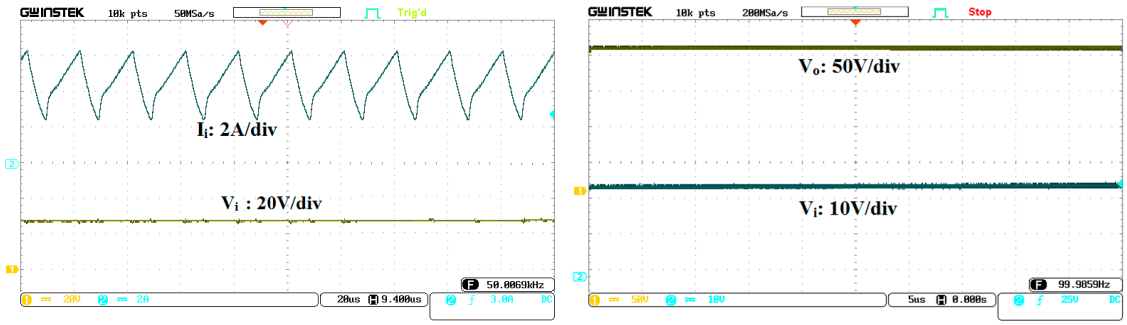

Figure 14. Various experimental waveforms of the proposed converter at full load. (**a**) V_{ds} vs. V_{gs}, (**b**) V_{ds} vs. I_{ds}, (**c**) V_{ds} vs. V_{Dc}, (**d**) I_{D1} vs. I_{Dc}, (**e**) V_{D1} vs. V_{D2}, (**f**) V_{D2} vs. V_{D3}, (**g**) I_{D2} vs. I_{D3}, (**h**) V_C vs. V_{Cox} vs. V_{Coy}, (**i**) V_{in} vs. I_{in}, (**j**) V_{in} vs. V_{out}.

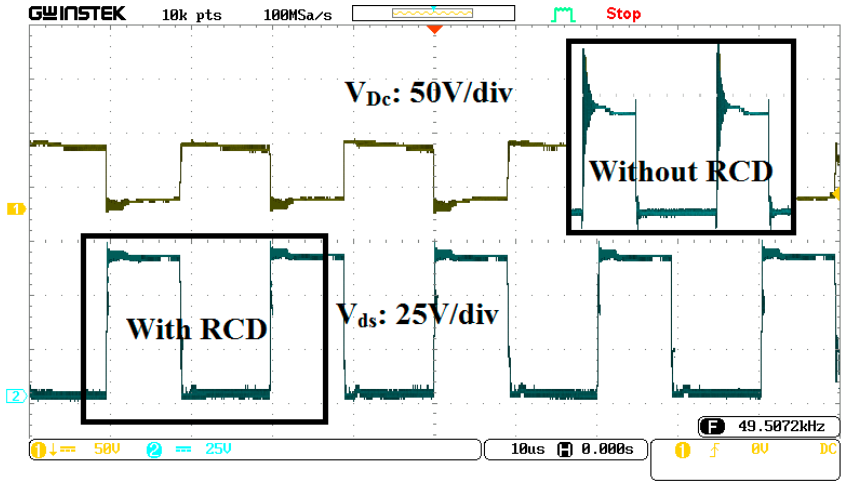

Figure 15. Voltage stress of the MOSFET switch with and without RCD clamp circuit.

Table 4. Power loss distribution of the proposed converter.

Components	$r_{ds\text{-}on}$/ESR (Ω)	Forward Voltage Drop (V)	RMS Current (A)		Average Current (A)		Power Loss (W)	
			Theoretical	Practical	Theoretical	Practical	Theoretical	Practical
S	0.008	-	4.58	4.76	-	-	0.1678	0.1812
D_1	0.02	0.975	1.1	1.05	1	0.96	0.999	0.9581
D_2	0.02	0.975	1.1	1.07	1	0.98	0.999	0.9783
D_3	0.02	0.975	1.1	1.13	1	1.06	0.999	1.0550
D_c	0.02	0.975	0.9	0.75	0.6	0.67	0.585	0.6532
C	0.005	-	1.85	2.15	-	-	0.0171	0.0231
C_{ox}	0.005	-	0.32	0.35	-	-	0.0051	0.0061
C_{oy}	0.005	-	0.17	0.15	-	-	0.0014	0.0011
R_c	3300	15	0.005	0.005	-	-	0.075	0.075
C_c	0.005	-	2.23	2.62	-	-	0.0241	0.034
L_1	0.051	-	4.85	5.25	-	-	1.1996	1.4056
L_2	0.096	-	0.92	1.05	-	-	0.0812	0.1058
Core Loss	-	-	-		-	-	0	1.28
			Total loss				5.1533	6.5753
			Full load conversion efficiency in %				95.10	93.83

The performance characteristics of the proposed converter are shown in Figure 16. It is observed that the maximum efficiency of the proposed converter is 95.1% and the full load efficiency of the converter is 93.83%.

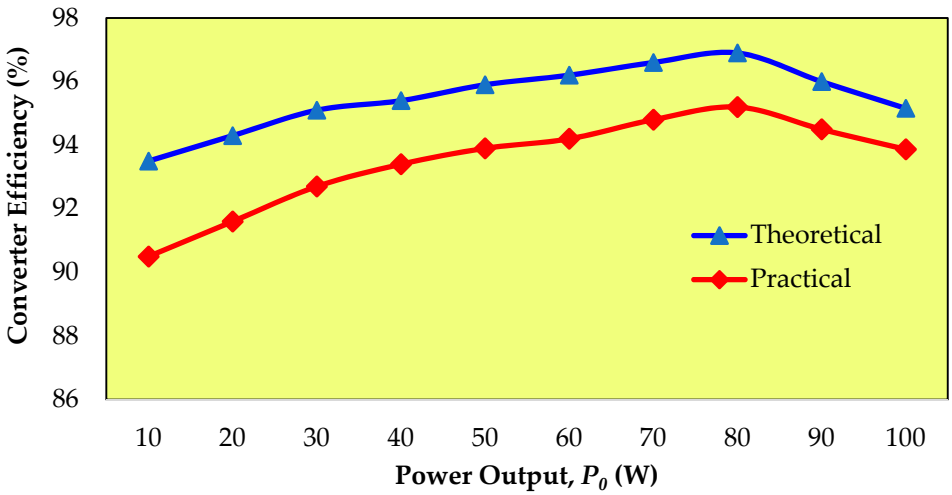

Figure 16. Performance evaluation of the proposed converter.

The various experimental values of the proposed converter are compared with the simulation values and the theoretical values, and the same has been presented in Table 5. The result proves that experimental values are nearly equal to theoretical and simulated values. From Table 5, it is observed a few variations in the voltage stress of the switch and diodes, and this is due to the parasitic components such as parasitic inductance, on-state resistance, and parasitic capacitance.

Table 5. Comparison details of the simulation and experimental results.

Analysis Type	V_{ds} (V)	I_{ds} (A)	V_{D1} (V)	V_{D2} (V)	V_{D3} (V)	V_C (V)	V_{Cox} (V)	V_{Coy} (V)	V_{out} (V)
Theoretical	50	4	150	100	100	100	150	50	200
Simulation	50	4.12	150	100	100	100	150	50	200
Experiment	60	4.56	147	102.5	104.5	98	146	51	197

The cost analysis of the proposed converter is listed in Table 6 for two different power ratings, such as 100 W and 1 kW [44]. It is clearly observed from Table 6 that the cost of the proposed converter reduces when the rating of the converter increases. The cost of the proposed converter is also compared with the other similar converters proposed in the literature and is presented in Table 7. From Table 7, it is noticed that the proposed converter holds a better cost position with respect to a high voltage gain capability along with an excellent conversion efficiency. The conversion efficiency of the proposed converter may be improved by proper design of the coupled inductor since the power losses supplied by the coupled inductor is more than 40% of the total power losses. Besides, the efficiency also increased by replacing the passive clamp circuit by the active clamp circuit if the rating is more than 500 W. However, for a low power application (say, <500 W), the proposed converter with RCD clamp circuit holds a better position in terms of cost, whereas, for the rating above 500 W, it is suggested to go with the active clamp circuit to have better conversion efficiency. The extension of the proposed converter with the active clamp circuit is also presented in Figure 17 for the researchers as a future extension and the same has been derived from [45]. However, the operation of the converter is similar to the previous discussions.

Table 6. Cost details of the proposed converter.

Component	Quantity	Type for 100 W	Cost in USD *	Type for 1 kW	Cost in USD *
Switch	1	IRFB4410	2.19	IXFB110N60P3	17.38
Diodes, D_1, D_2, D_3, D_c	4	MUR820	5.56	VS-15EWX06FN-M3	8.76
Capacitor, C	1	10 µF, 250 V, Electrolytic	0.9	10 µF, 600 V, Electrolytic	8.63
Capacitors, C_{ox} and C_{oy}	2	22 µF, 250 V, Electrolytic	2.08	22 µF, 250 V, Electrolytic	16.56
Clamp capacitor, C_c	1	6 nF, 25 V	0.69	6 nF, 250 V	3.62
Clamp resistor, R_c	1	3.3 kΩ, 10W	0.77	3.3 kΩ, 25 W	2.54
Coupled inductor	1	T = 2, EI33 Ferrite core (with winding)	5.02	T = 2, EE55 Ferrite core (with winding)	20.45
Driver circuit	1	TLP 250	2.02	TLP 250	2.02
Overall cost			19.23		79.96

* [44] Source: https://www.mouser.com/Electronic-Components/.

Table 7. Cost comparison among various converters for 100 W experimental prototype.

Ref.	No. of Components					Cost in USD *
	CI	D	C	S	L	
Proposed	1	4	4	1	-	19.23
[1]	1	1	3	1	-	13.68
[12]	1	4	5	1	1	25.32
[13]	1	2	2	1	1	18.83
[23]	1	2	3	1	1	19.68
[24]	1	4	5	1	-	22.69
[40]	1	5	7	1	1	28.48
[41]	2	5	6	1	1	31.04
[42]	1	4	6	1	1	25.69
[43]	-	3	4	1	3	25.18

* By assuming the same type of component/rating for all the converters.

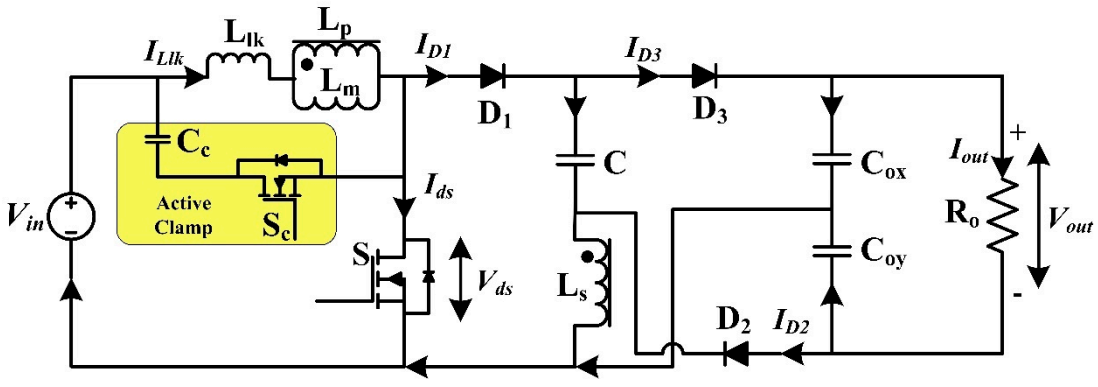

Figure 17. Proposed converter with active clamp circuit.

6. Conclusions

A new modified SEPIC dc-dc boost converter topology is proposed and discussed in this paper. The operation of the proposed converter is theoretically analyzed in both CCM and DCM modes. The proposed converter has advantages such as less voltage stress of the switch, and diodes, less output voltage ripple, and high conversion efficiency. The expressions for the static voltage gain, voltage and current stresses of various components are derived. In addition, the expression for the output

voltage with non-idealities and design guidelines are given sequentially. The conventional RCD clamp circuit has been used to reduce the voltage stress of the switch, and it helps to select the MOSFET with low $r_{ds\text{-}on}$, which reduces the conduction losses. Also, the loss due to device switching is diminished by the zero-voltage-switching technique. Therefore, the power loss of the proposed converter is less and hence increases the conversion efficiency. The proposed converter is compared with the similar converter topologies and concluded that the proposed converter has better voltage gain with less number of components. This feature enables the researcher to select the compact and high reliable converter for real-time applications. The maximum efficiency of the proposed converter is 95.2% at 80 W, and the full load efficiency is 93.83% at 100 W. Finally, it can be concluded that the proposed converter is best suitable for high voltage renewable energy systems.

Author Contributions: M.P. was originally responsible for conceptualization, methodology, simulation, experimentation and prepared the original draft of the article. U.S. verified the simulation data, experimental draft writing, and also provided technical guidance. H.H.A. and P.S. made a formal analysis of the technical write-up, review, editing, and supervision. All authors have read and agreed to the published version of the manuscript.

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