A New Efficient Step-Up Boost Converter with CLD Cell for Electric Vehicle and New Energy Systems

Muhammad Zeeshan Malik [1,*][ID]**, Haoyong Chen** [2,*]**, Muhammad Shahzad Nazir** [1][ID]**, Irfan Ahmad Khan** [3][ID]**, Ahmed N. Abdalla** [4]**, Amjad Ali** [5][ID] **and Wan Chen** [1]

1   Faculty of Automation, Huaiyin Institute of Technology, Huai'an 223003, China;
     msn_bhutta88@yahoo.com (M.S.N.); calvinchenw1979@163.com (W.C.)
2   Department of Electrical Engineering, South China University of Technology Guangzhou,
     Guangdong 510641, China
3   Marine Engineering Technology Department in a Joint Appointment with the Electrical and Computer
     Engineering Department, Texas A&M University, Galveston, TX 77554, USA; irfankhan@tamu.edu
4   Faculty of Electronic Information Engineering, Huaiyin Institute of Technology, Huai'an 223003, China;
     dramaidecn@gmail.com
5   Center of Research Excellence in Renewable Energy, King Fahad University of Petroleum and Minerals,
     Dhahran 31261, Saudi Arabia; amjad.ali@kfupm.edu.sa
*   Correspondence: malik4one@yahoo.com (M.Z.M.); eehychen@scut.edu.cn (H.C.); Tel.: +86-131-1525-6515 (M.Z.M.)

Abstract: An increase in demand for renewable energy resources, energy storage technologies, and electric vehicles requires high-power level DC-DC converters. The DC-DC converter that is suitable for high-power conversion applications (i.e., resonant, full-bridge or the dual-active bridge) requires magnetic transformer coupling between input and output stage. However, transformer design in these converters remains a challenging problem, with several non-linear scaling issues that need to be simultaneously optimized to reduce losses and maintain acceptable performance. In this paper, a new transformer-less high step-up boost converter with a charge pump capacitorand capacitor-inductor-diode CLD cell is proposed using dynamic modeling. The experimental and simulation results of the proposed converter are carried out in a laboratory and through Matlab Simulink, where 10 V is given as an input voltage, and at the output, 100 V achieved in the proposed converter. A comparative analysis of the proposed converter has also been done with a conventional quadratic converter that has similar parameters. The results suggest that the proposed converter can obtain high voltage gain without operating at the maximum duty cycle and is more efficient than the conventional converter.

Keywords: dynamic modeling; DC-DC converter; electric vehicle (EV); charge pump capacitor

1. Introduction

In recent years, due to the shortage of fossil fuels, research on renewable energy sources such as photovoltaic PV, wind, and fuel cells (FC), has gained immense popularity [1,2]. The intermittency associated with PV systems and low voltages at load end and electric vehicle (EV) or hybrid electric vehicle (HEV) charging needs a boost converter as depicted in Figures 1 and 2 [3–5]. Generally, EVs are powered by fuel cell stacks, supercapacitors, and battery systems. Thus, there is a need to step up the voltages [6–8].

A review of related literature depicts that various boost converters have been presented to overcome high voltage gain at the output. The traditional boost converters are preferred for their simple structure and low cost; however, they usually produce high input current ripples. For high voltage gain, this converter needs to work at a high duty ratio cycle, which causes switching problems [9–13].

The traditional solution to implement a DC-DC converter, with a high voltage transformation ratio, typically involves a magnetic transformer with a high turn's ratio, Due to the high cost of magnetic transformer components, several transformer-less topologies have been proposed that can achieve a high step-up ratio e at lower cost and size. The most common transformer-coupled topologies are derived from isolated versions of the basic converter types, i.e., buck, boost, buck-boost, cúk, single-ended primary-inductor converter (SEPIC) [14,15]. The forward converter is based on the buck topology; the flyback converter is based on the buck-boost topology; Full-bridge as well as Half-bridge converters can be both buck and boost derived. Moreover, converter types can be classified based on transformer core utilization [16]. Forward and flyback topologies have a net DC current in the transformer winding, which means the flux in the core must be reset at the end of each switching cycle. Full bridge, half-bridge and push-pull topologies provide bidirectional excitation to the transformer core; the net current in the winding is AC. This means that the flux in the core is reset automatically at the end of each switching cycle. The concept of using switching capacitor (SC) is obtained from [17] in which switching converters with wide DC conversion range are discussed by including a hybrid cell that multiplies current or voltage, as described in [18–20]. The high-frequency rectifier stage can be passive (half-wave, center-tapped half wave, full wave) or active, with switching devices. Some designs eliminate the high-frequency transformer and replace it with a parallel capacitor [21]. The shortcomings of wide frequency operation are EMI issues [22,23], higher switching loss at low power levels, difficulty in the design of magnetic components and the circulating currents independent of power level. Furthermore, phase-controlled converters operate at fixed frequencies and adjust power flow by varying phase shifts between the switching legs of a full-bridge inverter [24–26]. Similarly, modular DC–DC converters with input- and output-side series/parallel configurations are typically used for conditions where power processing exceeds the capacity of any single converter. However, these converters have control-related issues that do not provide balanced power-share between the constituent converter modules for different load conditions. Quadratic converters are DC–DC converters with a voltage conversion ratio that has a quadratic dependence on-duty ratio [27,28]. They are synthesized by cascading two converters in series and then eliminating redundant switches and controllers [29,30].
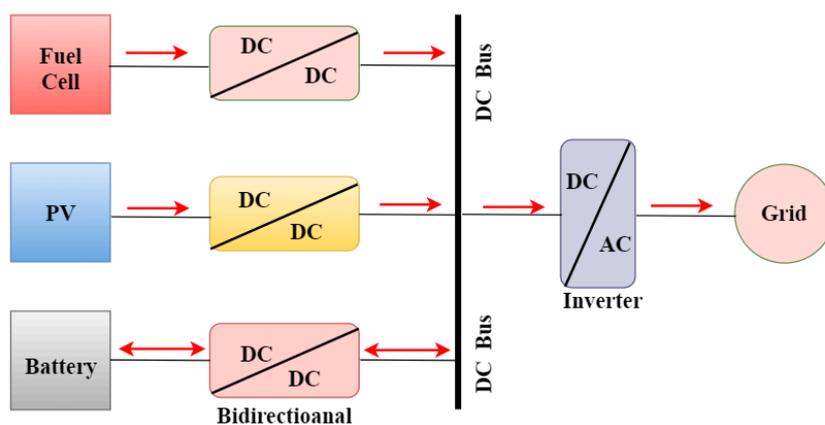

Figure 1. New energy technologies.

One of the main advantages of these converters is their higher voltage transformation ratio with a reduced number of components. However, the limitations of these converters arise from their cascaded nature. In addition, their combined efficiency is lower than the individual converter stages; and the voltage stresses on the boost diode and switch of the final stage are equal to the output voltage. Such problems can be solved by adding a switch to form a three-level boost converter [31]. Many other structures can also be integrated with quadratic converters like a capacitor-diode combination of the voltage multiplier or single/three-phase transformer windings [32]. There are different variations of boost converters, for instance, the quadratic boost zeta converter, quadratic tapped-boost converter

ZVS/ZCS quadratic converters, and quadratic converters based on non-cascading structures [33,34]. (SC) converters are a class of DC–DC converters, where the power stage consists of a network of only capacitors and switches. The capacitors are charged and discharged in sequence via input voltage to achieve the required voltage conversion ratio at the output [35]. The most significant advantage of SC converter is the absence of inductive storage devices. This makes the topology appropriate for monolithic integration and high-power density as both switches and capacitors can be fabricated on the same substrate using standard semiconductor manufacturing processes. One of its major shortcomings, which has been observed, is that the process of charge transfer results in impulse currents due to capacitors acting as charge pumps, which can lead to an increase in device stress and EMI issues. Another drawback is that at a fixed voltage transformation ratio, the efficiency of the converter drops quickly as the conversion ratio moves away from the designed operating mode. Furthermore, an additional limitation is that the voltage stress across all active switches is not equal [36].
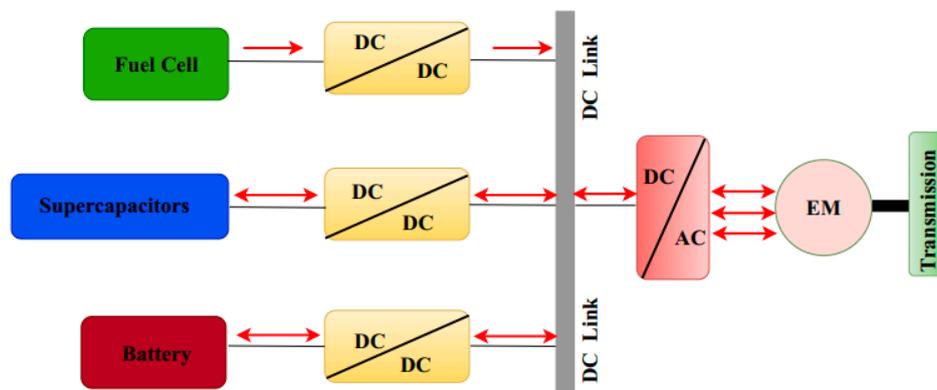

Figure 2. Block diagrams of the electric vehicle.

2. Related Work

The Cockroft–Walton (CW) circuit or voltage multiplier-based hybrid DC–DC Converters were introduced in 1932. This circuit operates as a voltage multiplier, which is fed by a pulsating low voltage waveform to generate a high voltage DC on its output terminal. Its main application is to generate high voltage DC required for insulation testing generators and particle accelerators. As the multiplication ratio increases, the CW circuit suffers from poor load regulation resulting in a significant voltage drop at its output terminal. For this reason, the CW circuit needs another converter to provide output voltage regulation. In [18,19], an isolated hybrid DC–DC converter composed of series-resonant and a CW circuit is proposed for a medical-use high-voltage X-ray power generator. In [37], a classical transformer-less multilevel boost converter with a hybrid connection of CW is introduced. Both converters in [37,38] can provide a considerable DC voltage step-up ratio at high efficiency. However, these circuits cannot be used for high-power applications as they share a similar high current-spike problem, which results from charging and discharging capacitors connected in parallel. This boost circuit is necessary to provide a pulsating input voltage waveform for the CW circuit and to produce output voltage regulation through use of Pulse Width Modulation (PWM). The presence of this boost circuit is inappropriate for high-power applications. Moreover, voltage multiplier hybrid DC–DC converters cannot achieve DC voltage step-down operation.

In this article, a new modified boost converter with a charge–pump capacitor and CLD cell is proposed (see Figure 3). The proposed converter can achieve very high voltage gain at the output without intensive duty ratio, and with lower switching stress across the switch. As the proposed converter consists of a charge pump capacitor which can control input current ripples, CLD cell can support high voltage gain at the output. Figure 3 represents the block diagram of proposed converter where V_s is an input voltage, the four capacitors are V_{c1}, V_{c2}, V_{c3}, and V_{c0}, S indicates metal–oxide–semiconductor field-effect transistor (MOSFET) switch three inductors are L_1, L_2, L_3

with same duty ratio. For proposed converter, the following assumptions have been made: (1) The proposed converter works with continuous conduction mode (CCM), (2) All components including input power are taken as ideal (no voltage drop and resistance),and (3) All the capacitors are large enough with constant voltages.
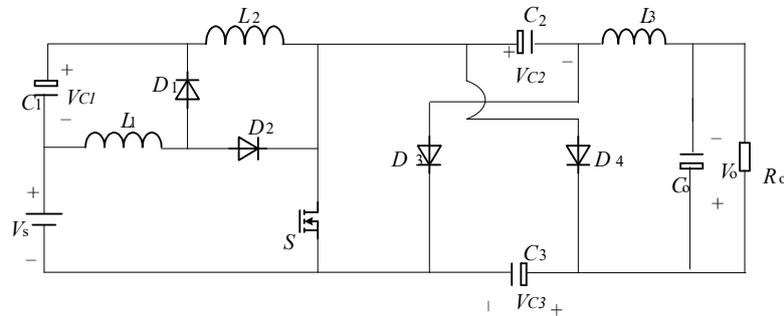

Figure 3. Diagram of the proposed converter.

3. Working Method of the Proposed Converter

The switching frequency of the proposed converter is fixed and has two switching states with one PWM signal. For one state ($t_0 − t_1$), MOSFET is switched ON; for other state ($t_1 − t_2$), MOSFET is switched OFF as illustrated in Figures 4 and 5. Furthermore, the characteristics of steady-state waveform, voltages, and currents of the proposed converter are shown in Figure 6.
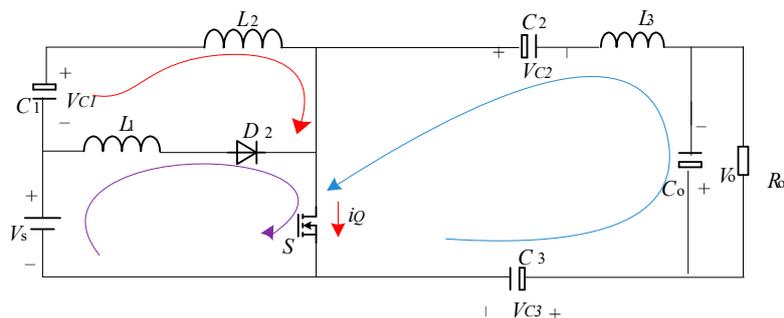

Figure 4. State-I.

3.1. MOSFET Switch ON State ($t_0 − t_1$)

In this state, when switch "S" is ON, diode D_2 will be forward biased while other diodes (D_1, D_3, and D_4) will work in reverse biased mode. This configuration of DC–DC converter is presented in Figure 4 with arrows indicating the direction of the current flow. The input voltage V_S/L_1 developed across inductor L_1, linearly increases the ($iL1$) inductor current and rise in $(V_S + V_{C1})/L_2$ across inductor L_2, increases the inductor current ($iL2$). In this state, capacitors C_2 and C_3 are in series, and the voltage output of these two capacitors is given as $V_{C2} + V_{C3} = 2V_{C2}$. And the inductor L_3 increases by $(2V_{C2} − V_0)/L_3$. The equation of this state is derived in Equations (1)–(5).

$$i_{L1} = i_{L1-t_0} + \frac{V_s}{L_1}t \tag{1}$$

$$\mathrm{u}i_{L2} = i_{L2-t_0} + \frac{V_s + V_{c1}}{L_2}t \tag{2}$$

$$i_{L3} = i_{L3-t_0} + \frac{2V_{c2} − V_0}{L_3}t \tag{3}$$

$$i_Q = i_{L1} + i_{L2} + i_{L3} \tag{4}$$

$$i_{in} = i_{L1} + i_{L2} \tag{5}$$

3.2. MOSFET Switch OFF State (t_1–t_2)

In this state, when semiconductor switch S is turned OFF, diode D_2 will be in reverse biased mode, as shown in Figure 5. As the voltage across the inductor L_1 becomes negative of V_{C1}/L_1, current changes its path from switch to diode D_1 and decreases linearly. At the same time, the voltage across inductor L_2 is $(V_S + V_{C1} - V_{C2})/L_2$, and inductor L_3 is $(V_{C2} - V_0)/L_3$, respectively. All the inductors current decreases linearly during this state. Equations for this state are (6)–(10) derived using Figure 5, as given below.

$$i_{L1} = i_{L1-t_1} - \frac{V_{c1}}{L_1}t \tag{6}$$

$$i_{L2} = i_{L2-t_1} - \frac{V_s + V_{c1} - V_{c2}}{L_2}t \tag{7}$$

$$i_{L3} = i_{L3-t_1} - \frac{V_{c2} - V_0}{L_3}t \tag{8}$$
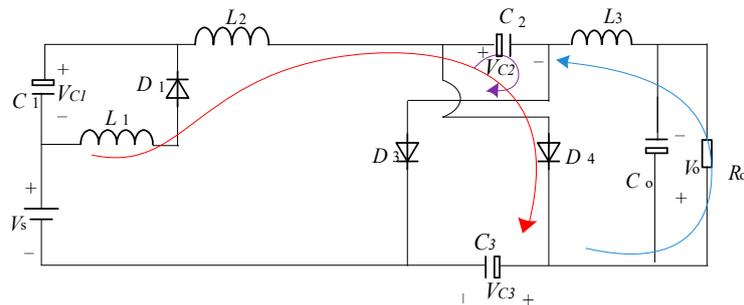
$$i_Q = 0 \tag{9}$$

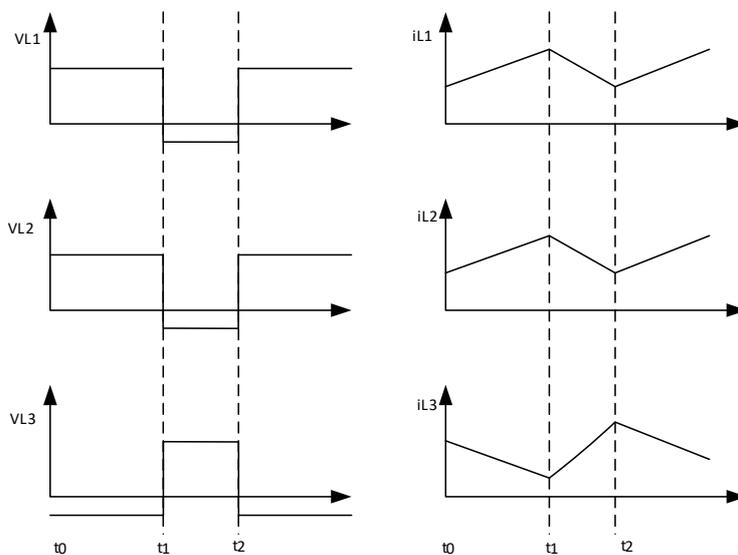$$i_{in} = i_{L2} \tag{10}$$

Figure 5. State-II.

Figure 6. Steady-state behavior.

4. Steady-State Analysis of the Proposed Converter

The steady-state analysis of the proposed converter is discussed below.

4.1. DC Conversion Ratio

The relationship between input and output voltage can be obtained through Equations (11)–(17) after applying inductor volt second balance (VSB) at inductor L_1, L_2, and L_3 for each state. Equations (11)–(13) describe state-I while Equations (14)–(16) refer to state-II.

$$V_{L1} = V_s \tag{11}$$

$$V_{L2} = V_s + V_{c1} \tag{12}$$

$$V_{L3} = 2V_{c2} - V_0 \tag{13}$$

$$V_{L1} = -V_{c1} \tag{14}$$

$$V_{L2} = V_s + V_{c1} - V_{c2} \tag{15}$$

$$V_{L3} = V_{c2} - V_0 \tag{16}$$

$$G = \frac{V_0}{V_s} = \frac{1+D}{(1-D)^2} \tag{17}$$

The voltage and current stress across semiconductor components are determined through Equations (18)–(25)

$$V_S = V_{c2} \tag{18}$$

$$V_{D1} = V_S + V_{c1} \tag{19}$$

$$V_{D2} = V_{c2} - V_S - V_{c1} \tag{20}$$

$$V_{D3,4} = V_{c2} \tag{21}$$

$$i_{D1,2} = \frac{V_s}{(1-D)^5 R_L} \tag{22}$$

$$i_{D3} = \frac{V_s}{(1-D)^2 R_L} \tag{23}$$

$$i_{D4} = \frac{V_s}{(1-D)^4 R_L} \tag{24}$$

$$i_Q = \frac{V_s}{(D)R_L} \tag{25}$$

4.2. Dynamic Modeling of the Proposed Converter

In this section, we assume that inductor current AC ripples and capacitor voltage ripples are monomers [39]. Figure 7 is derived from Figure 4 where,

V_s: input voltage,

$i_{L1,2,3}$: current across the inductor

$V_{c1,2,3,4}$: voltage across the capacitor.

When the switch "S" is ON, current across the diode $D_1 = i_{L1}$ and current across the switch $S = i_{L1} + i_{L2} + i_{L3}$. During this stage, diode $D_{1,2,3}$ are reversed biased, and the voltage across these diodes is equal to (V_s+V_{c1}), (V_{c2}), (V_{c3}), as shown in Figure 2.
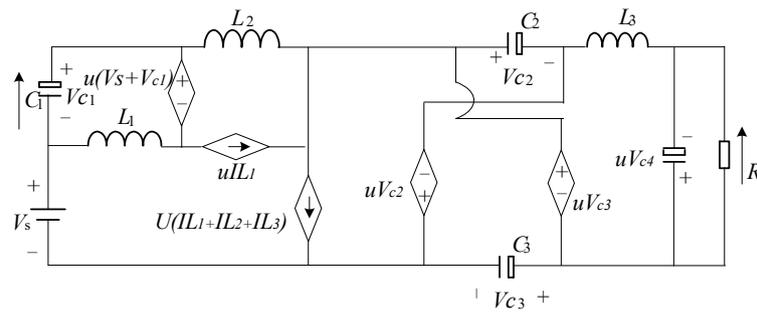
Figure 7. Average equivalent circuit of the proposed converter.

Figure 7 shows the equivalent circuit of the proposed converter where diode D_2 and switch are replaced by a current source, and diode D_1, D_3, and D_4 are replaced by the voltage source. In the equivalent circuit, after applying circuit theory, the equation derived is (26),

$$
\begin{bmatrix} \dot{i}_{L1} \\ \dot{i}_{L2} \\ \dot{i}_{L3} \\ \dot{V}_{c1} \\ \dot{V}_{c2} \\ \dot{V}_{c3} \\ \dot{V}_{c4} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & -(1-u)/L_1 & 0 & 0 & 0 \\ 0 & 0 & L_3/L_2 & 1/L_2 & -1/L_2 & -1/L_2 & -1/L_2 \\ 0 & 0 & L_2/L_3 & 0 & -1/L_3 & 1/L_3 & 1/L_3 \\ 1-u/C_1 & -1/C_1 & 1/C_1 & 0 & 0 & 0 & 0 \\ 0 & 1/C_2 & -1/C_2 & 0 & 0 & 0 & 0 \\ 0 & 1/C_3 & -1/C_3 & 0 & 0 & 0 & 0 \\ 0 & 1/C_4 & -1/C_4 & 0 & 0 & 0 & -1/R_L C_4 \end{bmatrix} \begin{bmatrix} i_{L1} \\ i_{L2} \\ i_{L3} \\ V_{c1} \\ V_{c2} \\ V_{c3} \\ V_{c4} \end{bmatrix}
$$

$$
+ \begin{bmatrix} \frac{u}{L_1} \\ \frac{1}{L_2} \\ -\frac{1}{L_3} \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} [e(t)] \tag{26}
$$

Without considering losses, the above equation can be written as,

$$
\dot{x}(t) = A(u)x(t) + B(u)e(t) \tag{27}
$$

where $e(t)$ is the input vector, $x(t) = [i_{L1}, i_{L2}, i_{L3}, V_{c1}, V_{c2}, V_{c3}, V_{c4}]^T R^7$ is the average value of state vector, $A(u)$ is a matrix in $R^{7 \times 7}$ and $B(u)$ is a vector in R^7; $V_s \in R$ = input voltage; R_L is the resistive load and u is a function of switch S with e binary value [0, 1]. Subsequently, [0] demonstrates that the switch is OFF, whereas [1] indicates that the switch is ON. Equation (27) is based on non-linear, whereas matrix $A(u)$, $B(u)$ is dependent on the control signal of $u(t) \in R$. The behavior of the proposed converter obtained after the linearization process results in small perturbations around an operating point. Therefore, the nominal steady-state operating condition of the proposed converter can be written by setting (27) as $AX + BE = 0$ and and is shown in Equations (28)–(34),

The voltage across the capacitors are given in Equations (28)–(31),

$$
V_{c1} = \frac{D}{1-D} Vs \tag{28}
$$

$$
V_{c2} = \frac{1}{(1-D)^2} Vs \tag{29}
$$

$$
V_{c3} = \frac{1}{(1-D)^2} Vs \tag{30}
$$

$$V_{c4} = \frac{1+D}{(1-D)^2} Vs \tag{31}$$

Current across the inductor is given in Equations (32)–(34),

$$i_{L1} = \frac{V_s}{(1-D)^5 R_L} \tag{32}$$

$$i_{L2} = \frac{V_s}{(1-D)^4 R_L} \tag{33}$$

$$i_{L3} = \frac{V_s}{(1-D)^2 R_L} \tag{34}$$

where D is the duty cycle of the switch S,

$$e(t) = E + \widetilde{e} \tag{35}$$

$$u(t) = U + \widetilde{u} \tag{36}$$

where $\tilde{u}$ is the small-signal perturbations of the nominal dusty cycle D, and $\widetilde{e}$ is the nominal input voltage V_s. Thus, the relationship between voltage and duty cycle above is given as (35)–(36), Where, $\widetilde{e} << E$ and $\widetilde{u} << D$, which can also be written as (37)–(38),

$$X(t) = X + \widetilde{x} \tag{37}$$

$$V_0(t) = V_0 + \widetilde{v}_0 \tag{38}$$

After substituting Equations (28)–(34) and (35)–(36) into Equation (26), the linear mode can be derived by assuming fewer perturbations, and avoiding non-linear terms as mentioned in Equation (39),

$$
\begin{bmatrix} \widetilde{\dot{i}_{L1}} \\ \widetilde{\dot{i}_{L2}} \\ \widetilde{\dot{i}_{L3}} \\ \widetilde{\dot{V}_{c1}} \\ \widetilde{\dot{V}_{c2}} \\ \widetilde{\dot{V}_{c3}} \\ \widetilde{\dot{V}_{c4}} \end{bmatrix}
=
\begin{bmatrix}
0 & 0 & 0 & -\frac{1-u}{L_1} & 0 & 0 & 0 \\
0 & 0 & \frac{L_3}{L_2} & \frac{1}{L_2} & -\frac{1}{L_2} & -\frac{1}{L_2} & -\frac{1}{L_2} \\
0 & 0 & \frac{L_2}{L_3} & 0 & -\frac{1}{L_3} & \frac{1}{L_3} & \frac{1}{L_3} \\
1-\frac{u}{C_1} & -\frac{1}{C_1} & \frac{1}{C_1} & 0 & 0 & 0 & 0 \\
0 & \frac{1}{C_2} & -\frac{1}{C_2} & 0 & 0 & 0 & 0 \\
0 & \frac{1}{C_3} & -\frac{1}{C_3} & 0 & 0 & 0 & 0 \\
0 & \frac{1}{C_4} & -\frac{1}{C_4} & 0 & 0 & 0 & -\frac{1}{R_L C_4}
\end{bmatrix}
\begin{bmatrix} \widetilde{i_{L1}} \\ \widetilde{i_{L2}} \\ \widetilde{i_{L3}} \\ \widetilde{V_{c1}} \\ \widetilde{V_{c2}} \\ \widetilde{V_{c3}} \\ \widetilde{V_{c4}} \end{bmatrix}
+
\begin{bmatrix}
\frac{D}{(1-D)L_1}Vs & \frac{u}{L_1} \\
\frac{1}{(1-D)^2 L_2}Vs & \frac{1}{L_2} \\
\frac{1}{(1-D)^2 L_2}Vs & -\frac{1}{L_3} \\
\frac{1+D}{(1-D)^2 L_3}Vs & 0 \\
\frac{V_s}{(1-D)^5 R_{Lc1}} & 0 \\
\frac{V_s}{(1-D)^4 R_{Lc2}} & 0 \\
\frac{V_s}{(1-D)^2 R_{Lc3}} &
\end{bmatrix}
\begin{bmatrix} \widetilde{u} \\ \widetilde{e} \end{bmatrix}
\tag{39}
$$

Furthermore, the above equation can be written as (40),

$$\dot{x}(t) = Ax(t) + Bv(t) \tag{40}$$

where, $x(t) \in R^7$ is the state vector, $A \in R^{7 \times 7}$ and B are the constant matrix in $R^{7 \times 2}$, R^2 is vector of input voltage and $V_{(t)} = \begin{bmatrix} \widetilde{u} & \widetilde{e} \end{bmatrix}$. When the perturbation input voltage is neglected $\widetilde{e} = 0$, matrix B is removed and small signal state-space model can be written as (41).

$$\begin{bmatrix} \widetilde{\dot{i}_{L1}} \\ \widetilde{\dot{i}_{L2}} \\ \widetilde{\dot{i}_{L3}} \\ \widetilde{\dot{V}_{c1}} \\ \widetilde{\dot{V}_{c2}} \\ \widetilde{\dot{V}_{c3}} \\ \widetilde{\dot{V}_{c4}} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & -(1-u)/L_1 & 0 & 0 & 0 \\ 0 & 0 & L_3/L_2 & 1/L_2 & -1/L_2 & -1/L_2 & -1/L_2 \\ 0 & 0 & L_2/L_3 & 0 & -1/L_3 & 1/L_3 & 1/L_3 \\ 1-u/C_1 & -1/C_1 & 1/C_1 & 0 & 0 & 0 & 0 \\ 0 & 1/C_2 & -1/C_2 & 0 & 0 & 0 & 0 \\ 0 & 1/C_3 & -1/C_3 & 0 & 0 & 0 & 0 \\ 0 & 1/C_4 & -1/C_4 & 0 & 0 & 0 & 1/R_L C_4 \end{bmatrix} \begin{bmatrix} \widetilde{i_{L1}} \\ \widetilde{i_{L2}} \\ \widetilde{i_{L3}} \\ \widetilde{V_{c1}} \\ \widetilde{V_{c2}} \\ \widetilde{V_{c3}} \\ \widetilde{V_{c4}} \end{bmatrix}$$

$$+ \begin{bmatrix} \frac{D}{(1-D)L_1}Vs \\ \frac{1}{(1-D)^2 L_2}Vs \\ \frac{1}{(1-D)^2 L_2}Vs \\ \frac{1+D}{(1-D)^2 L_3}Vs \\ \frac{V_s}{(1-D)^5 R_{Lc1}} \\ \frac{V_s}{(1-D)^4 R_{Lc2}} \\ \frac{V_s}{(1-D)^2 R_{Lc3}} \end{bmatrix} [\widetilde{u}] \qquad (41)$$

5. Simulation Results & Discussion

The simulation results of the proposed converter, which are performed in the Matlab Simulink environment, are shown in Figure 8. Figure 8a describes the switching signal of the MOSFET switch S; Figure 8b represents 10 V as an input voltage; in Figure 8c 100 V output voltages are obtained at the duty cycle of D = 0.6; and Figure 8d,e is the output voltage of capacitors C_1 and C_2, which are 62.50 V. In Figure 8f voltage stress across the switch S is 62.50 V. Thus, the output voltage of the proposed converter is higher than voltage stress. Furthermore, a comparison of results demonstrates that voltage gain of the conventional quadratic converter is significantly less than the proposed converter, whereas voltage stress across the switch is equal to output voltages [11]. Figure 8g–i shows the current across the inductor L_1, L_2, and L_3.
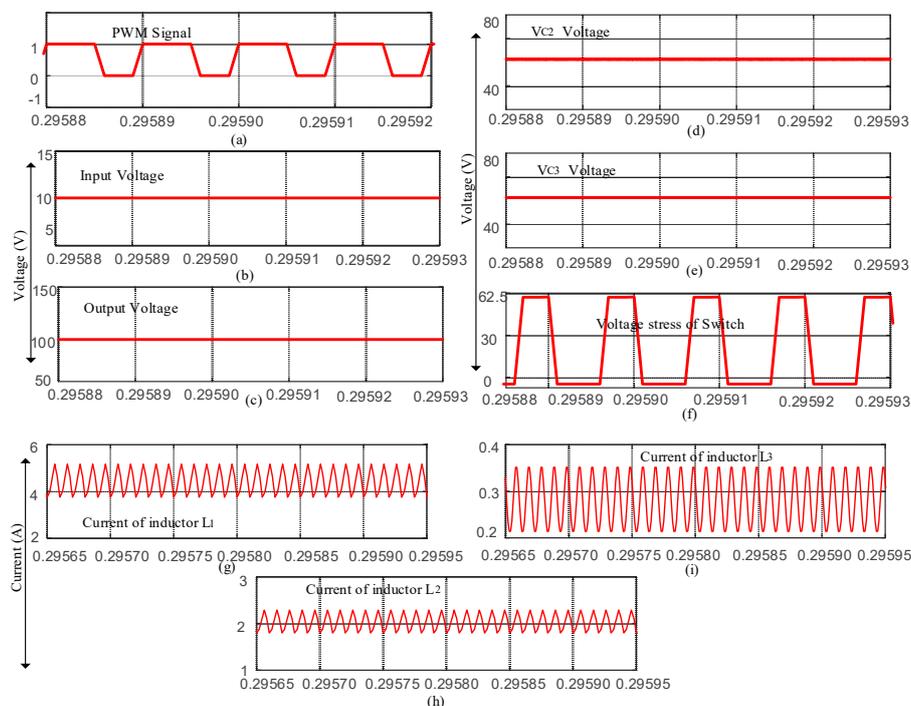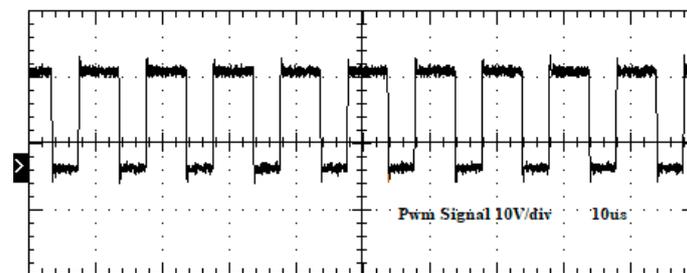

Figure 8. Simulation results of the proposed converter.

## 6. Experimental Results & Discussion

To validate results and effectiveness of the proposed converter, an experimental setup is prepared in the research laboratory with circuit parameters as given in Table 1. Experimental waveforms of the proposed converter are depicted in Figure 9 and a prototype of this converter is presented in Figure 10. The duty cycle of the proposed converter is assumed as D = 0.6. Figure 9a shows the switching signals of the proposed converter, and Figure 9b illustrates waveforms of input voltage, which is 10 V. Figure 9c shows that the output voltage of the proposed converter is 98 V, which is in accordance with voltage gain determined through Equation (17). The output voltage indicates that the proposed converter can achieve high gain without operating at a maximum duty cycle. The voltage conversion ratio of the proposed converter is ten times higher than the input voltage, which is quite high when compared to the traditional quadratic converter.
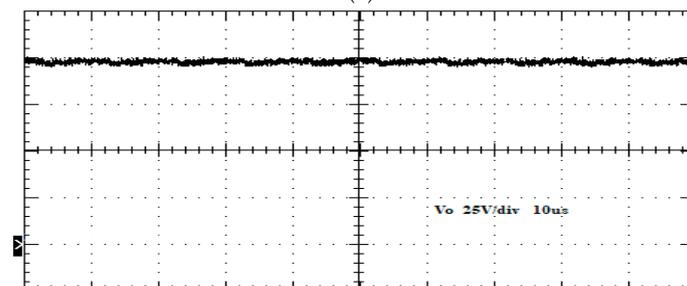
Table 1. Parameters for prototype.

Components	Symbol	Parameters
Output power	P_0	50 (W)
Input voltage	V_{in}	10 (V)
Output voltage	V_0	100 (V)
Load resistance	R	200 (Ω)
Frequency	F_S	100 (KHz)
Filter inductor	L_{1-3}	220 (μH)
Capacitor	C_{1-4}	440 (μF)
Diodes	D	MUR860
MOSFET Switch	S	IRFZ46N

(a)

(b)

(c)

Figure 9. *Cont.*
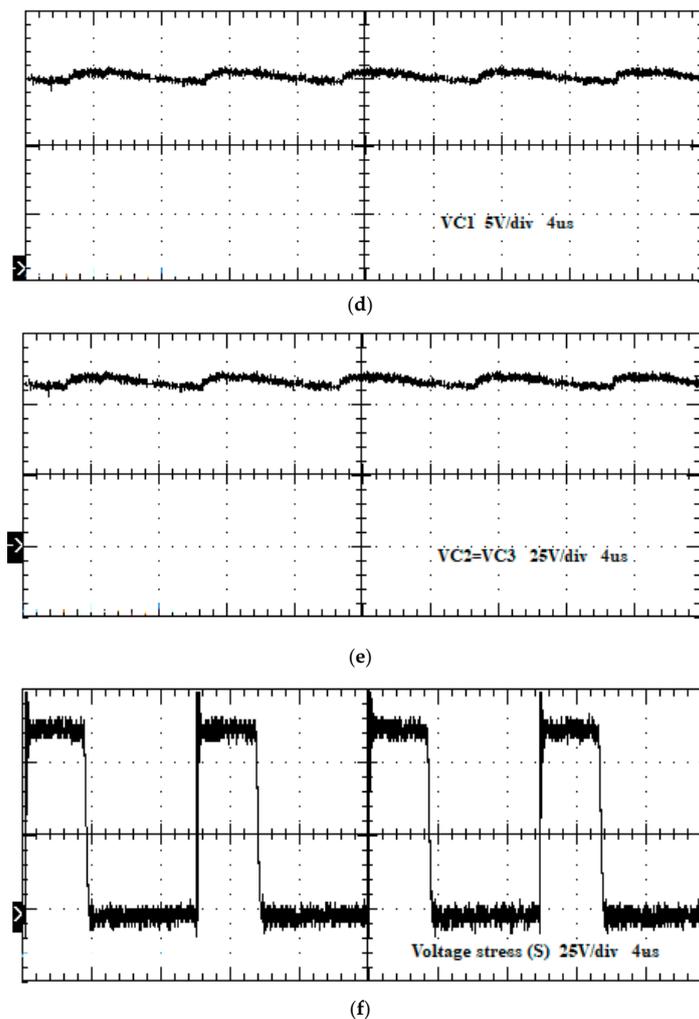
(d)

(e)

(f)
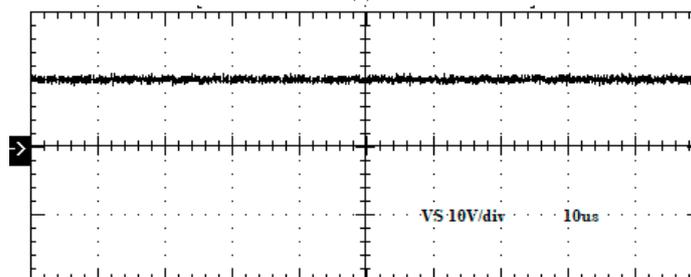
Figure 9. Experimental results of the proposed converter.
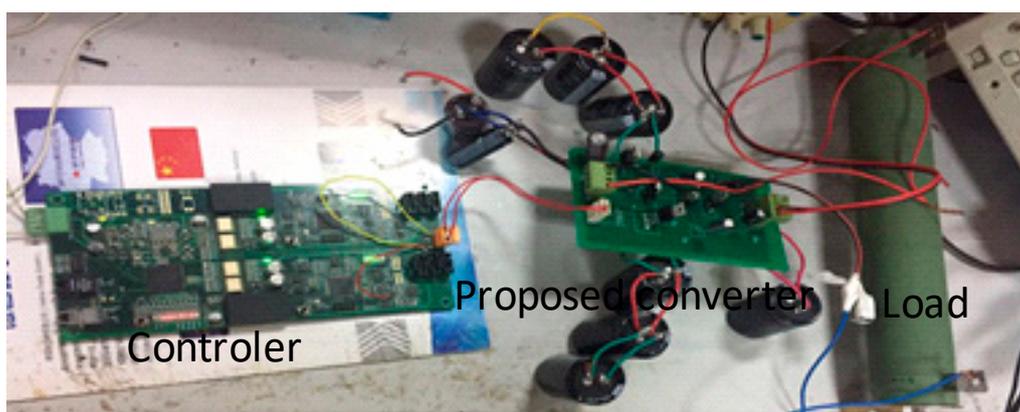

Figure 10. The prototype of the proposed converter.

In Figure 9d,e waveform of capacitor voltages V_{C1}, V_{C2}, and V_{C3} are shown, where the output voltage of capacitor V_{C1} is 15 V and of capacitor V_{C2} and V_{C3} is 61 V, that are in close proximity to capacitor Equations (28)–(31). Furthermore, Figure 9f shows the waveforms of switching stress across the MOSFETs switch S, where voltage stress across the switch is 62 V, which is less than the output voltage. The conventional quadratic converter has stress across the switch Vs-stress = V_0. From

experimental and theoretical analysis, it is proved that the proposed converter has many advantages over conventional quadratic converter.

In Figure 11, an efficiency graph of the proposed and conventional quadratic converter is given. The efficiency of both converters is calculated for different loads. It is observed that the maximum efficiency of the proposed converter is 95.91% and is achieved at an output power of 195 W. This is due to the fact that higher input voltages allow the converter to operate at higher output power. As maximum power is limited by thermal limit of the switches and lower current, it results in lower losses in switches, and attainment of minimum efficiency (86.74%) at an output power of 33 W. As compared to the conventional quadratic converter at the same load, maximum efficiency achieved by the proposed converter is 93.97%, and the minimum is 83.29%, which indicate that it has excellent efficiency at high voltage gain.
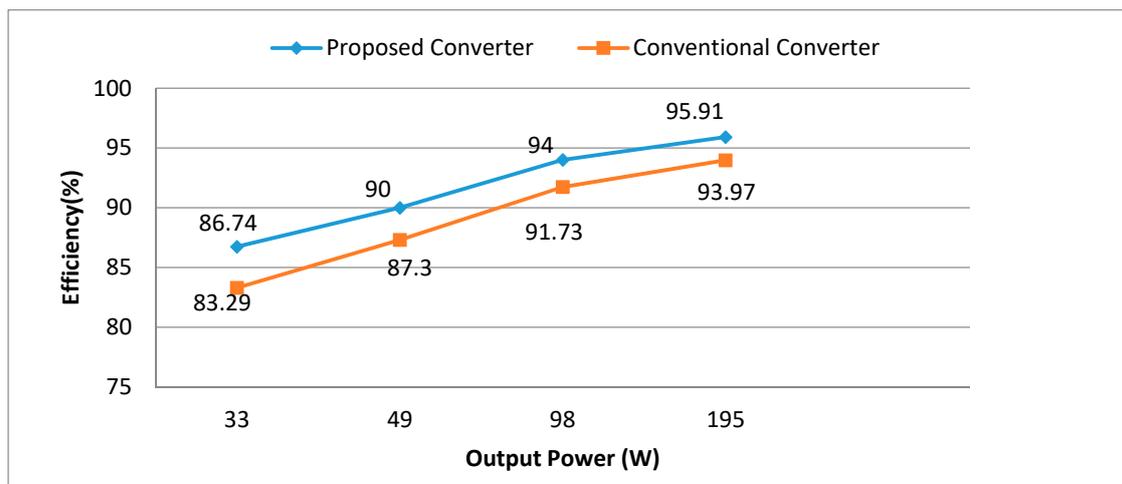

Figure 11. Efficiency graph.

7. Conclusions

In this paper, a DC–DC boost converter with charge pump–capacitor and CLD cell is introduced with its static and dynamic working principle. To investigate operational principles of the proposed converter, the simulation was performed in MATLAB/SIMULINK, and to validate the results, an experimental setup was developed in the laboratory. It is evident from results (Simulation and experimental) that the proposed converter holds certain advantages over traditional converters, such as efficient high voltage gain and low losses across the switch than the output voltage. The presented converter is suitable for converting low voltage to high voltage in various applications such as photovoltaic systems, where the wires from the PV modules are isolated from the earth, and there would not be a problem. If the input and output are (galvanically) separated and at different potentials. However, it may have some shortcomings for high voltage floating ground applications, for instance, where input source and output load share a common ground (some cases in automotive). In the floating ground system, it may have some safety concerns, because there is no low impedance path to ground. However, this type of grounding can facilitate in isolating a system from interference problems caused by ground loops.

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