

Perspective of Voltage-Fed Single-Phase Multilevel DC-AC Inverters

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Abstract: Standing out for their remarkable benefits, such as lower voltage stress on integrated semiconductor devices, reduction in total harmonic distortion, as well as lower electromagnetic effects, multilevel inverters (MLIs) increase their share in the field of energy supply. The multilevel inverter is an interesting research topic that realizes the generation of desired output voltage waveforms composed of small voltage steps. However, many studies have put a premium on the structure, efficiency, and output of the multilevel inverter, but there are relatively few studies on the THD and practical product applications. Consequently, in this brief perspective, some puzzles for MLIs are pointed out to explore new ideas as well as to present new questions.

Keywords: DC-AC inverter; multilevel; perspective; single-phase; voltage-fed

1. Introduction

Multilevel DC-AC inverters (MLIs) are able to set specific DC voltage levels directly to generate a desired AC voltage at the inverter's output terminals. Hence, MLIs are a preferable solution for AC power supplies, including interfacing photovoltaic energy systems [1], low-voltage wind energy systems [2], fuel cell energy conversion systems [3], chargers of fully electric vehicles [4], on-board in hybrid and fully electric vehicles [5] and off-board for electric buses [6], high-voltage renewable energy systems [7], as well as renewable energy conversion applications, such as reducing wind energy costs [8] and improving the efficiency [9] and reliability of photovoltaic energy systems [10] because their ability of low voltage stress, high efficiency, low common-mode voltage [11] provides high-quality output waveforms and improves the total harmonic distortion (THD) [12].

The basic operating principle of the multilevel DC-AC inverter is to utilize the switch path to make the output voltage stratified and to increase the number of voltage levels or filters to lead to the output voltage being sinusoidal-like. Since the output voltage of a multilevel DC-AC inverter is a stratified output voltage, the voltage stress on the switch can be clamped. Therefore, the high-voltage AC output can be constructed by low-voltage-withstanding components.

On the one hand, MLIs can be classified into two major categories, single-phase MLIs and three-phase MLIs. In general, three-phase MLIs have the advantage that all semiconductors are rated to the same voltage, despite the ratio of voltage levels over the number of power semiconductors being relatively low compared to low-power converters. Single-phase MLIs are also a wide research field in which a large number of voltage levels can be realized by sacrificing the voltage rating of semiconductors.

On the other hand, MLIs can be also classified into two categories for different applications, current-fed MLIs and voltage-fed MLIs. Since the voltage-fed MLI has low THD, it can be applied in many industrial applications, such as AC motors to reduce the torque ripple, low-frequency transformers to reduce the core loss, and utility parallel of green power with relatively low electric pollution.



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Voltage-fed single-phase MLIs can be mainly classified into three types, based on symmetrical structure and processing power, including neutral point clamp, the flywheel capacitor type, and series-connected-based type [13].

The neutral point clamp can be furthermore classified into active neutral point clamped (ANPC) and diode clamp. The active neutral point clamped is based on NPC, and can be classified by switched capacitors, T-type, F-type, K-type, and Class-D-type. Figure 1 shows the classification of the voltage-fed single-phase MLI.

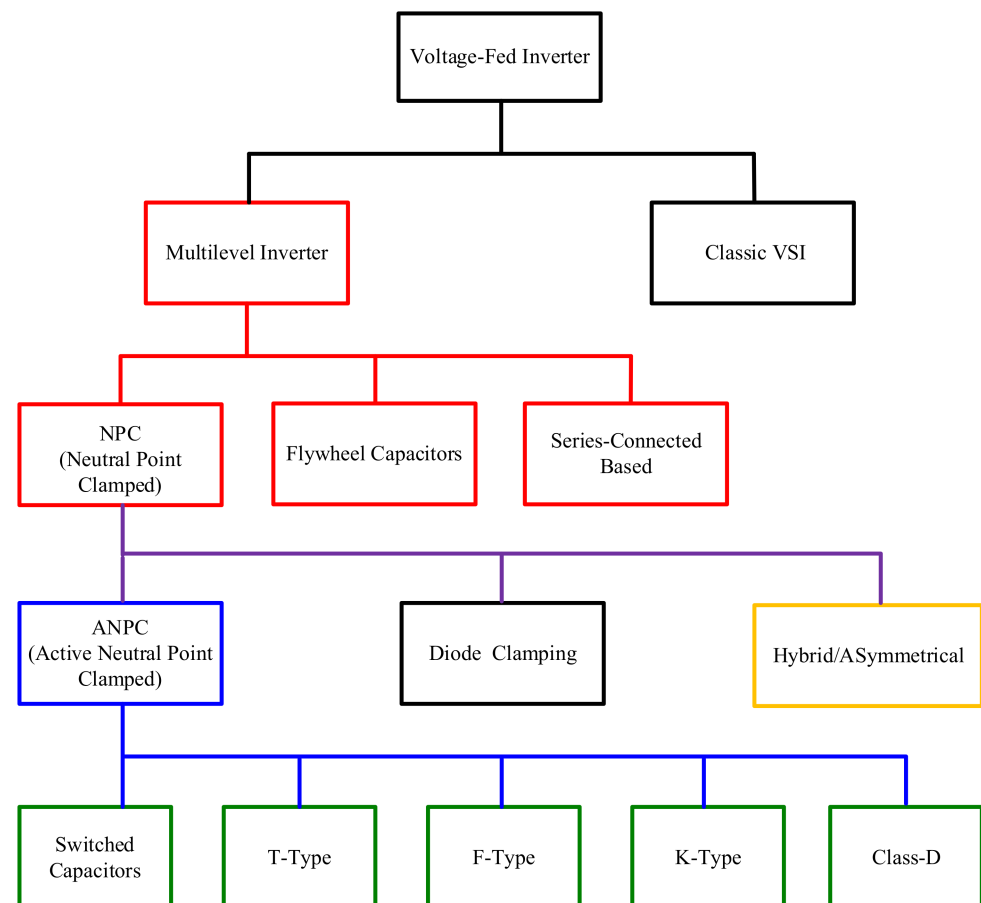


Figure 1. Voltage-fed DC-AC inverter classification.

2. Analysis of Basic Topologies of Systematic MLIs

In this section, we will analyze and explain the operation principles of three typical symmetrical structures of the five-level inverter: neutral point clamped, flywheel capacitors, and series-connected-based, as displayed in Figure 1.

2.1. Neutral Point Clamped Inverter

Figure 2 displays the five-level neutral point clamped (NPC) inverter circuit structure, which consists of eight switches $S_1, S_2, S_3, S_4, S_5, S_6, S_7$, and S_8 , six clamping diodes D_1, D_2, D_3, D_4, D_5 , and D_6 , four DC-link capacitors C_1, C_2, C_3 , and C_4 , and one output load resistor R_o , where V_{in} is the DC input voltage, V_o is the AC output voltage, and 'o' is the neutral point [14]. The operation of the inverter is described below. It is noted that each red line and arrow shows the current flow.

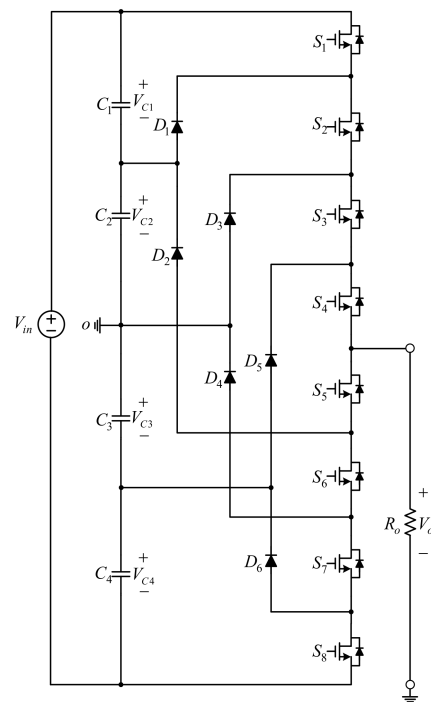


Figure 2. Circuit structure of a five-level neutral point clamped inverter.

Status I [$V_o = 0$]: As displayed in Figure 3, switches S_1, S_2, S_7 , and S_8 are cut off, while the switches S_3, S_4, S_5 , and S_6 are on, so the output voltage V_o is zero.

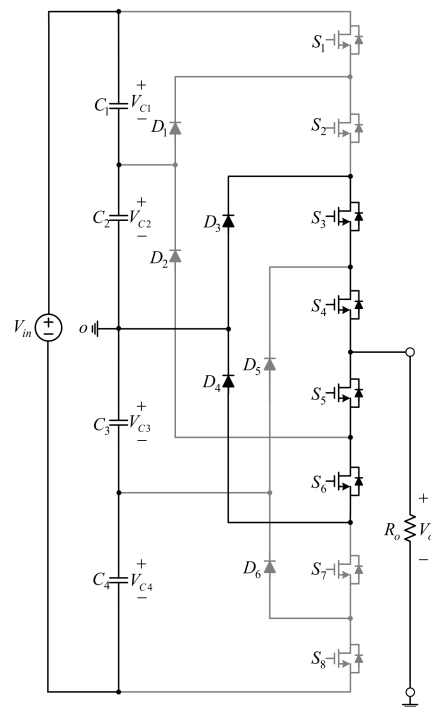
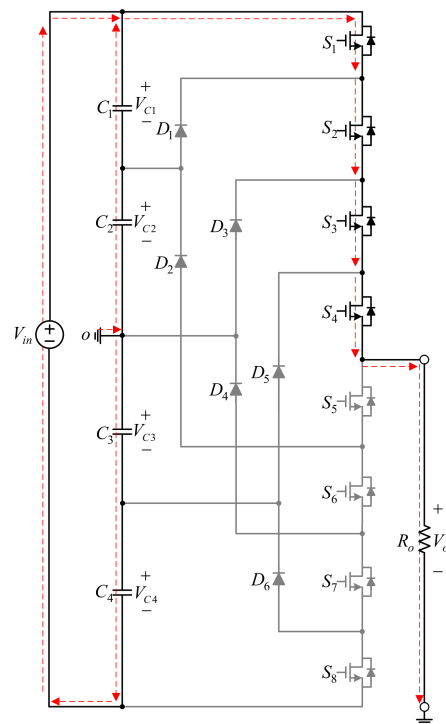
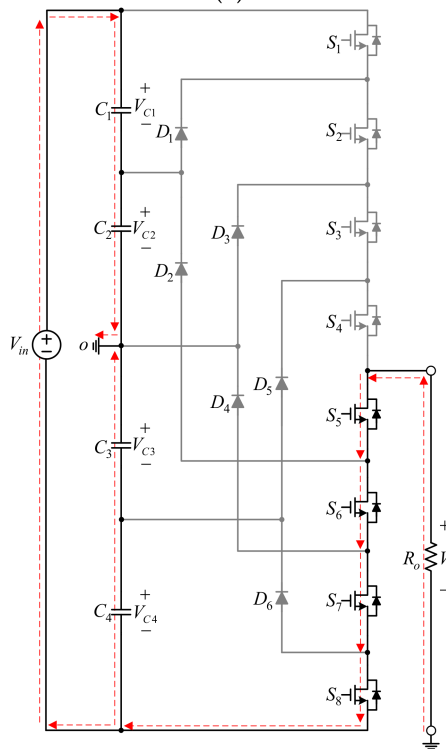


Figure 3. Zero voltage output of a five-level neutral point clamped inverter.

Status II [$V_o = 0.5 V_{in}$ or $-0.5 V_{in}$]: When the switches S_1, S_2, S_3 , and S_4 are on and S_5, S_6, S_7 , and S_8 are off, the circuit is displayed in Figure 4a, and the output voltage is $0.5 V_{in}$. When the switches S_5, S_6, S_7 , and S_8 are on and S_1, S_2, S_3 , and S_4 are off, the circuit is displayed in Figure 4b, and the output voltage is $-0.5 V_{in}$.



(a)



(b)

Figure 4. (a) Current flow direction of $0.5 V_{in}$ voltage output; (b) current flow direction of $-0.5 V_{in}$ voltage output.

Status III [$V_o = 0.25 V_{in}$ or $-0.25 V_{in}$]: When the switches S_2 , S_3 , S_4 , and S_5 are on and S_1 , S_6 , S_7 , and S_8 are off, the circuit is displayed in Figure 5a, and the output voltage

is $0.25 V_{in}$. When the switches S_4, S_5, S_6 , and S_7 are on and S_1, S_2, S_3 , and S_8 are off, the circuit is displayed in Figure 5b, and the output voltage is $-0.25 V_{in}$.

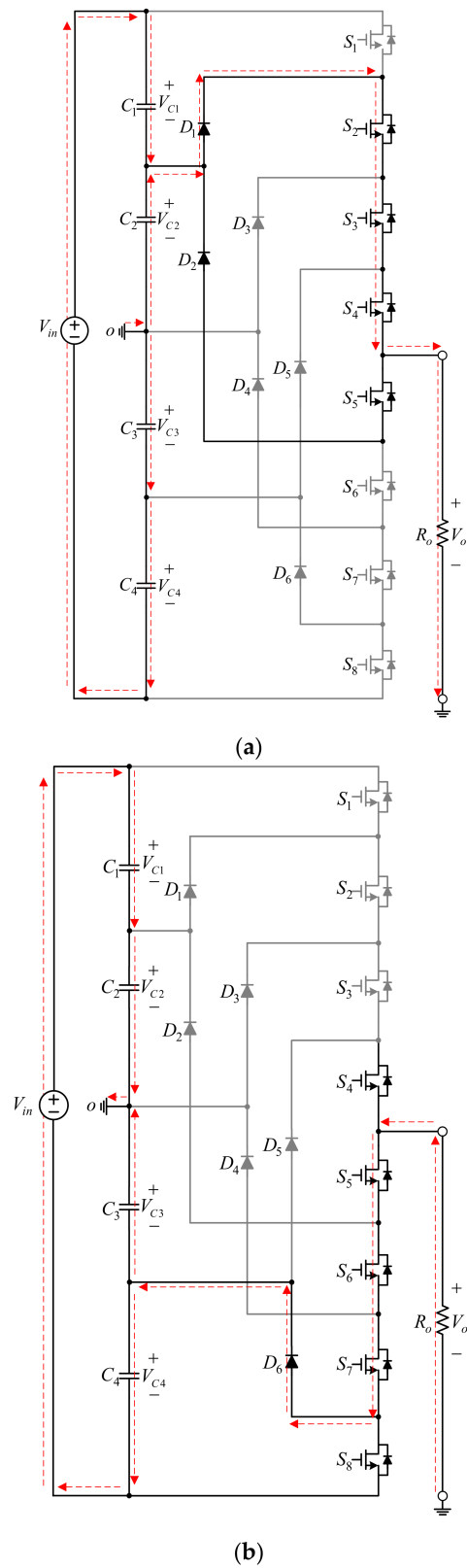


Figure 5. (a) Current flow direction of $0.25 V_{in}$ output voltage; (b) current flow direction of $-0.25 V_{in}$ voltage output.

For an m -level flywheel diode clamped inverter, the required number of components is displayed in Equations (1)–(3).

$$\text{Number of switches of an } m\text{-level flywheel diode clamped inverter: } 2(m - 1) \quad (1)$$

$$\text{Number of diodes of an } m\text{-level flywheel diode clamped inverter: } 2(m - 2) \quad (2)$$

$$\text{Number of capacitors of an } m\text{-level flywheel diode clamped inverter: } m - 1 \quad (3)$$

The NPC multilevel power inverter is used to generate the output terminal potential by clamping diodes to the neutral point [15]. However, when the number of voltage levels increases, more clamping diodes, semiconductor switches, and DC-link capacitors are required. As more clamping diodes are connected in series to block the higher voltage, more conduction losses are created, and reverse recovery currents are yielded, thereby increasing the switching losses.

2.2. Flywheel Capacitor Inverter

A flywheel capacitor inverter has a similar circuit structure to a diode clamping circuit, but the two structures and principles are different. The diode clamping inverter uses diode clamping voltage to achieve a hierarchical output voltage, while the flywheel capacitor inverter uses balanced capacitance to achieve a hierarchical output voltage.

Figure 6 shows the five-level flywheel capacitor inverter circuit structure which consists of eight switches $S_1, S_2, S_3, S_4, S_5, S_6, S_7$, and S_8 , ten DC-link capacitors $C_1, C_2, C_3, C_4, C_5, C_6, C_7, C_8, C_9$, and C_{10} , and one output load resistor R_o , where V_{in} is the DC input voltage, V_o is the AC output voltage, and 'o' is the neutral point of the DC input voltage [16]. The operation of the inverter is described below, where the voltage across all capacitors is $0.25 V_{in}$.

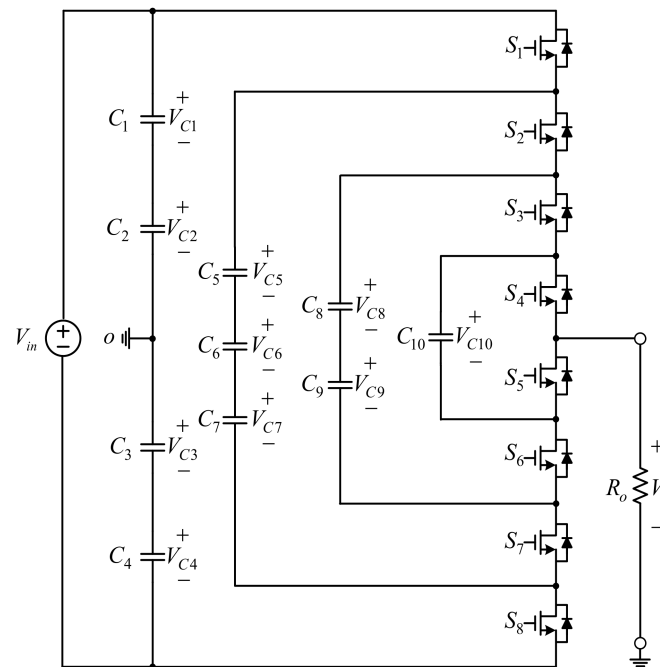


Figure 6. Circuit structure of a five-level flywheel capacitor inverter.

Status I [$V_o = 0$]: When the switches S_1, S_4, S_6 , and S_7 are on, and switches S_2, S_3, S_5 , and S_8 are off, the circuit is displayed in Figure 7a, and the output voltage is zero. When the switches S_2, S_3, S_5 , and S_8 are on and S_1, S_4, S_6 , and S_7 are off, the circuit is displayed in Figure 7b, and the output voltage is zero.

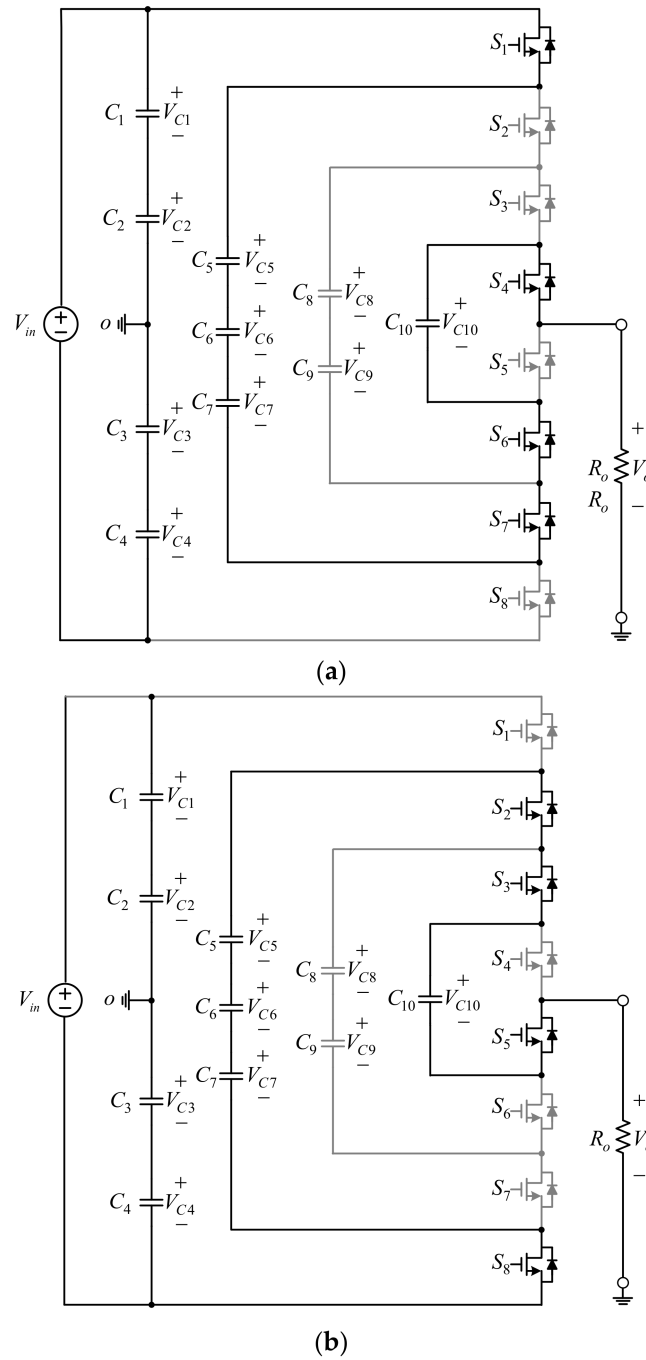


Figure 7. (a) one zero voltage output; (b) the other zero voltage output of a five-level flywheel capacitor inverter.

Status II [$V_o = 0.5 V_{in}$ or $-0.5 V_{in}$]: When the switches $S_1, S_2, S_3,$ and S_4 are on and the switches $S_5, S_6, S_7,$ and S_8 are off, the circuit is displayed in Figure 8a, and the output voltage is $0.5 V_{in}$. When the switches $S_5, S_6, S_7,$ and S_8 are on and the switches $S_1, S_2, S_3,$ and S_4 are off, the circuit is displayed in Figure 8b, and the output voltage V_o is $-0.5 V_{in}$.

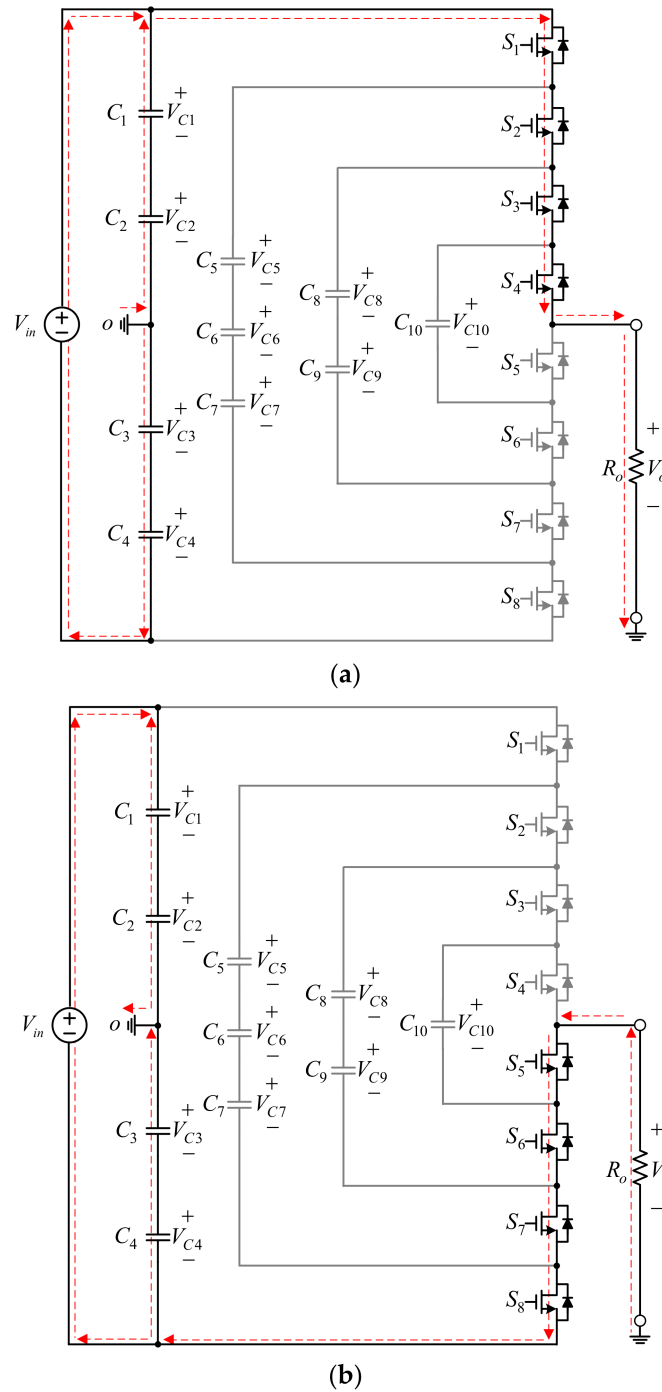


Figure 8. (a) Current flow direction of $0.5 V_{in}$ voltage output; (b) current flow direction of $-0.5 V_{in}$ voltage output.

Status III [$V_o = 0.25 V_{in}$ or $-0.25 V_{in}$]: When the switches S_1 , S_2 , S_4 , and S_6 are on and the switches S_3 , S_5 , S_7 , and S_8 are off, the circuit is displayed in Figure 9a, and the output voltage is $0.25 V_{in}$. When the switches S_3 , S_5 , S_7 , and S_8 are on and the switches S_1 , S_2 , S_4 , and S_6 are off, the circuit is displayed in Figure 9b, and the output voltage V_o is $-0.25 V_{in}$.

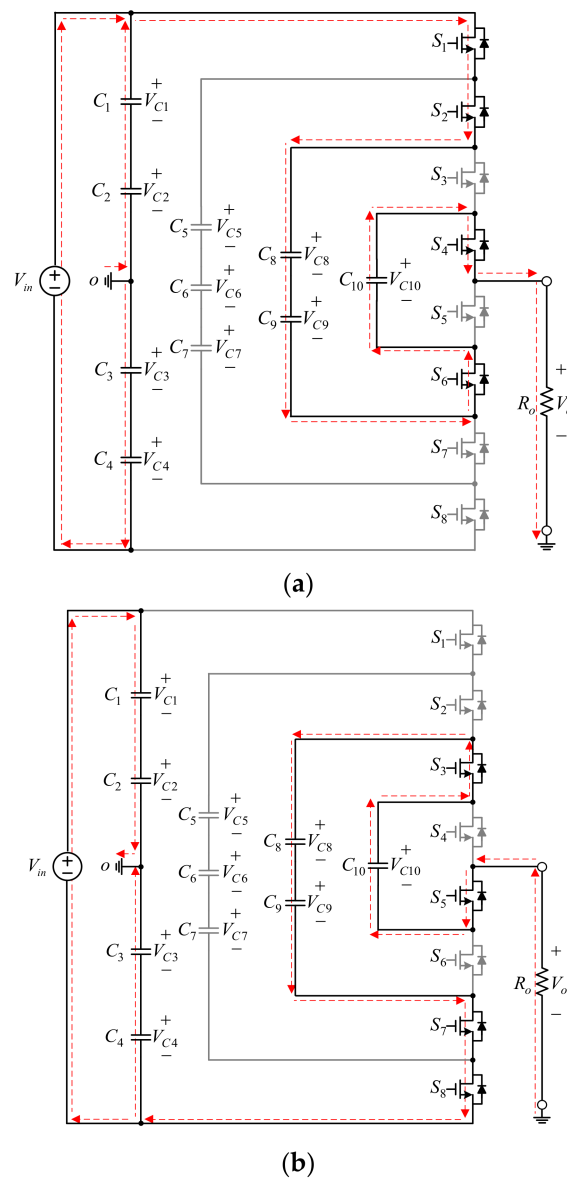


Figure 9. (a) Current flow direction of $0.25 V_{in}$ voltage output; (b) current flow direction of $-0.25 V_{in}$ voltage output.

For an m -level flywheel capacitor inverter, the required number of components is shown in Equations (4) and (5).

$$\text{Number of switches of an } m\text{-level flywheel capacitor inverter: } 2(m - 2) \quad (4)$$

$$\text{Number of capacitors of an } m\text{-level flywheel capacitor inverter: } 0.5m(m - 1) \quad (5)$$

The flywheel-capacitor-based multilevel DC-AC inverter is designed to realize the AC output voltage clamped by interconnecting multiple capacitors [17]. However, a large number of capacitors and complex control methods for capacitor voltage balancing are required to achieve a hierarchical output voltage.

2.3. Series-Connected-Based Inverter

A series-connected-based inverter is a circuit in which two or more identical H-bridge circuits are connected in series, and the number of series connections is adjusted according to the number of levels and output voltage required. Instead of using capacitors and diodes to clamp the output voltage, this type of circuit uses multiple power supplies to form the

step voltage and operates the switches in unipolar switching to realize the output step AC voltage. Therefore, the maximum value of the output sine wave voltage is equal to the sum of all power supply voltages.

Figure 10 shows the circuit structure of a five-level series-connected inverter circuit structure which consists of eight switches $S_1, S_2, S_3, S_4, S_5, S_6, S_7$, and S_8 to form an H-bridge circuit and one output load resistance R_o , where V_{in} is the DC input voltage, and V_o is the AC output voltage [18]. The operation of the inverter is described below.

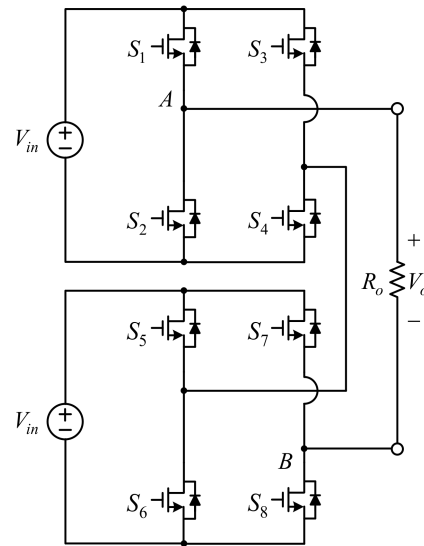


Figure 10. Circuit structure of a five-level series-connected inverter.

Status I [$V_o = 0$]: As displayed in Figure 11, all the switches are cut off in this state. Therefore, the output voltage V_o is zero, and there is no loop in the circuit.

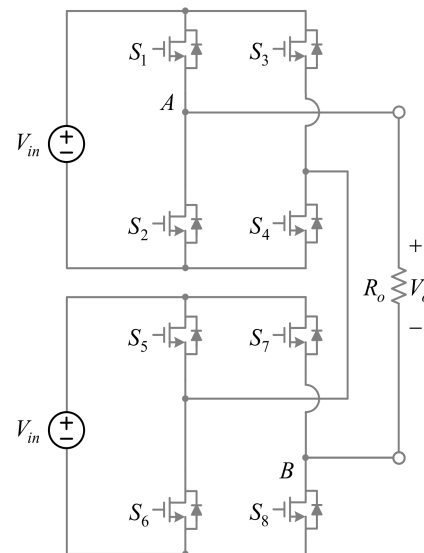


Figure 11. Zero voltage output of a five-level series-connected inverter.

Status II [$V_o = V_{in}$ or $-V_{in}$]: When the switches S_4, S_5 , and S_8 are on, and the switches S_1, S_2, S_3, S_7 , and S_6 are off, the circuit is displayed in Figure 12a, and the energy of V_{in} will be transferred to the load through S_4, S_5, S_8 and the body diode of S_2 , so the output voltage V_o is V_{in} . When the switches S_2, S_3 , and S_6 are on, and the switches S_1, S_4, S_5, S_7 , and S_8 are off, the circuit is displayed in Figure 12b, and the energy of the input voltage V_{in} will be transferred to the load through S_2, S_3, S_6 and the body diode of S_8 , so the output voltage V_o is $-V_{in}$.

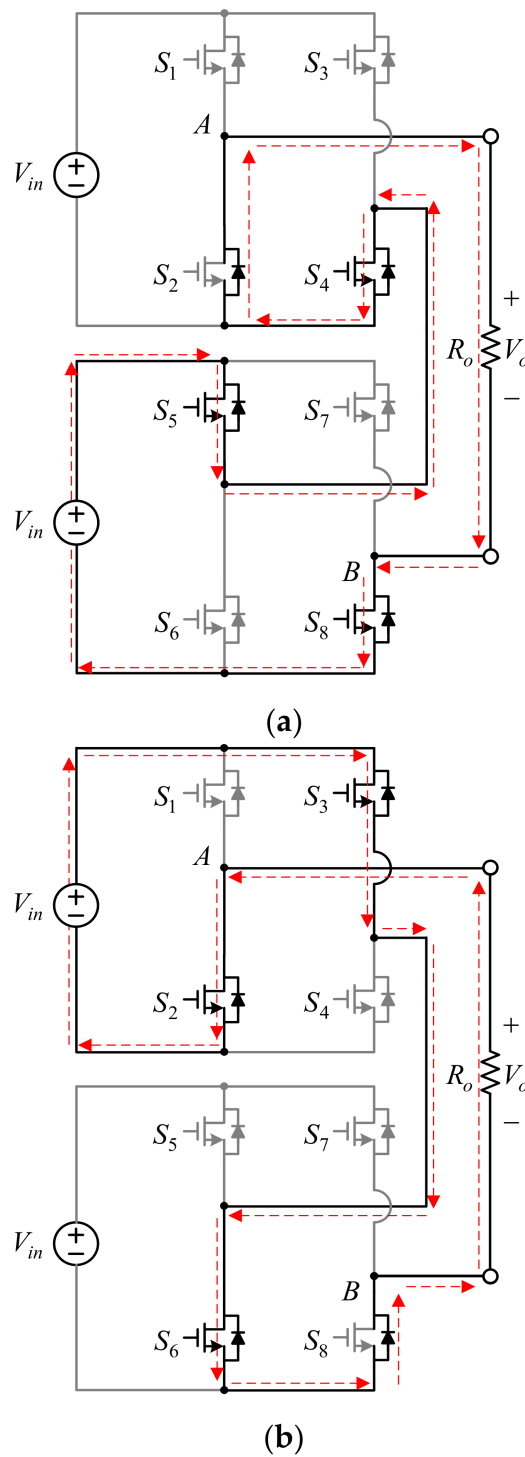


Figure 12. (a) Current flow direction of V_{in} voltage output; (b) Current flow direction of $-V_{in}$ voltage output.

Status III [$V_o = 2 V_{in}$ or $-2 V_{in}$]: When the switches S_1 , S_4 , S_5 , and S_8 are on, and the switches S_2 , S_3 , S_6 , and S_7 are off, the output voltage is $2 V_{in}$, and the circuit is displayed in Figure 13a. When the switches S_3 , S_5 , S_7 , and S_8 are on, and the switches S_1 , S_2 , S_4 , and S_6 are off, the output voltage is $-2 V_{in}$, and the circuit is displayed in Figure 13b.

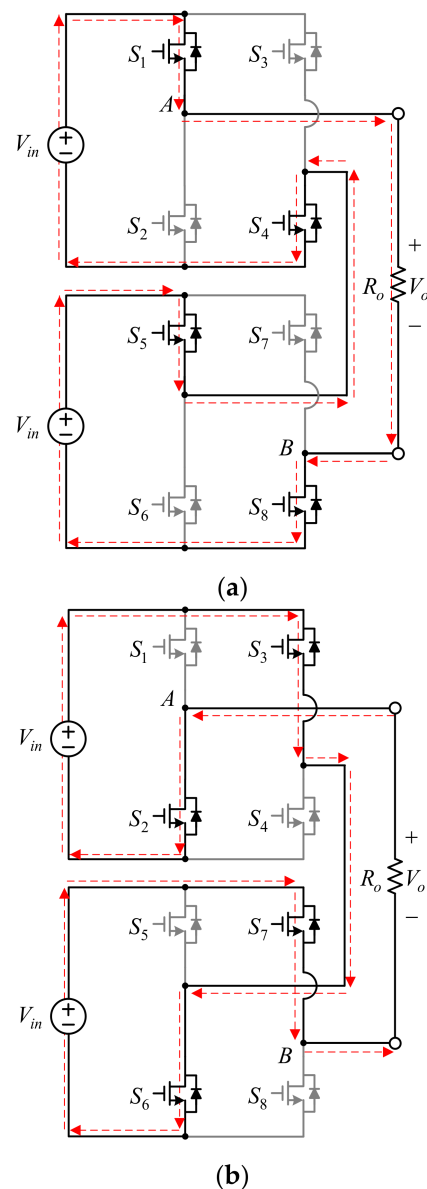


Figure 13. (a) Current flow direction of $2 V_{in}$ voltage output; (b) current flow direction of $-2 V_{in}$ voltage output.

For an m -level series-connected inverter, the number of components required is shown in Equations (6) and (7).

$$\text{Number of switches of an } m\text{-level series-connected inverter: } 2(m - 1) \quad (6)$$

$$\text{Number of power supplies of an } m\text{-level series-connected inverter: } 0.5(m - 1) \quad (7)$$

The series-connected-based multilevel DC-AC inverter is the only type having a modular design concept and adopts the fewest components among the three types [19]. However, the need for multiple independent power supplies to synthesize the required levels of the AC output voltage limits its applications.

Based on the above analysis, Table 1 displays the switching status of the systematic five-level MLIs and its corresponding output voltage.

Table 1. Switching status and output voltage of the systematic five-level MLIs (1: ON; 0: OFF).

Inverter Type	Level Voltage	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
Diode Clamped	$0.5 V_{in}$	1	1	1	1	0	0	0	0
	$0.25 V_{in}$	0	1	1	1	1	0	0	0
	$0 V_{in}$	0	0	1	1	1	1	0	0
	$-0.25 V_{in}$	0	0	0	1	1	1	1	0
	$-0.5 V_{in}$	0	0	0	0	1	1	1	1
Flywheel Capacitor	$0.5 V_{in}$	1	1	1	1	0	0	0	0
	$0.25 V_{in}$	1	1	0	1	0	1	0	0
	$0 V_{in}$	0	1	1	0	1	0	0	1
	$0 V_{in}$	1	0	0	1	0	1	1	0
	$-0.25 V_{in}$	0	0	1	0	1	0	1	1
	$-0.5 V_{in}$	0	0	0	0	1	1	1	1
Series-Connected	$2 V_{in}$	1	0	0	1	1	0	0	1
	V_{in}	0	0	0	1	1	0	0	1
	0	0	0	0	0	0	0	0	0
	$-V_{in}$	0	1	1	0	0	1	0	0
	$-2 V_{in}$	0	1	1	0	0	1	1	0

3. State of Recent Works

Recently, there have been many other existing papers presented for the voltage-fed single-phase MLIs [10,20–42] with a different number of levels, voltage gain, and circuit structure considered.

3.1. Series-Connected-Based MLIs

The traditional 3L FC inverter uses a PS-PWM control strategy, which is equivalent to the unipolar PWM control method, by simply adjusting the switches S_3 and S_4 . The literature [18] uses the above principle to simplify the complexity of the control strategy by using a PD-PWM plus unipolar.

In [20], a series-connected module approach is proposed to connect each module in series by means of transformer isolation. This approach eliminates the need to isolate the input power of each module from each other and allows the use of a single power source as the input source for each module. Practically, the transformer has a problem in leakage inductance and flux saturation.

In [21], a dual power series inverter module is proposed, using two power components to form a sub-multilevel inverter module, which is connected in series with the input power of the conventional series-connected inverter module, so that the inverter module can be connected in series with the input power of the conventional inverter module. This allows the inverter module to increase the number of voltage levels when using dual power supplies, and a single inverter module has five levels of output. The dual power supply design is based on two constant voltages of the same value that do not change due to load changes. If it is applied to PV, battery, or capacitor voltage divider, the average power of the two sources will not be equal under normal use, which may result in voltage level distortion.

The research in [22] also uses a sub-multilevel inverter module, but the sub-multilevel inverter module is used as a series-connected module. Furthermore, several series-connected modules are connected in series to increase the number of voltage levels and then connected to the H-bridge as an inverter. Considering that each series module is powered by the DC power supply with the same voltage as the input voltage, the voltage stress of the power

switch constituting the H-bridge will rise according to the number of levels, leading to higher switching loss.

3.2. Flywheel-Capacitor-Based MLIs

The research in [23] aims at increasing the number of voltage levels and the output voltage gain. The conventional three-level flying capacitor inverter with two power switches as a half-bridge structure can provide two voltage levels x_1 and x_0 instead of the original neutral voltage $x_{1/2}$ with a two-capacitor voltage divider. The conventional three-level flywheel capacitor circuit can provide three voltage levels x_1 , $x_{1/2}$, and x_0 , and the half-bridge structure, as the output, can provide a five-level inverter with voltage gain of 1.

The research in [24] aims at increasing the number of levels and reducing the voltage stress of the power switch. The active neutral clamping point circuit (ANPC) is connected in series with a flying capacitor as a five-level inverter with a voltage gain of 0.5. The corresponding maximum voltage capacity of the power switch in the ANPC is half of the input voltage, and the maximum voltage capacity of the power switch in the three-level flying capacitor inverter is only one-fourth of the input voltage. However, there is no real improvement of the ANPC neutral voltage problem, and the charging and discharging circuit paths between the neutral voltage-divided capacitor and the flywheel capacitor make the former charged and the latter discharged, resulting in the flywheel capacitor voltage being distorted so that the voltage level cannot be maintained at one-fourth of the input voltage.

The studies in [25,26] propose a T-type flywheel capacitor inverter, which replaces the flywheel capacitor in the conventional three-level flywheel capacitor inverter with two capacitors divided into a neutral point and a bi-direction switch connected to the output side so that the new topology can provide voltage levels x_1 , $x_{3/4}$, $x_{2/4}$, $x_{1/4}$, and x_0 . After this, adding the switched capacitor (SC) voltage doubler unit to the circuit provides voltage levels x_2 , x_1 , x_0 , and x_{-1} , and finally the whole structure is a 17-level inverter with a voltage gain of 2. In the studies of [25,26], the AOD-PWM is employed to maintain one-fourth of the input voltage of the two flywheel capacitors, because the current flow of the capacitor itself is different from that of the 3L FC inverter.

3.3. ANPC-Based MLIs

The ANPC multilevel inverter is presented to solve the shortcomings of the NPC and can be mainly classified into five types based on the symmetrical structure processing power, including switched-capacitor, T-type, F-type, K-type, and Class-D-type.

The research in [27] integrates a two-stage five-level ANPC inverter into a single-stage DC-AC converter with voltage boosting, which successfully reduces the number of power switches and capacitors while keeping the number of stages unchanged and also reduces the voltage across the power switches during the turn-off period. However, the C_1 capacitor cannot rely on SPWM to do self-balancing and must feed back the DC-link voltage $V_{dc-link}$ to control switch S_1 so that the C_1 capacitor voltage can be stabilized, and this makes it so other switches must be controlled with switch S_1 .

The study in [28] optimizes the three-stage active neutral clamping inverter, which is usually composed of a single power element in the conventional structure. However, in [28], it is composed of Si IGBT and SiC MOSFET together. By taking into account the characteristics of these IGBT and MOSFET, the control strategy of the inverter is to control the IGBT at a slow speed and the MOSFET at a fast speed. There two advantages in this control strategy. One is to significantly reduce the switching loss of the IGBT, and the other is to improve the power density. The MOSFET has better switching characteristics, and although increasing the fast switching frequency will increase the switching loss to some extent, the volume of magnetic material can be reduced. In addition, the output performance, efficiency, and loss analysis between 2-SiC and 4-SiC are compared with each other.

The research in [29] aims to improve the number of levels of ANPC as well as voltage gain, and the proposed circuit structure is based on the 5L-boost-ANPC inverter and expanded to 11 levels with a voltage gain of 2.5. Such an inverter uses a total of 12 power switches, and by taking an additional control strategy, this inverter can be changed to nine levels with a voltage gain of 1, which can reduce the voltage across the power switch during the turn-off period. The main difference between the two control strategies is that the voltages across the capacitors C_{f1} and C_{f2} are different. The nine-level control method treats C_{f1} and C_{f2} as flywheel capacitors and adjusts the output current direction of the inverter through the flywheel capacitors so that the voltages across C_{f1} and C_{f2} are maintained at $1/4 V_{in}$; the 11-level control method treats C_{f1} and C_{f2} as clamp capacitors and directly connects them in parallel to the input power or the capacitor-divided voltage, so that the voltages across C_{f1} and C_{f2} are maintained at $1/2 V_{in}$.

3.3.1. Switched-Capacitor-Based MLIs

The inverter presented by [30] can be considered as three modules. Module 1, called the single-pole switched capacitor (SPSC) circuit, consists of the switches S_3 and S_4 , the capacitor C_3 , and the diode D . Module 2, called the second-type active-clamp switched capacitor (ACSC) circuit, consists of the switches S_5 , S_6 , S_7 , and S_8 , and the capacitors C_1 and C_2 , where the switches S_7 and S_8 are used to keep the voltages on the capacitors C_1 and C_2 clamped to the input voltage V_{in} . Module 3, called the totem pole half-bridge (TPHB) circuit, is controlled by the switches S_1 and S_2 and operated in slow mode. These three modules use DC voltage as the SPSC input source, and ACSC and TPHB are connected in parallel to the output of the SPSC circuit to form a seven-level inverter with a voltage gain of 3.

In [31], the SC module is built up by the switches S_3 , S_4 , S_5 , S_6 , S_a and the capacitor C_1 . The proposed multilevel inverter is based on the switched-capacitor module with the same output characteristics as in [30] based on the SC voltage doubler unit. This inverter adopts the SC module cascaded with the three-level flywheel capacitor module and the totem pole half-bridge module and then is connected in parallel with the input source to achieve a nine-level inverter with voltage gain of 2. In addition, there are two derived circuits. One is the proposed original inverter cascaded with the SC module. The other is the proposed original inverter connected in series with the output side.

In [32], the proposed multilevel inverter is composed of the first capacitor clamping circuit based on the SC Voltage Tripler unit, the second capacitor clamping circuit based on the SC voltage doubler, and the totem pole half-bridge circuit. This multilevel inverter is similar to that in [30]. The two capacitor clamping circuits are fed by the DC voltage source, and the totem pole half-bridge circuit is connected in parallel with the output of the first capacitor clamping circuit to form a 13-level inverter with a voltage gain of 6, where the capacitor clamping voltages in these two capacitor clamping circuits are 3 times the input voltage V_{in} .

From the analysis mentioned above, one can see that the step switching multilevel DC-AC inverter adopts the DC power supply, semiconductor device, and capacitor to synthesize the AC output voltage. Although this inverter significantly reduces the number of switching cycles over one AC cycle, the DC-AC conversion current path is increased by too many semiconductor devices, thereby increasing conduction loss. Furthermore, since multilevel DC-AC inverters operate at low frequencies, the switched capacitors require a large capacity to provide voltage levels. In addition, the load transient response of this inverter is quite slow. For most of the capacitor clamping circuits, the capacitor charging is directly connected to the input power, and the charging will generate a huge inrush current.

3.3.2. T-Type

In [33], two conventional three-level T-type inverters are constructed as the symmetrical AC outputs, in which one cross-switched connection method is presented by using

switching elements to interleave the input sources of the T-type inverter. The number of levels is increased to nine with voltage gain of 2.

In [34], another cross-connected connection method is presented, in which the corresponding circuit can be regarded as a five-level totem pole T-type inverter with a 5-fold difference in voltage magnitude between two independent input voltage sources, which is connected in series with the output end to increase the number of levels by using the voltage difference between the two input sources to achieve a 25-level inverter.

In [35], a capacitor clamping circuit consisting of a conventional three-level T-type inverter cascaded with the switches S_3 to S_{10} . By using the concept of [1], the conventional three-level T-type inverter provides input voltage levels x_0 $x_1/2$ x_1 , and then the cascaded clamping circuit provides voltage levels $x-1$ x_0 x_1 x_2 to achieve a seven-level MLI with a voltage gain of 1.5.

3.3.3. F-Type

The research in [43] proposes a three-level F-type inverter. For a T-type inverter, the switches are placed like the letter T, and for an F-type inverter, the switches are placed like the letter F. By analyzing the loss distribution of the three-level T-type inverter, the positions of the power elements (e.g., the letter F) can be changed to reduce the voltage on some power elements during the turn-off period, which in turn reduces the switching loss of the power elements.

In [36], the three-level F-type inverter is used to increase the number of levels and voltage gain. The three-level F-type inverter is connected to a totem pole half-bridge module to boost the MLI to a five-level with a voltage gain of 1.

3.3.4. K-Type

In [37], the first K-type circuit is a three-level ANPC circuit with a floating capacitor added, in which two voltage dividing capacitors divide the neutral voltage, and then two power components are connected to this floating capacitor. In [37], the proposed topology is a five-level K-type inverter, which is finally upgraded to a seven-level K-type inverter by adding a totem pole module.

The inverter proposed in [38] is derived from the second K-type circuit. This circuit is based on an ACSC circuit. The main difference in the circuit between [38] and [37] is that in [38], the switches are placed like the letter K, so such a circuit is named K-Type. From the output manner, this circuit is also called the SC Half-mode unit. In addition, the study in [37] uses a continuous cascade manner to increase the voltage gain of the K-type.

3.3.5. Class-D-Type

The circuit presented by the study in [39] is based on an anti-noise Class-D amplifier for DC/AC power conversion, applied to 110 Vrms/60 Hz AC output with output power of less than 500 W, where this circuit can be used as a seven-level MLI with a voltage gain of 3. The proposed topology is a single-power symmetrical structure that uses an ACSC circuit to boost the voltage gain combined with a DNPC circuit for switching between levels. In particular, the control strategy focuses on improving efficiency, and the circuit structure can be designed to reduce the switching loss by only switching a single switch so as to achieve the switching level.

The research in [40] follows the DC-AC conversion application of the study [39]. The study in [39] focuses on the control strategy and DNPC structure to reduce the overall switching loss, while the research in [40] focuses on reducing the number of switches and the conduction loss. Both [39,40] are designed to maintain a circuit structure where only a single switch is switched to reach the switching level, but the proposed topology in [40] is a T-type structure modified from the DNPC of [39].

3.4. Diode-Clamped

In [10], the DNPC and T-type are combined in an asymmetric topology for the single-source AC output, where the DNPC has lower conduction loss for fast switching control and the T-type has lower switching loss for slow switching control to improve the inverter efficiency.

In [41], a full-bridge single-phase NPC structure is proposed to extend the traditional 3L-NPC to a 4L-NPC, where the full bridge refers to the 4L-NPC as a symmetric structure to provide the input voltage level $x0$ missing in the 4L-NPC and to enhance the overall multilevel inverter voltage gain. The neutral voltage of the conventional 3L-NPC is divided by two strings of capacitors, and its neutral voltage will change due to the change of load current, while the neutral voltage of 4L-NPC is divided by a factor of 3 of the input voltage for each of three high-capacitance capacitors, and its load current affects the neutral voltage more than 3L-NPC. It is necessary to consider the current compensation for the voltage across the voltage-divided capacitor.

The purpose of reference [42] is to increase the number of voltage levels and the output voltage gain of the inverter. The circuit can be considered as two 3L-NPC inverters with series output, where the front NPC circuit outputs to the rear neutral point of two voltage-divided capacitors. The voltage divider is converted to a clamping circuit by connecting the voltage-divided capacitor with a diode, and the rear capacitor is increased and clamped by a factor of 1.5 of the input voltage and clamped to achieve a single-phase seven-level NPC inverter with a voltage gain of 1.5.

Generally, the NP voltage of the intermediate DC-link capacitors in the diode-clamped MLI are balanced by proper operation. As the DC-AC stage has no NP balancing capability, the NP voltage has to be balanced by a preceding DC-DC stage, so the series connection of switches is allowed to avoid the complex problem of DC-link capacitor voltage balancing.

3.5. Comparison of the Recent Proposed MLIs

A comparison of the recent papers presented for the voltage-fed single-phase MLIs [10,20–27,29–42] under various criteria and feature emphases is tabulated in Table 2. In Table 3, the full names for all the abbreviations are as follows.

Table 2. Comparison of the recent papers presented for the voltage-fed single-phase MLIs.

	[10]	[20]	[21]	[22]	[23]	[24]
Number of Levels	5	9	5	9	5	5
Number of Switches	8	10	6	10	6	8
Number of Diodes	2	0	0	0	0	0
Number of Capacitors	2	4	0	0	1	3
Number of Transformers	0	2	0	0	0	0
Voltage Gain	0.78	2	2	4	1	0.5
Number of DC Power Sources	1	1	2	4	1	1
End of Output	two	two	two	two	two	two
Rated Load Power (W)	1000	—	—	—	25	300
Input Voltage (V)	400	50	—	—	24	128
Peak Output Voltage (V)	311	100	—	—	21.6	64
Rated Load THD (%)	—	12.50	17.66	8.90	33.27	3.86
Peak Efficiency (%)	97.09	95.77	—	—	95.21	—
Control Strategy	UP-PWM/ OLC-PWM	PD-PWM/ TPCS	PD-PWM	PD-PWM	PS-PWM	PS-PWM/ PD-PWM

Table 2. Cont.

Modeling	x	x	x	x	x	v
Feedback Controller Design	x	x	x	x	x	v
	[25]	[26]	[27]	[28]	[30]	[31]
Number of Levels	17	17	5	11	7	9
Number of Switches	9	11	7	12	10	11
Number of Diodes	2	0	0	0	1	0
Number of Capacitors	4	2	2	3	3	2
Number of Transformers	0	0	0	0	0	0
Voltage Gain	2	2	10	2.5	3	2
Number of DC Power Sources	1	1	1	1	1	1
End of Output	two	two	single	single	two	two
Rated Load Power (W)	480	480	400	500	60	330
Input Voltage (V)	160	160	40	100	30	50
Peak Output Voltage (V)	320	320	400	250	84.5	100
Rated Load THD (%)	—	6.96	35.11	—	5.30	13.51
Peak Efficiency (%)	98.36	97.80	97.50	96.67	97.61	97.30
Control Strategy	APOD-PWM	AOD-PWM	SPWM	SPWM	LS-PWM	PD-PWM
Modeling	x	x	x	x	x	x
Feedback Controller Design	x	x	x	x	x	x
	[32]	[33]	[34]	[35]	[36]	[37]
Number of Levels	13	9	25	7	5	7
Number of Switches	10	10	12	10	6	8
Number of Diodes	2	0	0	0	0	5
Number of Capacitors	4	4	4	4	2	3
Number of Transformers	0	0	0	0	0	0
Voltage Gain	6	2	—	1.5	1	1.5
Number of DC Power Sources	1	2	2	1	1	1
End of Output	two	two	two	single	two	two
Rated Load Power (W)	500	—	370	130	1250	1500
Input Voltage (V)	60	60	10 V + 50 V	100	350	200
Peak Output Voltage (V)	360	120	60	150	350	300
Rated Load THD (%)	—	9.36	3.26	—	1.55	—
Peak Efficiency (%)	97.32	98.94	—	98.20	98.70	96.60
Control Strategy	PD-PWM/	SHE-PWM	PD-PWM	SHE-PWM	PD-PWM	PD-PWM
Modeling	x	x	x	x	x	x
Feedback Controller Design	x	x	x	x	x	x
	[38]	[39]	[40]	[41]		[42]
Number of Levels	13	7	7	7		7

Table 2. *Cont.*

Number of Switches	14	12	10	12	8
Number of Diodes	0	8	6	8	6
Number of Capacitors	3	4	4	3	4
Number of Transformers	0	0	0	0	0
Voltage Gain	1.5	3	3	1	1.5
Number of DC Power Sources	1	1	1	1	1
End of Output	two	two	two	two	one
Rated-load Power (W)	1000	300	300	1200	100
Input Voltage (V)	260	56	56	400	180
Peak Output Voltage (V)	390	168	168	400	270
Rated Load THD (%)	5.30	2.75	3.36	—	21.09
Peak Efficiency (%)	96.80	97.90	97.42	96.80	95.39
Control Strategy	PD-PWM	LS-SPWM	LS-SPWM	SPWM	LS-PWM
Modeling	x	x	v	x	x
Feedback Controller Design	x	x	v	x	x

Table 3. Abbreviations of control strategy terminologies.

Number	Abbreviation	Full Name
1	SPWM	Sinusoidal Pulse Width Modulation [44]
2	OLC-PWM	One-Leg Clamping-PWM [45]
3	UP-PWM	Unipolar-PWM [46]
4	PD-PWM	Phase Disposition-PWM [47]
5	TPCS	Triangle and Parabolic Carrier Signals [48]
6	PS-PWM	Phase-Shifted-PWM [49]
7	APOD-PWM	Alternate Opposition Disposition-PWM [50]
8	LS-PWM	Level-Shifted-PWM [51]
9	SHE-PWM	Selected Harmonic Elimination-PWM [52]

4. Puzzles

From the above analysis, one can see that many researchers have focused on the structure, efficiency, and output of the multilevel inverter, but comparatively few researchers have focused on the THD and product usefulness. Here, some puzzles are presented for further thinking.

- (1) THD reduction and circuit symmetry, along with two-end output and self-balancing ability, should be investigated simultaneously. As a result, not only the interchangeability of mass production but also linear control can be easily achieved. Two-end output exhibits improved linearity, as the even harmonics of the switching frequency are very effectively suppressed in a perfectly symmetrical structure. Another advantage of a balanced configuration is that the supply voltage can be halved [53].

- (2) At present, there is no standard of the input voltage. Therefore, by taking 12 V as a base, a multiple of this base to obtain 24 V, 48 V, and 96 V, depending on customer needs.
- (3) Some special structures can reduce the number of switches, but they cannot be extended to the N -level.
- (4) Modeling and advanced control should be developed. To control the switching power converter, modeling is quite important, although there are numerous variations in analysis and measurement from the perspective of theory and implementation, respectively [54]. There are many strategies presented for modeling of the DC-DC converter, for example, the well-known state-space averaging method. However, very few examples of modeling of the multilevel DC-AC inverter can be found in the literature, and only open-loop waveforms are demonstrated in many studies. That is to say, transient responses are not taken into account. Consequently, modeling of the multilevel inverter and design of the closed-loop controller should be investigated.

5. Conclusions

Multilevel converters have been extensively developed over the last two decades and show several important advantages of power electronic circuits, such as operation at high voltages, harmonics reduction, higher efficiency, modularity, smaller size, and lower cost. Now, more and more commercial products are based on the multilevel inverter structure, and more and more worldwide research and development of multilevel-inverter-related technologies are in progress. This paper has provided a brief summary of multilevel inverter circuit topologies. Although this paper cannot cover or refer to all the related work, the fundamental principles of different multilevel inverters have been introduced systematically. Not only are the recent works surveyed, but some puzzles for MLIs are also pointed out to explore new ideas and pose new questions. The research and design engineer who possesses this perspective will be the freest and most able to venture into multilevel inverter technologies.

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