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Obtaining Robust Performance of a Current fed Voltage Source Inverter for Virtual Inertia Response in a Low Short Circuit Ratio Condition

Clint Z. Ally ^{1,2,*}  and Erik C. W. de Jong ²¹ Department of Electrical Engineering, Anton de Kom University of Suriname, Paramaribo, Suriname² Electrical Energy Systems, Eindhoven University of Technology (TU/e), 5612 AP Eindhoven, The Netherlands; E.C.W.de.Jong@tue.nl

* Correspondence: c.ally@tue.nl



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Abstract: Low inertia levels are typical in island power systems due to the relatively small rotational generation. Displacing rotational generation units with static inertia-less PV power results in a significant increase in the frequency volatility. Virtual inertia provided by inverter-storage systems can resolve this issue. However, a low short circuit ratio (SCR) at the point of common coupling together with a fast phase locked loop (PLL) will compromise the response performance of the system. To address this issue, a robust PI controller (RPI) for the inner current-loop of a current fed grid-connected inverter is proposed. The PLL disturbance and grid impedance are incorporated into a single model and recast to a generalized representation of the system, thereby allowing easy tuning of the RPI by the mixed sensitivity H_∞ method. The performance of the RPI is compared with that of a PI controller (PI) tuned by the regular loop-shaping method. The results show that when the SCR is above 10, the performance of both controllers is equivalent. However, lowering of the SCR compromises the performance of the system with PI and it becomes underdamped at $SCR < 2$. On the contrary, the system with the RPI is capable of maintaining the nominal performance throughout the same SCR decrease.

Keywords: virtual inertia; weak grid; current fed inverter; robust control

1. Introduction

Low inertia island grids have intricate frequency regulation challenges when inverter-based generation such as Photovoltaic systems (PV) are integrated. However, attractive financial incentives are driving the displacement of diesel-based generation by PV. The successful large-scale integration of PV into existing grids necessitates solutions aimed at mitigating the resulting increase in frequency volatility, thereby preventing PV curtailment, especially in low inertia grids. Field measurements on the island grids of Bornholm and Bonaire have shown that the time rate of change of frequency (ROCOF) can vary from 4 Hz/s to up to as high as 10 Hz/s [1,2]. This is in contrast to the ROCOF levels of 100 mHz/s to 1 Hz/s in the interconnected European system where inertia levels are sufficient [3]. ROCOF levels exceeding 2 Hz/s are undesirable for grid stability due to factors such as pole slipping in synchronous generators, stable connection of inverter-based generation where Phase Locked Loop (PLL) systems are employed, and inadequate operation of under frequency load shedding protection [4,5]. Frequency response measures such as Virtual Inertia Response (VIR) provided through grid-connected inverters with chemical battery energy storage systems (BESS) have proven to be a technically viable solution to increasing the amount of available inertia in the grid and thereby improving the ROCOF. It has been demonstrated that BESS-based VIR is capable of improving the zonal inertia in the South Australia grid where the penetration level of inverter-based generation can reach 60% of the demand [6]. The obtained improvement in the ROCOF level resulted

in a more stable interconnection (which is constrained by a 3 Hz/s ROCOF limit) with larger inertia segments of nearby existing grids. Other field experience in island grids have also shown that the capability of inverter-based storage systems to exchange power with the grid within 58 to 200 milliseconds after a frequency event have decreased the frequency volatility, thereby preventing power outages [7,8]. However, due to relatively large occurring ROCOFs in low inertia island grids, successful VIR implementation requires that the PLL necessary for measuring the frequency be of sufficient bandwidth (BW). Inadequate BW of the PLL may result in inaccurate frequency measurements [5] and, therefore, inaccurate calculation of the ROCOF. The results in [2] have shown that a ROCOF in the range of 10 Hz/s require that the PLL bandwidth be at least a decade greater than normally would be the case. The high BW requirement of the PLL unfortunately imposes another challenge for successful implementation of the inverter-based VIR. A low short circuit ratio (SCR) at the Point of Common Coupling (PCC) of the inverter and grid together with the high BW PLL will compromise the performance and stability of the inverter-storage system. Low SCR, a weak grid condition, is typical in island grids due to factors such as the radial structure of the grid and long sparse transmission lines [9]. A high BW PLL renders the behavior of the inverter closed-loop output impedance into that of a predominantly negative resistor at low frequencies. This behavior may cause instability upon interaction with a large enough grid impedance (low SCR) [10]. Power electronic converter stability issues due to interaction of the input impedance of the converter (the downstream impedance) and that of the upstream impedance (e.g., output filter, load or line) have long been an issue, resulting in Middlebrook's stability criteria for input filter design published in 1976 [11]. Since then, numerous studies have investigated the effect of the upstream impedance on the dynamics of power electronic converters and have presented solutions ranging from active damping to tuning methods for the inner-loop current controller. The work in [12] proposed an active damping scheme whereby the capacitor current of the LCL filter is used in a positive feedback proportional-integral (PI) control loop to virtually extend the positive equivalent resistance range, thereby obtaining robustness of the inverter against grid impedance variations. Essentially, this method prevents degradation of the phase margin (PM) due to grid impedance variations. The PLL impact on the inverter dynamics was, however, excluded. In [13], an adaptive block is added to the feedback loop of the PLL and a cancellation gain based on an estimation of the grid impedance is calculated to eliminate the coupling of the PLL and grid impedance. It is, however, unclear to what extent the estimation error and high BW PLL may compromise the method. Research has also given attention to the idea that an inner-loop current controller can be successfully designed to provide robustness of the inverter against upstream impedance interaction as demonstrated in [14]. Since then, others have followed and successfully designed various types of controllers. In [15], a filtered error tracking controller is adopted and implemented in the $\alpha\beta$ -frame, which eliminated the need for a PLL. These type of controllers are fundamentally designed to tightly track the reference. It was shown that once a set of smooth current references were provided to the controller, the inverter maintained nominal performance during a sudden increase of the grid impedance. Similarly, other types of controllers implemented in the $\alpha\beta$ -frame including a robustly tuned Proportional Resonant (PR) controller, and a combination of PR and a lead compensator are proposed in [16,17]. While these solutions in the $\alpha\beta$ -frame may be promising, VIR implementation requires determination of the grid voltage angle, and the synchronous reference frame PLL (SRF-PLL) is widely adopted in three phase inverters for this purpose [18]. Robust controller design methods such as H_∞ optimization have also been successfully applied to obtain robust controllers [19–21]. The obtained controllers were, however, of higher order compared to the simple structure of a PI controller, and the coupling between the PLL and the grid impedance was not taken into account. In [22], it was shown that the regular PI controller can be designed with adequate stability margins to withstand increases in the grid impedance and, as demonstrated in [23], even against the PLL-grid impedance coupling.

Based on the foregoing summary, the aim of this work is then to propose a solution that would allow successful VIR implementation in island grids where weak grid conditions of both low inertia and low SCR coexist and, as a result, degrade the performance of the inverter system. This work builds on the idea that the inner-loop current controller can be tuned to provide inverter robustness. Unlike previous research presented, this work takes a different approach and proposes adopting the H_∞ optimization method such that the regular and simple structure of the PI controller is maintained and tuned to achieve inverter robustness against PLL-grid impedance coupling. To achieve this, a validated small signal model of a current fed inverter is recast into a generalized representation and the PLL-grid impedance coupling is treated as a single multiplicative perturbation. The formulation of the PLL-grid impedance coupling into a single perturbation then allows for easy application of the mixed sensitivity H_∞ optimization method. It is shown that the H_∞ tuned PI controller is capable of providing inverter robustness against the coupling of a 50 Hz PLL and $SCR < 3$. The rest of this paper is organized as follows: in Section 2, a detailed switching model of a current fed inverter is built in MATLAB/Simulink (The MathWorks, Inc.: Natick, MA, USA) and validated with lab measurements. The transfer functions of the validated model are presented in Section 3 and verified through a frequency response comparison. In Section 4, a generalized representation of the inverter model together with the PLL-grid impedance coupling is developed. The performance of the obtained H_∞ PI controller in weak grid conditions is presented in Section 5, and finally, conclusions are formulated in Section 6.

2. Modeling and Validation

2.1. Validation of Detailed Switching Model

A current fed voltage source inverter (CFVSI) available in a lab is depicted in Figure 1 and the corresponding parameters are listed in Table 1. The schematic diagram of the CFVSI is shown in Figure 2, which also depicts the situation where the CFVSI system is connected to a grid through the line impedance Z_g . In the virtual inertia scheme, a reference signal can be issued to the DC-DC converter, thereby extracting (or absorbing) the corrective power from the BESS and exchanging it through the CFVSI with the grid. The time rate of change of the reference signal varies with the ROCOF, which is calculated by the “VIR control block” based on the angle δ issued by the PLL, as shown in Figure 2.

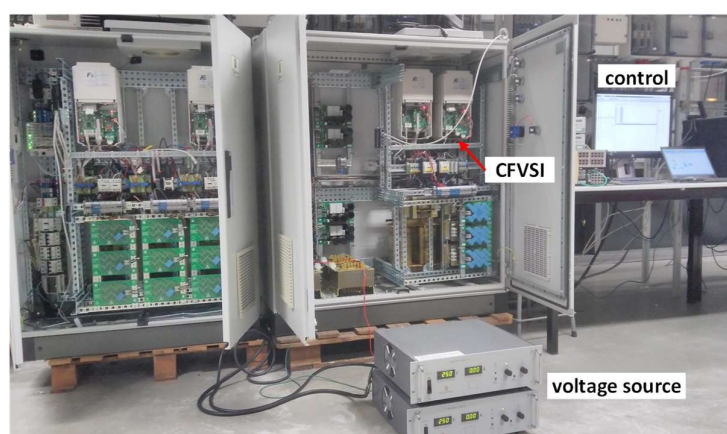
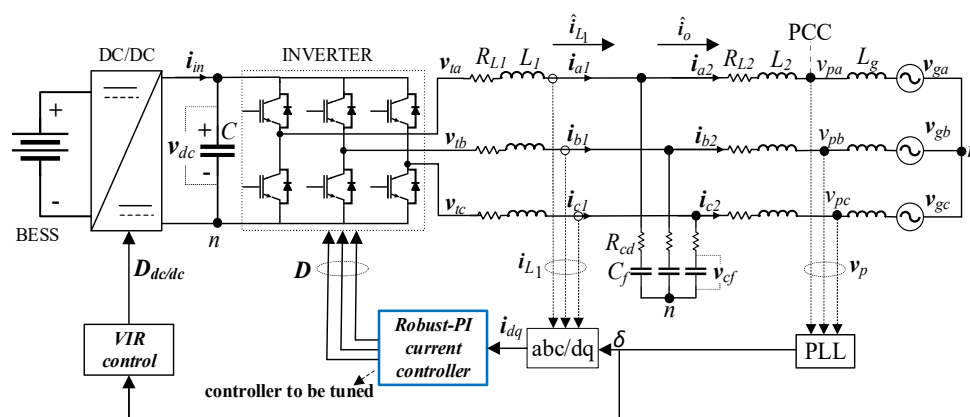


Figure 1. Lab-setup of CFVSI.

Table 1. CFVSI parameters.

Parameter	Value	Unit
Rated power	17	kVA
Rated voltage	400	V
DC link voltage	650–750	V
DC link capacitance C	0.75	mF
Filter inductance $L_1; L_2$	22.3; 1.28	mH
Filter resistance $R_{L1}; R_{L2}$	200	m Ω
Filter capacitance C_f	8.8	μ F
Switching frequency, f_s	8–20	kHz
Fundamental frequency	50	Hz

**Figure 2.** Schematic diagram of a typical current-fed voltage source inverter.

The control analysis in time-domain was conducted through simulations with a detailed switching model of the CFVSI built in the software package MATLAB/Simulink. To validate the model, the aforementioned VIR scheme was emulated in the lab and the CFVSI dynamic response of the DC link voltage, grid currents, and voltages in both dq- and abc-domains were recorded. The measurements were sampled at the inverter switching frequency of 8 kHz, which is well above the 1.5 kHz resonant frequency of the inverter LCL filter [24]. The same scheme was simulated with the MATLAB/Simulink model, and the simulated results were compared to the experimental recordings. Figures 3–5 show the measured and simulated responses of the DC link voltage of which the setpoint voltage was 650 V, and the d-component of the grid currents for the three current injections is as follows: 5 A at a rate of 5 A/s, 8 A instantaneously, and 10 A at 100 A/s.

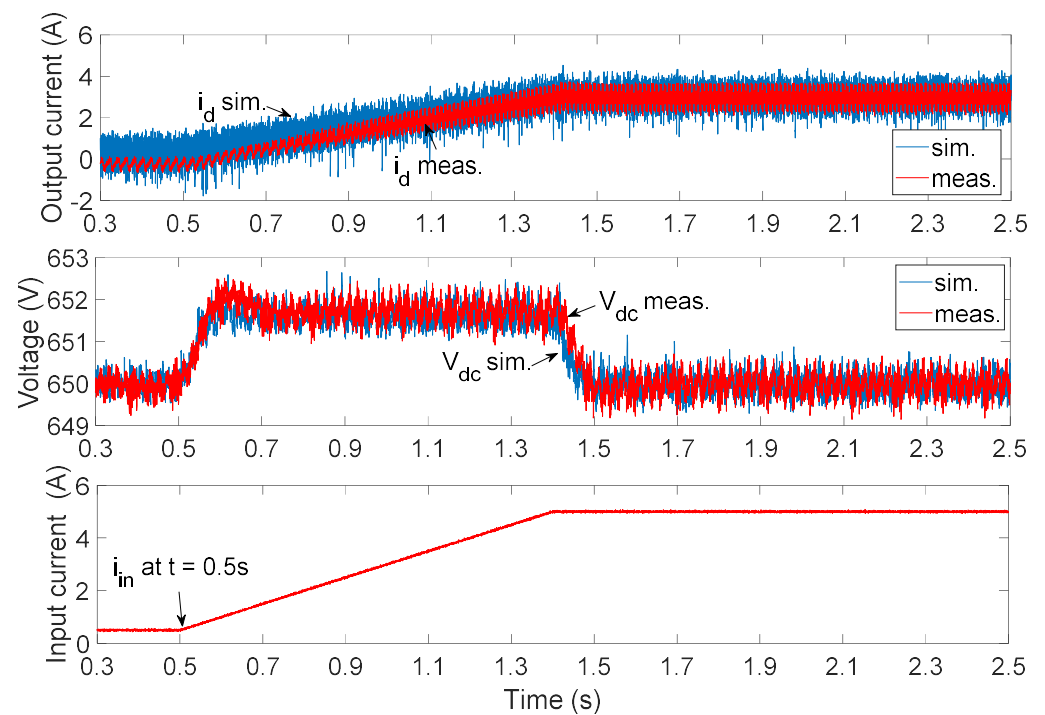


Figure 3. Current injection of 5 A at 5 A/s.

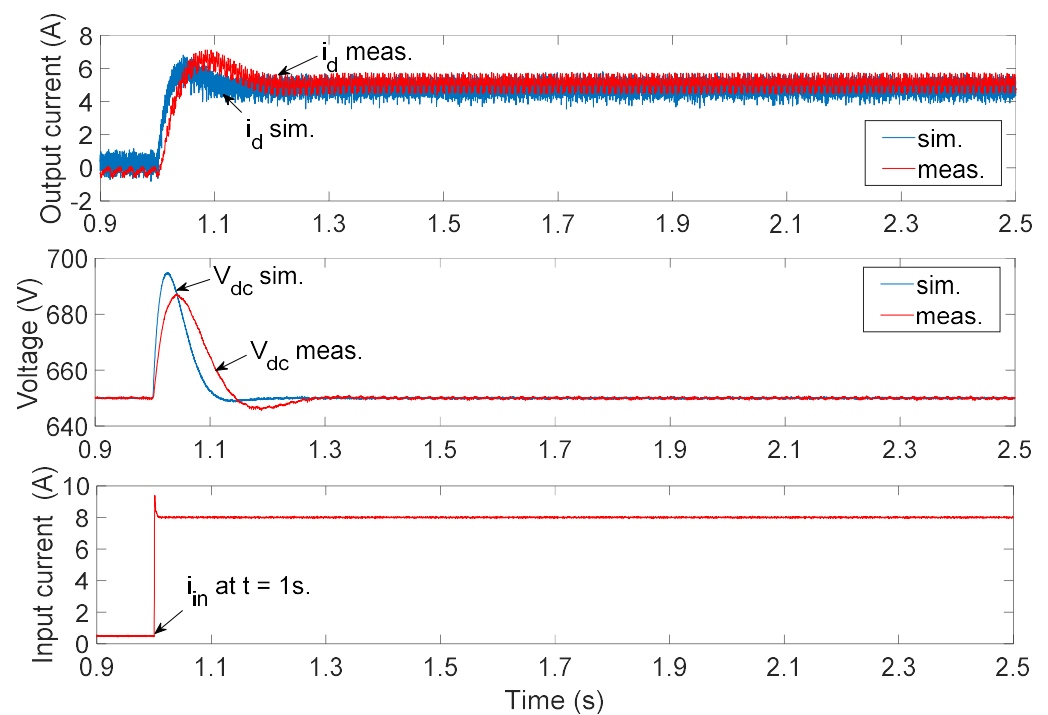


Figure 4. Current injection of 8 A instantaneously.

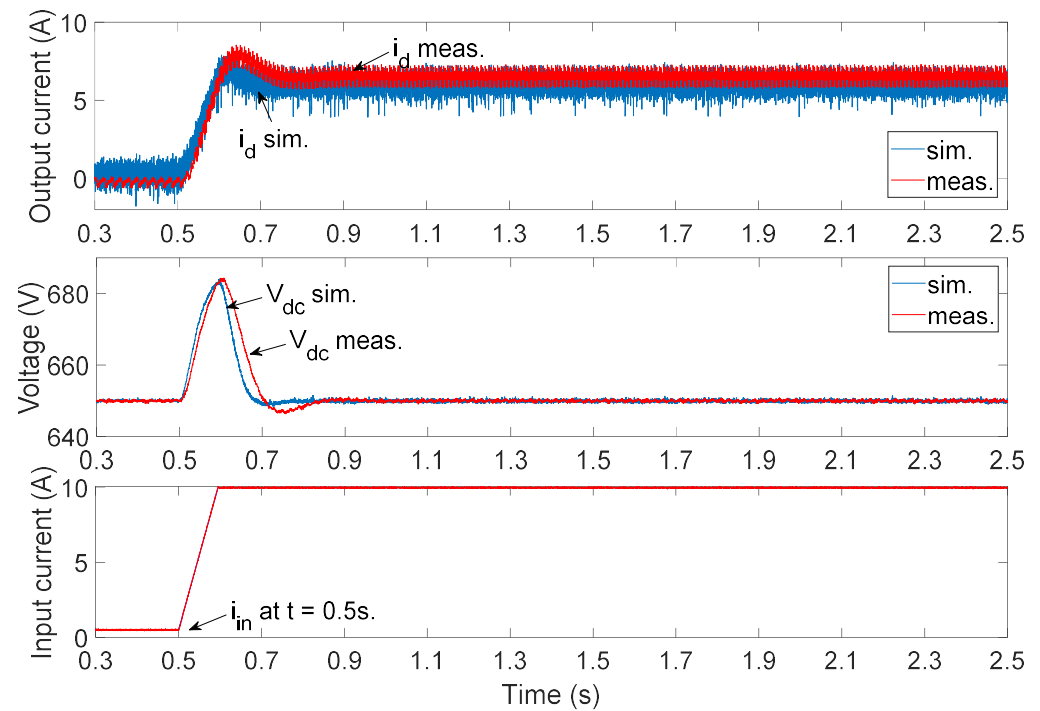


Figure 5. Current injection of 10 A at 100 A/s.

Comparison of the simulated responses to the recordings show that the model is capable of representing the dynamics of the real system.

2.2. Small Signal Model of the CFVSI

Next, a linear small signal model of the CFVSI was derived using space phasor variables. The inductor currents i_{L1} and i_o and capacitor voltages v_{dc} and v_{cf} , as depicted in Figure 2, were chosen as state variables of the system, with input and output variables defined, respectively, as: i_{in} , v_p , D ; and v_{dc} , i_{L1} , i_o . Referring to Figure 2, the set of simultaneous differential equations describing the dynamics of the balanced three phase system could then be formulated in space phasor form to give Equation (1).

$$\begin{cases} \frac{d\langle \vec{i}_{L1} \rangle}{dt} = \frac{1}{L_1} \left[\vec{D} \langle v_{dc} \rangle - \langle \vec{i}_{L1} \rangle (R_{L1} + R_{cd}) + \langle \vec{i}_o \rangle R_{cd} - \langle \vec{v}_{cf} \rangle \right] \\ \frac{d\langle \vec{i}_o \rangle}{dt} = \frac{1}{L_2} \left[\langle \vec{v}_{cf} \rangle + \langle \vec{i}_{L1} \rangle R_{cd} - \langle \vec{i}_o \rangle (R_{L2} + R_{cd}) - \langle \vec{v}_p \rangle \right] \\ \frac{d\langle \vec{v}_{cf} \rangle}{dt} = \frac{1}{C_f} \left[\langle \vec{i}_{L1} \rangle - \langle \vec{i}_o \rangle \right] \\ \frac{d\langle v_{dc} \rangle}{dt} = \frac{1}{C} \left[\langle i_{in} \rangle - \frac{3}{2} \vec{D} \langle \vec{i}_{L1} \rangle \right] \end{cases} \quad (1)$$

where the variables in brackets are averaged values.

After (1) is expanded (e.g., $\frac{d\langle \vec{i}_{L1} \rangle}{dt} = (i_{L1d} + j i_{L1q}) e^{j\delta(t)}$), solved, and linearized, the variables can be decomposed into their dq-components. The obtained expression can then be written in the state-space form of (2). The obtained corresponding state-space matrices are given in Appendix A.

$$\begin{cases} s\mathbf{X}(s) = \mathbf{A}\mathbf{X}(s) + \mathbf{B}\mathbf{U}(s) \\ \mathbf{Y}(s) = \mathbf{C}\mathbf{X}(s) + \mathbf{D}\mathbf{U}(s) \end{cases} \quad (2)$$

The open-loop transfer functions in the s -domain can be found by applying the transfer function matrix in (3) to (2), as elaborated in [25].

$$G(s) = \frac{Y(s)}{U(s)} = C(sI - A)^{-1}B + D \quad (3)$$

where I is the identity matrix.

The obtained open-loop transfer functions are collected in $G(s)$ and are given in Appendix A. The 2 by 2 transfer matrices relate the corresponding output to input vectors. With the open-loop transfer functions now available, the total system block diagram can be constructed, as shown in Figure 6. The block diagram includes the dynamics of the PLL and the grid impedance Z_g . The PLL transfer functions G_{PLL} and Y_{PLL} can be derived as elaborated in [26], and are given in Appendix A. The typical cascade control configuration contains an outer-loop voltage controller and an inner-loop current controller, denoted here, respectively, by G_{vPI} and G_{cPI} . The DC link voltage is regulated by issuing the reference current i_{dref} to G_{cPI} , thereby transferring the input power to the grid. The two loops are isolated by making the inner-loop faster than the outer-loop, i.e., designing G_{cPI} to be at least a decade higher than G_{vPI} [27].

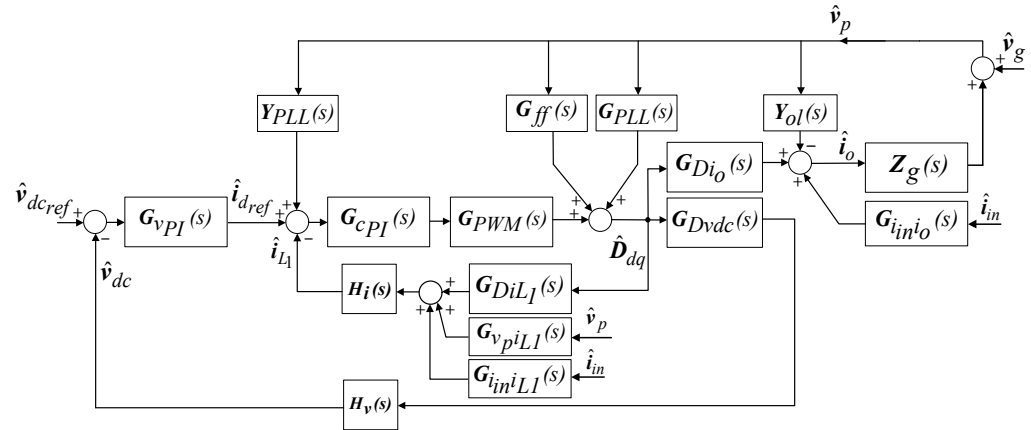


Figure 6. Total system block diagram.

3. Transfer Functions Verification

In this section, the closed loop transfer functions of the detailed CFVSI are presented and verified. It should be pointed out that, in the simulations, the grid current is measured on the inverter side, as shown in Figure 2; however, to take the effect of both the PLL and grid inductance into account, the closed-loop transfer functions are derived based on the current i_o entering Z_g . The closed-loop output admittance Y_{ocl} , i.e., the transfer function from $\hat{v}_p$ to $\hat{i}_o$ with both the inner current-loop and the outer voltage-loop closed, can be derived from the corresponding open-loop transfer functions. The open-loop transfer functions are obtained from the matrix $G(s)$ and given by (4) and (5), with the dq sub-subscripts omitted for brevity.

$$\hat{i}_o = G_{i_{in}i_o} \hat{i}_{in} - Y_{ol} \hat{v}_p + G_{Di_o} \hat{D} \quad (4)$$

$$\hat{v}_{dc} = G_{i_{in}v_{dc}} \hat{i}_{in} + G_{v_p v_{dc}} \hat{v}_p + G_{Dv_{dc}} \hat{D} \quad (5)$$

The closed-loop transfer functions for the inner current-loop are found by solving for the duty ratio $\hat{D}$ and then substituting the obtained expression into (4) and (5). By inspection of Figure 6, the following expression for $\hat{D}$, which includes the PLL dynamics, is obtained:

$$\hat{D} = (I + L_c)^{-1} \left\{ G_{PWM} G_{cPI} \hat{i}_{dref} - H_i G_{PWM} G_{cPI} G_{i_{in}i_{L1}} \hat{i}_{in} \right. \\ \left. \left[(G_{ff} + G_{PLL}) + G_{PWM} G_{cPI} (Y_{PLL} - H_i G_{v_p i_{L1}}) \right] \hat{v}_p \right\} \quad (6)$$

With, $L_c = H_i G_{Di_{L1}} G_{PWM} G_{cPI}$.

The closed-loop dynamics including the outer voltage-loop are found by replacing $\hat{i}_{d_{ref}}$ in (6) with the following expression obtained from Figure 6:

$$\hat{i}_{d_{ref}} = \left(v_{dc_{ref}} - H_v \hat{v}_{dc} \right) G_{vPI} \quad (7)$$

Substitution of the obtained $\hat{D}$ into (5) yields the following expression for the closed-loop dynamics:

$$\hat{v}_{dc} = G_{i_{in}v_{dc}}^{cl} \hat{i}_{in} + G_{v_p v_{dc}}^{cl} \hat{v}_p + G_{v_{dc_{ref}} v_{dc}}^{cl} \hat{v}_{dc_{ref}} \quad (8)$$

$$\hat{i}_o = G_{i_{in}i_o}^{il} \hat{i}_{in} - Y_o^{il} \hat{v}_p + G_{i_{d_{ref}}i_o} \left(\hat{v}_{dc_{ref}} - H_v \hat{v}_{dc} \right) G_{vPI} \quad (9)$$

Finally, replacing $\hat{v}_{dc}$ in (9) with (8) yields the total closed-loop dynamics of the output current, which is given by:

$$\hat{i}_o = G_{i_{in}i_o}^{cl} \hat{i}_{in} - Y_o^{cl} \hat{v}_p + G_{v_{dc_{ref}}i_o}^{cl} \hat{v}_{dc_{ref}} \quad (10)$$

The full expressions of the closed-loop transfer functions in (8) and (9) are given in Appendix A. The closed-loop output admittance of the inverter with both inner-and outer-loops closed is given by:

$$\frac{\hat{i}_o}{\hat{v}_p} = Y_o^{cl} = Y_o^{il} + G_{i_{d_{ref}}i_o} G_{vPI} H_v G_{v_p v_{dc}}^{cl} \quad (11)$$

Y_o^{cl} contains all the transfer functions necessary to tune the inner-loop current controller. Next, the verification of the obtained transfer functions follows before using them to design the controller. The validated detailed switching model of the CFVSI is used to verify the derived transfer functions by comparing the frequency responses of Y_o^{cl} . The frequency response of Y_o^{cl} of the detailed switching CFVSI model is obtained in MATLAB/Simulink by the frequency estimation method. A fixed-step sine sweep signal (appropriate for discrete simulation [28]) is adopted and a small perturbation (around 5% of rated terminal voltage) is added to terminal voltage of the inverter model. This was achieved by computing the dq-values of the terminal voltage, adding the excitation signal, and then transforming them back to time varying abc-voltages. The corresponding dq-components of the output current were computed with the PLL, thereby obtaining the frequency responses of Y_{od}^{cl} and Y_{oq}^{cl} , respectively. The inverter was operated at steady state points of, respectively, $i_{in} = 10$ A, and $i_{oq} = 2$ A.

The estimated frequency response of the detailed switching model and the frequency response of the derived transfer function for Y_o^{cl} are shown in Figure 7. The obtained results show good similitude, and deviations at the low frequency end may be ascribed to the initial conditions.

To include and evaluate the effect of changes in Z_g on $\hat{i}_o$, $\hat{v}_p$ in (10) is replaced with $\hat{v}_p = \hat{v}_g + Z_g \hat{i}_o$; this yields the following expression for $\hat{i}_o$ (with the term due to the dc-ref. voltage omitted):

$$\hat{i}_o = \left[G_{i_{in}i_o}^{il} \hat{i}_{in} - Y_o^{cl} \hat{v}_g \right] \frac{1}{I + Y_o^{cl} Z_g} \quad (12)$$

From (12), it is evident that the stability of the injected virtual inertia current, i.e., $\hat{i}_{in}$, is impacted by the interaction between the grid impedance and the inverter output impedance.

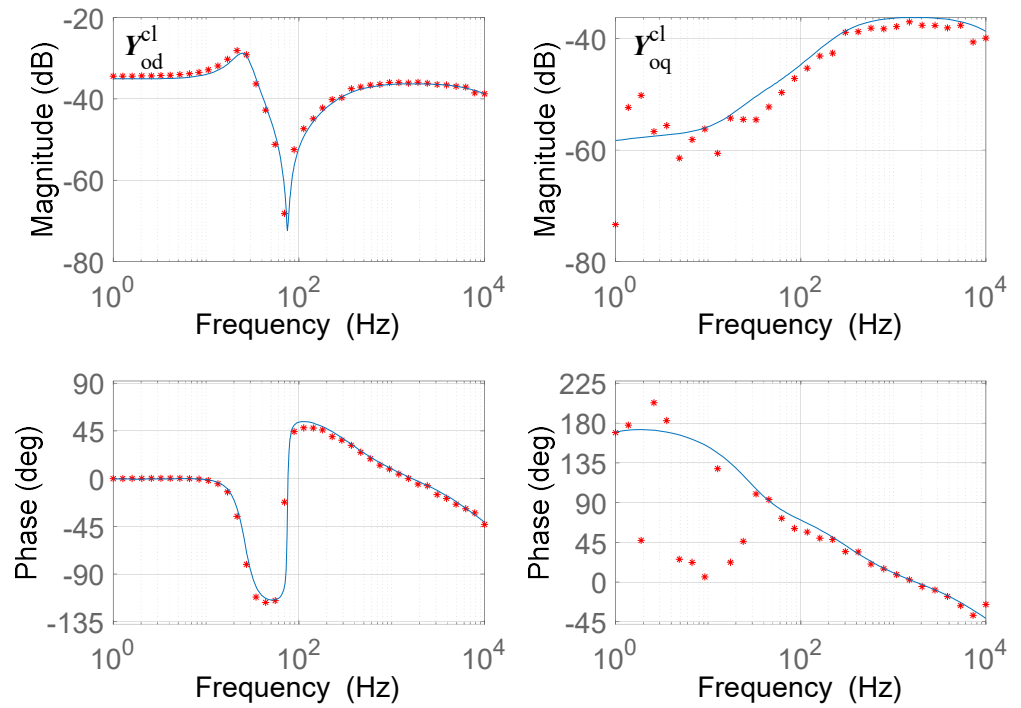


Figure 7. Frequency responses of Y_o^{cl} . Red-dotted: estimation; blue solid line: transfer function.

4. Generalized Representation and Controller Design

4.1. Generalized Representation

In this section, the verified transfer functions are used to translate the “inverter power exchange in weak-grid condition” problem into the framework of robust control. In this regard, a generalized representation of the inverter output dynamics is useful for analyzing and designing the robust inner-loop current controller. Therefore, the loops of the output stage of the inverter block diagram shown in Figure 6 are eliminated to produce the following equivalent transfer functions:

$$G_F = G_{PWM} G_{Di_o} [I + Z_g (Y_{ol} - G_{PLL} G_{Di_o})]^{-1} \quad (13)$$

$$G_B = (-Y_{PLL} Z_g + I) \quad (14)$$

G_F and G_B relate the input to output dynamics, respectively, of the duty ratio to output current, i_o , and the output current to the measured output current, i_{om} . Increases in Z_g are treated as a parametric uncertainty, which is useful for formulating the problem as a robust control problem.

The reduced block diagram, including the normalized uncertainties due to Z_g , i.e., $\Delta_F(s)$ and $\Delta_B(s)$, is shown in Figure 8. Note that $\Delta(s)$ represents the uncertainty normalized to the nominal plant ($Z_g = 0$), i.e.: $\Delta(s) = \left| \frac{G_{Z_g \neq 0}(s) - G_{Z_g = 0}(s)}{G_{Z_g = 0}(s)} \right|$.

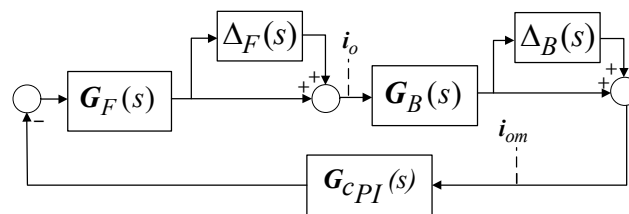


Figure 8. Reduced block diagram.

To obtain the generalized plant configuration P of the system, Figure 8 is recast to that shown in Figure 9 with: $G_{pe} = \frac{G_F}{I + G_F G_{cPI} (G_B - I)}$, and G_{cPI} as the controller to be tuned. Note that the control signal u is not penalized and, therefore, the weighting is omitted from the generalized representation.

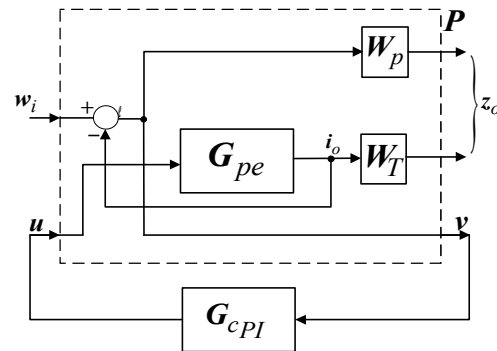


Figure 9. Generalized representation of the system.

The exogenous inputs to the generalized plant P are gathered in the input vector $w_i = [i_{d_{ref}} \ v_g \ i_{in}]^T$, and the controller input to P is specified by u . The weighted exogenous outputs of P are gathered in $z_o = [W_T i_o \ W_P v]^T$, with W_T and W_P weighting functions as explained in Section 4.2. The output vector v is given by $[e \ 0]$.

With these expressions, the generalized open-loop expression from $[w_i \ u]^T$ to $[z_o \ v]^T$ is given by,

$$\begin{bmatrix} z_o \\ v \end{bmatrix} = \begin{bmatrix} P_{11} & P_{12} \\ P_{21} & P_{22} \end{bmatrix} \begin{bmatrix} w_i \\ u \end{bmatrix} \quad (15)$$

where P is partitioned as follows:

$$P_{11} = \begin{bmatrix} 0 \\ W_P \end{bmatrix}; P_{12} = \begin{bmatrix} W_T G_{pe} \\ -W_P G_{pe} \end{bmatrix}; P_{21} = [I]; P_{22} = [-G_{pe}] \quad (16)$$

The closed-loop relation between the input and output vectors, respectively, w_i and z_o , is found by computing the linear fractional transformation of P and G_{cPI} as follows:

$N = P_{11} + P_{12} G_{cPI} (I - P_{22} G_{cPI})^{-1} P_{21}$, which results in,

$$N = \begin{bmatrix} W_T G_{pe} G_{cPI} (I + G_{pe} G_{cPI})^{-1} \\ W_P (I - G_{pe} G_{cPI} (I + G_{pe} G_{cPI})^{-1}) \end{bmatrix} = \begin{bmatrix} W_T T \\ W_P S \end{bmatrix} \quad (17)$$

The resulting vector N contains the expressions of both the weighted-complementary sensitivity and sensitivity transfer functions, referred to, respectively, by T and S . The expression given by N is used for synthesizing the robust controller by the mixed-sensitivity method, as discussed in the results section.

4.2. Weighting Functions

The weighting functions (which should be stable and proper functions [29]) can be viewed as the tuning knobs for synthesizing the robust controller. In the mixed-sensitivity tuning method, two weighting functions, W_T and W_P , are required for, respectively, T and S . The inverse of these weighting functions, i.e., $|W_T|^{-1}$ and $|W_P|^{-1}$, form upper bounds on the perturbed T and S in the frequency domain. The variation of Z_g creates a parametric uncertainty in T and S and is modelled as a multiplicative perturbation, as shown in Figure 8. If the block diagram in Figure 8 is redrawn to an equivalent block diagram, as shown below in Figure 10 below, a single perturbation $\Delta_{eq}(s) = \Delta_F(s) \Delta_B(s)$ is obtained.

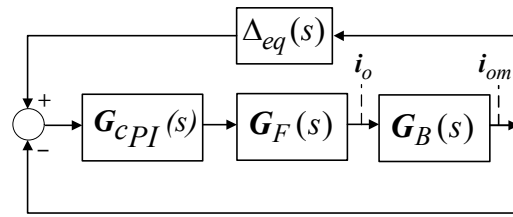


Figure 10. Simplified block diagram with single multiplicative perturbation.

It can then be easily deduced from Figure 10 that, in accordance with the small-gain theorem [29], if the H_∞ norm of $\Delta_{eq}T$ is satisfied, i.e., $|\Delta_{eq}(s)T(s)| < 1$ where T is derived with respect to i_o , the system will be stable throughout the uncertainty margin $\Delta_{eq}(s)$. The weighting function W_T is a representation of $\Delta_{eq}(s)$ and forms an upper bound across the entire frequency range; therefore, the following requirement is made of W_T :

$$\bar{\sigma}\{\Delta_{eq}(j\omega)\} < |W_T(j\omega)|.$$

With $\bar{\sigma}\{\Delta_{eq}(j\omega)\}$, the largest singular value of $\Delta_{eq}(s)$.

W_p^{-1} forms an upper bound on the perturbed sensitivity function S_Δ and contains the desired performance requirements. Based on the presented arguments, the following transfer functions were considered, respectively, for W_T and W_p :

$$W_T(s) = \left(\frac{\omega_{WT}^{-1}s + M_T^{-1/2}}{\omega_{WT}^{-1}A_T^{1/2}s + 1} \right)^2; W_p(s) = \frac{M_p^{-1}s + \omega_{WP}}{s + \omega_{WP}A_p}$$

Values of $M_T = 3$ and $M_p = 8$ were chosen to provide good roll off at high frequency. A_T and A_p were chosen to be small non-zero values, i.e., 10^{-6} , such as to obtain a Butterworth type filter characteristic. The bandwidths ω_{WT} and ω_{WP} were selected such that $\omega_{WP} < \omega_L < \omega_{WT}$, where ω_L is the loop cross-over frequency. The requirement that $|S+T| = I$ means that both S and T cannot be made less than I in the same frequency range. Therefore, their respective bandwidths should be sufficiently separated [29].

Hence, ω_{WP} was selected to yield a closed-loop time constant of around 1 ms and ω_{WT} was chosen to be 10^4 rad/s. Bode plots of the obtained weights and several plots of S_Δ (as Z_g is increased) and $\Delta_{eq}(s)$ are shown in Figure 11.

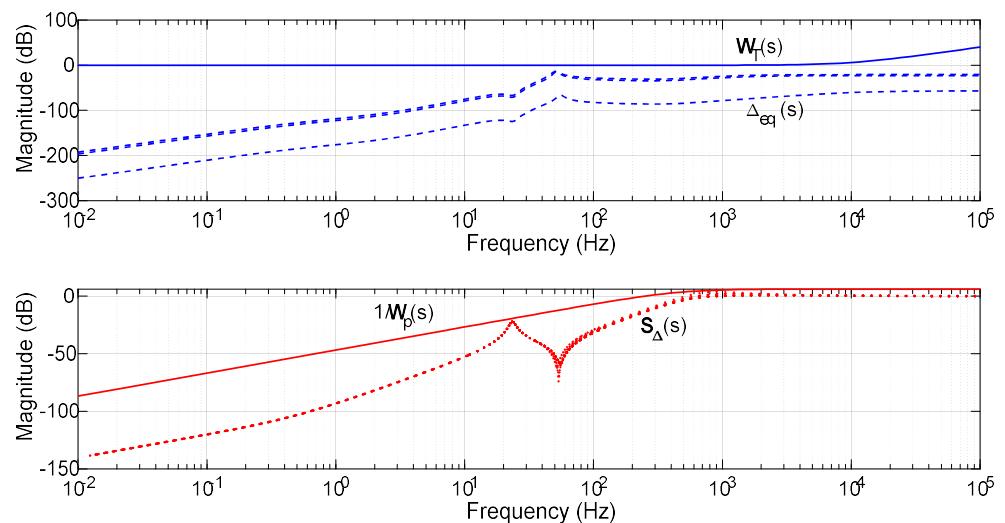


Figure 11. Weighted upper bounds on $\Delta_{eq}(s)$ and $S_\Delta(s)$.

5. Results

5.1. Synthesized Robust Controller

In the mixed-sensitivity approach, the H_∞ norm of (17) is minimized and, thus, the obtained controller provides robustness in that it is capable of maintaining the system stability ($|W_T T| < 1$) and performance ($|W_p S| < 1$) throughout the predefined uncertainty margin.

The so-called fixed-structure control synthesis is conducted in MATLAB by applying the structured H_∞ optimization method detailed in [30]. The vector N is computed by invoking the *lft()* function with the input arguments G_{pe} and $G_{c_{PI}}$. $G_{c_{PI}}$ is treated as a tunable fixed structured transfer function, while the variation of Z_g in G_{pe} is captured with the ureal function [31]. The outer-loop voltage controller $G_{v_{PI}}$ was designed to have a crossover frequency of 40 Hz, and the PLL a crossover frequency of 50 Hz. The performance of the tuned robust PI controller (RPI) was compared to that of a nominal PI controller (PI) tuned by the regular loop shaping method. The PI was tuned to have a 65° PM at a crossover frequency of 1/10 the switching frequency [32]. Below are the obtained controllers:

$$RPI_d = RPI_q = \frac{1.8s + 44}{s}; \text{ with final peak gain : } 1.03;$$

$$PI_d = PI_q = \frac{0.21s + 484}{s}$$

5.2. Sensitivity Analysis

In the sensitivity analysis, the uncertainty margin of the line inductance (L_g) is made to be in the range of 0 mH–20 mH. In this regard, the base case corresponds to the situation where L_g is smaller than 3 mH ($SCR > 10$) and weak grid conditions where L_g is made to be greater than 10 mH ($SCR < 3$). According to (12), the stability and performance of the injected virtual inertia current ($\hat{i}_{in}$) can be predicted by the Nyquist criterion of $Y_o^{cl} Z_g$ [25]. To illustrate the performance difference between the PI and RPI, the PLL crossover frequency is raised to 100 Hz. The resulting Nyquist plot of $Y_o^{cl} Z_g$ is shown in Figure 12 as the SCR is decreased from above 10 to below 2. It is evident from the Nyquist plot that the stability margins of the system with the PI (red loci) have larger sensitivity to decreases in the SCR than that of the system with RPI (blue loci). When the SCR is decreased from 2 to 1, the PM and gain margin (GM) of the system with PI decrease from, respectively, around 59° to 25° , and from around 11.1 dB to 4.8 dB. In comparison, the system with RPI has smaller changes in the stability margins, i.e.: the PM changes from around 66° to 41° , while the GM changes from around 13 dB to 6.8 dB. The stability margin achieved with RPI at a SCR of around 1 is similar to that achieved with PI at a SCR of 2.3. This indicates that the system with RPI can handle more than a 50% decrease in SCR than the system with PI.

The performance sensitivity of the system with the PI and RPI is further analyzed by considering the magnitude plot of the closed-loop transfer function from $\hat{i}_{d_{ref}}$ to $\hat{i}_o$, i.e., T , as the SCR is decreased as before. Increases in the magnitude of T are a good indicator of degradation of the system damping and, therefore, a good indicator of poor transient performance [29]. The magnitude plots of T are shown in Figure 13 for the system with PI (red) and RPI (blue). Comparison of the two plots shows larger changes in $|T|$ for the system with PI (2.3 dB to 18.5 dB) than for the system with RPI (1.14 dB to 8.8 dB) for the same decrease in SCR. This observation confirms the results from the Nyquist plot of $Y_o^{cl} Z_g$, i.e., there is higher performance sensitivity to changes in SCR for the system with PI than for the system with RPI.

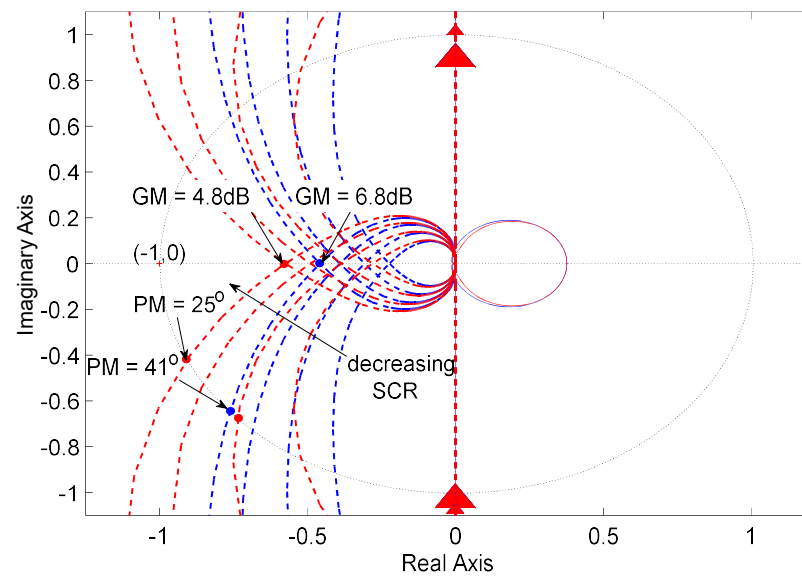


Figure 12. Nyquist plot of $Y_o^{cl} Z_g$. Red: PI; blue: RPI.

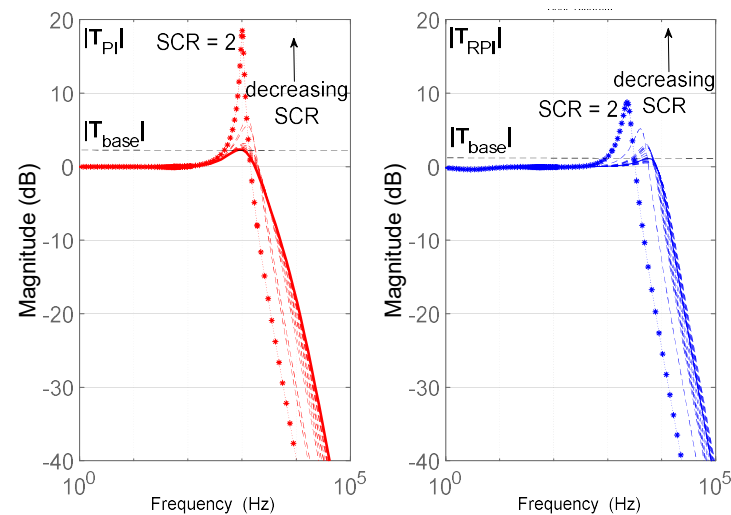


Figure 13. Magnitude plots of $|T|$. Red: PI; blue: RPI.

5.3. Time Domain Simulations

Finally, both controllers are used to perform time domain simulations with the validated detailed switching model of the CFVSI from Section 2. The PLL is fixed at 50 Hz, while the SCR is decreased from the base case of above 10 to the weak grid case of below 2. A step current of 10 A is injected at $t = 0.05$ s through the DC-DC boost converter, as previously outlined. Figure 14 shows that in the base case, i.e., $SCR > 10$, both controllers achieve identical response performance. However, as can be seen in Figures 15 and 16, the performance of the system with PI deviates from its nominal state as the SCR is decreased from the base case to the weak grid case. The response eventually becomes underdamped at $SCR < 2$, which is also visible in the initially distorted current waveforms in Figure 16. On the contrary, as shown in Figure 17 and the abc-waveforms in Figure 18, the system with RPI shows little performance degradation throughout the same SCR decrease. This is a satisfactory result as it shows that the robustly tuned inner-loop PI controller can maintain its nominal performance in a weak grid condition with a fast PLL.

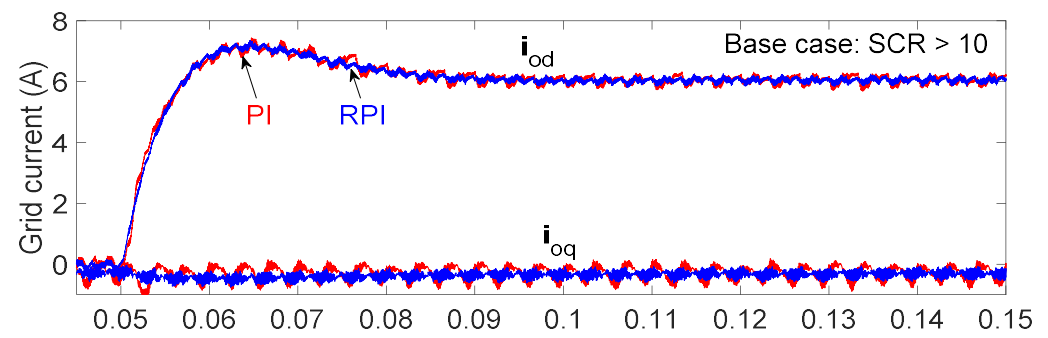


Figure 14. dq-grid currents with SCR > 10. Red: PI; blue: RPI.

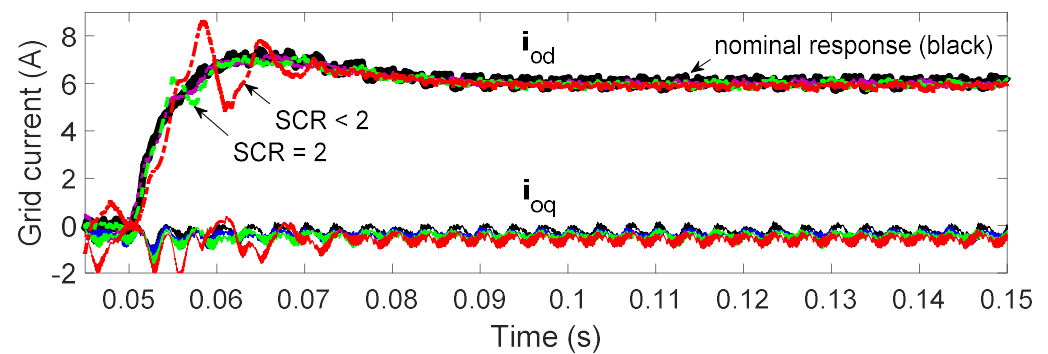


Figure 15. dq-grid currents of the system with PI for SCR < 10.

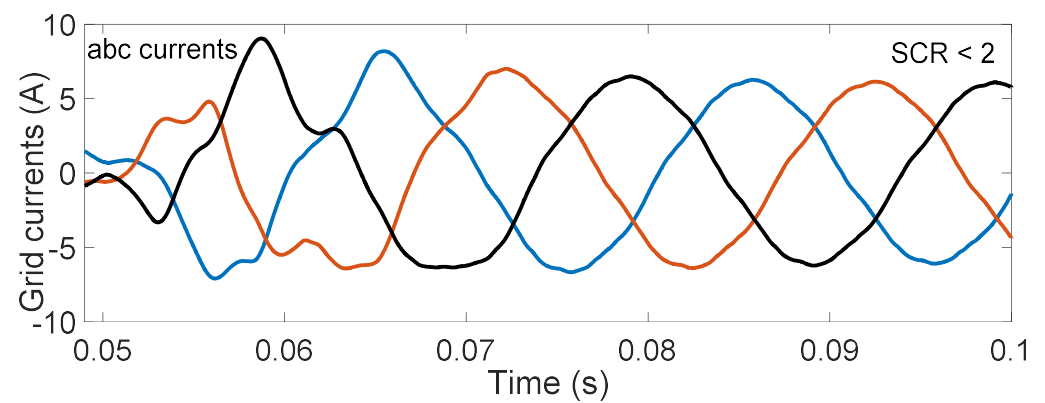


Figure 16. Grid current waveforms of the system with PI for SCR < 2.

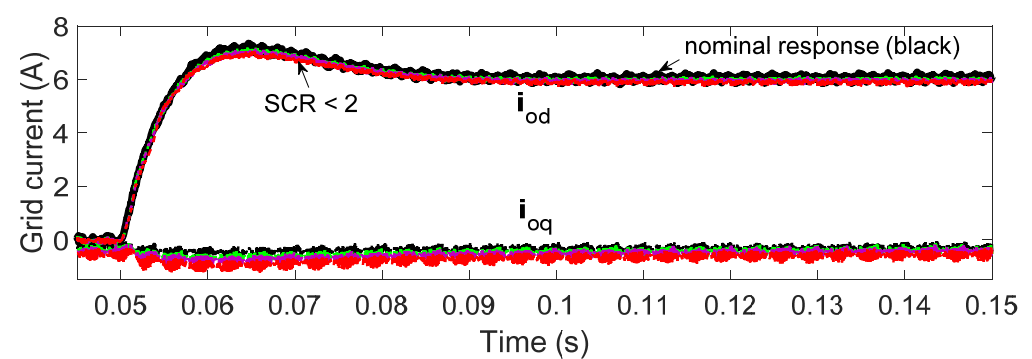


Figure 17. dq-grid currents of the system with RPI for SCR < 10.

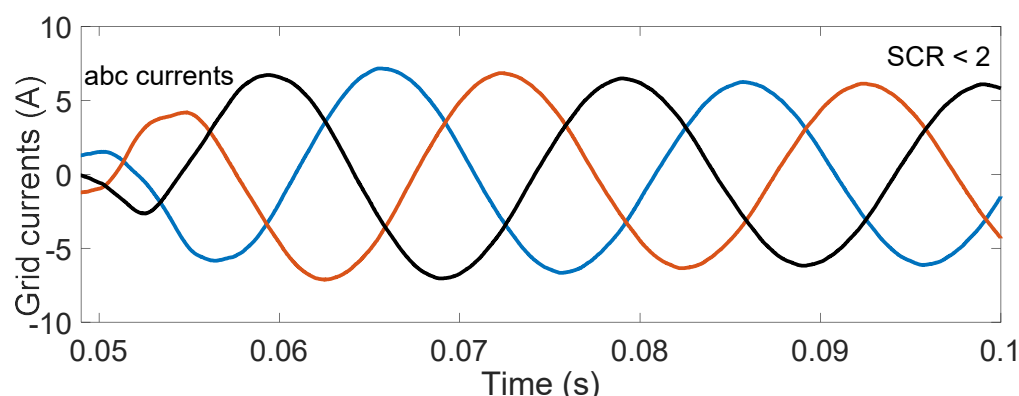


Figure 18. Grid current waveforms of the system with RPI for SCR < 2.

6. Conclusions

Fast frequency changes in low inertia grids will require a high BW PLL for virtual inertia response, and this requirement will degrade the stability margins of the inverter system should the SCR become low enough to create a strong PLL-grid impedance coupling. To address this problem, the design of a robust inner-loop current controller of a current fed grid-tie inverter system was investigated. It was shown that:

- While the regular loop-shaping method for tuning the inner-loop PI current controller is appropriate when the inverter-grid connection is strong (SCR > 10), it is inadequate in weak conditions (SCR < 3), even when the PLL-grid coupling dynamics are included in the loop transfer function.
- The proposed alternative solution, whereby the PLL-grid coupling was formulated as a single perturbation on the dynamics of the inverter system, allowed for easy translation of the problem into the H_∞ robust control framework. Adequate inverter dynamics in the presence of a strong PLL-grid impedance coupling can then be achieved by tuning the controller to minimize the H_∞ norm.
- The structured H_∞ method [30] can be applied to tune the inner-loop PI controller against the PLL-grid impedance coupling, thereby avoiding an H_∞ controller with higher order dynamics.

Nyquist analysis and simulations with a validated model of a current fed grid-tie inverter confirmed that the performance of the inverter system with the H_∞ tuned PI controller was improved in the weak grid case of SCR < 3 as compared to the system with a regularly tuned PI controller. As future research, it would be useful to investigate whether inverter harmonic stability can be incorporated, formulated, and resolved in a similar manner.

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Appendix A

$$\text{State vector } \mathbf{X}: \begin{bmatrix} \hat{\mathbf{i}}_{L1d} & \hat{\mathbf{i}}_{L1q} & \hat{\mathbf{i}}_{o_d} & \hat{\mathbf{i}}_{o_q} & \hat{\mathbf{v}}_{cf_d} & \hat{\mathbf{v}}_{cf_q} & \hat{\mathbf{v}}_{dc} \end{bmatrix}^T$$

System matrix **A**:

$$\begin{bmatrix} \frac{(-R_{L1}+R_{cd})}{L_1} & \omega_1 & \frac{R_{cd}}{L_1} & 0 & -\frac{1}{L_1} & 0 & \frac{D_d}{L_1} \\ -\omega_1 & \frac{(-R_{L1}+R_{cd})}{L_1} & 0 & \frac{R_{cd}}{L_1} & 0 & -\frac{1}{L_1} & \frac{D_q}{L_1} \\ \frac{R_{cd}}{L_2} & 0 & \frac{(-R_{L2}+R_{cd})}{L_2} & \omega_1 & -\frac{1}{L_2} & 0 & 0 \\ 0 & \frac{R_{cd}}{L_2} & -\omega_1 & \frac{(-R_{L2}+R_{cd})}{L_2} & 0 & \frac{1}{L_2} & 0 \\ \frac{1}{C_f} & 0 & -\frac{1}{C_f} & 0 & 0 & \omega_1 & 0 \\ 0 & \frac{1}{C_f} & 0 & -\frac{1}{C_f} & -\omega_1 & 0 & 0 \\ \frac{-3D_d}{2C} & \frac{-3D_q}{2C} & 0 & 0 & 0 & 0 & 0 \end{bmatrix}$$

Output matrix **C**:

$$\begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 1 \\ 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 \end{bmatrix}$$

Input vector **U**:

$$\begin{bmatrix} \hat{i}_{in} & \hat{v}_{pd} & \hat{v}_{pq} & \hat{D}_d & \hat{D}_q \end{bmatrix}^T$$

Input matrix **B**:

$$\begin{bmatrix} 0 & 0 & 0 & \frac{\hat{v}_{dc}}{L_1} & 0 \\ 0 & 0 & 0 & 0 & \frac{\hat{v}_{dc}}{L_1} \\ 0 & -\frac{1}{L_2} & 0 & 0 & 0 \\ 0 & 0 & -\frac{1}{L_2} & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ \frac{1}{C} & 0 & 0 & \frac{-3I_{L1d}}{2C} & \frac{-3I_{L1q}}{2C} \end{bmatrix}$$

Feedforward matrix **D** = 0.Output vector **Y**:

$$\begin{bmatrix} \hat{v}_{dc} & \hat{i}_{L1d} & \hat{i}_{L1q} & \hat{i}_{od} & \hat{i}_{oq} \end{bmatrix}^T$$

State-space representation:

$$\begin{bmatrix} \hat{v}_{dc} \\ \hat{i}_{L1d} \\ \hat{i}_{L1q} \end{bmatrix} = \mathbf{G} \begin{bmatrix} \hat{i}_{in} \\ \hat{v}_{pd} \\ \hat{D}_d \end{bmatrix}; \text{ with } \mathbf{G} = \begin{bmatrix} G_{i_{in}v_{dc}} & G_{v_{pd}v_{dc}} & G_{D_dv_{dc}} \\ G_{i_{in}i_{L1}} & G_{v_{pd}i_{L1}} & G_{D_d i_{L1}} \\ G_{i_{in}i_o} & -Y_{ol} & G_{D_d i_o} \end{bmatrix}$$

Closed-loop transfer functions with only the inner current-loop (*il*) closed: Output current,

$$\begin{aligned} \frac{\hat{i}_o}{\hat{i}_{in}} &= G_{i_{in}i_o}^{il} = G_{i_{in}i_o} - G_{Di_o}(I + L_c)^{-1}H_i G_{PWM} G_{cPI} G_{i_{in}i_{L1}} \\ \frac{\hat{i}_o}{\hat{v}_p} &= Y_o^{il} = Y_o - G_{Di_o}(I + L_c)^{-1} \left[(G_{ff} + G_{PLL}) + G_{PWM} G_{cPI} (Y_{PLL} - H_i G_{v_{pd}i_{L1}}) \right] \\ \frac{\hat{i}_o}{\hat{i}_{dref}} &= G_{i_{dref}i_o} = G_{Di_o}(I + L_c)^{-1} G_{PWM} G_{cPI} \end{aligned}$$

Closed-loop transfer functions with both inner current-and outer voltage-loop closed: dc-bus,

$$\begin{aligned} \frac{\hat{v}_{dc}}{\hat{i}_{in}} &= G_{i_{in}v_{dc}}^{cl} = (I + L_{in})^{-1} \left\{ G_{i_{in}v_{dc}} - G_{Di_{L1}}(I + L_c)^{-1} G_{PWM} G_{cPI} G_{i_{in}i_{L1}} \right\} \\ \frac{\hat{v}_{dc}}{\hat{v}_p} &= G_{v_{pd}v_{dc}}^{cl} = (I + L_{in})^{-1} \left\{ G_{v_{pd}v_{dc}} + G_{Di_{L1}}(I + L_c)^{-1} \left[(G_{ff} + G_{PLL}) \right. \right. \\ &\quad \left. \left. + G_{PWM} G_{cPI} (Y_{PLL} - H_i G_{v_{pd}i_{L1}}) \right] \right\} \\ \frac{\hat{v}_{dc}}{\hat{v}_{dcref}} &= G_{v_{dcref}v_{dc}}^{cl} = (I + L_{in})^{-1} \left\{ G_{Di_{L1}}(I + L_c)^{-1} G_{PWM} G_{cPI} \right\} G_{v_{pd}} \end{aligned}$$

Output current,

$$\begin{aligned} \frac{\hat{i}_o}{\hat{i}_{in}} &= G_{i_{in}i_o}^{cl} = G_{i_{in}i_o}^{il} - G_{i_{dref}i_o} G_{v_{pd}} H_v G_{i_{in}v_{dc}}^{cl} \\ \frac{\hat{i}_o}{\hat{v}_{dcref}} &= G_{v_{dcref}i_o}^{cl} = G_{i_{dref}i_o} G_{v_{pd}} - G_{i_{dref}i_o} G_{v_{pd}} H_v G_{v_{dcref}v_{dc}}^{cl} \end{aligned}$$

PLL transfer functions,

$$\begin{aligned} Y_{PLL} &= \begin{bmatrix} 0 & -H_{PLL} I_{oq} \\ 0 & H_{PLL} I_{od} \end{bmatrix} \\ G_{PLL} &= \begin{bmatrix} 0 & -H_{PLL} D_q \\ 0 & H_{PLL} D_d \end{bmatrix} \\ \text{with : } H_{PLL} &= \frac{K_{pPLL}s + K_{iPLL}}{s^2 + (K_{pPLL}s + K_{iPLL})V_{pd}} \end{aligned}$$

where: K_{pPLL} and K_{iPLL} are the gain values of the PLL PI controller; I_{od} ; I_{od} is the steady state dq-values of the output grid current; D_d and D_q are the steady state dq-values of the duty ratio. V_{pd} is the steady state d -value of the grid voltage.

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