

Article

Modular Multilevel Converter for Low-Voltage Ride-Through Support in AC Networks

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Abstract: New grid-connected systems have imposed additional requirements regarding reliability, power quality, high levels of power processing capacity, and fault support, where power converters have a crucial role in fulfilling these requirements. Overcoming one of these challenges, this paper proposes a new alternative application to improve the low-voltage ride-through (LVRT) support based on the arm impedance employment of the modular multilevel converter (MMC) by attenuating the fault impacts, avoiding overcurrents and overvoltages. This proposal does not require additional hardware or control loops for LVRT support, only using PI controllers. This paper evaluates symmetrical and asymmetrical grid fault impacts on the converter DC side of four converter topologies: two-level voltage source converter topology (2L-VSC), neutral point clamped (NPC), MMC, and 2L-VSC equipped with a DC-chopper, employing the same control structure for the four topologies, highlighting that the MMC contributed better to LVRT improvement under severe grid conditions.

Keywords: modular multilevel converter (MMC); fault support; low-voltage ride-through (LVRT); multilevel converters; grid-connected systems



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1. Introduction

The widespread penetration of grid-connected systems has provided high stability to the electrical grid, avoiding eventual load disconnections and unnecessary activation of protection systems [1]. Due to the manufacturing development of power electronic devices, converters achieved profound changes in their structures and control techniques, fulfilling several applications, among them LVRT support [2,3], which has made feasible the high penetration of grid-connected systems.

Major solutions adopted to provide enhanced support under LVRT conditions are based on physical devices such as protection relays, fuses, fault current limiters (FCLs), DC choppers, synchronous static compensators (STATCOMs), dynamic voltage restorers (DVRs), as well as modifications in the control loops [4,5]. Thus, in symmetrical and asymmetrical fault scenarios, these systems must have large fault support to mitigate or suppress overcurrents and overvoltages that may exceed the technical limits of devices, besides leading to a loss of control and stability [6].

Among traditional solutions for improving fault support, specific features of power converters can improve the system robustness through redundant stages, bringing blocking voltage capacity and supporting a high sudden current change di/dt rate. These characteristics make the multilevel converters an attractive solution [7]. The major multilevel converter topologies used at the industrial scale are: NPC [8], flying capacitors (FCs) [9], and cascaded H-bridges (CHBs) [10]. From a structural perspective, NPC is composed of clamping diodes to synthesize output voltage levels; the FC uses capacitors instead diodes; the CHB is composed of series-connected H-bridge cells with independent voltage sources. In the last ten years, with the evolution of CHBs, the MMC has become

a promising topology without the drawbacks of clamping diodes, flying capacitors, or independent voltage sources. In addition, its modular structure with easy expansiveness is suitable for high-power applications, such as HVDC systems, wind, and photovoltaic power conversion systems [11,12].

Low-voltage ride-through support under symmetrical and asymmetrical faults was discussed in [13]. A fourth leg is added to the three-phase 3L-NPC based on the flying capacitor, providing a fixed neutral voltage under normal operation and replacing the phase under fault condition by the fourth leg. In [14], a resilient framework for the MMC was proposed for voltage sag recovery against internal and external faults employing circulating arm currents and the capacitor voltage supervision algorithm with a modular multilevel capacitor-clamped DC/DC converter (MMCCC) inserted in each arm of the MMC. In [15], a positive/negative injection sequence droop control for microgrids was proposed, eliminating additional hardware use. The coordinated control employs a droop control with a virtual impedance loop and the positive/negative sequence droop scheme to coordinate power injection under grid faults.

In [16], a similar approach was presented by imposing a current injection limit during the fault, avoiding overcurrents and providing active power and reactive current injection without exceeding the maximum current peak of the grid-connected converter. In [17], a hybrid control-hardware strategy with a surplus active power energy storage scheme was proposed in the turbine generator mechanical system in a permanent magnet synchronous generator (PMSG) using a back-to-back NPC with a DC chopper, providing constant voltage under DC bus limits and avoiding the DC chopper activation in some cases. In [18], a DC bus adaptive control for a two-stage inverter in a photovoltaic system was proposed. The scheme controls the DC bus voltage to follow the grid voltage change, reducing high-frequency harmonics and providing an adequate DC bus voltage level under an LVRT.

The hardware-based strategies in [13,14] require the converter's structural modification, increasing the complexity of PWM signals and current and voltage control loops. Conversely, References [15,16] proposed ancillary service support based on coordinated control, a well-known solution with the drawback of control loop modifications. On the other hand, References [17,18] dealt with DC bus overvoltage using excess power dissipation and adaptive control, respectively. These last approaches also involve control reference modifications, being strongly dependent on the system parameters and the type of fault and requiring an excellent dynamic response from the controllers. Table 1 summarizes the aforementioned hardware- and control-based techniques for LVRT support.

Table 1. Summary of hardware- and control-based LVRT techniques.

Reference	Technique	Advantages	Drawbacks
[13]	Fourth leg addition to 3L-NPC-based flying capacitor.	Fixed neutral voltage under normal operation and phase replacement under LVRT.	Hardware addition; complex PWM and control loops.
[14]	Multilevel modular capacitor-clamped DC/DC converter (MMCCC); supervisory algorithm.	Postfault restoration scheme.	Hardware addition; complex control algorithm implementation; high implementation costs.
[15,16]	Positive/negative sequence droop control/ current injection.	Grid voltage support.	Complex two-layer hierarchical control implementation; control loop modification.
[17]	Surplus active power energy storage; DC chopper.	Avoids DC bus overvoltages under LVRT.	Hardware addition; control coordination requirement.
[18]	Adaptive DC bus voltage control.	High-frequency harmonics reduction; avoids DC bus overvoltages under LVRT.	Reference control loop modification; strongly dependent on the system parameters.

This paper aims to propose a new alternative application using the MMC for LVRT support improvement to overcome the hardware- and control-based strategies. Unlike the aforementioned state-of-the-art solutions, no additional hardware or control loop modification is required because the MMC arm impedance can use its fault-damping capability, reducing the overcurrents and overvoltages, besides maintaining controllability and protecting the power converter. Table 2 presents the major contributions of this paper's proposal.

Table 2. Summary of the proposed application for LVRT support.

Proposed Application	Advantages	Contributions
MMC for LVRT support.	No additional hardware; no complex control loops; avoids DC bus overvoltages under LVRT; avoids overcurrents under LVRT; easily expandable modular structure.	<ul style="list-style-type: none"> ✓ MMC arm impedance for overcurrent and overvoltage suppression under LVRT; ✓ avoids the protection activation; ✓ supports the grid connection under LVRT; ✓ maintains the controllability of the power converter.

Moreover, this standalone solution disregards the protection and controller response time, acting instantaneously under LVRT. This paper evaluated the performance of four-converter topologies under symmetrical and asymmetrical faults: 3L-MMC, 2L-VSC, 3L-NPC, and 2L-VSC equipped with a DC chopper.

2. Description of Converter Topologies

Figure 1 depicts the three-phase converter topologies 2L-VSC, 3L-NPC, and 3L-MMC implemented in this paper. A fourth configuration, 2L-VSC, equipped with a DC chopper was also implemented. The 2L-VSC is composed of six switches operating in a complementary fashion, synthesizing two output pole voltage levels: V_{bus} and zero, for V_{AO} , V_{BO} , and V_{CO} . However, the synthesized phase voltage levels V_{AN} , V_{BN} , and V_{CN} are: $\frac{-2V_{bus}}{3}$, $\frac{-V_{bus}}{3}$, 0 , $\frac{V_{bus}}{3}$, and $\frac{2V_{bus}}{3}$ [19]. The DC chopper used in the DC bus is described in this diagram, which is composed of a drive switch with a series-connected resistor. The chopper is activated under a grid fault condition when the DC bus overvoltage trigger level is reached, dissipating the surplus energy on the resistor [4]. In this paper, the DC chopper activation criterion adopted was 5% over the rated DC bus voltage.

The 3L-NPC topology is composed of four switches per phase, where S_1 and S_2 have their respective complementary switches \bar{S}_1 and \bar{S}_2 . Besides, the clamping diodes are connected to the DC bus midpoint, fixing the synthesized converter output voltage levels [8,20]. In this case, three pole voltage levels were synthesized: 0 , $\frac{V_{bus}}{2}$, and V_{bus} , while the phase voltages assumed nine voltage levels: $\frac{-4V_{bus}}{6}$, $\frac{-3V_{bus}}{6}$, $\frac{-2V_{bus}}{6}$, $\frac{-V_{bus}}{6}$, 0 , $\frac{V_{bus}}{6}$, $\frac{2V_{bus}}{6}$, $\frac{3V_{bus}}{6}$, and $\frac{4V_{bus}}{6}$.

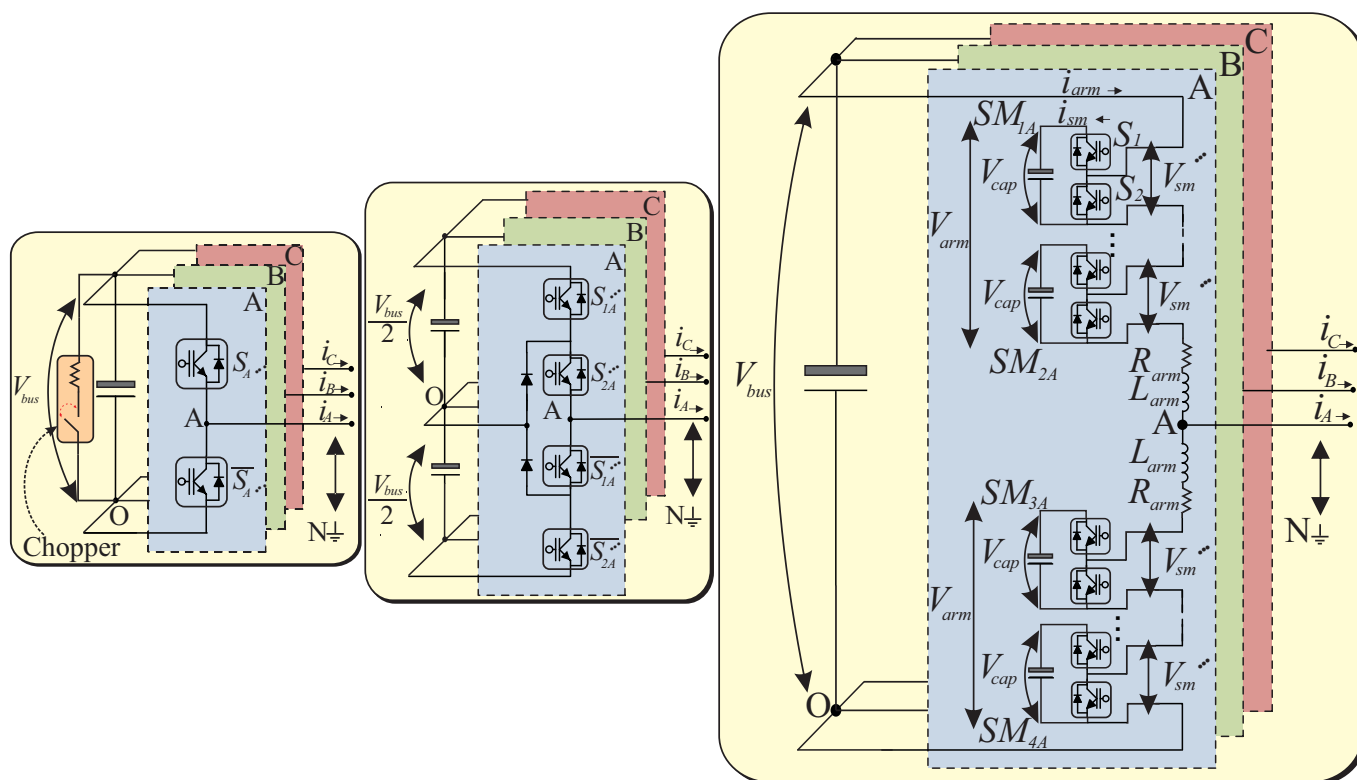


Figure 1. Three-phase converter topologies: 2L-VSC, 3L-NPC, and 3L-MMC.

The 3L-MMC topology is composed of series-connected half-bridge submodules, where each submodule has two switches (S_1 and S_2) and one capacitor C_{SM} . In addition, each arm has a series R-L (R_{arm} and L_{arm}) impedance equally distributed among the converter phases [11,12]. Table 3 summarizes the main differences between the three presented topologies.

Table 3. Comparative summary between the VSC, NPC, and MMC for any level.

Criterion	VSC	NPC	MMC
Clamping diodes	0	$(N - 1)(N - 2)$	0
Number of switches	6	$6(N - 1)$	$12(N - 1)$
Capacitors	DC bus	$(N - 1)$	$6(N - 1)+1$
Switch blocking voltage	V_{bus}	$\frac{V_{bus}}{(N-1)}$	$\frac{V_{bus}}{(N-1)}$
Modularity	No	No	Yes
Voltage balancing	No	DC bus	Per submodule
Redundancy	No	No	Yes

The synthesized voltage levels for the 3L-MMC are three pole voltage levels and nine phase voltage levels, such as in the 3L-NPC. According to the state of the MMC submodule switches, the capacitor is inserted or bypassed. Thus, the voltage of each submodule V_{SM} that synthesizes the output voltage levels can be described by a switching function as follows:

- If $S_1 = 1$ and $S_2 = 0$, $V_{SM} = V_{cap}$;
- If $S_1 = 0$ and $S_2 = 1$, $V_{SM} = 0$;
- Else $V_{SM} = 0$.

The average capacitor voltage of each submodule is given by:

$$V_{cap} = \frac{V_{bus}}{N_{SM}}, \quad (1)$$

where N_{SM} is the number of submodules per arm in which the number of output voltage levels is given by $(N_{SM} + 1)$. Each arm in the MMC is equivalent to a controlled voltage source V_{arm} with the instantaneous voltage amplitude given by:

$$V_{arm} = \frac{SM_{active} V_{bus}}{N}, \quad (2)$$

where SM_{active} and N are the number of active submodules and the number of converter levels, respectively. Considering that V_{SM} is the submodule voltage, V_{arm} and therefore the MMC voltage levels are given as a function of the sum of the submodule voltages and the voltage drop across R_{arm} and L_{arm} ; thus:

$$V_{arm} = \sum_{n=0}^{SM_{active}} (V_{SM}) + L_{arm} \frac{di_{arm}}{dt} + R_{arm} i_{arm}. \quad (3)$$

The sinusoidal pulse width modulation (SPWM) technique based on triangular carriers compared to the three-phase reference voltages generates the trigger signals for the 2L-VSC switches [21]. The topologies 3L-NPC and 3L-MMC use the phase disposition pulse width modulation (PDPWM) technique, which is based on triangular level-shifted carriers, where the number of carriers N_{tri} is given by $(N - 1)$ [22]. The MMC topology requires a voltage classification algorithm for capacitor insertion based on the number of active submodules providing voltage equalization, depicted in Figure 2.

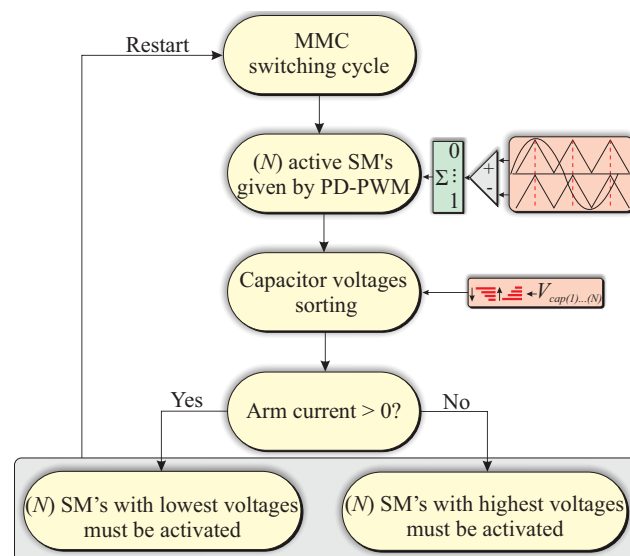


Figure 2. MMC capacitor voltage balancing algorithm.

3. The Proposed Application

The proposed application considers the damping characteristic of the MMC circuit. Unlike other topologies, the representative circuit per phase of the MMC can be described by a series RLC circuit, where the capacitance is variable and given by the time-varying active submodules. Thus, the damping is derived from $v(t) = L \frac{di(t)}{dt}$ and $i(t) = C \frac{dv(t)}{dt}$, which are the basic L-C voltage–current relations, respectively. In this case, these relations indicate opposition to sudden current and voltage variations since they are state variables that cannot vary instantaneously [4]. In terms of the RLC second-order circuit and considering C_{SMinst} as the total active submodule instantaneous capacitance, Equation (2) can be rewritten as:

$$V_{arm} = \frac{1}{C_{SMinst}} \int_t i_{arm} dt + L_{arm} \frac{di_{arm}}{dt} + R_{arm} i_{arm}. \quad (4)$$

This means that this characteristic is critical to avoid high levels of overcurrents and overvoltages under LVRT conditions. Thus, the network terminals see the MMC as a dampened circuit [23], as depicted in Figure 3.

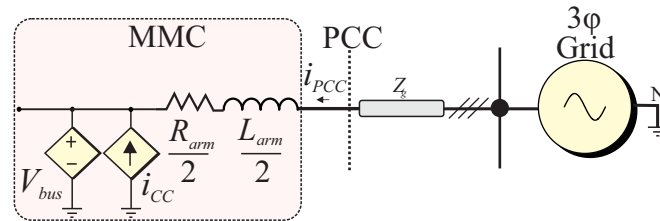


Figure 3. MMC per phase average circuit.

In Figure 3, V_{bus} and i_{CC} are the DC bus voltage and the MMC arm current, respectively, controlled by the control scheme depicted in Figure 4.

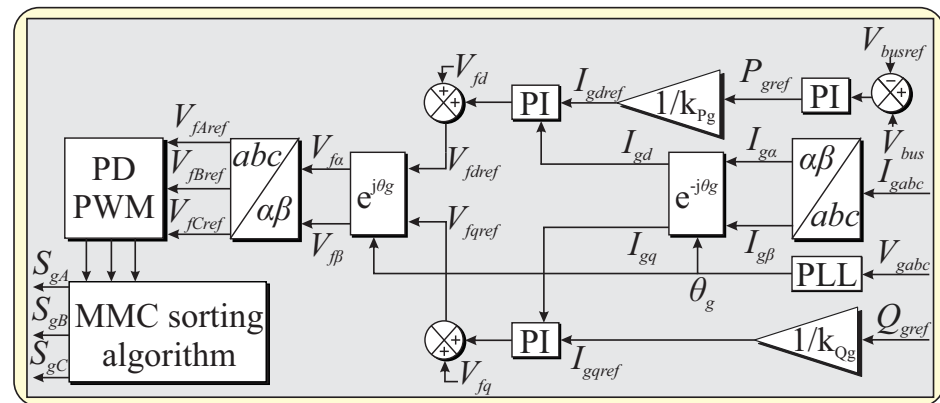


Figure 4. MMC control scheme.

The MMC control scheme (Figure 4) is based on vector control in synchronous reference frame $dq0$, in which the DC bus voltage, V_{bus} , is controlled by an outer PI controller generating the active power reference, P_{gref} , by means of I_{gdref} . Another controller is responsible for the reactive power, Q_{gref} , by means of I_{gqref} ; this reference was adopted as zero, which indicates that there is no reactive power delivered to the grid.

On the other hand, the currents measured at the PCC were transformed to the $dq0$ reference using the Clarke and Park transforms, thus generating the I_{gd} and I_{gq} that were applied to the inner controllers; these controllers provide the grid reference voltages by means of V_{fdref} and V_{fqref} , used in the Park inverse transform to generate the trigger signals by means of the PWM. A PLL was used for the grid synchronization, providing the angle, θ_g , used in Park direct and inverse transforms.

The PDPWM technique provides the number of active submodules by means of a comparison of the reference voltages, V_{fAref} , V_{fBref} , and V_{fCref} , between two level-shifted triangular carriers in phase with each other. To equalize the MMC submodules capacitor voltages, the voltage balancing algorithm was employed as depicted in Figure 2; the algorithm was based on the MMC upper and lower arms' current direction, in which the number of active submodules is given by the PDPWM and used in the algorithm to determine which submodule should be inserted or bypassed. If the arm current is positive, the N submodules with the lowest voltages must be activated; conversely, if the arm current is negative, the N submodules with the highest voltages must be activated. Finally, after determining the active submodules, the trigger signals are sent to the converter.

The selection criterion of the L_{arm} and C_{SM} parameters used in this paper can be obtained based on the procedure presented in [11,24]. R_{arm} was adopted using typical commercial values based on the resistance per length of the wire used in making the MMC arm reactor; for simplicity, this paper adopted the R_{arm} , L_{arm} , and C_{SM} parameters according to Table 4. Furthermore, the selection of L_{arm} and C_{SM} has different objectives such as to reduce the voltage ripple across the submodules' capacitors, suppress the MMC circulating current, and the damping of the fault current rise rate in HVDC systems, as discussed in [24,25]. The MMC application in LVRT support additionally allows the arm impedance parameters' adjustment, submodule capacitance, and the increase of the number of levels, improving the overcurrents' and overvoltages' reduction for a wide range of power levels.

Table 4. System parameters.

Parameter	Value
Grid voltage	380 V
Grid frequency	60 Hz
DC bus voltage	600 V
DC capacitor	2000 μ F
Switching frequency	5 kHz
MMC arm resistance (R_{arm})	0.5 Ω
MMC arm inductance (L_{arm})	5 mH
MMC submodule capacitance (C_{SM})	1000 μ F
Grid line resistance (R_g)	0.487 Ω
Grid line inductance (L_g)	4.2 mH
Capacitor bank filter (C_b)	380 μ F
Converter filter resistance (R_f)	0.4 Ω
Converter filter inductance (L_f)	15 mH
Fault resistance (R_{fault})	1 m Ω
Fault inductance (L_{fault})	0.1 mH

4. Performance Assessment

Figure 5 depicts the background of the implemented scenario, composed of a grid-connected converter with a generic distributed generation system represented by a precharged DC bus capacitor C_{bus} . This system is connected to the three-phase network represented by an infinite bus with a line impedance Z_g .

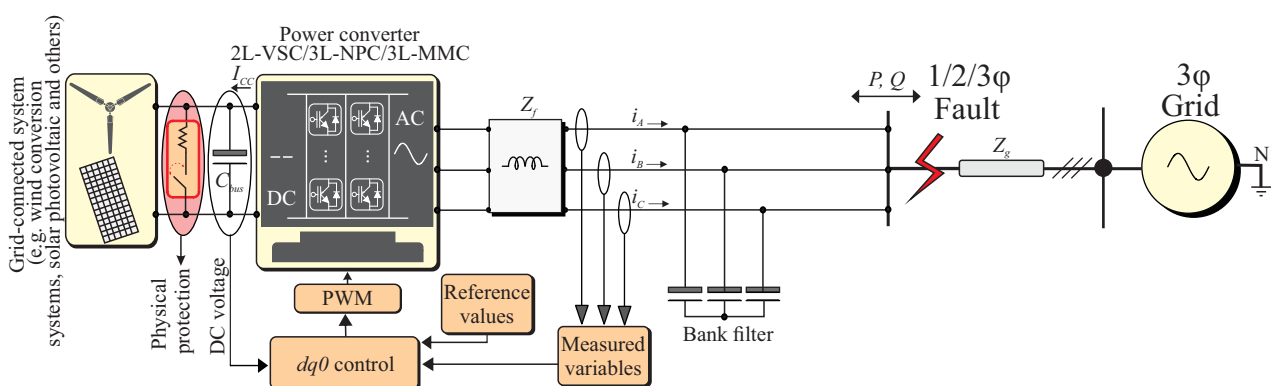


Figure 5. Implemented system background.

The MMC for LVRT support was demonstrated in scenarios with symmetric and asymmetric faults: single line-to-ground (SLG), double line-to-ground (DLG), line-to-line (LL), and three-phase (LLL) with a 125 ms duration. Table 4 presents the parameters of

the implemented system and LVRT scenarios. For the performance assessment, the same control structure was used in the four converter topologies, ensuring a reliable comparison.

Figure 6 depicts the results obtained for the 2L-VSC and 2L-VSC with the DC chopper, 3L-NPC, and 3L-MMC, which are addressed in the remainder of this section.

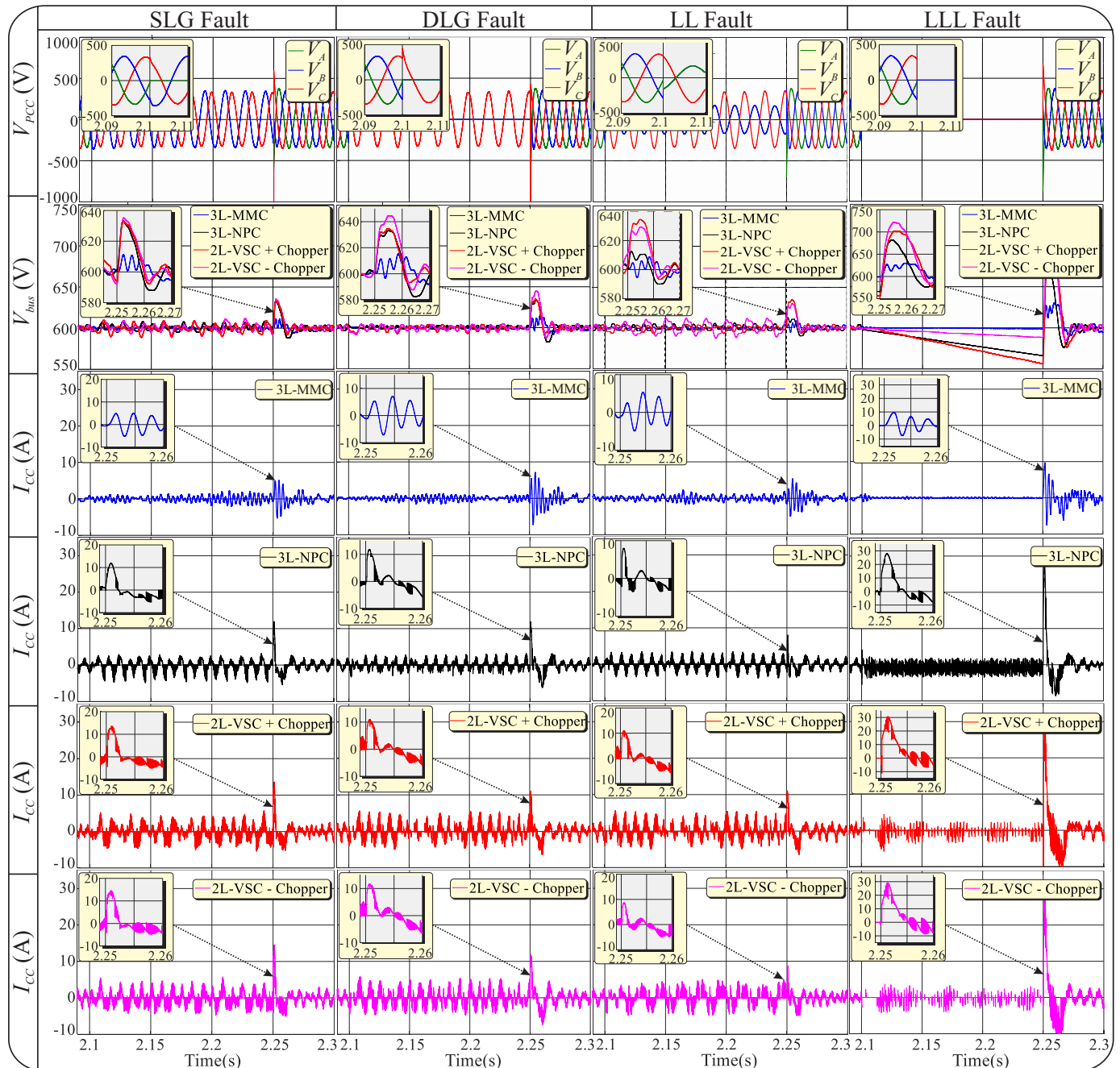


Figure 6. Obtained results for the 2L-VSC, 3L-NPC, and 3L-MMC for the SLG, DLG, LL, and LLL faults.

4.1. 2L-VSC in the LVRT Scenario

The 2L-VSC without the DC chopper presented the following performance (Figure 6):

- SLG fault: The control maintained V_{bus} within the reference values during the fault period. However, when the PCC voltage returned to the prefault values, an overvoltage occurred: V_{bus} reached approximately 637 V, which was an increase of 6.16% compared to the steady-state value, while the DC current (I_{cc}) reached approximately 15 A, representing about four-times the steady-state current;

- DLG fault: V_{bus} reached a maximum of approximately 641 V, representing an increase of 6.83%, while I_{CC} presented a similar behavior to the LG fault scenario;
- LL fault: V_{bus} reached a maximum of approximately 635 V, which was an increase of 5.83% compared to the steady-state value, while I_{CC} reached approximately 9.5 A, representing about 2.53-times the steady-state current;
- LLL fault: For the worst-case scenario, V_{bus} reached a maximum of 720 V, representing an overvoltage level of 20%, while I_{CC} reached 30 A, being more than nine-times the steady-state. The obtained results demonstrated that the 2L-VSC has a lower LVRT support, resulting in a higher possibility of damaging several system components during a severe grid fault.

The 2L-VSC with the DC chopper presented the following performance (Figure 6):

- SLG fault: Around the fault's initiation, the control maintained V_{bus} at the reference value. When V_{PCC} reestablished its prefault voltage, an overvoltage 5% lower than without the DC chopper occurred. Conversely, I_{CC} reached a maximum value of approximately 12 A with a reduction of 20% compared to the 2L-VSC without the chopper;
- DLG fault: V_{bus} reached a maximum value of 635 V, while I_{CC} reached a peak of 10.2 A, representing a reduction of 9.36% and 7.27% compared to the case without the DC chopper, respectively;
- LL fault: V_{bus} reached a maximum value of 637 V, while I_{CC} reached a peak of 10.5 A, representing a V_{bus} increase of 0.31%, while I_{CC} increased 10.52% compared to the previous case;
- LLL fault: V_{bus} reached a maximum of 700 V, while I_{CC} reached a maximum of 30.5 A. There was a reduction of V_{bus} compared to the previous case of 2.83%. Conversely, I_{CC} obtained an increase of 3.33%.

4.2. 3L-NPC in the LVRT Scenario

The 3L-NPC presented the following performance (Figure 6):

- SLG fault: Similar to the previous cases, the control maintained V_{bus} within the reference value, reaching a maximum of 633 V when V_{PCC} started to recover to the prefault condition, while I_{CC} reached a peak of 11 A. The 3L-NPC obtained a performance similar to the 2L-VSC without the DC chopper;
- DLG fault: The 3L-NPC achieved similar performance to 2L-VSC with the chopper, with V_{bus} reaching a maximum value of 632 V, while I_{CC} reached a peak of 11 A;
- LL fault: V_{bus} reached a maximum value of 615 V, while I_{CC} reached a peak of 9 A;
- LLL fault: The 3L-NPC obtained superior performance compared to 2L-VSC with and without the chopper, with V_{bus} reaching a maximum of approximately 675 V and I_{CC} reaching a peak of 28.7 A, representing a reduction of 6.25% and 3.33% compared to the 2L-VSC without the chopper, respectively, as well as 3.57% and 1.03% compared to the 2L-VSC with the chopper, respectively.

4.3. 3L-MMC in LVRT Scenario

The 3L-MMC presented the following performance (Figure 6):

- SLG fault: The control maintained V_{bus} within the reference value at the fault occurrence. When V_{PCC} recovered to the prefault voltage levels, V_{bus} reached a maximum value of 615 V, while I_{CC} reached a peak of 5 A. Compared to the steady-state value, V_{bus} and I_{CC} increased 2.5% and approximately 1.5-times, respectively. However, the 3L-MMC presented the best performance, reducing by approximately 42.85% the overvoltage level and 50% the overcurrent level compared to the 2L-VSC with and without the DC chopper and the 3L-NPC;
- DLG fault: V_{bus} reached a maximum of 617 V, while I_{CC} reached a maximum of 8 A, representing an increase of 2.83- and 2.28-times the steady-state value, respectively;

- LL fault: V_{bus} reached a maximum of 612 V, while I_{CC} reached a maximum of 5.2 A, representing a V_{bus} decrease of 0.48%, while I_{CC} decreased 41.11% compared to the 3L-NPC topology;
- LLL fault: The 3L-MMC obtained for V_{bus} a maximum of 625 V and for I_{CC} a peak of 10 A, representing an increase of 4.16% and 2.85-times the steady-state value, respectively. However, the 3L-MMC provided a reduction of the overvoltage and overcurrent level of 4.8-times and 3-times, respectively, compared to the 2L-VSC without the chopper. Regarding the 2L-VSC with the chopper, there was a reduction of four- and three-times V_{bus} and I_{CC} , respectively, besides three-times for 3L-NPC in both cases.

4.4. Comparison of the 2L-VSC, 3L-NPC, and 3L-MMC under LVRT Scenarios

Based on the obtained results, the use of the DC chopper in the 2L-VSC as a physical protection provided a slight improvement in all fault scenarios. Nevertheless, the support requirement during a voltage sag was effectively achieved using the 3L-MMC, which presented the best performance among all the topologies, reducing the overvoltage and overcurrent levels about 50% and four-times lower than the steady-state values, respectively, considering the worst-case without the DC chopper.

Moreover, even with the chopper activation and the use of the 3L-NPC, no meaningful contribution was verified to improve low-voltage ride-through support. On the other hand, the MMC structure provided the best transient response during the three fault scenarios, indicating that the structure composed of the submodules with capacitor voltage equalization provided considerable robustness and reliability to the grid-connected system, avoiding the harmful effects during a severe network voltage sag in the system components. In addition, based on the DC chopper threshold activation of 5% over the rated DC bus voltage $V_{bus} > 630$ V, in any fault scenario, the MMC would not activate the protection. Table 5 presents the performance assessment heat map highlighting the best performance of the MMC in all fault scenarios.

Table 5. Performance assessment heat map.

Topology	V_{bus} Peak (V)				I_{CC} Peak (A)			
	SLG	DLG	LL	LLL	SLG	DLG	LL	LLL
2L-VSC	637	641	635	720	15	15.1	9.5	30
2L-VSC+DC chopper	615	635	637	700	12	10.2	10.5	30.5
3L-NPC	633	632	615	675	11	11	9	28.7
3L-MMC	615	617	612	625	5	8	5.2	10

5. Conclusions

This paper presented a new application proposal to improve the low-voltage ride-through in grid-connected systems based on the modular multilevel converter impedance fault current damping capability. Comparisons to the two-level converter with the DC chopper and the neutral point clamped converter employing the same control loops indicated the better performance of modular multilevel converters for symmetrical and asymmetrical faults.

The study also demonstrated that a modular multilevel converter structure can mitigate the activation of physical protection under severe network faults, not only suppressing overvoltages and overcurrents, but also contributing effectively to increasing the robustness and control transient dynamic response, avoiding the hardware requirement or complex control loops' implementation. In particular, this proposal can be extended to systems with higher low-voltage ride-through susceptibility, effectively contributing to meeting international grid codes, such as: wind energy conversion systems based on doubly fed induction generators, squirrel cage induction generators, and permanent-magnet synchronous generators. Therefore, the modular multilevel converter can be an alternative solution in grid-connected systems for low-voltage ride-through support improvement.

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