




Review

Multilevel Inverter: A Survey on Classical and Advanced Topologies, Control Schemes, Applications to Power System and Future Prospects

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Abstract: In recent years, multilevel inverters (MLIs) have emerged to be the most empowered power transformation technology for numerous operations such as renewable energy resources (RERs), flexible AC transmission systems (FACTS), electric motor drives, etc. MLI has gained popularity in medium- to high-power operations because of numerous merits such as minimum harmonic contents, less dissipation of power from power electronic switches, and less electromagnetic interference (EMI) at the receiving end. The MLI possesses many essential advantages in comparison to a conventional two-level inverter, such as voltage profile enhancement, increased efficiency of the overall system, the capability of high-quality output generation with the reduced switching frequency, decreased total harmonic distortions (THD) without reducing the power of the inverter and use of very low ratings of the device. Although classical MLIs find their use in various vital key areas, newer MLI configurations have an expanding concern to the limited count of power electronic devices, gate drivers, and isolated DC sources. In this review article, an attempt has been made to focus on various aspects of MLIs such as different configurations, modulation techniques, the concept of new reduced switch count MLI topologies, applications regarding interface with renewable energy, motor drives, and FACTS controller. Further, deep insights for future prospective towards hassle-free addition of MLI technology towards more enhanced application for various fields of the power system have also been discussed. This article is believed to be extremely helpful for academics, researchers, and industrialists working in the direction of MLI technology.

Keywords: flexible AC transmission systems (FACTS); multilevel inverter (MLI); renewable energy resource (RER); selective harmonic elimination (SHE); space vector control (SVC); total harmonic distortions (THD)



Citation: Choudhury, S.; Bajaj, M.; Dash, T.; Kamel, S.; Jurado, F. Multilevel Inverter: A Survey on Classical and Advanced Topologies, Control Schemes, Applications to Power System and Future Prospects. *Energies* **2021**, *14*, 5773. <https://doi.org/10.3390/en14185773>

Academic Editor: Ching-Ming Lai

Received: 19 July 2021

Accepted: 7 September 2021

Published: 13 September 2021

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1. Introduction

Recently, the MLI has been regarded as state of the art technology for power conversion from DC to AC in the fields of generation, transmission, distribution, and employment of electrical energy. They have been innovated as a competent solution for wide range of power applications such as RER [1–6], FACTS [7–10], high-voltage direct current (HVDC) [11–14], static compensators (STATCOMs) [15–18], unified power flow controllers (UPFCs) [19–21], dynamic voltage restorers (DVRs) [22,23], active filters (AFs) [24,25], motor drives used for traction/transportation [26–33], marine propulsion [34–38], conveyors [39,40], mine hoists [41], magnetic resonance imaging system (MRI) [42] and induction heating power supply [43]. The conventional two-level inverters fail to operate in the

medium voltage range due to the semiconductor's blockage voltage limitation. However, MLIs play a key role in medium-voltage and high-power operations.

Further, for the same power ratings, MLIs have merit over a two-level inverter in terms of reduced harmonic contents of line-to-line voltage that are fed to load with respect to its level of switching frequencies [44]. The primary reasons behind the MLI serving as a vital revolution in the era of industrialization for potent performance are as follows: (i) compatible in design; (ii) capability of operating at higher current and voltage due to its modular structure; (iii) lesser voltage derivatives on power electronic switches as the voltage stress gets divided across the switches at various levels; (iv) easy interface with RER and motor drives where the load sharing is brought about by DC link; (v) enhanced power quality performance with low harmonic content and better electromagnetic compatibility; (vi) produces lower common-mode voltage; (vii) ability of transformer-less operation; (viii) enhanced efficiency level due to switching at fundamental frequency thus decreasing losses due to conduction and switching; (ix) draws input current with fewer distortions and (x) uses various control approaches and reduced switching states for achieving fault-tolerant operation. Table 1 highlights the primary differences between a traditional two-level inverter and the MLI.

Table 1. Comparison between traditional two-level inverter and MLI.

Properties	Two-Level Inverter	MLI
Structure	Complicated	Modular
Operation at high voltage and current stress on power electronic switches	Can operate (for parallelized structures) More	Can operate Less
Application	Low voltage	High voltage
Power quality performance	Low	High
Harmonic content	Low	High
Electromagnetic interference (EMI) Immunity/susceptibility	Less	More
Production of common-mode voltage	Higher	Lower
Ability of transformer-less operation	No	Yes
Efficiency	Low	High
Switching losses	High	Low
Operation at the fundamental frequency	Fails	Can operate
Input current distortions	High	Low
Fault tolerant operation	Impossible	Possible
Rate of change of voltage	High	Low
Ability to operate at low/high/fundamental frequency	More	Less
Production of multiple voltage level	Not possible	Possible
Electromagnetic interference (EMI) generation	High	Low

The basic principle behind MLI is that it consists of one or more DC sources and an array of low-rated power semiconductor switches for generating an output voltage with a stepped voltage waveform to achieve higher power levels [45,46]. The main objective of MLI is to synthesize an approximately sine wave of voltage with various steps by using the appropriate switching signal of the power electronic switches with the help of different direct current voltage sources such as batteries, supercapacitors, fuel cells, solar panels, etc. [47]. The number of levels of the output waveform can be increased for attaining pure sinusoidal voltage without the use of heavy transformers and passive filters [47,48]. The most traditional MLI topologies, according to their structure, are classified into three types (i) neutral point clamped (NPC); (ii) flying capacitor (FC), and (iii) cascaded H-bridge (CHB) [49]. The three-level NPC type of MLI is widely used in the application of motor drive. The FC type of MLI uses balancing capacitors on phase buses to generate multilevel output voltage waves clamped by capacitors instead of diodes. The CHB is extensively

used as it's more flexible due to its modular configuration and uses the least number of semiconductor switches for a particular level of operation. It generally comprises an array of H-bridge cells for synthesizing a required voltage from numerous isolated DC sources [50]. However, the classical MLIs undergo a crucial shortcoming: the increase in the count of driving circuits and devices in proportion to the number of levels makes the control circuit very complicated. The increased number of device components, in turn, reduces the overall stability of the system. Consequently, many authors have investigated new configurations intending to optimize the utilization of components and enhance the output voltage waveform [51].

Amongst the different topologies developed are the cascaded H-bridge, hybrid series and parallel sources (HSPSs), criss-cross, packed-U cells, and cascaded-bipolar switched cells have been reported by many researchers and have acquired worldwide consideration. Authors in [49] have researched the classical Voltage Source Inverter (VSI) development for the MLI application. Consequently, the research has been expanded to investigate the performance of numerous control approaches to improve the operation of MLIs and optimize their performance with various topologies. The modulation methods in MLIs have been endorsed by their range of switching frequencies. Nevertheless, the high-frequency modulation methods are restricted in the medium voltage range because the losses incurred during switching reduce the inverter component values and the system's overall efficiency.

The SPWM approach is implemented in industrial applications to lower the harmonic content on the output voltage waveform. Space vector modulation (SVM) technique possesses remarkable performance in 3-level MLI topologies. Other techniques involving modulation methods at a low switching frequency that have attained more demand in a broader field of function are Staircase modulation, space vector control (SVC), and selective harmonic elimination (SHE) [39]. A detailed study of these techniques has been discussed further in this article. Figure 1 illustrates the summary of the review methodology adopted in the present research work.

The significant contributions of this research paper include:

- (1) More than 260 recent research articles have been critically reviewed, and a detailed literature summary about the evolution, classification of the MLI topologies, various modulation techniques, and application have been presented.
- (2) A detailed discussion concerning the various types of conventional MLI techniques has been carried out.
- (3) An extensive valuation of a wide range of possible new reduced switch count MLI topologies has been explored and presented in-depth.
- (4) A clear idea of the different modulation techniques required for MLI has been apprehended.
- (5) Further, this research paper also highlights a thorough knowledge of MLI novel applications in various fields of power system networks such as renewable energy interface, FACTS controller, and motor drives based on a comprehensive research survey.
- (6) Finally, this article also elaborately discusses the issues faced by the present MLI technology and suggests some more in-depth vital points to be adopted in the future for further better application in the electric power grid network.
- (7) This comprehensive article is alleged to serve as a good guidance for enhancing the understanding of readers, academics, and industrialists for researching in the area of MLI concerning the proper choice of topology for definite application, accurate selection of parameters, switching, control schemes, and application in other power system fields.

The entire research article is structured into seven major sections. Section 2 addresses the development of MLI Topologies. A thorough classification of MLI topologies in terms of classical versus new reduced switch count topology and single versus multiple DC sources is projected in Section 3. Section 4 represents the detailed categorization of various modulation schemes depending upon the switching frequency. The novel applications of MLI after a rigorous survey of literature on MLI are highlighted in Section 5. The key

points to be dealt with seriously for further enhancement in MLI technology in the future have been meticulously discussed in the Section 6. Finally, the conclusion from the entire study is presented in Section 7.

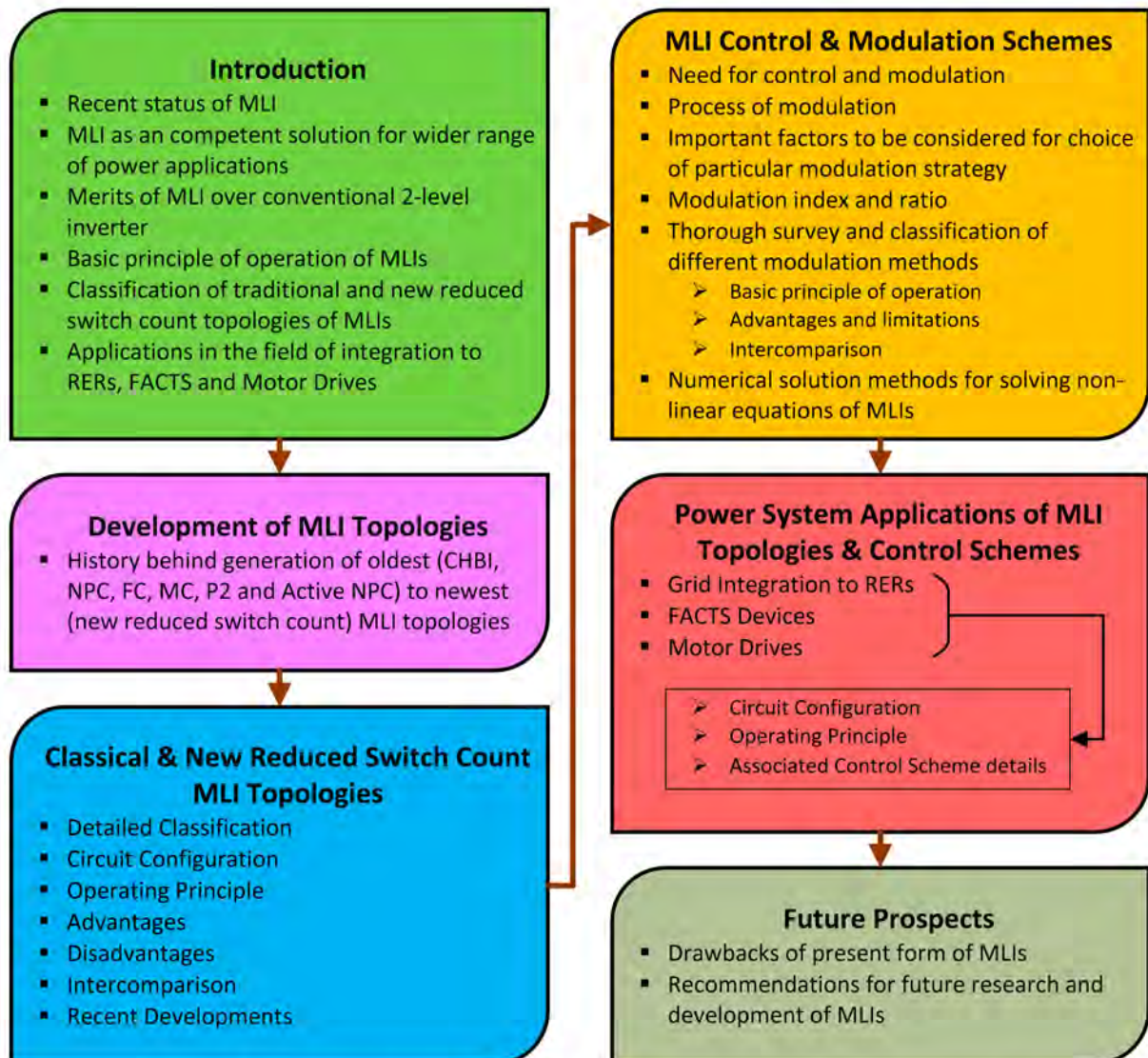


Figure 1. A summary of the review methodology adopted in the present research work.

2. Development of MLI Topologies

An outlook on the development of various topologies of MLI is depicted in Figure 2. A thorough study of this evolution has been discussed in this section. CHB was first developed by Baker and Bannister [52] in the 1970s, which possessed the capability of generating multilevel voltage using different DC source voltage [53–55]. The next advancement in MLI topology was the NPC inverter, first evolved by Nabae et al. [56] in the 1980s [57–59]. In the 1990s, Meynard and Foch [60] and Lavieville et al. [61] developed the FC type of MLI. These three classical types of MLI-based topologies were regarded as the foundation of most MLI inverters presented in the modern era. The next invention was the modular multilevel converter (MMC), primarily applied in industrialization [62,63]. In 2000 [64], a generalized MLI named P2 was introduced. Authors in [65] have proposed active neutral point clamped (ANPC) topology. Many other new MLI configurations with application-based approaches have been proposed and conferred in the recent past. Authors have also focused on developing a new reduced switch count topology of MLI [66,67]. The new topology of

MLI can be categorized as (i) symmetric type based on the use of equal DC sources [68–80]; (ii) asymmetric type based on the use of unequal DC sources [69,70,81–85]; (iii) having inherent negative level [68–70,81–85]; (iv) without inherent negative level [72–80]; (v) use of capacitors links with single sources [81–86]; (vi) regenerative configuration for operation as both an inverter and a rectifier [73–75] and (vii) hybrid approach of NPC, FC and CHB [84–87].

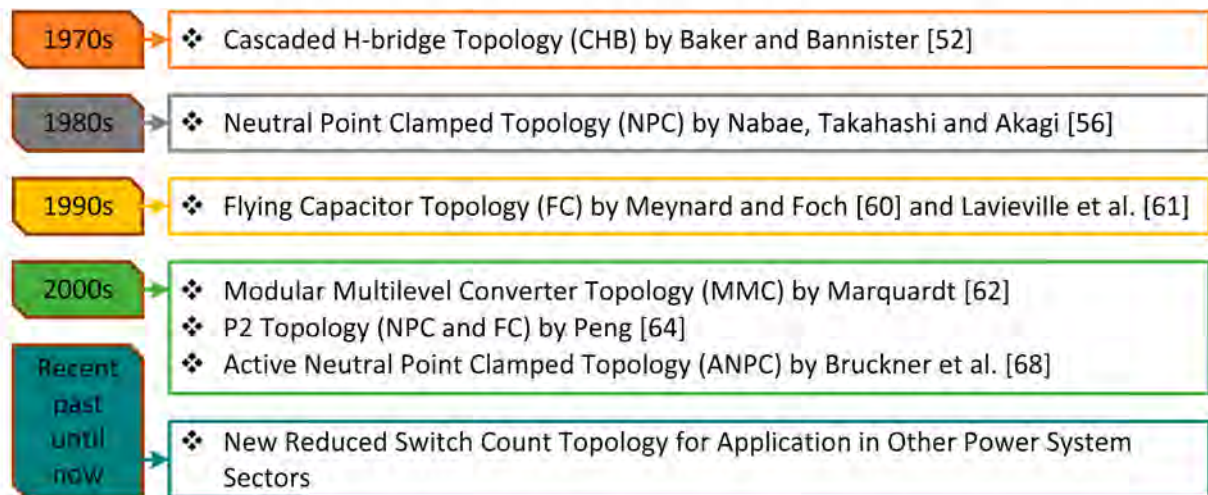


Figure 2. An outlook on the development of various MLI topologies.

3. Classical and New Reduced Switch Count MLI Topologies

The concept of MLIs was first introduced in 1975 [52] and then pursued by combative work to develop numerous topologies based on modifying the configuration regarding arrangements of power electronic semiconductor switches and DC sources. Research was also conducted to achieve greater power by the series combination of switches using DC sources with a small voltage range to convert power and synthesize voltage. The most frequently used voltage sources which could be configured in one (single) and more (multiple) units are RER, batteries, and capacitors. The broad categorization of MLI on several DC sources used and their structure is given in Figure 3. In addition, a comprehensive survey of the literature yields various classifications of MLI based on different strategies as suggested by many researchers.

Nevertheless, this research article is an attempt to broadly classify all possible types of MLIs depending upon the structure of DC source (either single or multiple units) used. The multiple uses of capacitors can produce multiple voltage levels. Table 2 summarizes the significant advantages and disadvantages of various MLI configurations.

3.1. Single DC Source

This type of topology is extensively endorsed in the industrial field, considering its simple structure, high efficiency, and power rendering [88]. The different categories of MLIs using a single DC source are discussed below [89].

3.1.1. Neutral Point Clamped Multilevel Inverter (NPC-MLI)

Nabae, Takashi, and Akagi in 1981 proposed the diode clamped multilevel inverter (DC-MLI), also termed NPC-MLI [56]. These inverters have been broadly adopted on account of their immense proficiency in high-power and medium-voltage operations with comparatively high efficiency. It is a three-level structure with two diodes that clamp the switching voltage to half the supply voltage magnitude. Further, it guarantees equal sharing of the supply voltage among the two halves of the switches being held at these points consisting of a neutral point between them. The middle voltage level is termed

the neutral point. This topology employs multiple capacitor banks in series for providing multiple DC voltage levels, as illustrated in Figure 4.

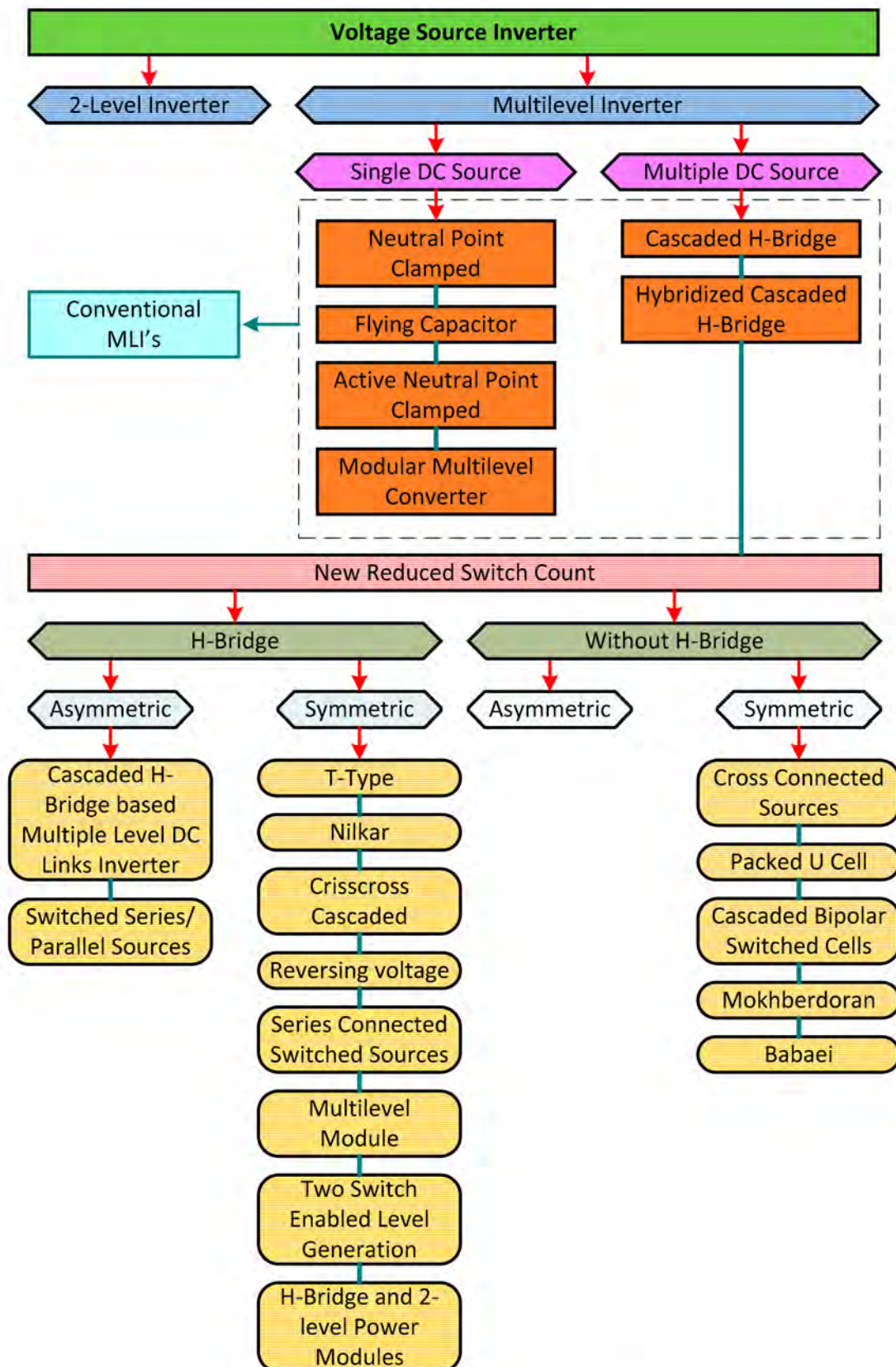


Figure 3. Overall classification of MLI.

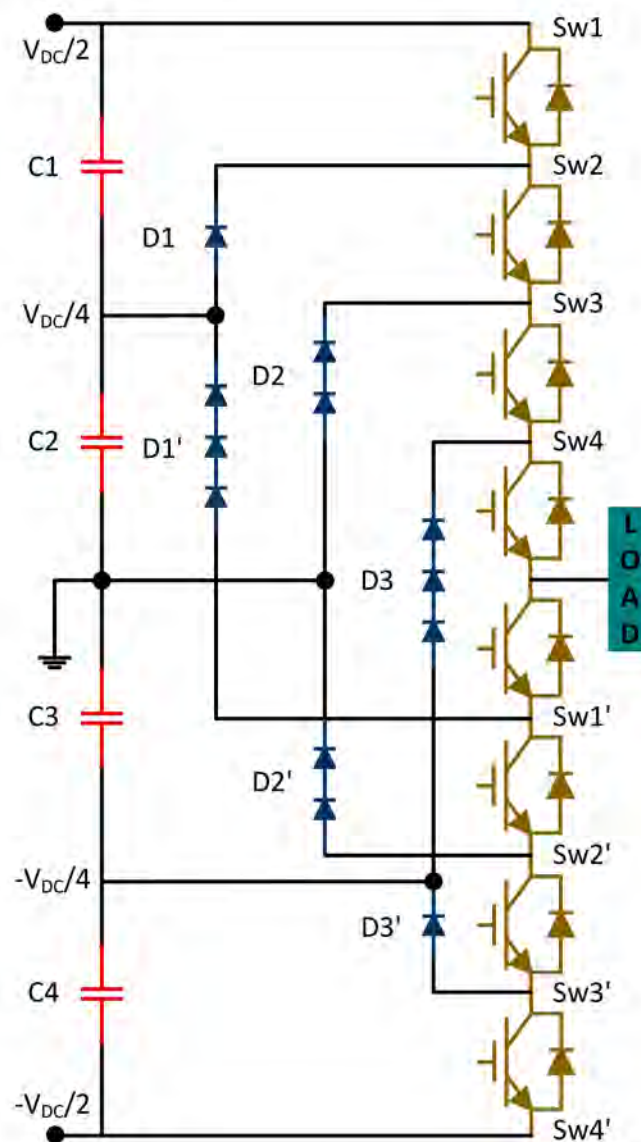


Figure 4. Topology of neutral point clamped multilevel inverter.

The major benefits of this topology are: (i) the capacity demand of the converter is minimized as all of the phases share a common DC bus; (ii) enhanced capability of reducing the THD; (iii) the capability of the capacitors to be pre-charged as a group; (iv) provides higher efficiency and (v) the number of switches, clamping diodes and capacitors can be enhanced to obtain higher voltage levels. However, this topology faces some demerits such as: (i) implementation cost can be increased as additional reactors are needed for mitigation of elevated voltage levels and THD of current as this topology uses fundamental frequency for switching; (ii) although voltage level can be increased by enhancing the number of capacitors and clamping diodes it increases the complexity of the overall configuration; (iii) due to deviation in the switching characteristics, the voltage at the neutral point fluctuates which creates difficulty in the static and dynamic sharing of the voltage across the switching units and (iv) due to imbalance in capacitor voltage and over-voltage issues, the actual application of this topology are confined to three-level only. NPC-MLI finds its application in the following ways: static VAR compensation (SVC), variable-speed motor drives, high voltage system interconnections, and be assimilated with high voltage AC/DC transmission system [90–95].

3.1.2. Flying Capacitor Multilevel Inverter (FC-MLI)

In 1992, Meynard and Foch [60] and Lavieville et al. [61] proposed the FC-MLI topology to mitigate the issue of static and dynamic sharing of the voltage across semiconductor switches as built in the NPC-MLI topology. The main architecture of FC-MLI is identical to NPC-MLI. Nevertheless, here the clamping diodes are replaced by capacitors, as illustrated in Figure 5. This topology is termed FC. In FC, capacitors that replaced the diodes of the DC-MLI are autonomous (flying) as compared to the other capacitors present in the total configuration. The voltage on every capacitor varies from that of the adjacent capacitor. This MLI topology possesses numerous advantages as compared to NPC-MLI, such as: (i) improved stability of the FC is attained by the redundancy of switching within the phase; (ii) capability in controlling both the active and reactive power; (iii) it has transformerless working and (iv) more flexible in synthesizing voltage by using capacitors instead of clamping diodes.

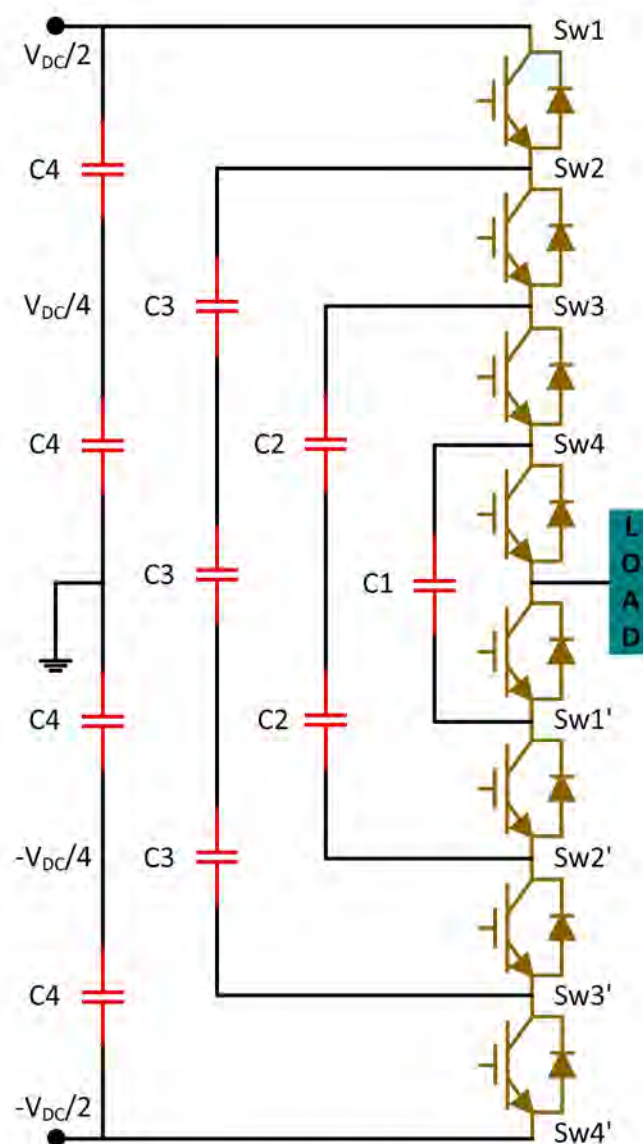


Figure 5. Topology of flying capacitor multilevel inverter.

Although this topology marks the issues of the NPC, it also has some disadvantages such as: (i) the proper charging and discharging control of capacitors is restricted due to an increase in the voltage levels; (ii) the increment in the number of the capacitor leads to increased cost, reduced lifetime and system becomes bulky; (iii) increase in the

number of levels leads to increase the number of capacitors thus limiting its operation to maximum 3–5 level; (iv) complexity in start-up and same level pre-charging of all the capacitors; (v) high switching losses due to operation at high frequency and (vi) large numbers of levels creates packaging issues. The major attractive applications of FC-MLI includes [39,60,94]: (i) static var generation; (ii) AC motor drives; (iii) active filter operations; (iv) switched converters; (v) sinusoidal current rectifier and (vi) converters with THD-reducing capacities.

3.1.3. Active Neutral Point Clamped Multilevel Inverter (ANPC-MLI)

Bruckner et al. [68,96] have proposed the ANPC-MLI topology. This inverter helps to overcome the insufficient and uneven losses which are shared between the outer and inner switches. It was possible by placing power switches rather than normal diodes [97]. Figure 6 demonstrates the nine-level ANPC inverter with the combination of NPC and FC-based MLI topologies [97]. In this configuration, the number of the two-level inverter can be found out by $(n - 1)/2$, where 'n' is the number of output levels of the inverter. So, four number of two-level inverters were cascaded to obtain a nine-level inverter. In Figure 6, switches 'Sw1' to 'Sw8' and capacitors 'C1' to 'C3' belong to the first part, whereas the switches 'Sw17' to 'Sw24' and capacitors 'C7' to 'C9' belong to the second part of the MLI. Switches 'Sw9' to 'Sw16' and capacitors 'C4' to 'C6' belong to part three, used for connecting the inverter to the load.

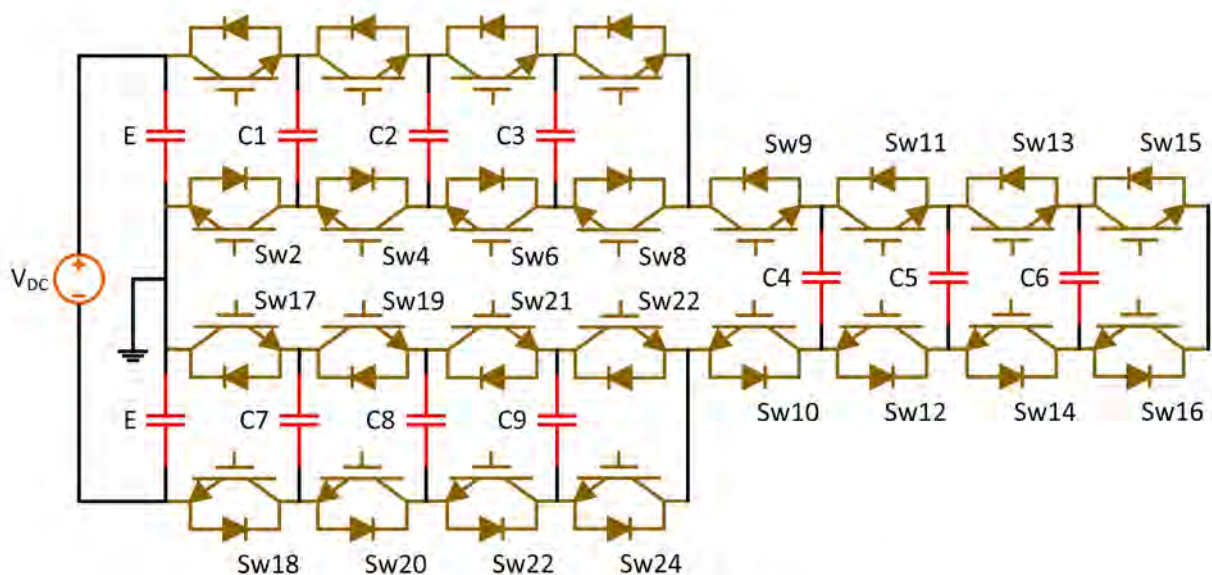


Figure 6. Topology of active neutral point clamped multilevel inverter.

3.1.4. Modular Multilevel Converter (MMC)

The MMC was first proposed in 2001 by Lesnicar and Marquardt in a German patent [62], and later in 2002, it was employed for a wide-scale power range [98]. MMC offers numerous merits in comparison to other available topologies such as [99,100]: (1) large range of voltage operation by cascading cells; (2) independent PQ control; (3) negligible losses; (4) high modularity; (5) low switching frequency; (6) output almost sinusoidal so does not need AC filters; (7) mechanical structure is simple; (8) voltage and current quality generated is high and (9) high reliability, availability, and efficiency. Therefore, they are often preferred for medium to high voltage applications because of their high-quality output and modular structure.

Over recent years, MMC has been successfully operated as an efficient power converter in numerous power system applications such as HVDC system [101–104], FACTS devices [105–107], energy storage devices [108–110], electric vehicles [111,112], motor

drives [113–115], active power filters [116,117] and renewable energy [118–121]. Presently, the primary vital concerns of MMC include capacitor voltage balancing (CVB) and circulating current suppression (CCS). Authors in [122] have reported an efficient CVB method for MMC using the carrier-based phase shift pulse width modulation method for designing a flexible mission profile emulator for the test of MMC under various working conditions. In [123], a step up non-isolated DC-DC MMC having self-voltage balancing and soft-switching has been discussed. Researchers in [124] and [125] have proposed a sensorless switch clamp MMC for voltage balancing and inter-cluster voltage balancing control for MMC during unbalanced grid voltage. CVB control strategy for MMC has been reported in [126,127]. A novel voltage balancing control with dv/dt reduction for 10-kV SiC MOSFET-based medium voltage MMC has been proposed in [128]. Authors have also carried out hardware implementation based on the peak current mode switching cycle control for CVB of MMCs [129]. Numerous techniques have been designed and implemented for the voltage balancing of MMCs, as reported in the literature [130–134]. The CCS in MMC has been carried out efficiently through various techniques as proposed by several researchers [135–137]. In [138], authors have analyzed effective ways of CVB and CCS for a three-phase four-wire split capacitor DSTATCOM. Authors have applied various methods such as fuzzy logic controller [139,140], predictive control method [141], dead beat control [142], sliding mode approach [143], and frequency adaptive spatial repetitive [144] for suppressing the circulating current harmonics in an MMC. Many other methods have been studied and incorporated for efficient CCS of MMC [145–149].

The basic circuit of the three-phase MMC is illustrated in Figure 7, which consists of a DC voltage source, three phases (legs) with two arms per leg (upper and lower arm), each arm consisting of series connections of several (N) sub modules (SM) producing a multilevel voltage signal at its output terminal and a series inductor for smoothening and filtering the circuits. Different types of SM topologies are reported in the literature [99,100]. Recently, authors have proposed MMC basing on interleaved half-bridge submodules [150]. Some of the basic configurations are illustrated in Figure 8. Half-bridge SM, full-bridge SM, single clamped, and double clamped and shown in Figure 8A, Figure 8B, Figure 8C, and Figure 8D, respectively.

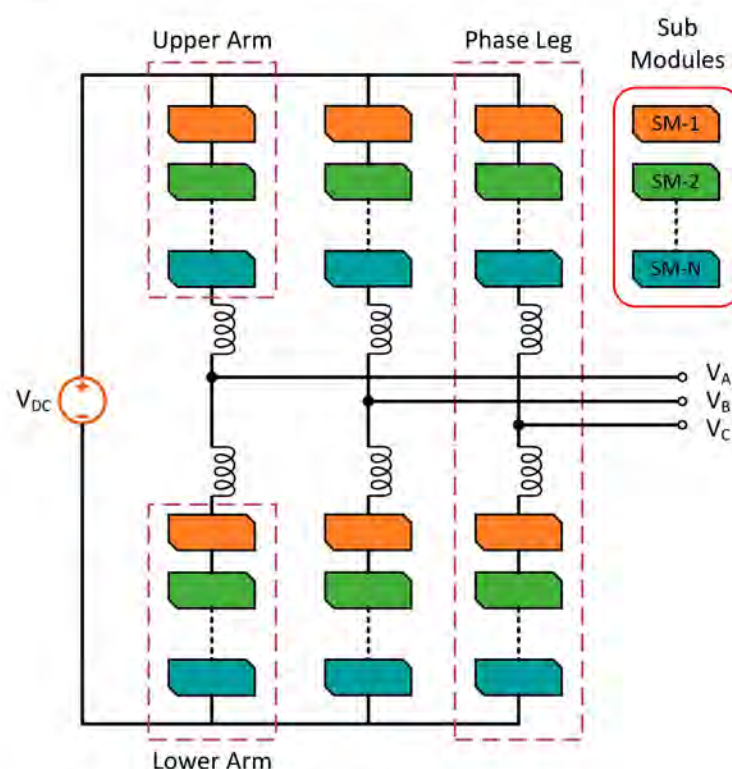


Figure 7. Topology of modular multilevel inverter.

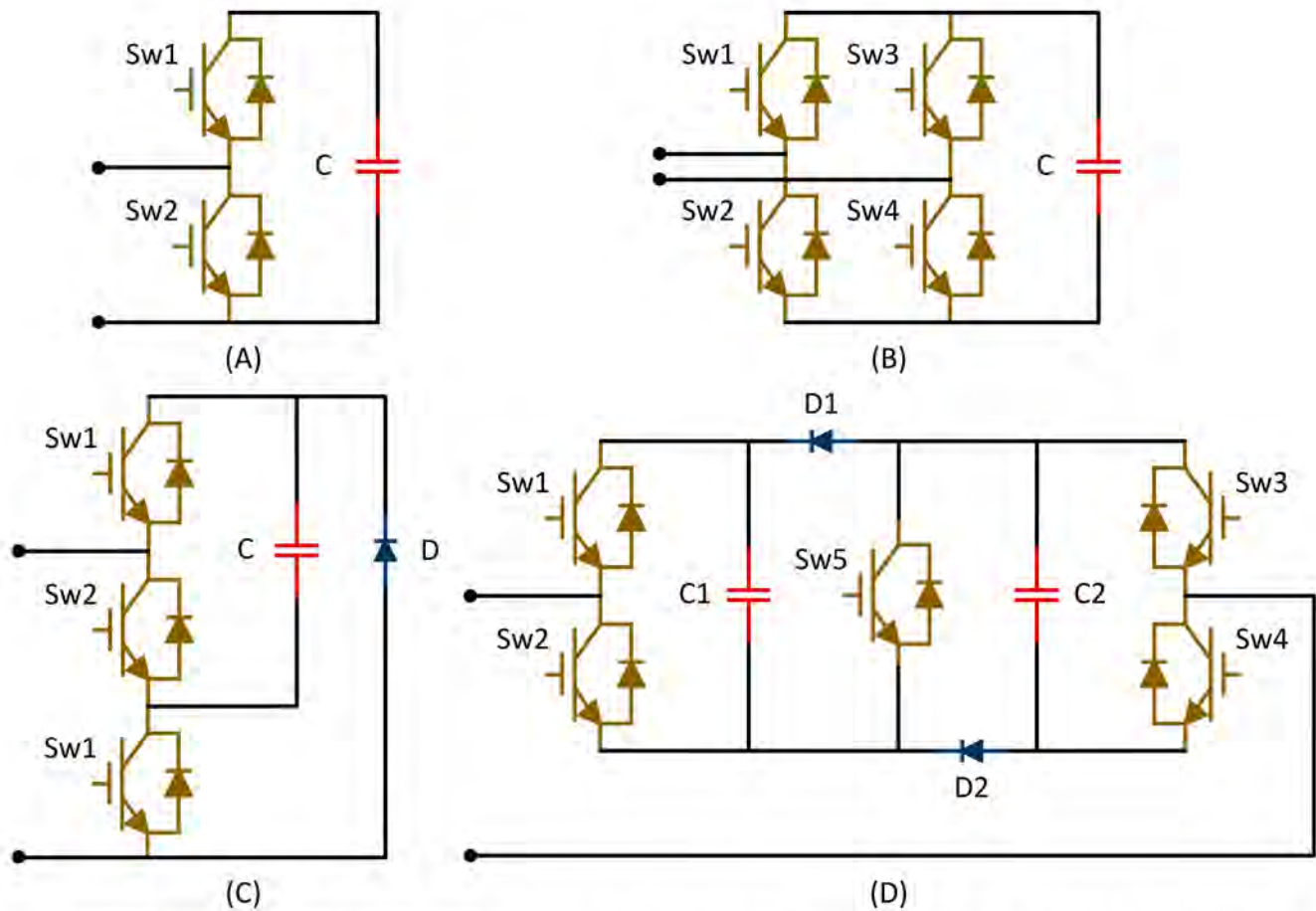


Figure 8. Topologies of sub modules (A) half-bridge, (B) full-bridge, (C) single clamped, and (D) double clamped.

3.2. Multiple DC Source

Authors in [33,90,93] have proposed MLI topologies with multiple sources (DC) as the use of a single source (DC) is limited for achieving greater voltage levels. In this section, various topologies of MLI with multiple DC sources are discussed in detail.

3.2.1. Basic Multiple DC Source Topology

Cascaded H-bridge Multilevel Inverter (CHB-MLI)

Baker and Bannister [52] proposed the first patent on this topology which was considered to be a viable substitute to previously described topologies as it requires a significantly fewer number of power devices. This topology was termed CHB-MLI, which constitutes the series connection of H-bridges with separate DC sources. Numerous series-connected H-bridge structures generate the multilevel stepped waveform. By cascading the general H-bridge cell, the resultant CHB-MLI can form an unlimited number of levels theoretically. This property of CHB-MLI allows modulation. The advancement of the technique for eminence follows the trade-off for high power medium voltage operations, which have now reached the level of megawatt by industries. It is an effective solution to voltage imbalance found in the NPC and FC configurations due to its modular structure. CHB generally comprises power conversion cells, each of which is supplied by an isolated DC source on the DC side, obtained from batteries, ultracapacitors, fuel cells, and series connected on the AC side [151]. A schematic diagram of the CHB topology has been shown in Figure 9.

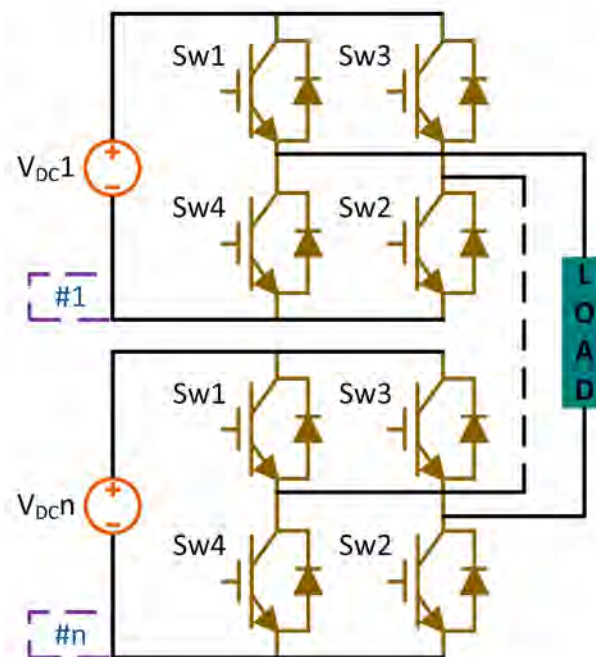


Figure 9. Topology of cascaded H-bridge multilevel inverter.

The advantages of CHB-MLI topology are as follows: (i) easy modulation, control, protection, and maintenance during failure due to compatible structure; (ii) capable of handling higher voltages and absence of voltage imbalance; (iii) ability to eliminate common-mode voltages by proper selection of modulation scheme; (iv) generates almost sinusoidal output and hence almost requires no output filter; (v) less component requirement being equated to other topologies; (vi) no requirement of flying capacitors or clamping diodes and (vii) uniform distribution of load power amidst all switching devices [152]. However, despite several merits, this topology faces some serious drawbacks such as: (i) requirement of numerous separate DC sources and (ii) need of many DC link voltage controllers. Various fields of application of this topology include RER interface, motor drives, electric vehicle drives, laminators, blowers, fans, conveyors, DC power source utilization, frequency link systems, and power factor compensators [39,56,153–155].

Hybridized Cascaded H-bridge Multilevel Inverter (HCHB-MLI)

HCHB-MLI was first introduced by Odeh and Nnadi [156], as illustrated in Figure 10. HCHB-MLI signifies that the inverter is employed with: (i) various semiconductor device technology; (ii) various amplitude and characteristics of DC sources; and (iii) combination of many modulation strategies [157]. Figure 10 depicts a nine-level HCHB-MLI, which consists of two DC sources. Two five-level hybrid inverters are interconnected for providing nine-level of voltages per cycle. This topology is quite identical to the earlier discussed CHB-MLI topology. However, the significant difference between HCHB and CHB topology are: (i) in HCHB, each H-bridge cell is added with an auxiliary switch for the harmonic profile improvement of output waveforms; (ii) the number of devices required in this HCHB topology is comparatively significantly less in comparison to the CHB topology for the same level of output voltage waveform [158] and (iii) with the operational and switching activities, HCHB topology possesses double RMS output voltage, voltage steps quantity and reduced number of DC sources. However, the major demerit is that it cannot be employed for high voltage applications.

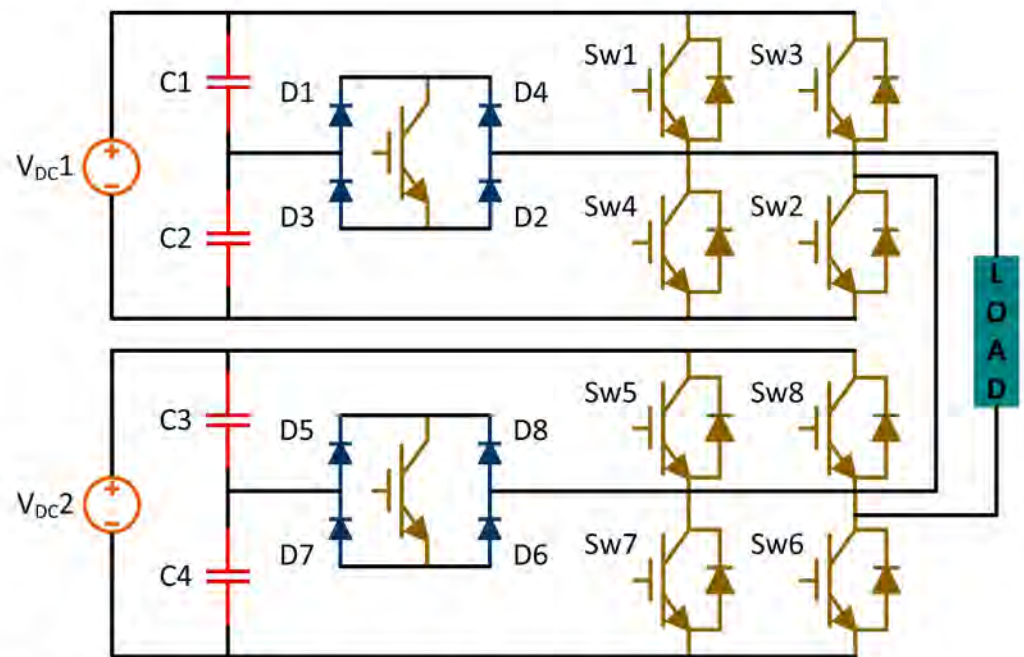


Figure 10. Topology of hybridized cascaded H-bridge multilevel inverter.

3.2.2. New Reduced Switch Count Topology

Topologies with H-bridge broadly consist of asymmetric and symmetric types.

H-bridge Topologies

(i) Asymmetric H-bridge Topology

Asymmetric MLI is usually CHB-MLI type in which the value of the voltage of any one DC source varies dynamically [159,160]. The main merits include: (i) generation of output voltage waveform with minimum THDs [39,161,162]; (ii) requires reduced number of semiconductor devices in comparison to symmetric topology [163]; (iii) needs only 12 switching units to attain seven, nine, fifteen and twenty-one levels [164]; (iv) operates with reduced dimension and cost of the inverter [165] and (v) enhanced reliability due to operation with fewer semiconductor switches and capacitors [166]. Asymmetric topologies with H-bridge have been further classified into two types, and the details are highlighted below [167].

A. Cascaded H-bridge based Multiple Level DC Links Inverter

Gui Jia Su et al. [72] proposed this topology which comprises the CHB with multiple level DC links (MLDCL). Figure 11 represents an MLDCL inverter consisting of 2 input DC sources. The circuit comprises of 'n' number of half-bridge units in cascade, and each unit has one DC source with two switches connected in series. A stepped DC voltage waveform is produced with the help of these cascaded units, which are also known as level-generation parts. A full multilevel AC waveform is generated using the H-bridge by changing the polarity of the output voltage. MLDCL topology utilizes only fewer semiconductor switches to generate the same output voltage level [39]. Major applications of this configuration include: (i) permanent magnet (PM) motor drives with low range of power (<100 kW); (ii) metal oxide semiconductor field effect transistors (MOSFETs); (iii) insulated gate bipolar transistors (IGBTs) and (iv) solar and fuel cell integration [168,169].

Table 2. A comprehensive summary of merits and demerits of various MLI configurations.

Configuration	Merits	Demerits
NPC [56,90–95]	<ul style="list-style-type: none"> ➤ Modular in design ➤ Better dynamic response ➤ Cost effective (only for three-level structure) ➤ Less number of DC sources needed for operation ➤ Good fault-tolerant characteristics ➤ Absence of floating capacitors ➤ Back-to-back inverters are employed ➤ Maximum efficiency when operated at fundamental frequency ➤ Plays a vital role for application in industries 	<ul style="list-style-type: none"> ➤ DC level may discharge due to improper control and monitor ➤ An increase in voltage level results in an increase in the number of clamping diodes ➤ Uneven distribution of losses across inner and outer switches ➤ Costlier and less reliable due to an increase in number of diodes
FC [39,60,61,94]	<ul style="list-style-type: none"> ➤ Can be employed for fault-tolerant operation ➤ Uses less number of DC sources ➤ Cost effective if used for high-level structures ➤ Does not require clamping diodes ➤ Ability to lessen voltage derivation stress on the power electronic components 	<ul style="list-style-type: none"> ➤ Capacitor requirements are greater, which is more expensive than diodes ➤ Voltage balancing unit is complex ➤ Switching efficiency is minimum ➤ Complication in overall system control ➤ Complex structure ➤ Less reliable ➤ Use of more voltage sensors ➤ Gives rise to ripples at low switching frequencies
ANPC [68,96,97]	<ul style="list-style-type: none"> ➤ Losses across each switch are uniform ➤ Dynamic response is good ➤ Simple in structure ➤ Cost effective, compact in size, and requires no floating capacitor for a three-level structure ➤ Uses power switches than normal diodes 	<ul style="list-style-type: none"> ➤ For levels greater than 3, more numbers of floating capacitors are required ➤ Control circuit is complex in comparison to NPC ➤ When operated at higher voltage levels, power switches of various voltage ratings are needed
MMC [62,98–121]	<ul style="list-style-type: none"> ➤ Possesses voltage scalability by cascading identical cells ➤ Capable of independent PQ control ➤ Losses are negligible ➤ Level of modularity at the cell level is maximum ➤ Switching frequency is low ➤ Does not require AC filters as output is purely sinusoidal ➤ Simple in structure ➤ Quality of voltages and currents is high ➤ High availability, reliability, and efficiency 	<ul style="list-style-type: none"> ➤ Need of more power electronic interfaces ➤ Uses more number of capacitors and cells ➤ Control unit for circulating current and voltage balancing of cell is needed

Table 2. Cont.

Configuration	Merits	Demerits
CHB [39,52,56,151–155]	<ul style="list-style-type: none"> ➤ Structure is simple and modular ➤ Ease of extending to higher levels ➤ Simplicity in storing and packaging ➤ Voltage derivative stress is lowered due to the production of common-mode voltage ➤ Reliability is higher ➤ Control is simple ➤ Absence of floating capacitors ➤ Minimum harmonics in the input current ➤ Ability to operate both at fundamental and switching frequencies ➤ Output signal has less distortion without any filter unit ➤ Best suited for applications of fault tolerance ➤ Needs only unidirectional switches ➤ It can employ asymmetric source topology ➤ Can operate as single DC source unit 	<ul style="list-style-type: none"> ➤ Requirement of more power switches ➤ The level of output voltage is comparatively less ➤ Cost of implementation is large ➤ Voltage rating across switches varies for asymmetric configuration ➤ Requires a greater number of DC sources ➤ Requires more complex controller unit
HCHB [156–158]	<ul style="list-style-type: none"> ➤ Presence of an auxiliary switch for harmonic profile improvement of output waveforms ➤ Requires a smaller number of switching units and devices ➤ Utilizes reduced number of DC sources 	<ul style="list-style-type: none"> ➤ Cannot be employed with high voltage application ➤ Costly for implementation
MLDLC [39,72,168,169]	<ul style="list-style-type: none"> ➤ Uses less number of semiconductor switches ➤ Circuit layout is optimized ➤ No requirement of extra clamping diodes or capacitors 	<ul style="list-style-type: none"> ➤ Costly as it involves capacitors for storage ➤ With the increase in number of DC sources, output level increases ➤ Power rating of device increases due to reduced device count which leads to damage of the device by causing its operating temperature to exceed safe levels as well increases its overall cost
SSPS [168,170–172]	<ul style="list-style-type: none"> ➤ Ability to generate more levels of output voltage using very few numbers of switches ➤ Simple structure ➤ Uniform sharing of load is possible ➤ Needs less number of gate driver circuit ➤ Can operate as single DC source configuration 	<ul style="list-style-type: none"> ➤ Cannot be applied for fault-tolerant operations ➤ Switches with the highest voltage rating fail to operate at fundamental frequency ➤ Cannot be operated as asymmetric configuration ➤ Due to reduced switch count, the overall power rating is higher leading to threat in damage to the entire system

Table 2. Cont.

Configuration	Merits	Demerits
T-type [80–82,173]	<ul style="list-style-type: none"> ➤ Control structure is simple ➤ Does not require floating capacitors and diodes 	<ul style="list-style-type: none"> ➤ Voltage derivative stress is higher on switches ➤ Switching losses are high ➤ Operation at high-frequency results in low efficiency ➤ Cannot operate for high voltage and power applications
Nilkar [174]	<ul style="list-style-type: none"> ➤ Can operate with less number of switches ➤ The net harmonic content is less ➤ Employs batteries and capacitors as the DC voltage source 	<ul style="list-style-type: none"> ➤ Complicated structure ➤ Costly as power rating of reduced number of switches is more ➤ Not feasible for fault-tolerant operation ➤ Operation with less number of switches increases power rating and in turn makes its operating temperature exceed safe levels
CCHB [51,175]	<ul style="list-style-type: none"> ➤ Peak inverse voltage of the system is low ➤ Both symmetric and asymmetric topology are possible ➤ Ability to operate both with positive & negative voltage 	<ul style="list-style-type: none"> ➤ Switches with bidirectional operation are required ➤ Needs isolated input DC link for operation
RV [78,176]	<ul style="list-style-type: none"> ➤ Three-phase operation can be carried out by single DC link ➤ Non-isolated type of DC links are operated ➤ Rated switches are operated at peak voltage and at switching frequency 	<ul style="list-style-type: none"> ➤ Load sharing is not uniform ➤ Asymmetric configuration is not possible
SCSS [76,77]	<ul style="list-style-type: none"> ➤ Modular structure ➤ Rated switches can operate at peak voltage and switching frequency 	<ul style="list-style-type: none"> ➤ System requires to operate at only symmetric configuration ➤ Rating of voltage varies from one switch to another ➤ Load sharing is not uniform
MLM [79]	<ul style="list-style-type: none"> ➤ Can operate with reduced number of DC voltage sources ➤ Requires fewer semiconductor switches, transistors, and power diodes 	<ul style="list-style-type: none"> ➤ Fails for application in asymmetric configuration ➤ Requires isolated DC sources ➤ Power rating of device increases due to reduced device count which leads to damage of the device by causing its operating temperature to exceed safe levels as well increases its overall cost
2SELG [83,168]	<ul style="list-style-type: none"> ➤ Needs minimum number of switches ➤ Structure is simple 	<ul style="list-style-type: none"> ➤ Fails to operate at fundamental switching frequency ➤ Complex control ➤ Requires isolated DC sources ➤ Use of minimum number of switches leads to increased cost and temperature level higher
HBTPM [177]	<ul style="list-style-type: none"> ➤ Simple structure ➤ Appropriate for high voltage applications 	<ul style="list-style-type: none"> ➤ Fails to synthesize various levels of voltage waveform at bus end ➤ All the individual levels accessible by sources could not be achieved ➤ Fails to operate in asymmetric configuration

Table 2. Cont.

Configuration	Merits	Demerits
CCS [51,69]	<ul style="list-style-type: none"> ➤ Ability to produce possible values of minimum step voltage ➤ Requires less number of basic sub-inverter cells and switching devices ➤ Possesses minimum blocking voltage for a particular level ➤ Modular in structure 	<ul style="list-style-type: none"> ➤ Operates only with isolated DC sources ➤ Requires on-state switches ➤ Not so cost effective ➤ Operation with less number of switches increases power rating and in turn makes its operating temperature exceed safe levels
PUC [168,178–182]	<ul style="list-style-type: none"> ➤ Structure is simple ➤ Possibility of adding more crossover switches 	<ul style="list-style-type: none"> ➤ Not modular ➤ Operation with asymmetric configuration is mandatory ➤ Different switches have different voltage ratings ➤ Fault-tolerant applications are impossible ➤ Cost of implementation is more
CBSC [71]	<ul style="list-style-type: none"> ➤ Reduced operational cost ➤ Simple circuit 	<ul style="list-style-type: none"> ➤ Cannot work with asymmetric topology
Mokhberdorani [51,183]	<ul style="list-style-type: none"> ➤ High level of voltage can be achieved by cascading basic units in series ➤ Enhanced system efficiency ➤ Modular structure ➤ Cost effective 	<ul style="list-style-type: none"> ➤ Requirement of switches and gate driver circuit is more ➤ Individual DC sources are required for operation
Babaei [51,70,184]	<ul style="list-style-type: none"> ➤ Simple and modular structure ➤ Power is equally shared among all cells ➤ Operation for symmetric and asymmetric configuration is possible 	<ul style="list-style-type: none"> ➤ Requires DC sources that are isolated ➤ Needs switches for various ratings of voltage

B. Switched Series/Parallel Sources based Multilevel Inverter (SSPS-MLI)

Hinago and Koizumi [170] proposed the SSPS-MLI topology. It is comprised of two major units; the “level-generation” unit, where a staircase voltage waveform with positive polarity is generated, and the “polarity-generation” unit, where the staircase DC voltage waveform gets converted to AC voltage as depicted in Figure 12. This configuration possesses the primary merit of generating more output voltage levels using very few numbers of switches in contrast to other conventional MLI topologies. Therefore, SSPS-MLI can be applied in the areas of: (i) electric vehicle where a single unit of the battery can be composed of several series-connected battery cells [171]; (ii) vehicle drive system to meet voltage or power need by a possible combination of two or more sources either in series or in parallel and (iii) traction purposes by possible joining of multiple sources in various flexible configuration [168,172].

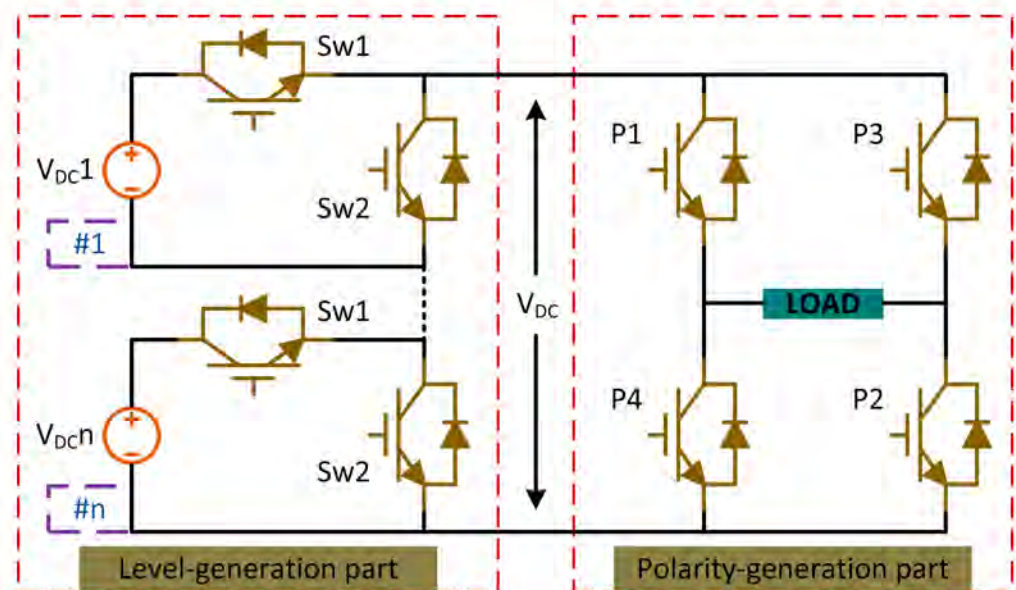


Figure 11. Topology of multiple level dc links inverter.

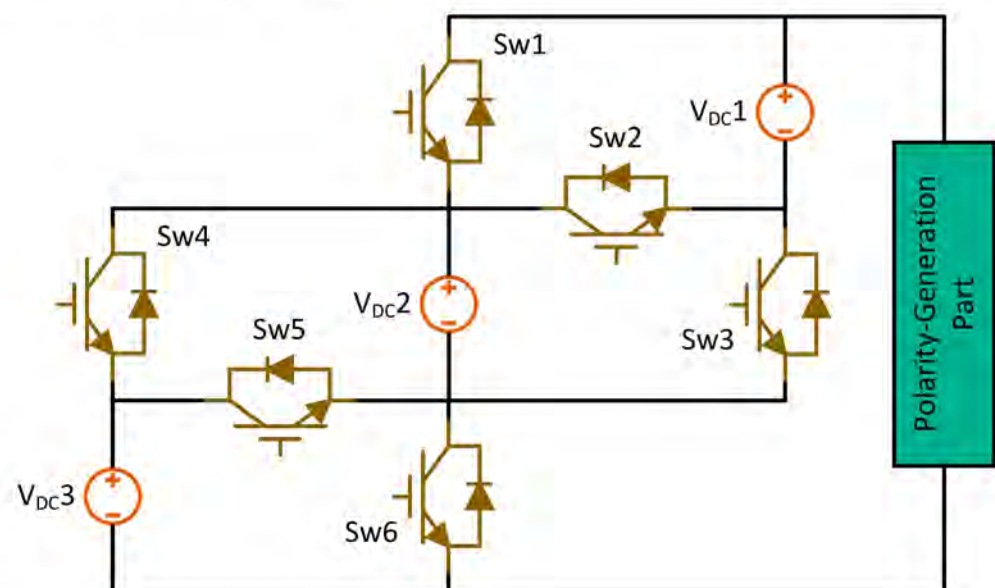


Figure 12. Topology of switched series/parallel sources based multilevel inverter.

(ii) Symmetric H-bridge Topology

This family of MLI usually consists of inverters where the magnitude of all the isolated supply DC sources to each of the H-bridge cells is identical. The symmetric H-bridge topology is further classified into different types. This section throws light on each of the Symmetric H-bridge topologies in specific.

A. T-type Multilevel Inverter

A novel T-type configuration with a five-level single phase inverter was first proposed by Gerardo Ceglia et al. [80–82]. The primary benefit of it is that the designed configuration reduces the use of more switches. A T-type inverter topology is depicted in Figure 13 below. Compared with other traditional topologies, T-type topology delivers an extraordinary improvement regarding the lower count of switches used and lower layout complexity. Further, almost 40–50% reduction in power switch count is achieved without diodes or capacitors [173]. This configuration has an H-bridge and an auxiliary bidirectional switch for controlling the connection of the supply from the DC sources to generate the staircase output voltage. However, this topology fails to render switching states to have all essential levels, as in the asymmetric H-bridge topologies [80].

B. Nilkar Multilevel Inverter (N-MLI)

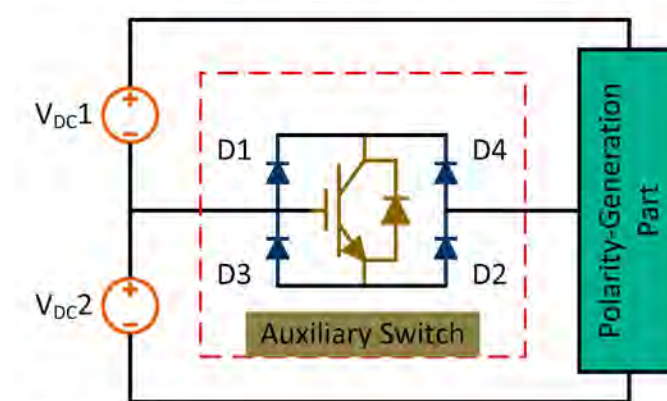


Figure 13. Topology of T-type symmetric H-bridge topology.

Nilkar et al. proposed the Nilkar inverter topology [174]. The basic module of N-MLI is comprised of two identical DC voltage sources with four semiconductor switching units for generating a staircase DC voltage waveform with positive polarity, which is further connected to an H-bridge consisting of 4 switching devices as demonstrated in Figure 14. The H-bridge helps in alternating the polarity of voltage for producing a complete sinusoidal alternating output signal. This topology renders many advantages, such as: (i) operates with significantly less number of switches; (ii) THD is effectively lessened in comparison to other available classical MLI topologies, and (iii) batteries and capacitors can be used as the DC voltage source. This topology can be used for various RER's (such as solar and fuel cell) interface and medium to high voltage applications in industries.

C. Crisscross Cascaded Multilevel Inverter (CCHB-MLI)

In [175], Khosroshahi proposed a CCHB-MLI topology consisting of the basic units in cascade. Figure 15 shows a CCHB inverter configuration comprising of two sources of DC voltage and a combination of one-way and two-way switches. It has two units; the first is the level generation unit, and the second is the polarity generation unit. The level-generation unit has two power switches, namely Sw2 and Sw3, which are unidirectional. The other switches Sw1 and Sw4, are bidirectional conducting and blocking switches, respectively. The four power switches P1, P2, P3, and P4 constitute the polarity-generation part. The benefits of this topology are: (i) usage of the reduced number of semiconductor switches; (ii) limited use of isolated DC voltage sources as compared to other classical topologies; and (iii) low cost and volume as compared to CHB-MLI [51].

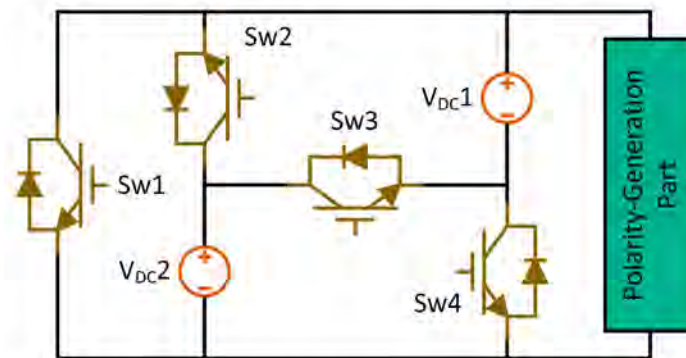


Figure 14. Topology of Nilkar multilevel inverter.

D. Reversing Voltage Multilevel Inverter (RV-MLI)

Reversing voltage MLI topology was first suggested by Najafi et al. in [78,176]. In this topology, the sinusoidal output voltage is produced in both level generation and polarity generation stages. The positive and negative polarity of voltages is generated in the level generation and polarity generation stage, respectively, as shown in Figure 16. By duplicating the centre stage operation with any number of levels can be possible, so application to three phases can also be extended. It has flexibility in the switching sequence and needs very few components for its work. Therefore, it can be useful in the areas of applications such as FACTS and HVDC. However, operation using different DC sources is not possible in this topology, as it is practically impossible to combine additive and subtractive DC sources.

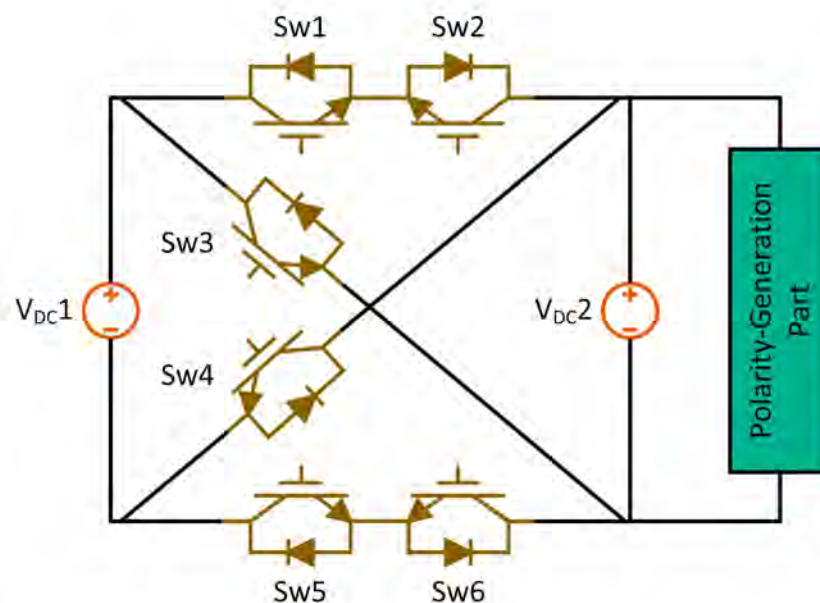


Figure 15. Topology of crisscross cascaded multilevel inverter.

E. Series Connected Switched Sources Multilevel Inverter (SCSS-MLI)

In this topology, the basic concept lies in the series connection of sources by the switches [76,77]. Figure 17 shows SCSS based MLI configuration. Here the poles of the voltage sources with lower magnitude are being associated with semiconductors. They are also in contact with the voltage poles with a higher magnitude of the upstream source. The link can synthesize a DC voltage with multiple levels, which take into account both the polarities with the help of the H-bridge. This structure also helps in reducing the number of switches for the symmetrical structure of the inverter. Nevertheless, the main shortcomings

of this topology are: (i) power semiconductor used must be of the same rating; (ii) load sharing is impossible as input stage requires various configurations and (iii) high rated switches need to be switched with the minimum possible frequency.

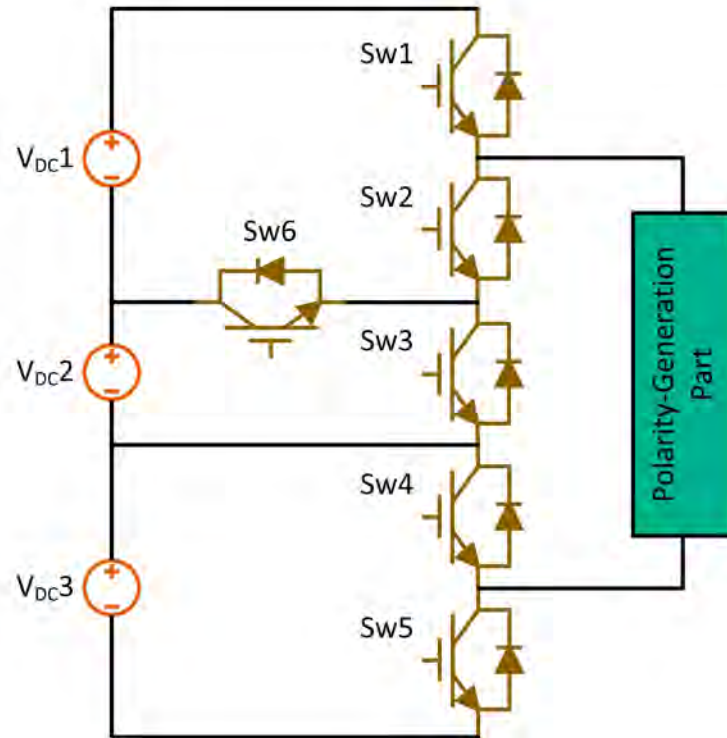


Figure 16. Topology of reversing voltage multilevel inverter.

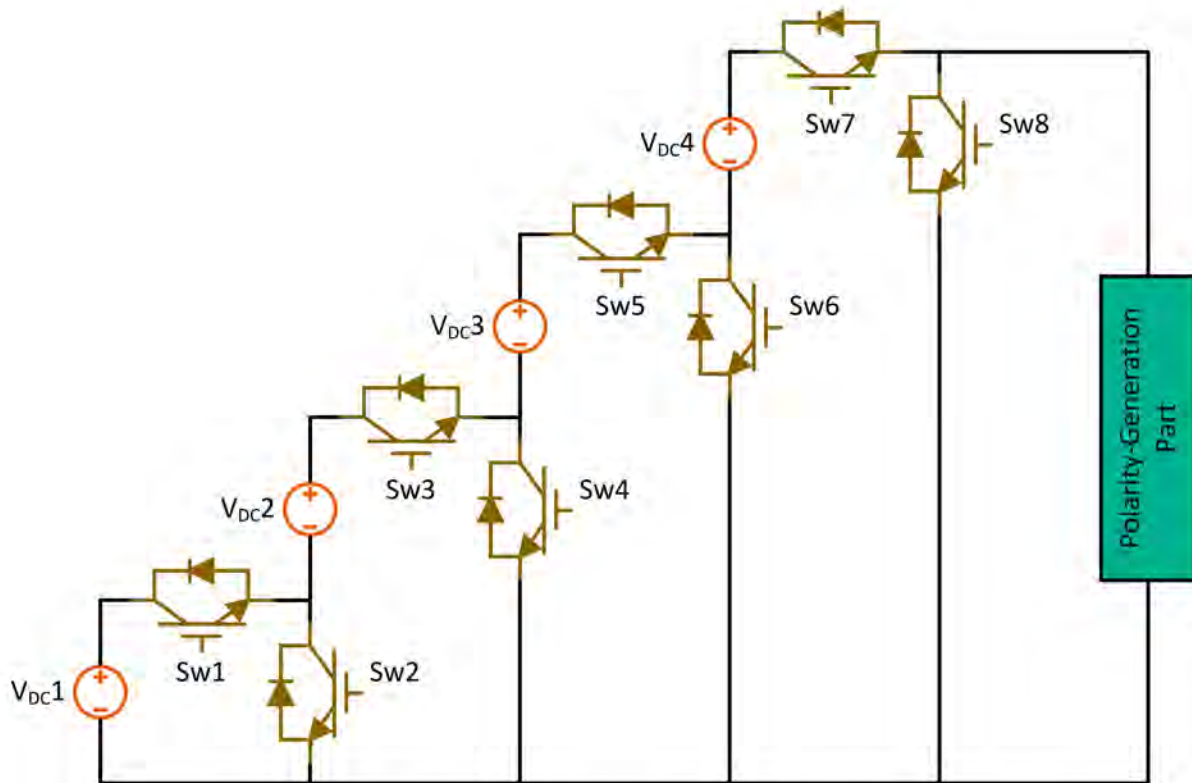


Figure 17. Topology of series connected switched sources multilevel inverter.

F. Multilevel Module Based Multilevel Inverter (MLM-MLI)

Babaei in [79] suggested the MLM-MLI topology, which comprises the level generation part and the polarity generation part. Figure 18 illustrates an MLM-MLI with four DC input sources. With the increase in output voltage level, this configuration can operate with the reduced number of DC voltage sources, semiconductor switches, transistors, and power diodes. The major demerit is that it fails for application in an asymmetric configuration. However, it can be used for high power quality applications that use an ample number of DC voltage sources [79].

G. Two Switch Enabled Level Generation Based Multilevel Inverter (2SELG-MLI)

Babaei in [83] discovered the level-generation based MLI Topology with two switches and seven input levels, as shown in Figure 19. This topology has two different stages, a level-generation stage and a polarity-generation stage. The name 'Two Switch' justifies that this configuration needs only two number of conducting switches in the level generation stage for synthesizing any level of voltage. However, this inverter fails to work in asymmetric topology. The major disadvantage is that as the level generation stage fails to realize the zero level of its own, the operation with a fundamental switching frequency becomes impossible [168].

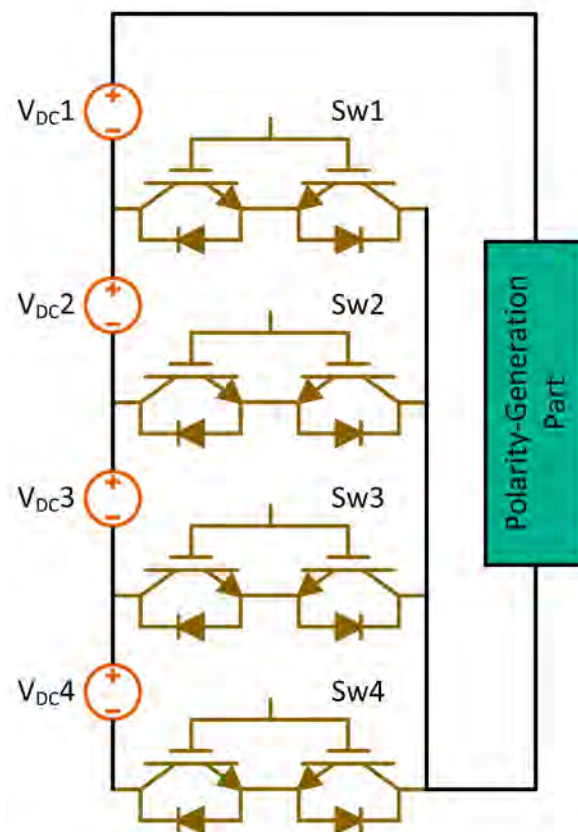


Figure 18. Topology of multilevel module based multilevel inverter.

H. H-bridge and two-level Power Modules Based Multilevel Inverter (HBTPM-MLI)

In [177], Suroso and Noguchi presented HBTPM-MLI. An HBTPM based inverter configuration has been illustrated in Figure 20, which consists of 4 input DC sources (V_{DC1} to V_{DC4}). Semiconductor switches are used to interconnect the terminals with a source of low potential. Further, the proceeding source is attached to a high potential terminal using power switches. Switches P1 to P4 are for the polarity generation stage, and switches 'Sw1' to 'Sw6' form the level generation unit. The structure is simple, but it fails to synthesize

various levels of the voltage waveform at the bus end. However, this topology fails to operate in asymmetric configuration for further reducing the count of the switch.

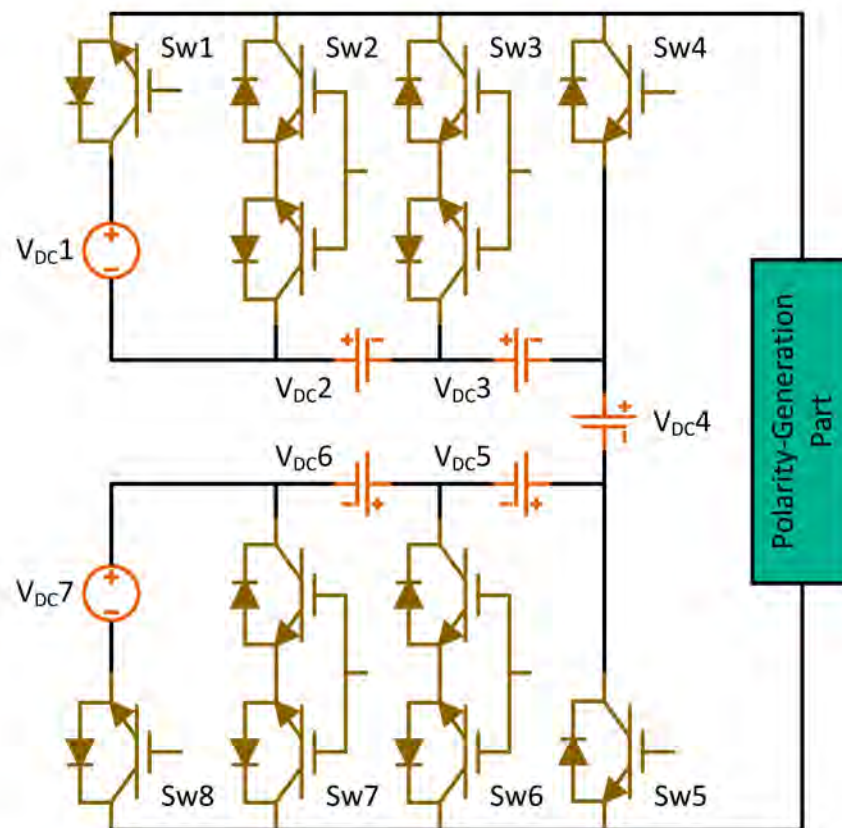


Figure 19. Topology of two switch enabled level generation based multilevel inverter.

Topologies without H-bridge

Topologies without H-bridge can be either asymmetric or symmetric type. However, mostly they are of a symmetric type.

(i) Asymmetric Topology without H-bridge

This category of MLI consists of numerous DC voltage sources, among which at least one differs dynamically. They do not consist of H-bridge cells or units.

(ii) Symmetric Topology without H-bridge

In this topology, the magnitude of all the isolated supply DC sources are identical, but they do not form an H-bridge configuration. In this section, different types of symmetric topology without H-bridge structure have been reviewed.

A. Cross Connected Sources Based Multilevel Inverter (CCS-MLI)

Authors in [69] have introduced the CCS-MLI topology comprising input DC sources isolated for every cell, as depicted in Figure 21. In this topology, a switch connects the two different terminals of two different sources and vice-versa. It requires a minimum number of switches for its operation and is usually active where isolated DC sources are present [51].

B. Packed U Cell Multilevel Inverter (PUC-MLI)

A novel MLI topology was offered by Youssef Ounejjar et al. and was named "PUC" [178–182]. The circuit of PUC-MLI is represented in Figure 22, which constitutes ten power semiconductor switches and four DC sources. Every individual U-cell has a single DC input level and two switching units [168]. The main advantage of this technology is

that the maximum voltage-producing switch can be operated at the minimum frequency. Further, it allows easy change in the voltage level number, reduces stress on the switch, and enhances the overall converter operation.

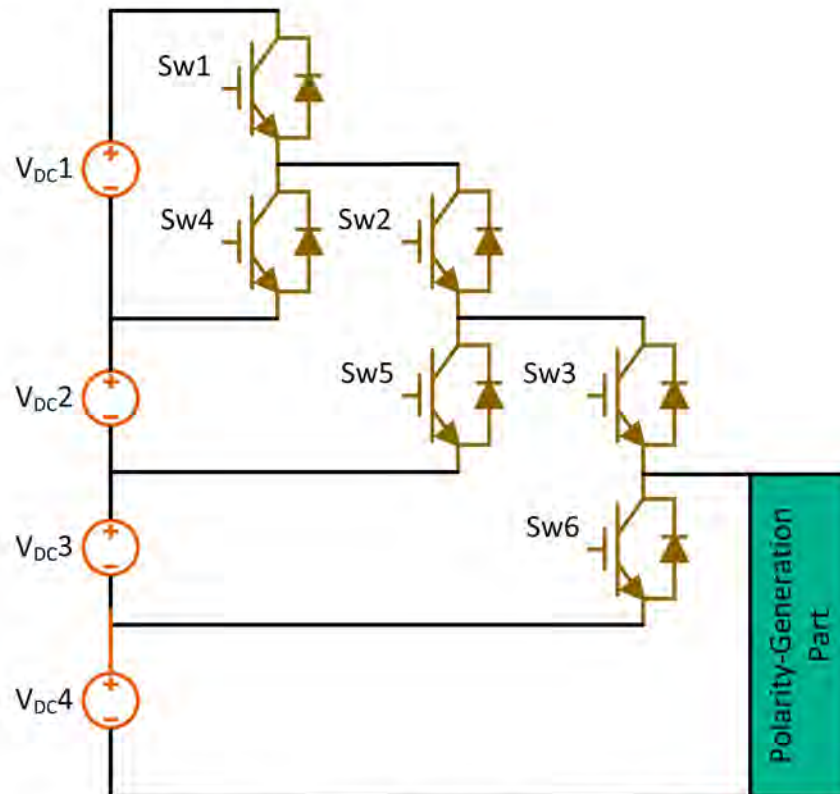


Figure 20. Topology of H-bridge and two-level power modules-based multilevel inverter.

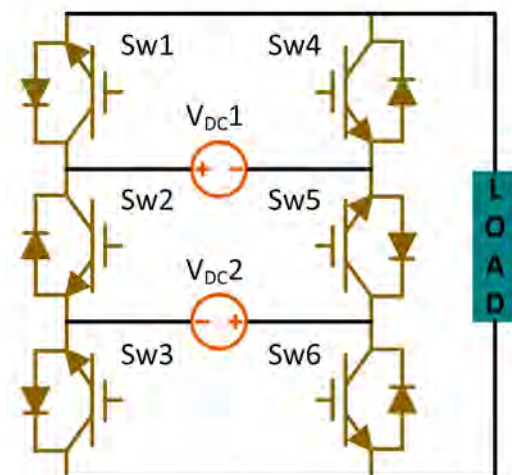


Figure 21. Topology of cross connected sources based multilevel inverter.

C. Cascaded Bipolar Switched Cells Multilevel Inverter (CBSC-MLI)

Babaei et al. in [71] have introduced this topology, as shown in Figure 23. The circuit comprises 4 DC sources and 10 bidirectional power semiconductor switches capable of generating voltage levels in both positive and negative polarities. Every bidirectional switch needs two IGBTs and is equal to the number of gate drive circuits. This concept helps in decreasing the operational cost and overall complexity of the circuit. The major shortcoming is that this topology is that it cannot work with an asymmetric configuration.

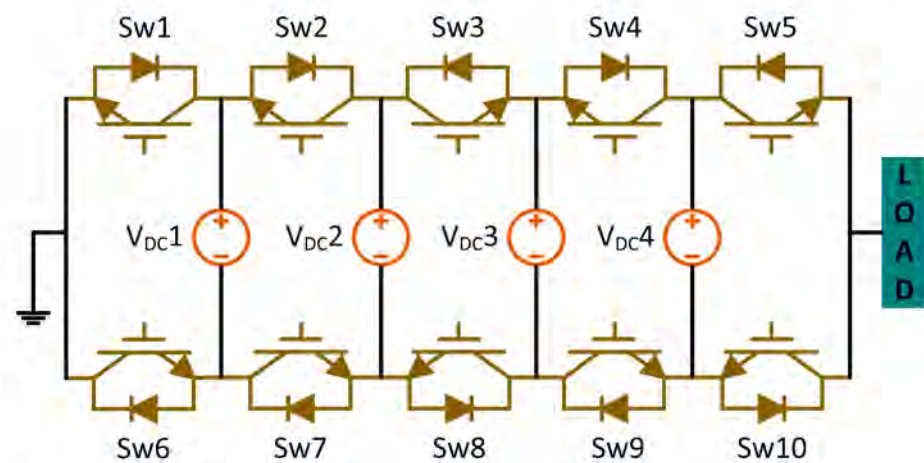


Figure 22. Topology of packed U-cell multilevel inverter.

D. Mokhberdorran Multilevel Inverter (M-MLI)

This topology is named after Mokhberdorran as in [183]. The basic circuit of M-MLI is illustrated in Figure 24, which comprises of two symmetric DC voltage sources, six switches, and eight diodes. Here to obtain a higher level of voltage, the basic units are cascaded in series [51]. The topology is such designed that it utilises a significantly fewer number of switching devices. The entire operation is divided into two parts depending upon frequency, such as low and high. This enhances the efficacy of the configuration. The structure is modular, and the cost of this unit is also minimum. Mokhberdorran technology usually finds its application in high power operations [183].

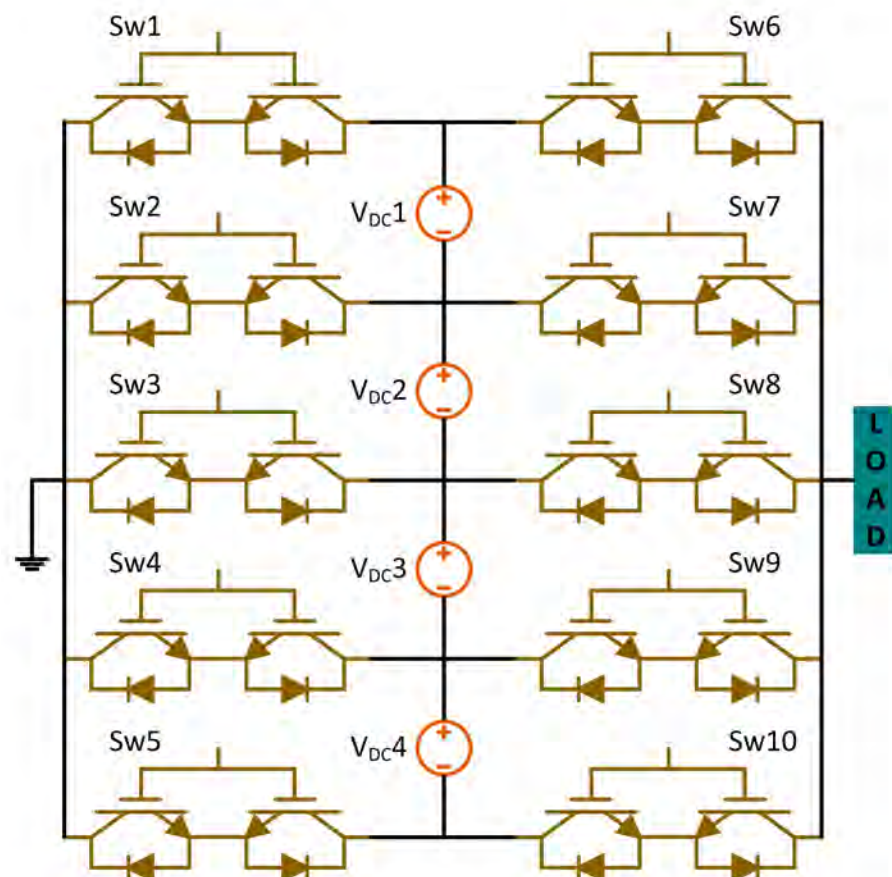


Figure 23. Topology of cascaded bipolar switched cells multilevel inverter.

E. Babaei Multilevel Inverter (B-MLI)

Figure 25 illustrates the B-MLI topology as proposed in [70,184]. The key elements are composed of six unidirectional switches and two symmetrical DC voltage sources. For increasing the output voltage level, the circuit developed can be reproduced by connecting in series [51].

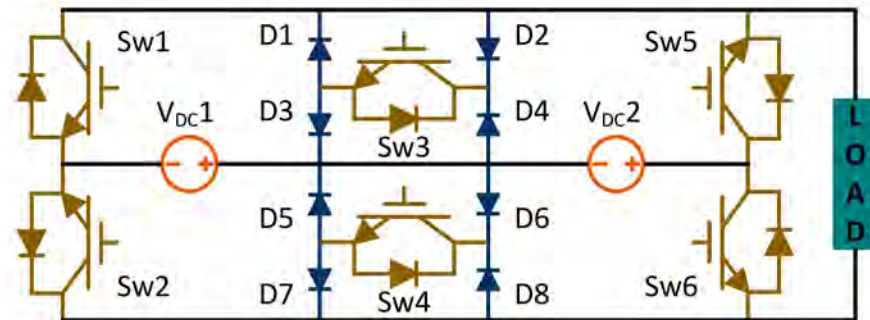


Figure 24. Topology of Mkhberdoran multilevel inverter.

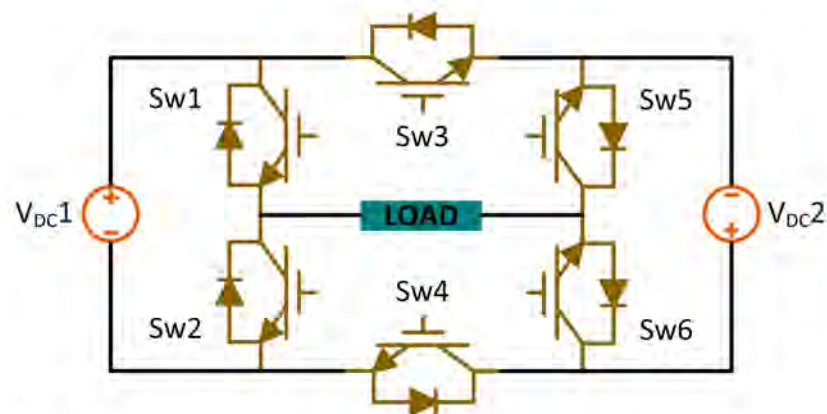


Figure 25. Topology of Babaei multilevel inverter.

4. MLI Control and Modulation Schemes

Modulation techniques play a principal role in governing the overall efficiency parameters such as harmonic reduction and switching losses used to control the inverter and turn the entire system [185]. They also have the responsibility to synthesize reference control signals to maintain all voltage sources balanced. The major purpose of modulation is to generate a staircase DC voltage signal, nearest a reference signal that is generally sinusoidal in a steady state [186]. The modulation process usually involves a variety of single or multiple attributes of a carrier signal waveform with a modulating waveform. Modulation is also referred to as a strategy to control the switching action by changing the characteristics of a particular signal (carrier signal) using another signal (reference signal). Every family of MLI has a selected appropriate modulation scheme for optimizing the circuit working and achieving the target criteria. Following are the major important factors basing on which a particular modulation technique is chosen for a particular MLI family: (i) total generated harmonics; (ii) level of distortion; (iii) frequency of switching; (iv) amount of losses and (v) response speed. The MLI modulation methods have the following needs to be fulfilled before operation: (i) quality of voltage should be high; (ii) should have modular structure; (iii) switching of multiple voltage levels simultaneously is not permitted; (iv) power devices should operate with minimum frequency; (v) load sharing should be uniform among the power modules; (vi) algorithm used for control should be easy and simple and (vii) cost of implementation must be minimum [51].

The modulation index also has a vital role in all control schemes. Modulation also depends upon modulation ratio (either over or under modulation), and the THD varies accordingly. Multiple techniques are proposed by authors in the literature depending upon the switching frequency, either fundamental or high frequency [187,188]. However, low losses are found when switched at fundamental or low frequency. A thorough survey of various modulation methods is highlighted in this section below. Figure 26 illustrates the various control and modulation schemes for MLI. Table 3 lists the merits and demerits of different modulation schemes discussed in this review article.

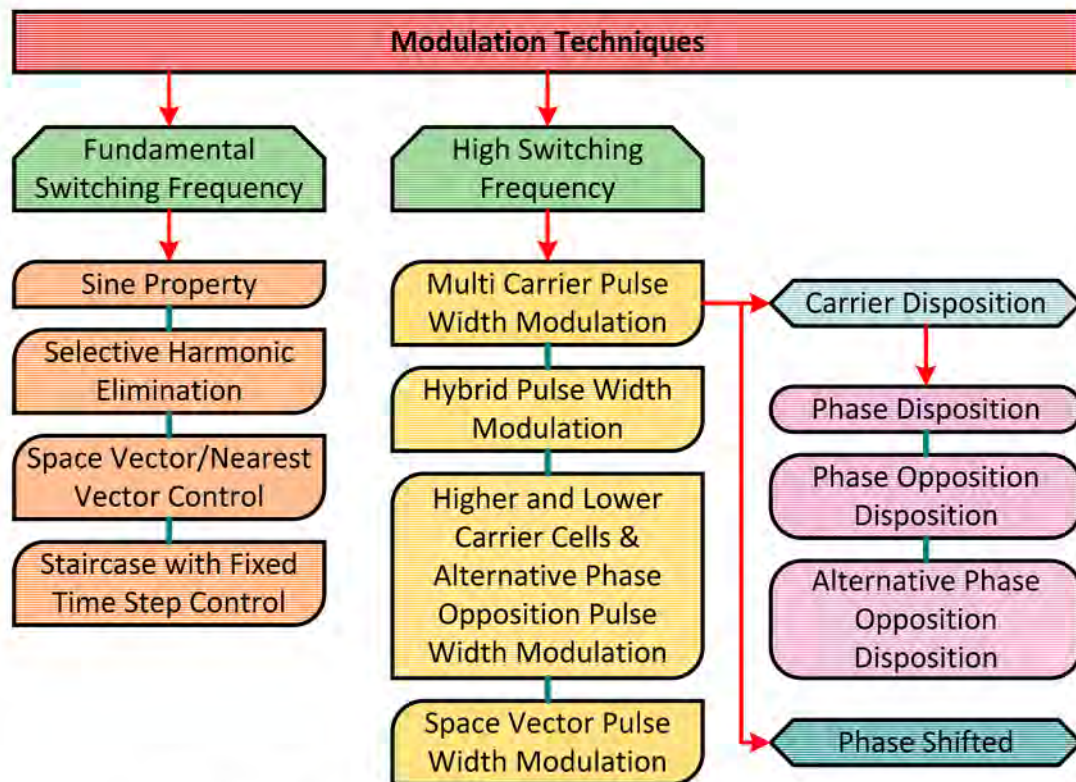


Figure 26. Categorization of modulation schemes for multilevel inverter.

4.1. Fundamental Switching Frequency Pulse Width Modulation (FSF-PWM) Techniques

These techniques generate a staircase waveform performing single or multiple commutations of the power electronic switches [189,190]. Here, an increased number of levels is obtained by adding extra units without creating any complexity in the generation of the switching signals. Moreover, due to switching at low frequency, the losses incurred are very less. Various FSF-PWM methods have been discussed below.

4.1.1. Sine Property

It is a modern method for calculating the firing angle that is to be provided to the switching units [191–193]. Calculation of firing angle is easy on adopting this technique. The firing angle is generally obtained in degrees and has the provision of appropriate conversion to any other unit of time such as ‘seconds’ for the easy performance of simulations.

4.1.2. Selective Harmonic Elimination

Researchers in 1973 suggested a voltage control and harmonic elimination theory known as SHE. This technique is utilized for eliminating the most dominant selected lower order harmonics [194–197]. In SHE, there is a possibility of lowering the THD and the size of the output filter. As the switching angles are pre-determined off-line, it is assumed to be an open-loop modulation method [198,199]. Authors have also reported

that many Fourier equations are utilized for calculating the firing angle for the switching purpose [195]. Selection of correct values of the firing angle for the Fourier series equation, the odd harmonics can be limited for any level of MLI. A microcontroller device is then used to supply these firing angles to the switches. Thus, it does not require a closed-loop controller for its implementation.

The vital functions of the SHE are: (i) maintaining the fundamental component of the waveform; (ii) harmonic reduction individually; (iii) decrease in THD, and (iv) lower switching losses. However, a major drawback of the SHE technique is that it requires the design of massive passive filters to limit the lower-order harmonics [196]. To counteract the above-cited issue of the SHE method, a novel technique known as selective harmonic mitigation (SHM) has been proposed in the literature by researchers [200]. In the SHM method, switching angles are calculated to reduce the individual harmonic distortion without the grid code limits. SHM is also an open-loop control technique and an offline procedure for calculating the switching angles and cost function that can be minimized using a search algorithm [201]. Numerous solutions can be utilized to solve the non-linear equation of MLI, such as: (i) iterative numerical methods [202]; (ii) artificial intelligence-based methods [203], and (iii) resultant theory [204]. A new technique for the SHE method named Groebner Bases Theory Method has been developed [205,206]. This method has been carried out with a three-level inverter. This method has the advantage of finding the most accurate switching angles as no initial value for iteration is required.

Recently numerous evolutionary algorithms based on SHE techniques for MLI are reported in the literature [207–218]. Authors in [185,207] have implemented a genetic algorithm (GA) to minimize low-count switch MLI distortions. In [208,209], the output voltage regulation and improvement of the harmonic profile are carried out by particle swarm optimization (PSO) technique. Additionally, PSO is used in [210,211] for the control of THD. The ant colony system (ACS) algorithm was incorporated in [212] for removing the harmonic content of a 3-phase inverter with a unipolar output voltage waveform. Researchers have used bee algorithm (BA) for ninety-seven-level CHB-MLI [213]. THD reduction is brought about by bacterial foraging algorithm (BFA) in CHB-MLI. In [215], a clonal search algorithm (CSA) has been reported for a three-phase inverter. The harmonics in the line voltage of an inductor motor are eliminated using the evolutionary programming algorithm (EPA) as in [216]. Authors in [217,218] have suggested using the differential evolution (DE) algorithm for a 3-phase inverter to enhance the level of output voltage, improve the harmonic profile for rapid convergence and better efficiency.

4.1.3. Space Vector/Nearest Vector Control (SVC/NVC)

The space vector control (SVC) is also known as nearest vector control (NVC). It is reported as an alternative to SHE and can operate at a low switching frequency. Like SHE, it does not generate the average value of the required load voltage for every switching time interval. The major function of the SVC technique is to select a vector closest to the reference vector for minimizing the distance between them or the space error [187]. However, in SVC, the lower distortions produced due to switching at low frequency are usually not eliminated like in the SHE technique. The NVC technique is very simple and applicable for higher output voltage levels as the higher density of vectors can generate only small errors about the reference vector. Authors in [219] have discussed the principle of an eleven-level inverter with SVC control. Recently the SVC finds its implementation in numerous MLIs, including both classical as well as newly proposed reduced switch count technology. In [220], a five-level MLI configuration with quasi Z-source has been designed in which the NVC has been utilized as the control scheme.

4.1.4. Staircase with a Fixed Time Step Control Scheme

Staircase with a fixed time step control scheme generates the output voltage signal is generated from uniform time steps within each level. The main merit is that the structure is simple and hence makes the inverter control very easy. The major drawback is that the

output voltage profile consists of lower order harmonics and thus increases the THD. The waveform is divided into equal time intervals similar to the number of levels to find equal switching instants. In this control scheme, the inverter input voltage can be controlled, but the output voltage is not controllable.

4.2. High Switching Frequency Pulse Width Modulation (HSF-PWM) Techniques

The HSF-PWM techniques are usually employed for high switching frequency applications in the order of kHz and consist of many commutations per cycle [39]. A detailed classification of each type of this technique has been deliberated in this section.

4.2.1. Multi-Carrier Pulse Width Modulation (MC-PWM) Techniques

In this technique, only a single modulating sinusoidal signal is produced using multiple triangular carriers. Usually, the number of employed carriers is ' $(n-1)$ ', where ' n ' is the level of the inverter [39]. The MC-PWM techniques are further categorized into two types: (i) carrier disposition PWM and (ii) phase shifted PWM. The basic diagrams containing modulating and carrier signals for carrier disposition and phase shifted PWM methods have been reported by numerous authors in the literature [221,222].

Carrier Disposition Pulse Width Modulation (CD-PWM) Techniques

In this scheme, the reference waveform is produced by comparing the amplitude of the carrier waveform to a reference waveform amplitude. It is further classified into three various types [223]. The details of each are highlighted in this section.

(i) Phase Disposition (PD) Method

The important feature of the phase voltage spectrum of a PD Method is the initial distortion of the carrier. Therefore, this method generates a very good performance of the line voltage. Generally, all the carrier signals have equal amplitude and frequency and lie in one phase. PD method is usually used for asymmetric MLI, and with the increase in the number of voltage levels, the harmonic contents are decreased [224].

(ii) Phase Opposition Disposition (POD) Method

In this modulation scheme, the in-phase components are the positive carrier signals, whereas the carrier signals with negative polarity are 180° out of phase.

(iii) Alternative Phase Opposition Disposition (APOD) Method

This method involves all the carriers to be in phase opposition by 180° to the nearest carriers [224].

Phase-Shifted Pulse Width Modulation (PS-PWM) Technique

In the PS-PWM method, the multiple carriers are phase-shifted accordingly. It requires ' $(m-1)$ ' triangular carriers for an ' m '-level inverter. This triangular carrier possesses identical frequency and amplitude; however, adjacent carriers have a definite phase shift between them [225]. The gate signals of the MLI switches are produced with the help of the on/off state of some logic circuit switches [224].

4.2.2. Hybrid Pulse Width Modulation (H-PWM) Technique

The low-frequency and high-frequency modulation techniques are combined to form H-PWM. This control scheme is applied for CHB-MLI having a varying magnitude of DC sources. This method majorly aims to lower the inverter's losses by reducing the switching frequency of the higher power units. The lower power unit is controlled by using the unipolar pulse width modulation method [224].

Table 3. Comparative study highlighting the merits and demerits of basic modulation schemes.

Modulation Schemes	Merits	Demerits	References
Sine Property	<ul style="list-style-type: none"> ➤ Easy performance of simulations ➤ Has constant switching frequency ➤ Easy thermal design 	<ul style="list-style-type: none"> ➤ Requires more computational efforts 	[191–193]
Selective Harmonic Elimination (SHE)	<ul style="list-style-type: none"> ➤ Ability to eliminate lower order harmonics ➤ Low harmonics ➤ Reduced output filter size ➤ Appropriate for high power application ➤ High efficiency ➤ Low losses during switching operation ➤ Better steady-state response 	<ul style="list-style-type: none"> ➤ Overall dynamic response is slower ➤ Ineffective voltage balancing operation ➤ Requires massive passive filters 	[194–218]
State Vector Control (SVC)	<ul style="list-style-type: none"> ➤ Can operate at low switching frequency ➤ Simple technique ➤ Low harmonics with high efficiency ➤ Less number of switching states ➤ Lower dv/dt stress ➤ Better dynamic response ➤ Does not require huge passive filters 	<ul style="list-style-type: none"> ➤ Lower order harmonics generated are not eliminated ➤ Complex for structure involving more number of voltage levels 	[187,219,220]
Phase Shifted PWM (PS-PWM)	<ul style="list-style-type: none"> ➤ Modular and simple structure ➤ Rotation of switching patterns is not required 	<ul style="list-style-type: none"> ➤ High harmonic content ➤ Poor voltage balancing strategy ➤ Poor dynamic response 	[224,225]
Phase Disposition PWM (PD-PWM)	<ul style="list-style-type: none"> ➤ Better voltage profile ➤ Optimal switching is achieved ➤ All carriers have same frequency and amplitude 	<ul style="list-style-type: none"> ➤ Uneven power distribution ➤ Poor dynamic response 	[224]

4.2.3. High and Low Carrier Cells and Alternative Phase Opposition Pulse Width Modulation (HLCCAPO-PWM) Technique

HLCCAPO-PWM is a modification of the PD method. Here two different carrier groups are introduced by dividing them as per each carrier period. The method renders the use of higher modulation frequency by reducing the switching losses effectively. Further, this technique also reduces the dissipation of energy as the energy shifts from the lower to higher-order harmonics. It mostly finds its application in hybrid clamped MLI.

4.2.4. Space Vector Pulse Width Modulation (SV-PWM) Technique

The SV-PWM technique consists of many vector states that are utilized for modulation of the reference waveform. This method is usually based on the digital modulation method for generating PWM voltages under a known voltage [226]. Here the values of the control algorithm are directly taken from the control system [227]. However, this scheme fails to operate with a large number of levels as identifying sectors and selecting switching sequences are very crucial. Generally, for an 'n'-level inverter, ' $(n - 1)^2$ ' vector combination per sector, six sectors, and ' n^3 ' switching sequences are required [228]. Reduction in the common-mode voltage, losses due to switching, and the control of the DC link voltages can be brought about by appropriate selection of modulation vector and switching combinations. Generation of a particular voltage level takes place by redundancy switching states.

Various authors have reported in the literature the application of this technique in numerous areas. In [229], a space vector hysteresis current control (SVHCC) scheme has been implemented. The SVHCC has been used with a recent MLI configuration, as suggested in [230]. The use of SVC is also projected in [231] for a T-type MLI system that implements a fault-tolerant control scheme. Amit Kumar Gupta et al. in [232] addressed a simple SV-PWM method for MLI operation in the over-modulation range. In [233], Mohan M. Renge suggested a technique for reducing common-mode voltage at the output of MLI that used the 3-D SV-PWM technique.

Better values of fundamental voltage ratio and harmonic elimination are achieved in this technique as compared to the sinusoidal PWM method. In addition, the maximum peak value of the output voltage is almost 15% more in SV-PWM than in the triangular carrier-based modulation method. Although the requirement of a look up table and identification of sectors for determining the switching intervals for all sectors make the SV-PWM technique complex, the microprocessor and digital signal processing units serve as a better solution for preparing the preparation of the process the algorithm.

5. Applications of MLI Topologies and Control Schemes

This section throws light on the detailed application of various MLI topologies and control schemes in different fields of power system networks, such as (i) integration of RERs to grid; (ii) FACTS devices, and (iii) electric motor drives. Table 4 provides a brief idea of the application of various MLI topologies in numerous power system domains.

Table 4. Application of various MLI topologies in numerous power system domains.

MLI Topologies	Applications
NPC-MLI	<ul style="list-style-type: none"> ❖ High speed motor drives ❖ Renewable energy ❖ Power systems
FC-MLI	<ul style="list-style-type: none"> ❖ Renewable energy ❖ Motor drives
ANPC-MLI	<ul style="list-style-type: none"> ❖ Renewable energy (solar inverters) ❖ Active power filters
CHB-MLI	<ul style="list-style-type: none"> ❖ FACTS ❖ Renewable energy ❖ Drives

Table 4. Cont.

MLI Topologies	Applications
HCHB-MLI	<ul style="list-style-type: none"> ❖ Motor drives ❖ Renewable energy
MLDCL-MLI	<ul style="list-style-type: none"> ❖ PM motor drives (<100 KW) ❖ MOSFETs ❖ IGBTs ❖ Solar and fuel cell integration
SSPS-MLI	<ul style="list-style-type: none"> ❖ Renewable energy ❖ Vehicle drive system ❖ Traction purposes
T-type-MLI	<ul style="list-style-type: none"> ❖ AC drive system ❖ Renewable energy ❖ Power train drive
N-MLI	<ul style="list-style-type: none"> ❖ Renewable energy ❖ Medium/high voltage industries
CCHB-MLI	<ul style="list-style-type: none"> ❖ Motor drives ❖ FACTS ❖ Renewable energy
RV-MLI	<ul style="list-style-type: none"> ❖ FACTS ❖ HVDC
SCSS-MLI	<ul style="list-style-type: none"> ❖ Electric vehicles ❖ FACTS ❖ Submarine propulsion
MLM-MLI	<ul style="list-style-type: none"> ❖ Renewable energy
2SELG-MLI	<ul style="list-style-type: none"> ❖ HVDC ❖ Renewable energy
HBTPM-MLI	<ul style="list-style-type: none"> ❖ Renewable energy
CCS-MLI	<ul style="list-style-type: none"> ❖ Photovoltaic system
PUC-MLI	<ul style="list-style-type: none"> ❖ Motor drives ❖ Renewable energy
CBSC-MLI	<ul style="list-style-type: none"> ❖ Renewable energy
M-MLI	<ul style="list-style-type: none"> ❖ HVDC ❖ Wind systems
B-MLI	<ul style="list-style-type: none"> ❖ HVDC

5.1. Grid Integration of RERs

The control schemes for RERs integration are categorized as (1) time and (2) frequency domain schemes. Fast Fourier Transformation is usually not employed because of more computational time and delay in computing reference signals [234]. On the other hand, p-q theory and d-q theory based on time-domain control algorithms are highly adopted due to lesser computation time in deriving the instantaneous compensating current or voltage signals. The DC quantities are assumed to be the fundamental components in the d-q algorithm. Furthermore, authors in [80] have studied the sensorless control of voltage waveform in packed U-cell topology to reduce control complexity and redundancy switching state. This operation keeps the capacitor voltage constant at half the magnitude of the DC source. Figure 27 depicts the controller for adjusting the amplitude and the phase shift of the current injected from the inverter to the grid.

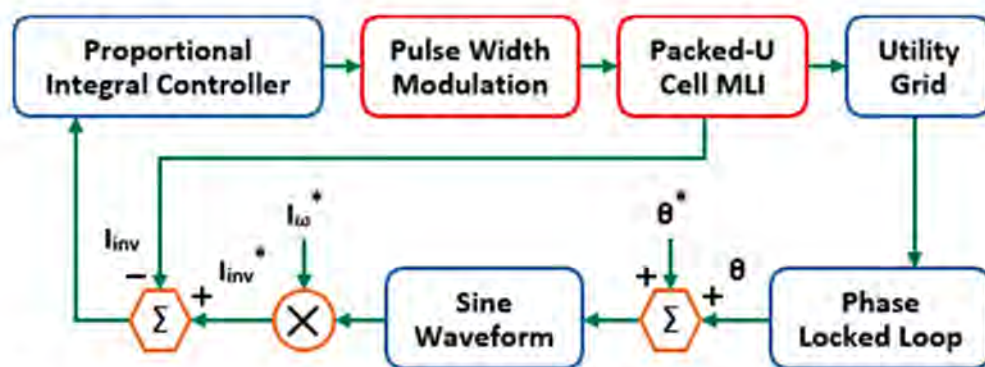


Figure 27. Block diagram of a single phase grid connected packed U-cell based MLI.

In [235–237], researchers have addressed the use of a solar-based MLI for enhancement in the waveform quality and reduction in issues on power quality. For a three-level NPC-MLI, instantaneous power theory control is studied for generating the perfect reference signal. Here, two control loops are defined, one for controlling the DC bus voltage and the other for controlling the current. Source active power and load reactive power are computed using the fuzzy logic controller (FLC), and in the α - β reference frame, the p-q theory was used to find the reference current [238]. Authors in [239] have proposed a digital proportional integral (PI) Controller to inject the current from the photovoltaic source to the utility grid to achieve maximum dynamic operation with minimum harmonics. Figure 28 describes the block diagram of the control part of the above study, which comprises maximum power point tracking (MPPT) control and inverter control.

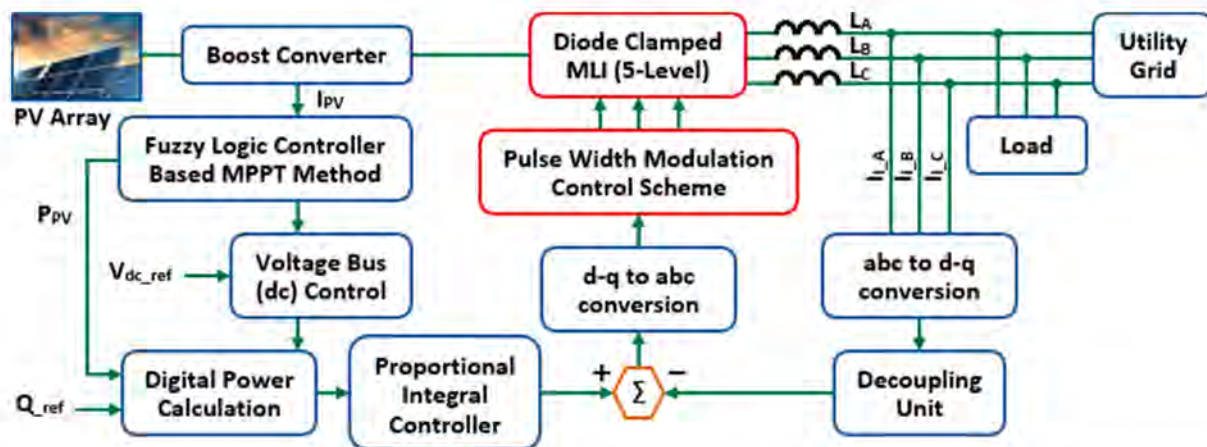


Figure 28. Block diagram of grid tied PV system with digital proportional integral control and fuzzy logic control.

The authors have introduced the dual-loop control method for a three-level inverter, as demonstrated in Figure 29. Here, two loops are present, the outside loop controlling the DC bus voltage and the current being controlled by the inner loop [240]. In NPC-MLI, the predictive control method is utilized to balance the DC link voltage. As suggested by authors in [241], a dual loop d-q controller is used to control the active and reactive power distribution. Different topologies of MLI in various combinations are interfaced with RERs for grid-tied applications [242–248]. In the recent past, the MLI topologies are also applied for application in the areas of marine [245] and microgrid [246,249].

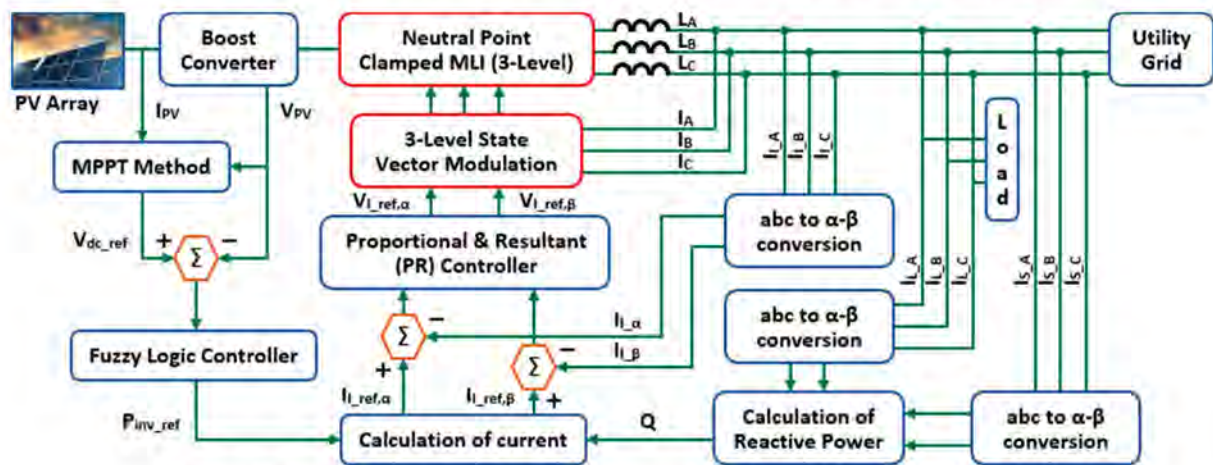


Figure 29. Block diagram of the dual loop control method for a three-level inverter.

5.2. FACTS Device

STATCOM is considered to be a vital controller among all other types of available FACTS devices. The most appropriate topology for STATCOMs operation is the CHB-MLI for direct connection to medium voltage networks [250]. It does not need injecting active power for a normal range of operation [251]. In [17,252], authors have reported that CHB-MLI can be placed in series to achieve the operational voltage without using a transformer. A reactive current reference control scheme is proposed to enhance the transient operation of STATCOM, as depicted in Figure 30. In Figure 30, the phase locked loop (PLL) block is utilized to determine the reference phase angle of the grid voltage. The STATCOM output voltage and current are transformed into d-q reference frame vectors by adopting Park’s Transformation. The feedback operation is preferred by the controller and produces the switching pulses with a proper modulation index.

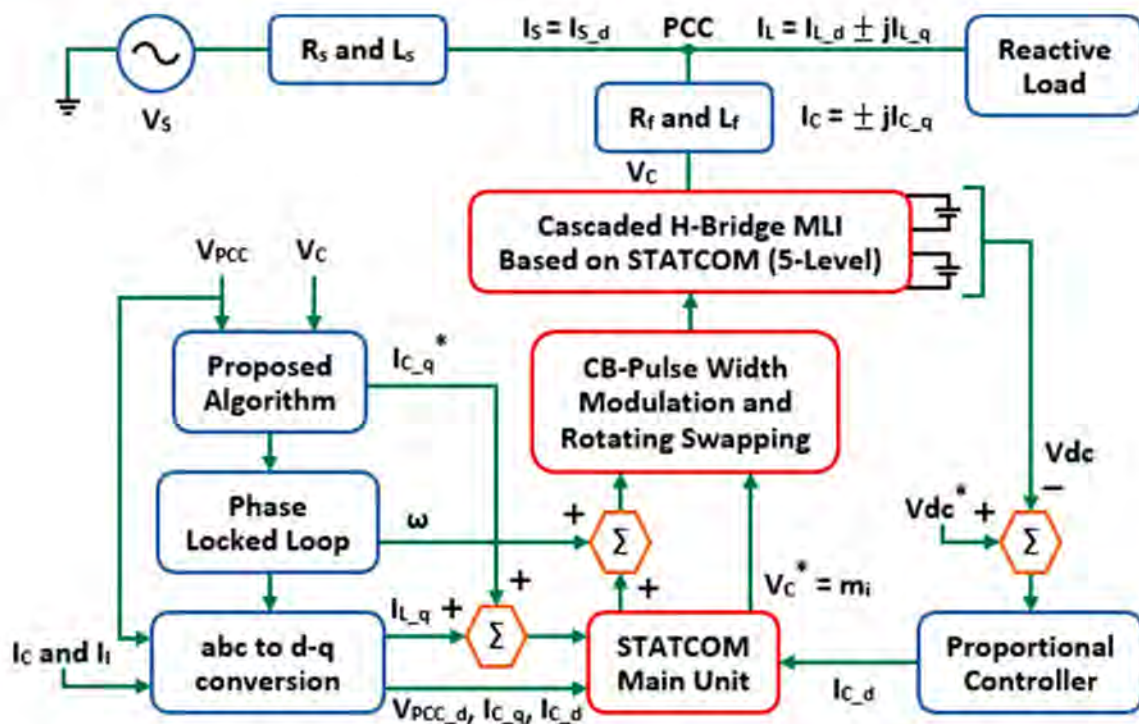


Figure 30. Block diagram for control technique for STATCOM application.

Researchers have suggested a novel hybrid control method for STATCOM application for delta CHB-MLI subjected to an unbalanced condition [253]. A current control method is proposed for every phase individually to control every link's active and reactive power independently. The hybrid control approach consists of four different parts as follows: (i) PLL; (ii) active current reference; (iii) reactive current reference; and (iv) instantaneous current tracking. The PLL determines the phase angle of the system. However, the compensation model is used to calculate the amplitude of the voltage, which lags the phase of reactive current by 90° . The overall value of phase current can be obtained by summing up the active and reactive current reference [254].

DVR plays a vital role in eliminating voltage-related problems like sudden rise or fall of voltage, spikes, swell, etc. It injects a voltage to prevent any disturbance in the load side voltage and is connected in series with the source side voltage [255]. The use of MLI in DVR enhances the capability of voltage injection to the maximum that can be applied for medium voltage application without using a transformer [256]. Here, the grid voltage and reference voltage comparison yield the reference value for the DVR output voltage (voltage sag value). PI controller is utilized to regulate the voltage level of the load and output voltage of the boost converter having a feedback control. The reference signal of MLI can be calculated by dividing the control output by the DC link voltage. The transformation ratio of the boost converter can be computed by its duty cycle. A crucial issue in DVR is the transformer's magnetic saturation, which causes the production of a large inrush current. Authors in [257] have suggested a novel modulation scheme called direct magnetizing flux linkage control for preventing the transformer from getting saturated, as illustrated in Figure 31. The overall modulation approach is divided into three loops depending upon their functions.

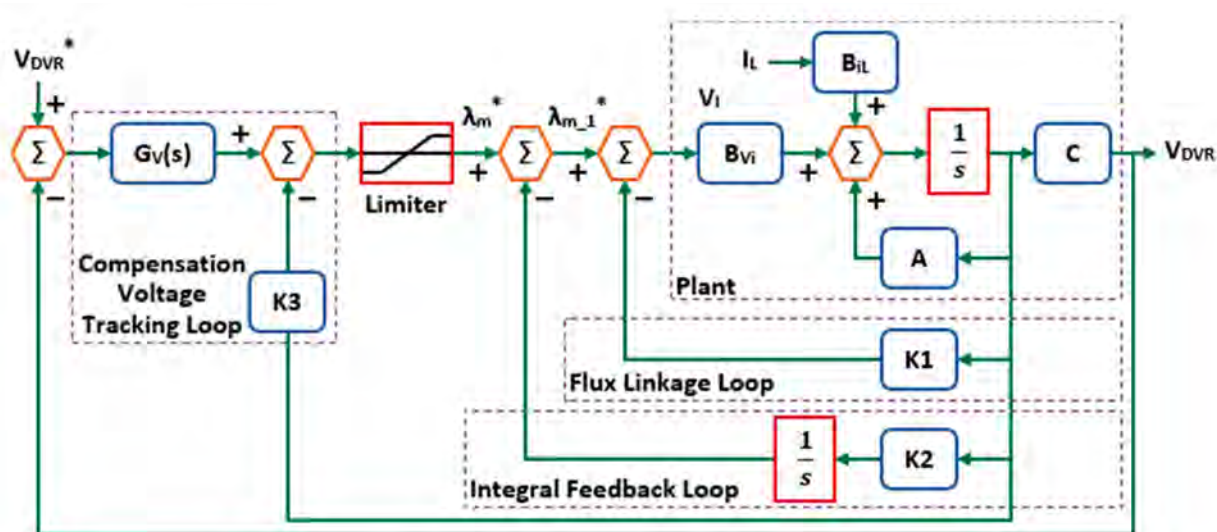


Figure 31. Block diagram for direct flux linkage control technique in DVR.

Loop 1 is called the flux linkage loop for tracking the flux linkage command. For attenuating the DC flux, linkage loop two, known as the integral feedback loop, is present. Loop 3 is utilized for tracking the compensation voltage command. To limit the linkage of flux, a flux linkage limiter is added between loop two and loop 3. Researchers in [258,259] have discussed the importance of MLI for unified power quality controller (UPQC) operations. A CHB-MLI is applied for DVR operation in [260].

5.3. Motor Drives

The basic necessity for an extraordinary function of an electric motor drive unit is its accurate torque control. A deep insight into the present literature reveals that control of field and torque for an induction machine serve as the two most remarkable control

schemes [261]. In [262], authors have stated that direct control of torque can be directly switched on to an inverter without needing the regulation of stator current. However, the torque and flux generating units are separately controlled for field control. In [263], a recent control scheme is proposed for IM by CHB-MLI prone to a faulted condition. The block diagram of rotor flux linkage-oriented control as used in [263] is demonstrated in Figure 32. In [264–266], artificial neural network control [267] is used in IM to improve performance parameters. In addition to that, a reduced switch count MLI topology was executed with IM control for enhancing the quality of power, thereby lowering the THD of the output voltage.

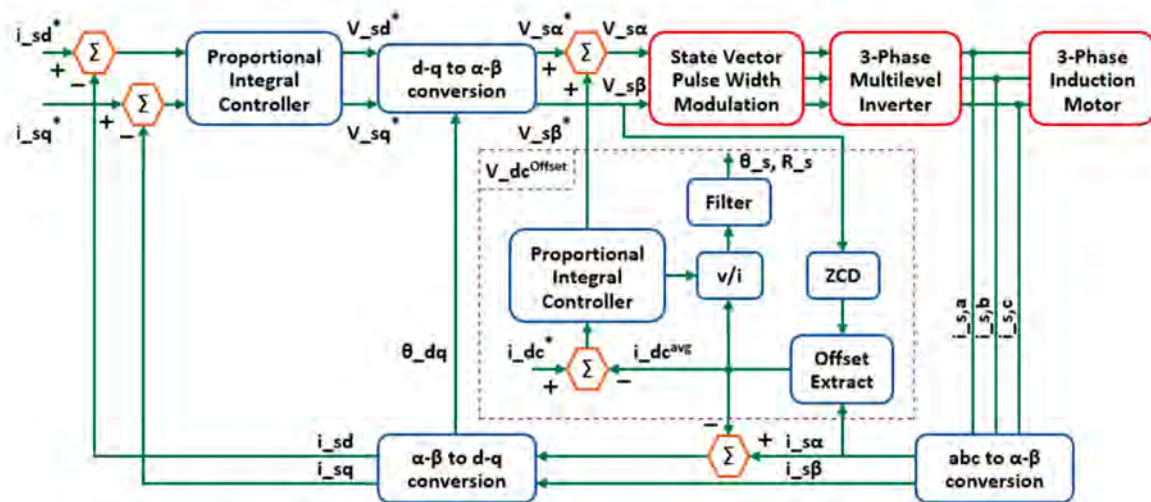


Figure 32. Block diagram for rotor flux linkage oriented control method of motor drive system.

6. Future Work

MLIs undoubtedly have been the state of art and technology for power conversion from DC to AC, electrical energy employment, and a wide range of power applications in the present era. However, some of the major shortcomings in the implementation of MLI technology can be listed: (i) cost of manufacturing enhances as the number of switching devices used is more and (ii) addition of power electronic units may lead to the incorporation of more gate driving circuits, voltage and frequency control methods and complicated switching techniques making the control unit more complicated.

In order to cope up with the above issues, researchers are opting out ways for a trade-off among the increased levels and complications in the design and working. Intending to assist the hassle-free integration of MLI technology in the present era, this comprehensive review has suggested some vital points that can be adopted in the future for further possible enhanced application of MLI technology in the various field of power systems.

- (1) More research on contemporary topologies regarding the use of less power electronic interfaces, low cost, enhanced reliability, and efficiency should be developed.
- (2) Studies on designing a less complex inverter should be carried out.
- (3) Semiconductors with a large bandgap can be adopted for considerable increment in the switching frequency, thus facilitating the use of the smaller size of switching units.
- (4) The control and modulation schemes for MLI implementation should be further enhanced with more robust, modular, and fault-tolerance capability.
- (5) More in-depth work in the area of numerical methods for the solution of non-linear equations of MLI needs to be undertaken.
- (6) Extensive study is also required to balance the rise in temperature of the semiconductor devices used in the MLIs.
- (7) Integration of faster microprocessor units with the ability to work with high-level inverters and faster switching device applications should be adopted.

- (8) Building up more robust modulation schemes to assure uniformity in the rise of temperature of all devices and reduction in the complication of the controllers.
- (9) Design of reduced capacitor size by undertaking new voltage balancing methods needs to be used in MLI to enhance inverter's power density.
- (10) Setting up of resonant converters basing on single DC source MLIs is recommended.

7. Conclusions

The upgradation and advancement of different industries and academic research globally have led to an increased demand for high energy-based efficient converters. The MLIs have attained tremendous demand due to their inherent merits and play a significant role in DC/AC conversion operations for both high/medium voltage and high power applications. In this regard, this review article attempts to critically survey the evolution of MLIs, which would serve as a prominent guideline for the researchers working in this area. This comprehensive paper throws light on the traditional MLI topologies, new reduced switch count topologies, various control approaches, applications of MLI to renewable energy interface, FACTS devices, and motor drives in detail. A thorough review of the literature reveals that the recently developed reduced switch count MLI topologies possesses many merits over the classical techniques in terms of better clarity of output waveform, low modularity, reduced number of switches, occupies minimum space, ease of control, and cost effectiveness.

Further, for easy analysis, a precise comparison among all the categories of MLI about advantages and shortcomings has been tabulated. This research article also projects a thorough idea about all conventional and newly adopted modulation techniques for different MLI topologies. This review also serves as a major objective to understand the vital role played by MLI in the areas of application for renewable energy, FACTS devices, and electric motor drives. The article's primary focus is the suggested key points to be incorporated in future research work to integrate the MLI technology more efficiently. The article is promising for obtaining maximum useful knowledge to the academicians, pursuing research in MLI field, in the fact of the suitable configuration selection for definite operation, proper schemes of switching and control, parameter selection and manifests real-time application to other sectors of the power system.

Author Contributions: Conceptualization, S.C and T.D; methodology, S.C.; validation, M.B., S.K. and F.J.; formal analysis, S.C and F.Z; investigation, S.C and M.B.; resources, S.K. and F.J.; writing—original draft preparation, S.C.; writing—review and editing, S.C, and T.D.; supervision, F.J.; All authors have read and agreed to the published version of the manuscript.

Funding: This research received no external funding.

Institutional Review Board Statement: NA.

Informed Consent Statement: NA.

Data Availability Statement: Authors may provide data on due request.

Conflicts of Interest: The authors declare no conflict of interest.

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