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Design of a Highly Efficient N-Stage Harmonic Terminated Voltage Multiplier for Wireless Power Transfer

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Abstract: This paper proposes a 5.8 GHz highly efficient rectifier design using harmonic termination for wireless power transfer. The diode used to convert the received RF power to DC is a non-linear device, and a harmonic component is generated, which causes performance degradation. Therefore, in this paper, we designed a band stop filter for harmonic termination and proposed the N-stage harmonic terminated voltage multiplier (N-stage HTVM). The number of stages N can be designed differently to operate with high efficiency at various input powers for the proposed rectifier. In the proposed rectifier circuit, mathematical analysis of output DC voltage, power loss of the diode, and the power conversion efficiency (PCE) were evaluated through voltage/current waveform analysis of the diode. The design method of the filter for terminating harmonics is presented. Furthermore, the change of PCE according to the increase in the number of stages was analyzed using the equivalent model of the proposed circuit and verified through measurement. The maximum PCE of one-stage HTVM was 68% when 18 dBm of input power was applied. The DC output voltage was measured to 11.6 V. When the RF input power was 25 dBm and the load was 1500 Ω , the maximum PCE of the two-stage HTVM was 71% and the maximum DC output voltage was measured as 15.8 V. The measured performance of three-stage HTVM had a PCE of 67% and DC output voltage of 19.8 V when the input power was 30 dBm.

Keywords: 5.8 GHz wireless power transfer; harmonic termination; filter; N-stage harmonic terminated voltage multiplier (N-stage HTVM)



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1. Introduction

Microwave wireless power transfer (MRWPT) is being actively studied as a technology for wireless charging in various environments, such as artificial satellites, medical devices, and smart offices. MRWPT is a method of radiating generated microwave power to phased array antennas and supplying power through an electromagnetic field. MRWPT can transmit a longer distance than magnetic resonant WPT, but the power transfer efficiency (PTE) decreases as the transmitter (TX) and receiver (RX) distance increases. The performance of the MRWPT is determined not only by the PTE but also by the power amplifier (PA), phased array antenna (PAA), beamforming algorithm and receiver performance [1].

The RX for MRWPT is used not only for WPT but also for energy harvesting. It consists of an array receiving antenna, the impedance matching unit, the rectifier, and a load. The part that determines the performance of the receiver is the rectifier. There are various rectifier design methods [1–6]. A half-wave rectifier circuit [1,2] can convert the input signal in the positive or negative region to DC by arranging Schottky diodes in series or shunts. A series of diode rectifiers was proposed, and a dual-band rectenna at 2.4 and 5.8 GHz was designed [1].

The power conversion efficiency (PCE) of the rectifier is 63% at 2.4 GHz and 54.8% at 5.8 GHz at an input power of 10 mW. A shunt diode rectifier using load-pull [2] has PCE of 63% at an input power of 10 dBm. Although the shunt diode rectifier requires low

design difficulty with simple structure, it has low rectification efficiency and a very high impedance of the load. A full-wave rectifier circuit, which converts the entire input signal to DC using two or four Schottky diodes, with harmonic termination of 5.8 GHz signal has PCE of 65.3% at 15 dBm [3]. It has higher rectification efficiency than a half-wave rectifier circuit [1].

However, its structure is complicated. A Class C single Schottky diode rectifier and Class F⁻¹ GaN transistor rectifier based on the power amplifier theory was also proposed [4]. A Class C rectifier operating at a 2.45 GHz band uses a shunt diode shorted to the second and third harmonics. It has a PCE of 72% at an input power of 7 dBm [4]. A Class F rectifier using even order harmonic control with shorted stubs and odd order harmonic control with open stubs has been proposed [5]. When operating at 5.81 GHz, it has a PCE of 69.2% using series diode and harmonic cancellation at an input power of 8.2 dBm [5]. A Class F rectifier using Dickson charge pump in 5.2 GHz band has a PCE of 64% at an input power of 23 dBm [6].

As mentioned above, there have been studies on the design of rectifiers using various topologies. However, Refs. [5,6] targeted systems that convert relatively low RF power into DC, such as energy harvesting and Internet of Things (IoT) sensor driving. However, the power density delivered to the receiver varies depending on the surrounding environment and location. In the wireless power transfer environment, the received power density changes due to the distance of the transmitting/receiving antenna, beamforming performance, etc., in particular.

Existing topologies [5,6] are challenging to apply to a wireless power transfer system to which a high power density is used due to the performance limitations of diodes. Therefore, it is necessary to design a rectifier with high PCE according to various input powers. This paper proposes a rectifier design that shows PCE when high power density is applied in various wireless power transfer environments.

Ref. [7] proposed a rectenna design that exhibits more than 50% PCE in a wide range of input power (−10~25 dBm) in a wireless power transfer system. Ref. [7] designed an impedance matching unit according to low power density and high power density and showed a maximum PCE performance of 70.2% at an input power of 17 dBm. Ref. [8] proposed array rectifiers with an adaptive power distribution network (APDN). APDN consists of a rectifier cell for high frequency and high power and a rectifier cell for low frequency and low power intensity.

Ref. [9] designed a rectenna showing high PCE (86%) performance at high input power (27 dBm) in a scenario where multi-tone (1.7 GHz and 2.4 GHz) is applied to the receiver. Ref. [10] proposed a rectifier designed to operate in various frequency ranges by using harmonic termination when a two-tone or four-tone signal is applied to the receiver.

Ref. [11] proposed a power recycling network (PRN) during a study to receive a wide input power range in a wireless power transmission environment and showed more than 50% PCE performance in the input power range of 10.5~31.8 dBm. The PRN consists of two rectifier cells, and unlike [8], an impedance matching unit was designed so that the reflected power can be applied to other rectifier cells.

Ref. [12] proposed a structure of two rectifier cells like [8,11], and, to compensate for the reflected power, a hybrid coupler and a phase shift unit were implemented. The rectifier circuit proposed in [12] showed more than 50% of PCE performance even when the size range of the load (8 to 97 kΩ) was wide. The diodes used in studies covering the low input power range to the wide input power range were mainly Schottky diodes. Ref. [13] proposed a wire-bonded GaN diode rectifier to show high performance at high input power.

As above, existing studies have proposed a rectifier operating at relatively low power and high load impedance [1–6], or a receiver operating over a wide input power range in a changing wireless power transfer environment [7–12]. Alternatively, a rectifier using a GaN device for high input power has been proposed. GaN diodes exhibit higher breakdown voltage characteristics than Schottky diodes made of silicon, and thus they are suitable for

high input power devices. The design difficulty of GaN diodes in the C-Band (4~8 GHz) or higher band is very difficult, and the manufacturing cost is high.

However, to sufficiently supply power to devices, such as sensors and smartphones through PAA beamforming, it is necessary to design and mathematically analyze a rectifier with high PCE performance at high input power. Since a diode or transistor, which is a core element of a rectifier, is a nonlinear element, it is essential to design it through a nonlinear analysis and a behavioral model [14,15]. In addition, a diode must be selected according to the input power level, and a rectifier was designed based on the electrical characteristics of the adopted diode.

In this paper, we propose a method to derive the output voltage, current, and power loss of the rectifier to be designed using a nonlinear mathematical approach based on the electrical characteristics of the diode. Therefore, the proposed method was analyzed using the voltage and current waveforms of diodes, and a harmonic termination filter was designed to improve switching efficiency. Finally, an N-stage harmonic terminated voltage multiplier (N-stage HTVM) was designed. The proposed N-stage HTVM was analyzed with mathematical analysis of the diode waveform and power loss of the diode.

This paper is prepared with the following structure. First, the mathematical analysis of the proposed rectifier is shown in Section 2. Section 3 describes the design process of the harmonic termination filter. The performance of the N-stage HTVM is validated by simulation and measurement in Section 4, and our conclusions are made in Section 5.

2. N-Stage Harmonic Terminated Voltage Multiplier Theory

A one-stage voltage multiplier (VM) consists of two diodes and two capacitors with DC voltage twice the input voltage as output. However, the output voltage decreases due to the built-in potential (threshold voltage) the loss caused by parasitic components and junction capacitors. Therefore, the N-stage VM is composed of diodes and capacitors with a DC voltage of less than the input voltage as output.

Figure 1 shows the circuit diagram of N-stage HTVM. A harmonic terminated rectifier, like Class F or Class F⁻¹, has different performances depending on which diode the filter is positioned. The design method of the filter is also different. In this paper, if there are diodes, the harmonic termination filter is placed behind the diode. Impedance characteristics of the harmonic termination filter applied in the proposed rectifier show that the impedance of the even order term is short, and the impedance of the odd order term is open, like a Class F rectifier.

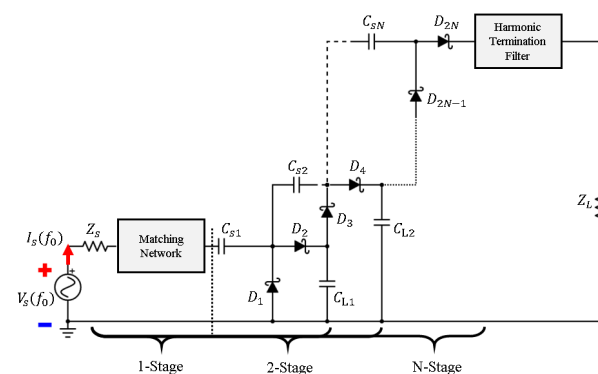


Figure 1. The proposed N-stage HTVM schematic.

2.1. Mathematical Analysis of N-Stage HTVM under Breakdown Voltage Region

If characteristics of the harmonic termination filter show that the impedance of even order is short and that of odd order is open and that the filter is located behind the diodes arranged in series shown in Figure 2a. The voltage and current waveforms of the diode connected to the shunt will appear as sine waves, respectively, as shown in Figure 2b.

The voltage waveform of the diode will appear as a square wave as shown in Figure 2c in the low input power region and the current waveform will appear as a sine wave when the voltage is 0. The voltage will appear as a non-zero value in the section due to the built-in potential. However, as shown in Figure 2, the diode voltage and current waveforms are satisfied in the low power region when the input power before the breakdown voltage of the diode is applied.

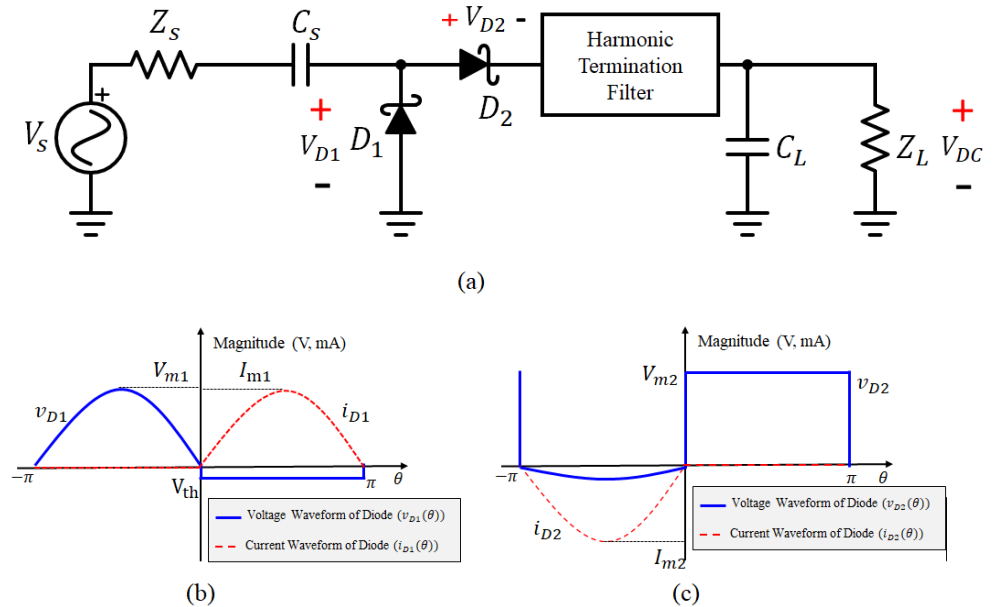


Figure 2. One-stage HTVM circuit diagram and diode waveforms in low power region. (a) One-stage HTVM circuit diagram; (b) voltage and current waveform of diode D_1 ; and (c) voltage and current wave-form of diode D_2 .

In Figure 2a, C_s is the charging capacitor for boosting voltage, v_s is the source voltage, Z_s is the source impedance, v_{D1} and v_{D2} are the voltages across diodes D_1 and D_2 , C_L is the equalization capacitor, Z_L is the load impedance, where V_{DC} is output DC voltage, and V_{m1} and V_{m2} are the maximum magnitude of v_{D1} and v_{D2} . I_{m1} and I_{m2} are the maximum magnitudes of i_{D1} and i_{D2} where current is flowing through D_1 and D_2 . R_s is the parasitic resistance in the diode. The voltage and current in Figure 2b are expressed as Equations (1) and (2) as shown in Figure 2c.

$$v_{D1}(\theta) = \begin{cases} V_{m1} \sin \theta & -\pi < \theta < 0 \\ -V_{th} & 0 < \theta < \pi \end{cases} \quad i_{D1}(\theta) = \begin{cases} 0 & -\pi < \theta < 0 \\ I_{m1} \sin \theta & 0 < \theta < \pi \end{cases} \quad (1)$$

$$v_{D2}(\theta) = \begin{cases} -V_{th} + I_{m2}R_s \sin \theta & -\pi < \theta < 0 \\ V_{m2} & 0 < \theta < \pi \end{cases} \quad i_{D2}(\theta) = \begin{cases} I_{m2} \sin \theta & -\pi < \theta < 0 \\ 0 & 0 < \theta < \pi \end{cases} \quad (2)$$

DC components (V_{01} and V_{02}) of the voltage across D_1 and D_2 during one cycle, can be expressed as Equations (3) and (4).

$$V_{01} = \frac{1}{2\pi} \int_{-\pi}^{\pi} v_{D1} d\theta = \frac{2V_{m1} - \pi V_{th}}{2\pi} \quad (3)$$

$$V_{02} = \frac{1}{2\pi} \int_{-\pi}^{\pi} v_{D2} d\theta = \frac{-2I_{m2}R_s - \pi V_{th} + V_{m2}}{2\pi} \quad (4)$$

where V_{th} is the built-in potential of the diode. V_{DC} across the load can be expressed as Equation (5) where N is the number of stages (consisting of one shunt diode and one series diode):

$$V_{DC}(N) = N(V_{01} + V_{02}) = N \frac{2V_{m1} + V_{m2} - 2\pi V_{th} - 2I_{m2}R_s}{2\pi} \quad (5)$$

where ω is the angular frequency. Since the output voltage is calculated, the DC output power $P_{out} = V_{DC}I_{DC} = V_{DC}^2/Z_L$ is defined, and PCE η is defined as Equation (6):

$$\eta = \frac{P_{out}}{P_{out} + P_{loss}} \quad (6)$$

P_{loss} consists of a loss due to the built-in potential of the diode and the junction capacitor. Losses like these can cause an overlap section between the voltage and current waveforms of the diode. In Figure 2c, overlap sections of v_{D2} , i_{D2} are defined as Equation (7). In the case of D_1 , the power loss is zero since there is no overlapping section.

$$P_{loss,V_{th}} = \frac{1}{2\pi} \int_{-\pi}^0 v_{D1} i_{D1} d\theta = \frac{I_{m2}(I_{m2}R_s\pi + 4V_{th})}{4\pi} \quad (7)$$

A junction capacitor C_j exists inside the diode. This component generates a rising edge loss and a falling edge loss when the diode is turned on and off. The rising edge and falling edge are factors that cause voltage and current waveforms to overlap with each other and lead to a loss. These losses can be calculated with Equations (8)–(10), where f is the operating frequency and δ is the Dirac delta function [16]. The magnitude of the rising edge loss and falling edge loss is proportional to the magnitude and frequency of the junction capacitor. Since the voltage waveform of D_1 is not dynamically switched, losses caused by the junction capacitor are neglected.

$$v_{D2} \Big|_{t=0} = \frac{1}{2}(v_{D2}|_{t=0^+} + v_{D2}|_{t=0^-}) = \frac{V_{m2}}{2} \quad (8)$$

$$i_{D2} \Big|_{t=0} = C_j \frac{dv_{D2}}{dt} \Big|_{t=0} = C_j v_{m2} \delta(t - 0) \quad (9)$$

$$P_{loss,C_j} = \frac{1}{2\pi} \int_{-\pi}^{\pi} v_{D2}|_{t=0} i_{D2}|_{t=0} d\theta = \frac{1}{2} f C_j V_{m2}^2 \quad (10)$$

If Equations (7) and (10) are arranged with the number of stages, the following is obtained:

$$P_{loss}(N) = N(P_{loss,V_{th}} + P_{loss,C_j}) = N \frac{2\pi V_{m2}^2 f C_j + I_{m2}(I_{m2}R_s\pi + 4V_{th})}{4\pi} \quad (11)$$

By substituting Equations (5) and (11) of V_{DC} and P_{loss} into Equation (6), PCE under breakdown voltage η_1 is arranged as follows, where $B = 2V_{m1} + V_{m2} - 2\pi V_{th} - 2I_{m2}R_s$

$$\eta_1 = \frac{V_{DC}^2}{V_{DC}^2 + Z_L P_{loss}} = \frac{NB^2}{NB^2 + \pi Z_L \{2\pi V_{m2}^2 f C_j + I_{m2}(I_{m2}R_s\pi + 4V_{th})\}} \quad (12)$$

2.2. Mathematical Analysis of N-Stage HTVM over Breakdown Voltage Region

In a diode, the current flows in a forward direction. No current flows in the reverse direction. However, if the reverse voltage is continuously raised, a current can suddenly flow at any moment. The voltage at this time is called the breakdown voltage. When a voltage greater than the breakdown voltage is applied to the diode in the reverse direction, leakage current will flow, which is the main cause of degradation of the diode parameters.

When the region above the breakdown voltage is referred to as the high power region, the voltage and current waveforms of the diode overlap each other more than the low power region and appear, including a leakage current. Figure 3 shows the voltage and current waveforms of D_1 and D_2 over the breakdown voltage region.

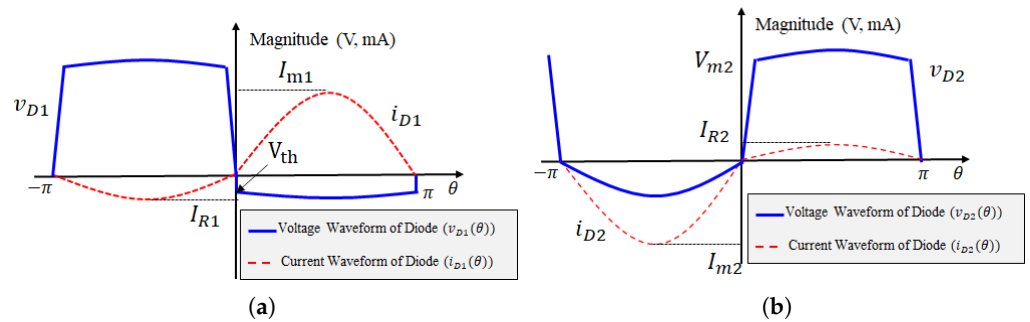


Figure 3. One-stage HTVM circuit diagram and diode waveforms over the breakdown voltage; (a) voltage and current waveform of diode D_1 ; (b) voltage and current waveform of diode D_2 .

Assuming that the voltage and current of the diode for one cycle in the high power region are $v_{D1_{br}}$, $v_{D2_{br}}$, $i_{D1_{br}}$, and $i_{D2_{br}}$, the following equations are given.

$$v_{D1_{br}}(\theta) = \begin{cases} V_{br} + I_{R1}R_s \sin \theta & -\pi < \theta < 0 \\ -V_{th} + I_{m1}R_s \sin \theta & 0 < \theta < \pi \end{cases} \quad i_{D1_{br}}(\theta) = \begin{cases} I_{R1} \sin \theta & -\pi < \theta < 0 \\ I_{m1} \sin \theta & 0 < \theta < \pi \end{cases} \quad (13)$$

$$v_{D2_{br}}(\theta) = \begin{cases} -V_{th} + I_{m2}R_s \sin \theta & -\pi < \theta < 0 \\ V_{br} + I_{R2}R_s \sin \theta & 0 < \theta < \pi \end{cases} \quad i_{D2_{br}}(\theta) = \begin{cases} I_{m2} \sin \theta & -\pi < \theta < 0 \\ I_{R2} \sin \theta & 0 < \theta < \pi \end{cases} \quad (14)$$

where V_{br} is the breakdown voltage, I_{m1} and I_{m2} are the maximum magnitudes of forward current, and I_{R1} and I_{R2} are the maximum magnitude of the reverse current. The DC voltage component $V_{01_{br}}$ and $V_{02_{br}}$ and power loss $P_{loss_{br}}$ can be obtained from the voltage and current waveform of the diode defined above.

$$V_{01_{br}} = \frac{1}{2\pi} \int_{-\pi}^{\pi} v_{D1_{br}} d\theta = \frac{\pi V_{br} - \pi V_{th} + 2I_{m1}R_s - 2I_{R1}R_s}{2\pi} \quad (15)$$

$$V_{02_{br}} = \frac{1}{2\pi} \int_{-\pi}^{\pi} v_{D2_{br}} d\theta = \frac{-2I_{m2}R_s + 2I_{R2}R_s - \pi V_{th} + \pi V_{br}}{2\pi} \quad (16)$$

Power losses on the junction capacitance at the two transition periods are zero since the losses at the rising and falling edges will cancel out each other. The power loss on R_s due to the current induced by C_j can be calculated as follows:

$$P_{loss, C_j_{br}} = \frac{1}{2\pi} \int_0^{\tau\pi} \left(C_j \frac{dV_{D2}}{d\theta} \frac{d\theta}{dt} \right)^2 R_s d\theta + \frac{1}{2\pi} \int_{(1-\tau)\pi}^{\pi} \left(C_j \frac{dV_{D2}}{d\theta} \frac{d\theta}{dt} \right)^2 R_s d\theta = \frac{4f^2 C_j^2 V_{br}^2 R_s}{\tau} \quad (17)$$

where τ is the ratio of rising and falling time with respect to half the period assumed. The loss due to V_{th} can be calculated by integrating the instantaneous voltage and current across the diode during one period as follows:

$$P_{loss, V_{th}_{br}} = \frac{1}{2\pi} \int_{-\pi}^{\pi} v_{D1_{br}} i_{D1_{br}} + \frac{1}{2\pi} \int_{-\pi}^{\pi} v_{D2_{br}} i_{D2_{br}} = \frac{\pi I_{m2}^2 R_s + \pi I_{R2}^2 R_s + 4I_{m2} V_{th} + 4I_{R2} V_{br}}{2\pi} \quad (18)$$

Therefore, the voltage applied to the load in the high power region of the N-stage HTVM is as follows:

$$V_{DC_{br}}(N) = N(V_{01_{br}} + V_{02_{br}}) = N(V_{br} - V_{th}) + \frac{NR_s(I_{m1} - I_{m2} + I_{R2} - I_{R1})}{\pi} \quad (19)$$

The loss occurring in the diode in the high power region can be expressed as the sum of the loss due to C_j and V_{th} as in Equation (11). Losses increase as the number of stages increases. Finally, the PCE over breakdown voltage is as follows, where $A = 8\pi f^2 C_j^2 V_{br}^2 R_S + \tau (\pi I_{m2}^2 R_S + \pi I_{R2}^2 R_S + 4I_{m2} V_{th} + 4I_{R2} V_{br})$.

$$\eta_2 = \frac{P_{out_br}}{P_{out_br} + P_{loss_br}} = \frac{V_{DC_br}(N)^2}{V_{DC_br}(N)^2 + Z_L P_{loss_br}(N)} = \frac{2N\{\pi(V_{br} - V_{th}) + R_S(I_{m1} - I_{m2} + I_{R2} - I_{R1})\}^2}{2N\{\pi(V_{br} - V_{th}) + R_S(I_{m1} - I_{m2} + I_{R2} - I_{R1})\}^2 + Z_L \pi A} \tag{20}$$

Diode parameters C_j , R_S , V_{th} , and V_{br} and rectifier parameters Z_L , N , P_{in} , f , and τ are known variables that can be easily obtained. By calculating Equation (20), the efficiency of N-stage HTVM (η_2) in the high input power region can be obtained. By calculating Equation (14), the efficiency of N-Stage HTVM (η is the sum of results of η_1 and η_2 intervals) in the low power region can be obtained. By dividing η_1 and η_2 based on V_{br} , the PCE for the input power of N-Stage HTVM can be calculated. A termination filter design is required to form the diode’s voltage and current waveforms as above. The filter design is described in the next chapter.

3. Design Method of Harmonic Termination Filter

The harmonic termination (HT) filter can be designed through the transmission line theory. A HT filter is mainly designed to pass and block with an input impedance determined by the electrical length of the open-ended stub and short stub. There are various other HT filter design methods. In this paper, only open-ended stubs are used and designed as shown in Figure 4. The filter is designed using only open stubs because it is easy to design. In addition, characteristics do not change dramatically even when the deformed form is the same as the bent form. Thus, it is suitable for miniaturization and tuning.

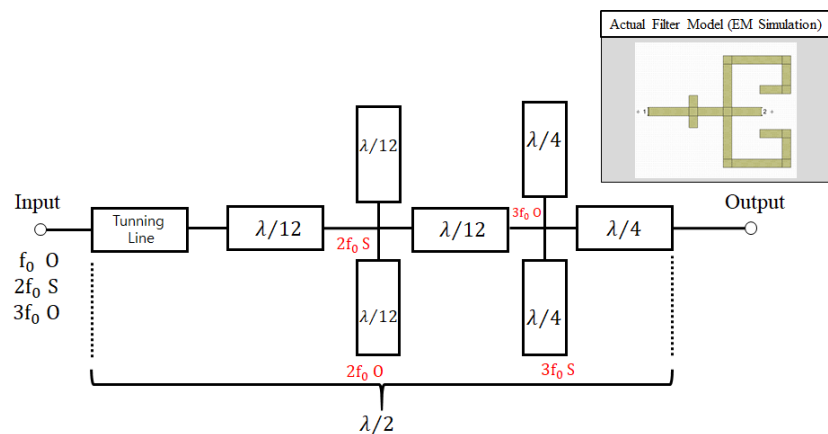


Figure 4. Harmonic termination filter using open-ended stub.

The third harmonic term appears to be short in the admittance characteristic seen from the input terminal of the open-ended stub having an electrical length of $\lambda/12$. However, its impedance characteristic, which is the reciprocal of it, appears to be open. Therefore, the impedance characteristics of harmonic components seen from the input $Z_{\lambda/12}$ can be expressed as follows:

$$Z_{\lambda/12}(\omega) = -jZ_{01} \cot\left(\frac{\pi \omega}{6 \omega_0}\right) = \begin{cases} \infty & \omega = 0 \\ -1.73jZ_{01} & \omega = \omega_0 \\ -0.57jZ_{01} & \omega = 2\omega_0 \\ 0 & \omega = 3\omega_0 \end{cases} \tag{21}$$

where Z_{01} is the characteristic impedance of $\lambda/12$ electrical length open-ended stub, and ω is the fundamental angular frequency. As for the input admittance characteristics of an open-ended stub having an electrical length of $\lambda/4$, the second harmonic term appears to be open, and the third harmonic term appears to be short. However, since the impedance characteristic seen from the input terminal has an inverse relationship, the second harmonic term seems to be short, and the third harmonic term appears to be open, which can be expressed as the following equation:

$$Z_{\lambda/4}(\omega) = -jZ_{01} \cot\left(\frac{\pi \omega}{6 \omega_0}\right) = \begin{cases} \infty & \omega = 0 \\ 0 & \omega = \omega_0 \\ \infty & \omega = 2\omega_0 \\ 0 & \omega = 3\omega_0 \end{cases} \quad (22)$$

where Z_{02} is the characteristic impedance of $\lambda/4$ electrical length open-ended stub. The HT filter was designed with impedance characteristics obtained from Equations (21) and (22). The sum of electrical lengths of transmission lines between each stub is $\lambda/2$. Furthermore, if double open-ended stubs are configured, the characteristic impedance is reduced. Thus, the bandwidth increases, rather than composing an HT filter with one open-ended stub, as shown in Figure 4. Figure 5 shows input impedance and E-field through EM simulation of the designed filter.

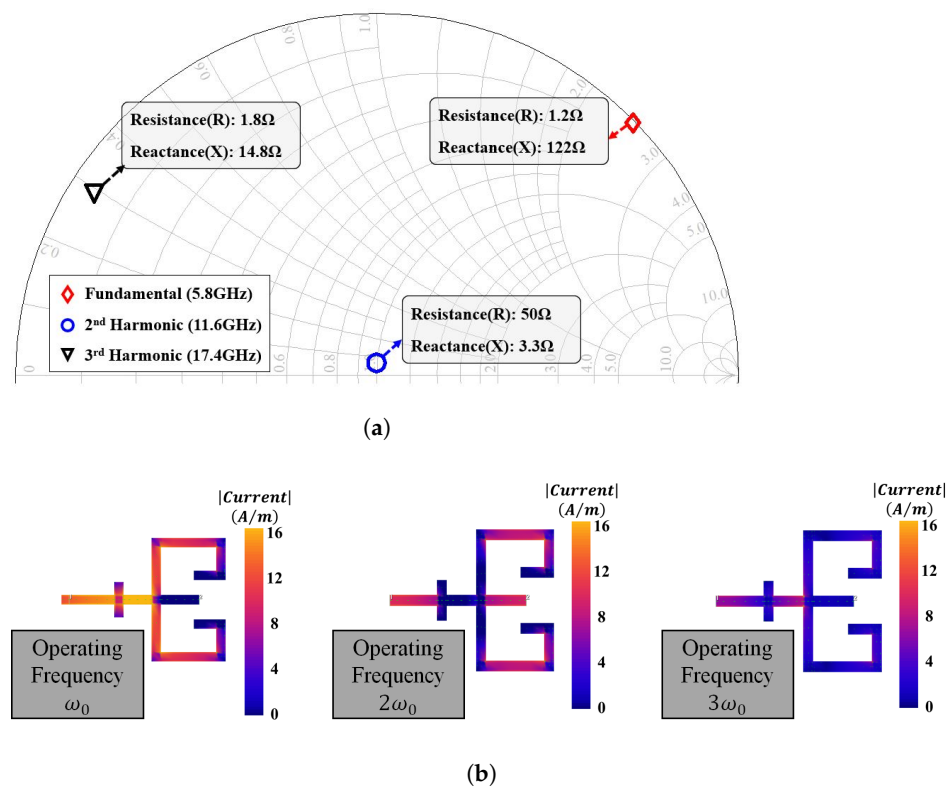


Figure 5. Characteristics of the designed HT filter; (a) the input impedance according to harmonics and (b) E-field according to harmonics.

When the center frequency of the HT filter designed in Figure 5 is 5.8 GHz, odd harmonic terms (5.8 and 17.4 GHz) seems to be open, while even harmonic term (11.6 GHz) seems to be short. EM simulation confirmed that the desired frequency characteristics were obtained from the E-field distribution.

4. Simulation and Measurement

The performance of N-stage HTVM was determined through model verification and circuit simulation based on measurement results. Table 1 shows the parameters used for model verification and circuit simulation.

Table 1. Simulation and measurement parameters.

Parameters	Unit	Description	Value
C_{j0}	pF	Zero junction capacitance	0.39
R_s	Ω	Series parasitic resistance	2.65
V_{br}	V	Breakdown voltage	2.65
V_{th}	V	Built-in potential	0.224
N	-	Number of stages	1–3
f	GHz	Frequency	5.8
Z_L	Ω	Load impedance	100–2000
Z_{01}, Z_{02}	Ω	Characteristic impedance	100

Figure 6 shows diode voltage and current waveforms in the time domain, and Figure 7 shows harmonics in the frequency domain when the number of stages is 1–3. One of the reasons for the difference between Figures 2, 3 and 6 is that C_j and R_s have different sizes. As C_j and R_s are smaller, the voltage waveform of the diode appears ideally. Figure 6 shows a simulation using the actual diode parameters shown in Table 1.

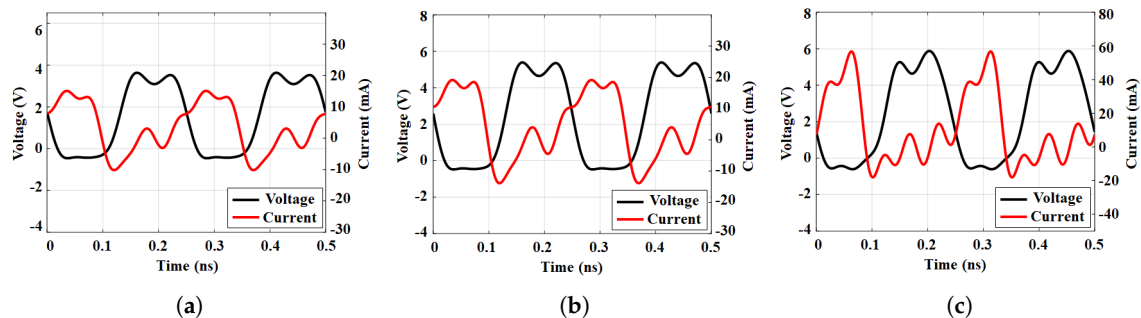


Figure 6. Diode voltage and current waveforms according to the number of stages; (a) one—stage HTVM; (b) two—stage HTVM; (c) three—stage HTVM.

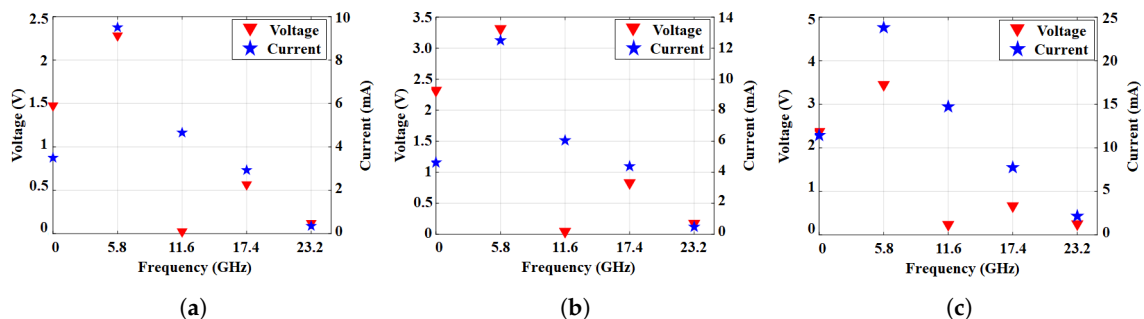


Figure 7. Diode harmonic components of voltage and current according to the number of stages; (a) one—stage HTVM; (b) two—stage HTVM; (c) three—stage HTVM.

As the number of stages increases, the voltage across the diode increases. According to the impedance characteristics of the HT filter, the voltage waveform of the diode appears as a square wave, and the third harmonic term seems to be higher than the even-order term as shown in Figure 7.

To verify the model proposed in Figure 8, circuit simulation results were compared. The red dotted line shows the model composed of V_{DC} and V_{DC_br} according to the input power, and the black solid line shows results of the Microwave Office (MWO) simulator. Figure 9 shows the measurement setup and the fabricated PCB to measure the performance of the N-stage HTVM. NI Universal Software Radio Peripheral (USRP B210) was used to generate RF signal at 5.8 GHz, and Qorvo's QPA9501 PA was used to apply RF power of 10 dBm or more. The amplitude of the USRP input signal was swept using Labview software and applied to the proposed rectifier up to 39 dBm, the maximum output power of PA.

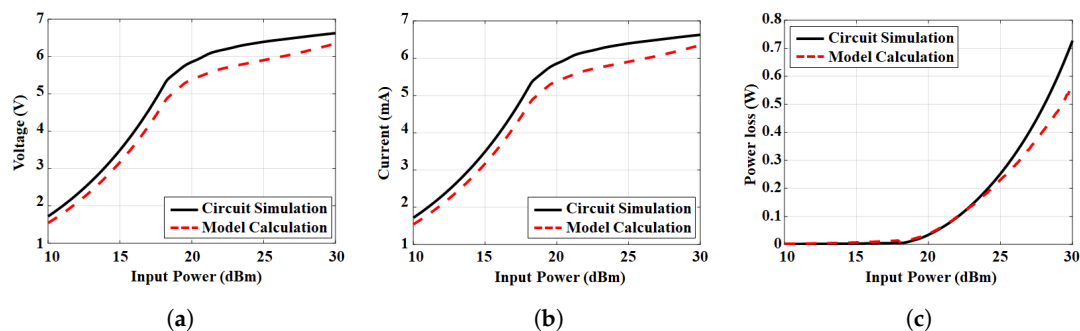


Figure 8. Output voltage, current and diode power consumption according to input power of the proposed model and circuit simulation ($N = 1$); (a) output voltage; (b) output current; and (c) diode power loss.

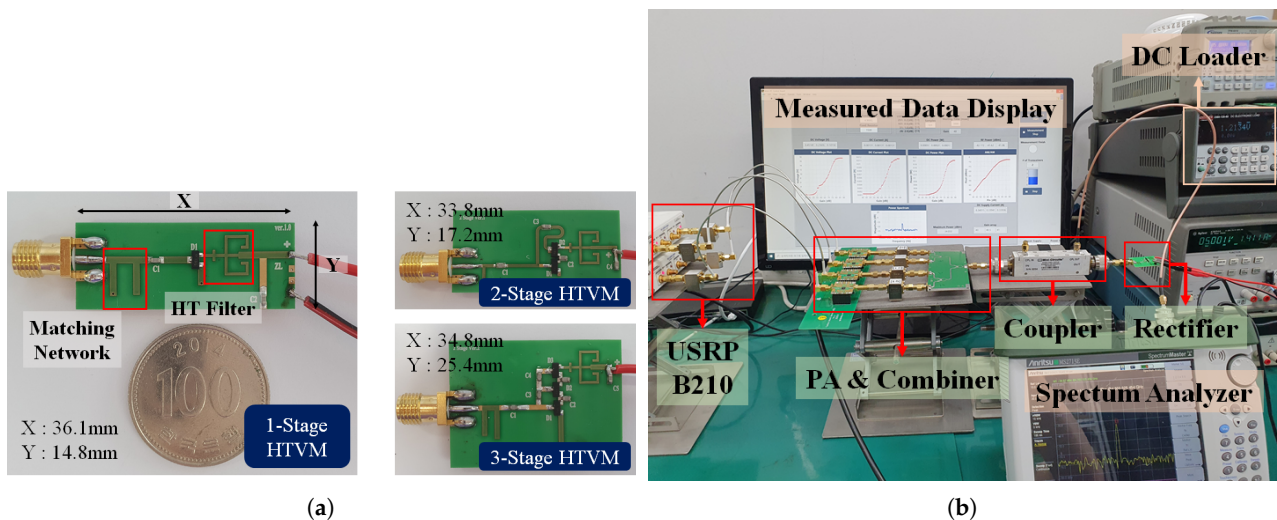


Figure 9. Measurement set-up and fabricated N-stage HTVM ($N = 1,2,3$); (a) fabricated N-Stage HTVM and (b) measurement set-up.

To monitor the input power applied to the rectifier, a 34.5 dB bi-directional coupler from Mini-Circuits was used and the reflected power was also observed. An Anritsu MS2713E spectrum analyzer was used to monitor the RF Power. Finally, to measure the DC output voltage and current of the rectifier according to the size of the load, a Keithley's 2380-120-60 DC electronic load was used. Figure 10 shows the measured and calculated output voltages and PCEs according to the input power for a 1500 Ω load. The black and red solid lines indicate the measured output voltage and the calculated output voltage, respectively. The black dotted line and red dotted line show the measured PCE and the calculated PCE, respectively.

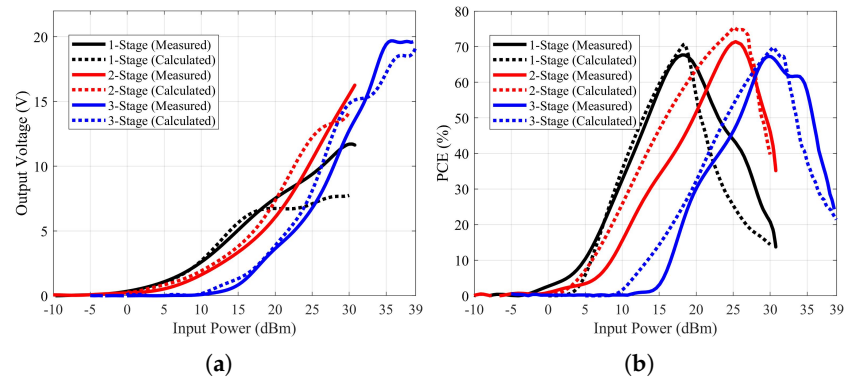


Figure 10. Measured and calculated output voltage and PCE of N-Stage HTVM; (a) output voltage and (b) PCE.

The results of Figure 10 are summarized in Table 2. Table 3 shows the performance of the rectifier proposed in this paper compared with previous studies.

Table 2. Performance summary of the measured N-stage HTVM.

Number of Stages (N)	Maximum Value	
	V_{DC} (V)	PCE (%)
1	11.6	68% @18 dBm
2	15.8	71% @25 dBm
3	19.8	67% @30 dBm

Table 3. Performance comparison between the rectifier proposed in this study and those reported in other previous works.

	Circuit Topology	Device Type	Freq. (GHz)	Input Range (dBm)	Optimum Load (Ω)	Max PCE (%)	Technique
[15]	Class F	Schottky Diode (N/A)	5.8	10~16	1300	71	Harmonic Termination (third)
[4]	Class C	Schottky Diode (SMS7630)	2.45	0~10	200~1200	72.8	Harmonic Termination
[2]	Shunt Diode	Schottky Diode (SMS7630)	1.96	0~10	200~1200	63	Rectenna
[16]	Class F	Schottky Diode (HSMS2820)	5.8	0~17	300~700	80	Harmonic Termination (second, third)
[17]	Class F	Schottky Diode (HSMS2822)	2.45	10~28	1000	75.4	Harmonic Termination
[18]	Class F ⁻¹	Schottky Diode (HSMS2860)	2.35	0~18	100~1000	80.4	Harmonic Termination (second, third)
[3]	Full wave	Schottky Diode (MA4E2054)	5.8	0~22	100~800	65.3	Harmonic Termination (second)
[1]	Series diode	Schottky Diode (HSMS2860)	5.8	-10~15	1000	51.5	Dual band impedance matching
[5]	Shut diode	Schottky Diode (BAT1503)	5.81	0~9	1300	69.2	Harmonic Termination (second, third)
[6]	Dickson charge pump	Schottky Diode (HSMS2862)	5.8	21~25	1000	64	Harmonic Termination (third)
This work	N-stage HTVM	Schottky Diode (BAT1704)	5.8	0~32	1500	68 (one-stage), 71 (two-stage), 67 (three-stage)	Harmonic Termination (second, third)

5. Conclusions

In this paper, we proposed an N-stage HTVM with a designed harmonic termination filter. When a HT filter was applied, the DC component and loss were calculated based on the voltage and current waveforms of the diode. Finally, the PCE was derived. The proposed model was verified by comparing the circuit simulation and measurement results.

The voltage and current waveforms of the diode were analyzed according to the number of stages.

When the operating frequency was 5.8 GHz, the load impedance was 1500 Ω , and the input power was 18 dBm, the maximum output voltage of one-stage HTVM was 11.6 V, and the maximum PCE was 68%. When the load impedance was 1500 Ω and the input power was 25 dBm, the maximum output voltage of the two-stage HTVM was 15.8 V, and the maximum PCE was 71%. Finally, when the load impedance was 1500 Ω and the input power was 30 dBm, the maximum output voltage of the three-stage HTVM was 19.8 V and the maximum PCE was 67%.

Experiments and model verification confirmed that the input power had the maximum voltage, and the PCE increased as the number of stages increased. The PCE results derived at high input power were higher than those of previous works. Based on the results of this study, it will be possible to design a receiver with high PCE in response to changing input power in a wireless power transfer environment in the future.

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