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Novel Interleaved High Gain Boost Converter Using Switched Capacitor

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Abstract: The increase in global energy demand has led to increased research in harvesting solar energy. Solar energy is widely used in homes, electric vehicles and is a great solution to power remote areas. DC–DC converters are essential in extracting power from solar panels. One of the main problems in designing converters for solar energy applications is boosting the low output voltage of the solar panel to meaningful levels. While there are several topologies to achieve high gain, some of the problems faced by them are the extreme duty ratio, complex design and discontinuous input current. This paper presents a novel topology that uses an interleaved input, a voltage lift capacitor and a hybrid switched capacitor network to achieve high gain without an extreme duty ratio or bulky magnetics. The proposed converter is controlled using a microcontroller which regulates the output voltage. The voltage lift capacitor and the switched capacitor network enhances the voltage gain over a conventional boost converter without an extreme duty ratio. The analysis and design of the proposed converter are presented and verified with a 100 W prototype. The results show that the converter provides a gain of 10, at a duty ratio of 30%, while delivering the designed output power with considerably high efficiency.

Keywords: energy conversion; renewable energy; interleaved; switched capacitor; DC–DC

Citation: Ramanathan, G.G.; Urasaki, N. Novel Interleaved High Gain Boost Converter Using Switched Capacitor. *Energies* **2021**, *14*, 8091. https://doi.org/10.3390/en14238091

Academic Editor: Adolfo Dannier

Received: 8 November 2021
Accepted: 1 December 2021
Published: 3 December 2021

1. Introduction

There is a growing need for global energy conservation, reduced emission and minimizing carbon footprint which is resulting in a shift of focus from fossil fuels to clean energy alternatives [1,2]. Solar energy is one such popular renewable alternative that is rapidly developing, finding a place in distributed generation, smart homes and electric vehicles. It provides a viable power solution to areas that are far from the grid. The voltage output of solar panels, in addition to being low, is strongly influenced by several factors, mainly, temperature and solar irradiation. Additional issues such as partial shading and panel angle further complicate its use [3–6]. DC–DC converters are essential in extracting power from solar panels.

There are several topologies to achieve high gain, which are discussed subsequently. The classic way of increasing gain is by using the standard boost converter topology [7–9]. Though the standard boost converter could theoretically provide the high gain necessary, practically, this is limited by switch stress and high duty ratio operation. In the standard boost converter, the output voltage is clamped to the single active switch. The higher the output voltage, the greater the stress on the switch is. To achieve voltage gains greater than five, the converter needs to operate at a duty ratio of 80% or greater. At higher frequencies, this reduces the time available for the switch to fully turn off, resulting in unstable converter

operation. The standard boost topology is superseded by several other topologies which offer greater gain and finer control over the output voltage.

The isolated converters discussed in [10–12] use the turns ratio of the transformer to adjust the output voltage. However, this in turn requires additional snubbing circuits to suppress the voltage spikes caused by the leakage inductance. Inductive and/or capacitor-based switched networks alter the output voltage by changing the number of energy storage elements and diodes [13,14]. This unavoidably increases the size and cost of the final product. Multi-level topologies also offer gains in stages, as discussed in [15–17], offering modularity as a feature. This, however, results in increased input current fluctuation, reduced noise immunity and the size of the converter increases as the number of modules increase. Cascaded converters produce high gain by cascading the output of several converters [18–22]. In [23], converters utilizing a switched capacitor network are presented. These converters offer gains greater than that of a classical boost converter with small modifications to the classical boost network.

Interleaved boost converters are a popular branch of boost converters for photovoltaic applications. They use a multiphase phase-displaced input which serves to reduce the input current fluctuations, which are important for photovoltaic applications [24–26]. Though these converters addressed the issue of input current ripple and showed promising results in managing the effects caused by partial shading, the voltage gain provided by an interleaved network was still identical to a classical boost converter [27,28].

Interleaved hybrid converters combined the advantages of interleaving and addressed the issue of gain by using a coupled inductor/switched capacitor network. In [29], an interleaved boost converter with coupled input inductors is presented. This converter provided a gain of $\frac{1}{1-(D_1+D_2)}$, where D_1 and D_2 are the duties of each phase, i.e., it operated as a classical boost converter with duty $D_1 + D_2$. In [30], an asymmetrical interleaved boost converter is presented. This converter provided a gain of $1 + \frac{1}{1-D}$, where D is the duty, which is only slightly greater than the gain provided by a classical boost converter. In [31], a zero-voltage switched interleaved boost converter with an active clamping circuit is presented. This converter provided a gain of $\frac{2\times N+2}{1-D}$ where N is the turns ratio of the coupled inductors and D is the duty. The gain is a function of the duty cycle and the turns ratio of the coupled inductor. It approached a gain of 10 when operating at a duty ratio of 60% for a turns ratio of $N = 1$. This topology is complex because of the presence of the additional clamp switches and could become bulky if N was increased.

This paper presents a novel interleaved converter using a switched capacitor network. This topology utilizes a two-phase input stage with two active switches. The output of one phase is combined with the output of the other phase through a voltage lift capacitor. This output is fed to the switched capacitor network which consists of two diodes and two capacitors. The features of this converter are high gain at a low duty, continuous input current and low peak overshoot. The proposed converter utilizes an interleaved input stage which consists of a two-phase input, and the outputs of each interleaved stage are coupled using a voltage-lift capacitor. The output of this stage is fed to a switched capacitor network which consists of two diodes and two capacitors. The details of the topology and its operations are discussed subsequently.

1.1. Power Circuit

Figure 1 shows the proposed power converter circuit. Inductors L_1 and L_2 and switches Q_1 and Q_2 form the two interleaved stages. The input current splits through the two interleaved phases, and this reduces the current stress of each switch. Furthermore, the circuit always operates in continuous conduction mode. The capacitor C_{VL} is the voltage lift capacitor. The presence of the voltage lift capacitor makes the interleaved network asymmetric. The output from this stage is fed to the switched capacitor network. Diodes D_2 and D_3 and capacitors C_1 and C_2 make up the switched capacitor network. The output inductor L_{out} and output capacitor C_{out} filter the output current and voltage.

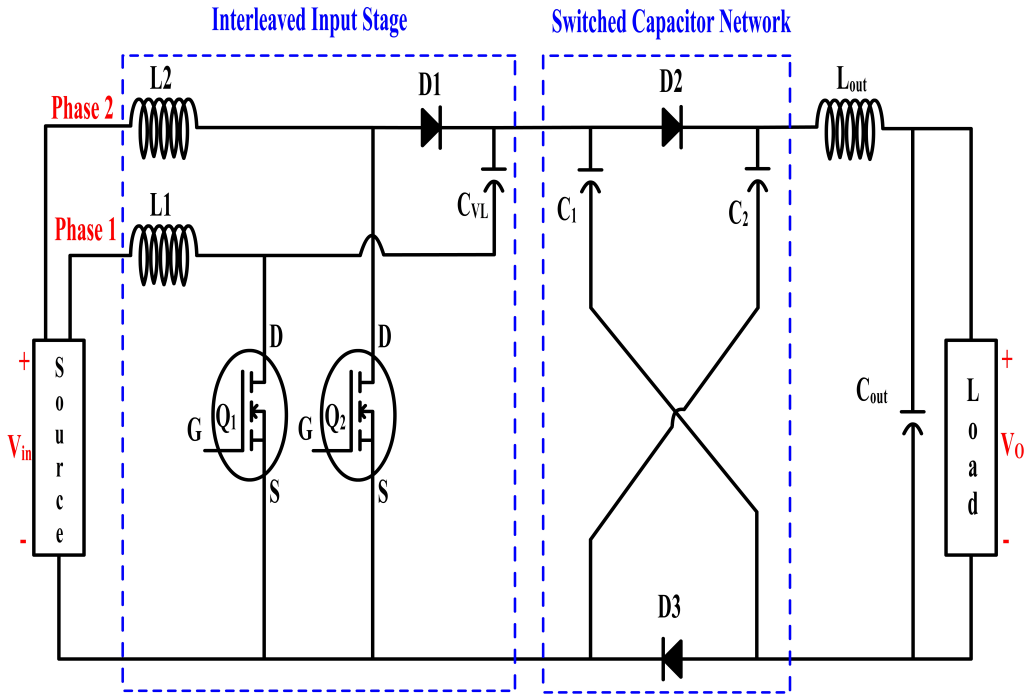

Figure 1. Power circuit diagram of the proposed converter.

1.2. Steady State Modes of Operation

Based on the switching pattern, the overall operation of the proposed converter may be split into several distinct modes. V_{g1} and V_{g2} are the gate pulses given to the switches. V_{D1} and V_{D2} are the voltages across diodes D_1 and D_2. V_{C_1} and V_{C_2} are the voltages across capacitors C_1 and C_2.

1.2.1. Mode 1 ($0 < t < t_1$)

Switch Q_1 is ON and switch Q_2 is OFF. Diode D_1 is conducting and diodes D_2 and D_3 are OFF. The current through inductor L_1 (I_{L1}) rises. Capacitors C_1 and C_2 discharge into the output capacitor and load through switch Q_1. This is the power delivery stage.

1.2.2. Mode 2 ($t_1 < t < t_2$)

Switches Q_1 and Q_2 are OFF. Diodes D_1 turns OFF and diodes D_2 and D_3 turn ON. The voltage across the source, the input inductors and the voltage lift capacitor charge the capacitors C_1, C_2 and the load.

1.2.3. Mode 3 ($t_2 < t < t_3$)

Switches Q_1 and Q_2 are OFF. Diode D_1 turns ON. Diodes D_2 and D_3 turn OFF. During this mode, the output capacitor freewheels through C_1, C_2, C_{VL} and the source, i.e., the output voltage decreases.

1.2.4. Mode 4 ($t_3 < t < t_4$)

Switch Q_1 remains OFF and switch Q_2 turns ON. All diodes turn OFF. The output continues its freewheeling. The current through Inductor L_2 (I_{L2}) rises. The output voltage continues to decrease.

1.2.5. Mode 5 ($t_4 < t < T$)

Switches Q_1 and Q_2 are OFF. Diodes D_1, D_2 and D_3 are OFF. The circuit continues its freewheeling and the output voltage continues to decrease.

The characteristic waveforms are shown in Figure 2.

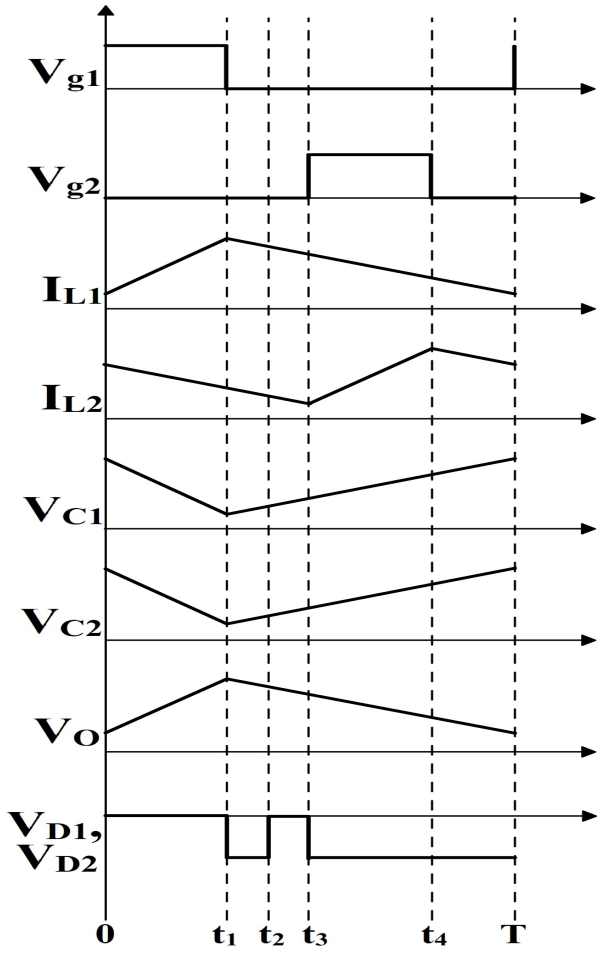

Figure 2. Characteristic waveforms of the proposed converter.

2. Analysis of the Proposed Converter

The gain of the proposed converter can be obtained by multiplying the gain of the interleaved stage and the switched capacitor network. Figures 3 and 4 show the stages individually. The gain expressions of the interleaved stage and the switched capacitor stage are analyzed separately and presented in the subsequent sections.

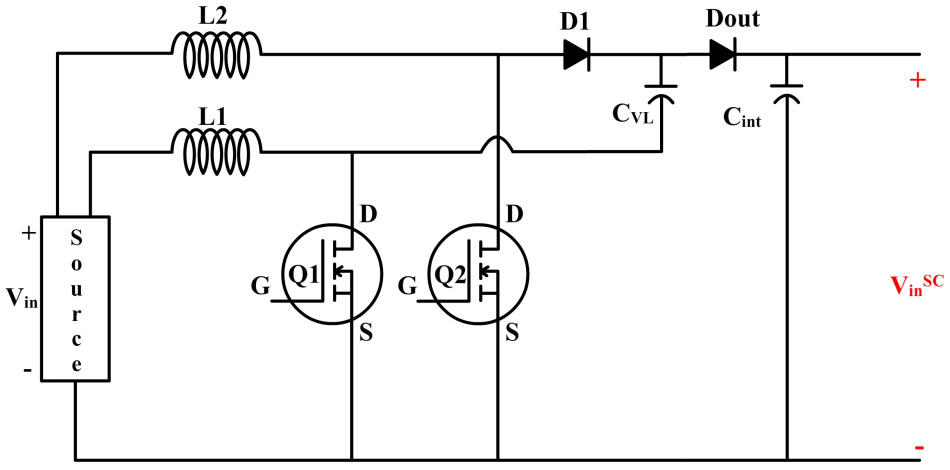

Figure 3. Interleaved stage of the proposed converter.

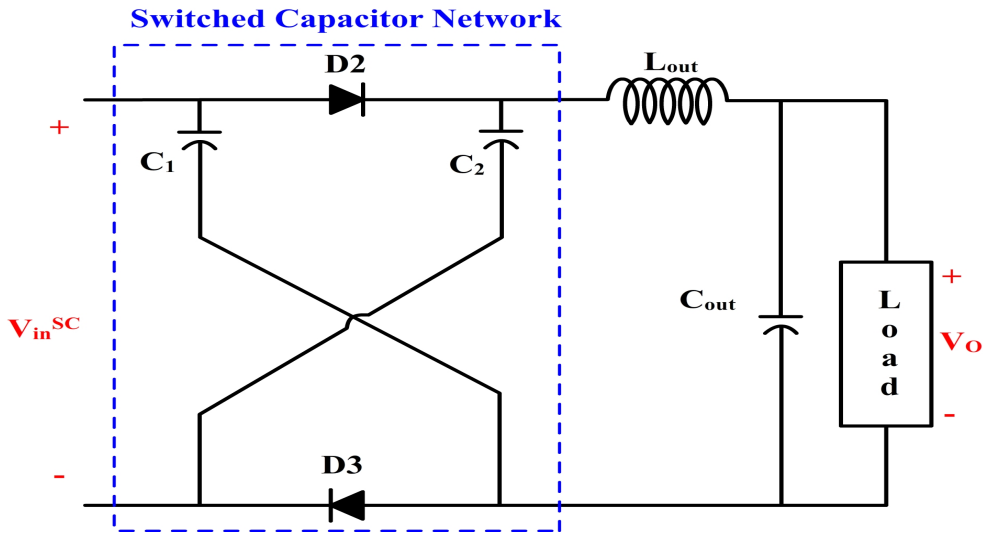

Figure 4. Switched capacitor network of the proposed converter.

2.1. Interleaved Stage Gain

The capacitor C_{VL} is charged from the source by the switching of Q_2:

$$V_{C_{VL}} = \frac{V_{in}}{1-D} \tag{1}$$

Consider inductor L_1:
When Q_1 is ON:

$$V_{L1} = V_{in} \tag{2}$$

When Q_1 is OFF:

$$V_{L1} = -(V_{C_{int}} - V_{C_{VL}} - V_{in}) \tag{3}$$

Averaging over one cycle, we obtain the gain of the interleaved stage as follows:

$$V_{in} \cdot T_{ON} - (V_{C_{int}} - V_{C_{VL}} - V_{in}) \cdot T_{OFF} = 0 \tag{4}$$

$$Time\ Period\ T = T_{ON} + T_{OFF} \tag{5}$$

$$Duty\ Cycle\ D = \frac{T_{ON}}{T} \tag{6}$$

Dividing Equation (4) by T and applying Equations (5) and (6), we obtain:

$$V_{in} \cdot D - (V_{C_{int}} - V_{C_{VL}} - V_{in}) \cdot (1-D) = 0 \tag{7}$$

$$V_{in} + V_{C_{VL}} \cdot (1-D) = V_{C_{int}} \cdot (1-D) \tag{8}$$

Substituting Equation (1) and simplifying it, we obtain:

$$2V_{in} = V_{C_{int}} \cdot (1-D) \tag{9}$$

$$V_{C_{int}} = \frac{2}{1-D} V_{in} = V_{in}^{SC} \tag{10}$$

This is the input to the switched capacitor network.

2.2. Switched Capacitor Network Gain

The gain of the switched capacitor network, shown in Figure 4, is discussed in detail in [23]. Following a similar method and including the voltage lift capacitor:

On the output side:

$$(2V_{C_1} - V_O) \cdot D + (V_{C_1} - V_O)(1 - D) = 0 \tag{11}$$

$$V_O = V_{C1} \cdot (1 + D) \tag{12}$$

On the input side:

$$V_{in}^{SC} \cdot D - (V_{C_1} - V_{C_{VL}} - V_{in}^{SC}) \cdot (1 - D) = 0 \tag{13}$$

$$V_{C1} = \frac{2}{1 - D} \cdot V_{in}^{SC} \tag{14}$$

Substituting Equation (14) in Equation (12), the gain of the switched capacitor network is as follows:

$$V_O = \frac{2 \times (1 + D)}{1 - D} \times V_{in}^{SC} \tag{15}$$

2.3. Overall Gain

From (10) and (15), the overall gain expression of the proposed converter can be written as:

$$G_{proposed} = \frac{V_{in}^{SC}}{V_{in}} \times \frac{V_O}{V_{in}^{SC}} = \frac{V_O}{V_{in}} = \frac{4 \times (1 + D)}{(1 - D)^2} \tag{16}$$

The plot of gain vs. the duty of the proposed converter is shown in Figure 5. It is seen that this gain is significantly higher than the gains presented in [29–31].

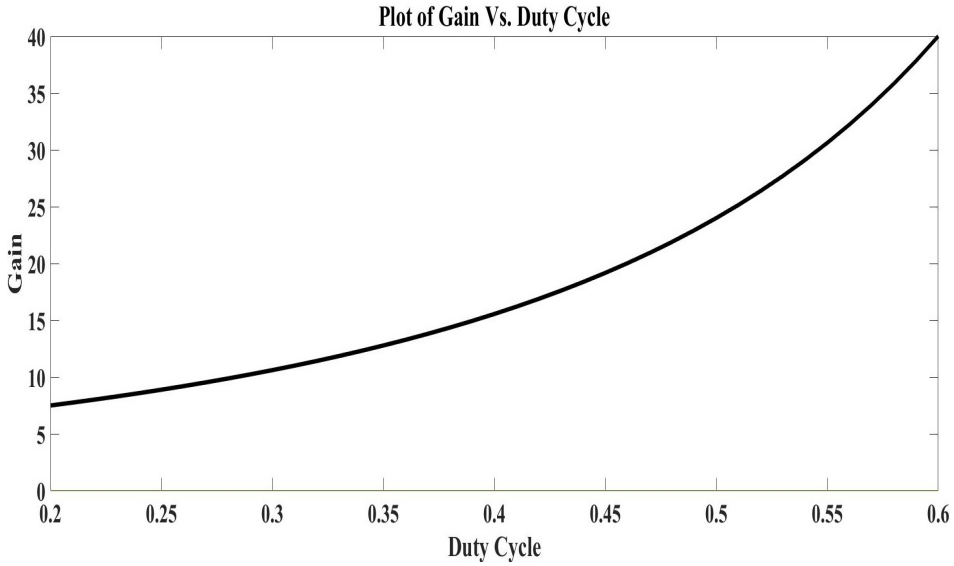

Figure 5. Gain plot of the proposed converter.

3. Converter Design

The proposed converter was simulated in PSIM, and the results are compared to the practical results of a prototype. The hardware prototype of the proposed converter was designed for an output of 310 V/100 W. The PI control of the prototype is conducted using a Microchip PIC16F455. The feedback system maintains a constant output voltage and manages the peak overshoot and settling time. The output voltage is sensed using a LV25-P voltage sensor. Figure 6 shows the photograph of the converter prototype, and Figure 7 shows the control board with the voltage sensor and microcontroller. The overall block diagram of the proposed converter is shown in Figure 8. The details of the prototype are shown in Table 1.

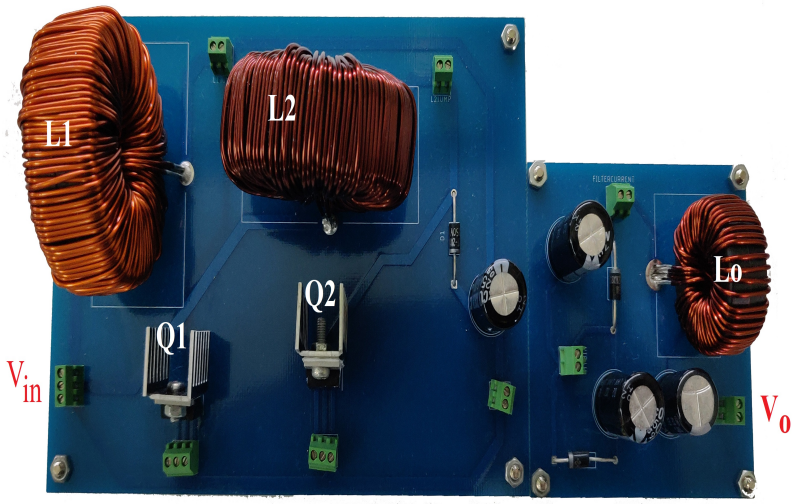

Figure 6. Prototype of the proposed converter.

Figure 7. Control board.

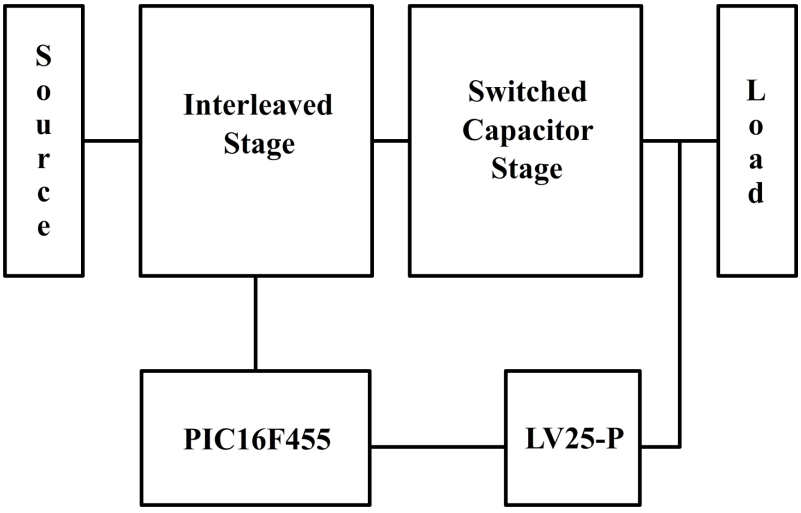

Figure 8. Overall block diagram.

Table 1. Prototype details.

Parameter	Value/Description
L_1	300 µH
L_2	300 µH
C_{VL}	47 µF/250 V
C_1	47 µF/250 V
C_2	47 µF/250 V
L_O	20 µH
C_O	22 µF/350 V
Switches Q_1 and Q_2	FDP2532
Diodes D_1, D_2 and D_3	SBYV27
Voltage Sensor	LV25-P
Controller	Microchip PIC16F455
MOSFET Drivers	TLP250
Switching Frequency	20 kHz

4. Results and Discussion

The 310 V/100 W hardware prototype was tested, and the results were compared to the corresponding PSIM simulation results.

Figures 9 and 10 show the hardware and simulation waveforms of hte gate pulses to switches Q_1 and Q_2, the input voltage and the output voltage. The input voltage is 31.7 V, and the converter is operating at a duty cycle of 30%, delivering an output voltage of 310 V. This demonstrates the voltage gain capability of the proposed converter. The gain at this duty cycle is 10, and this matches the gain expression of Equation (16). It is seen that the results of the prototype closely match those of the simulation.

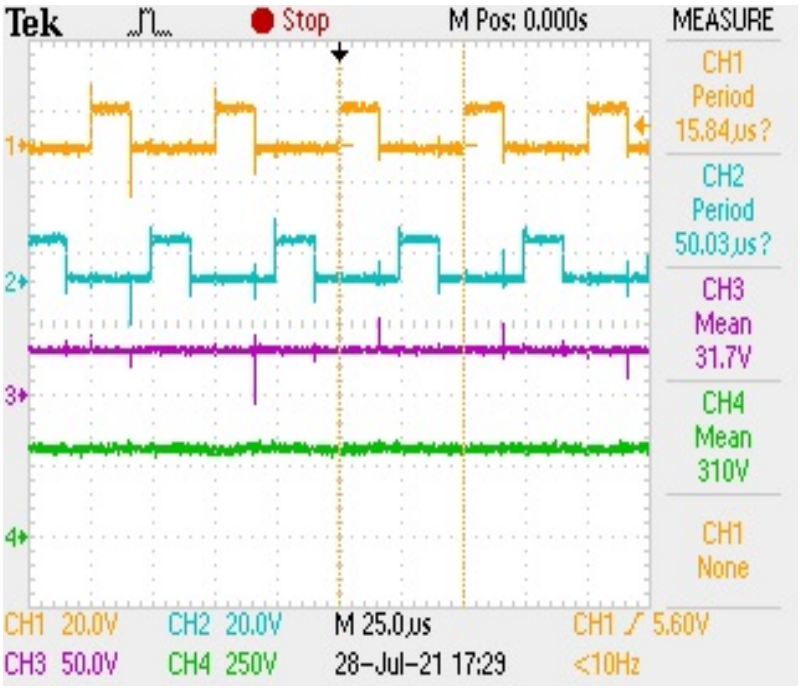

Figure 9. Gate pulses: input voltage and output voltage.

Figures 11 and 12 show the hardware and simulation waveforms of the input voltage, input current, output voltage and output current. It is seen that the average values of the simulation and hardware waveforms closely match each other. As mentioned before, one of the advantages of an interleaved input is the continuous input current, and it can be seen that the input current waveform is continuous without any major fluctuations. From these figures, we can calculate the input and output powers. It is seen that the converter

is delivering an output power of 99.2 W while drawing an input power of 106.8 W. The efficiency of the converter is 92.88% without soft-switching.

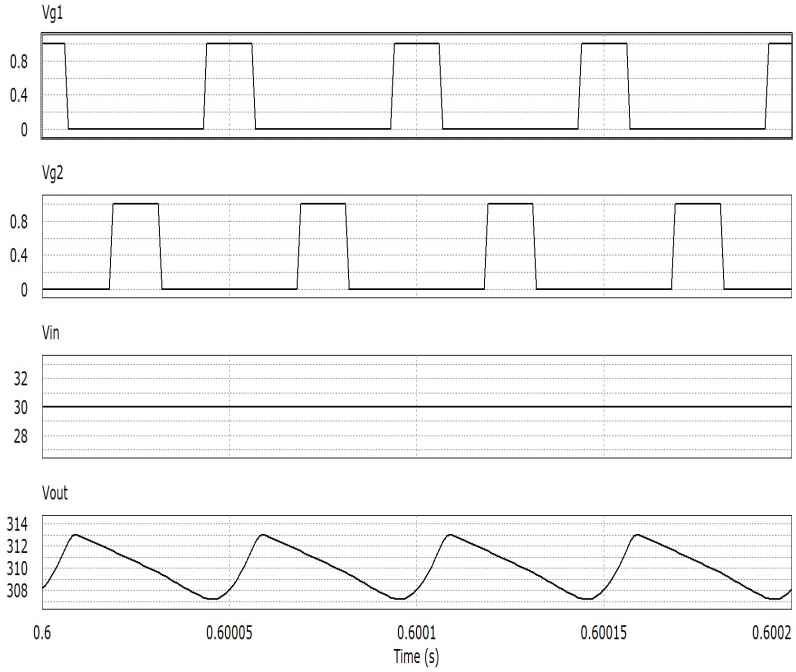

Figure 10. Simulation of gate pulses: input voltage and output voltage.

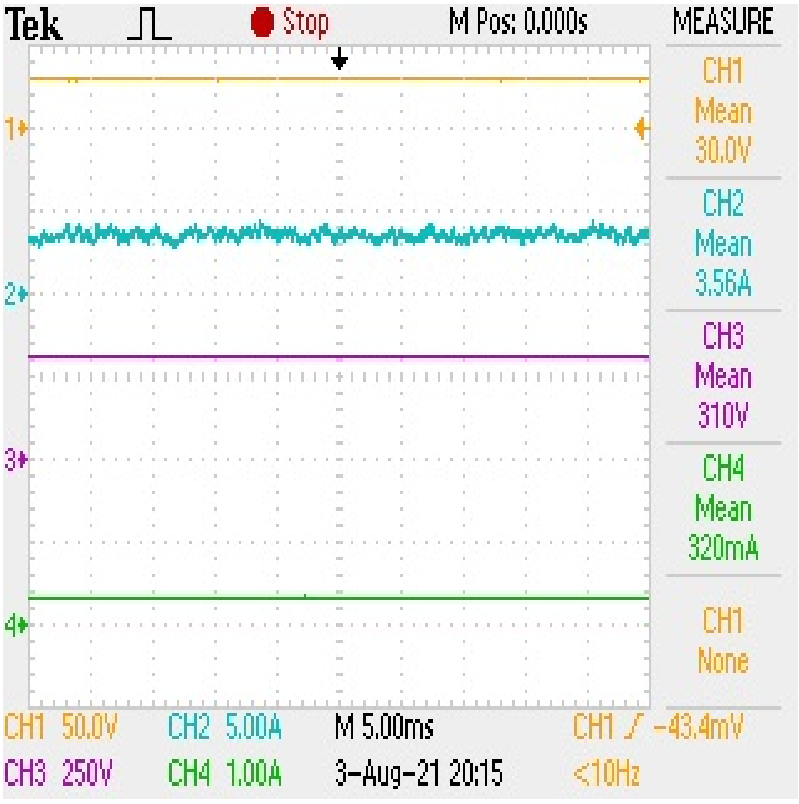

Figure 11. Input voltage, input current, output voltage and output current.

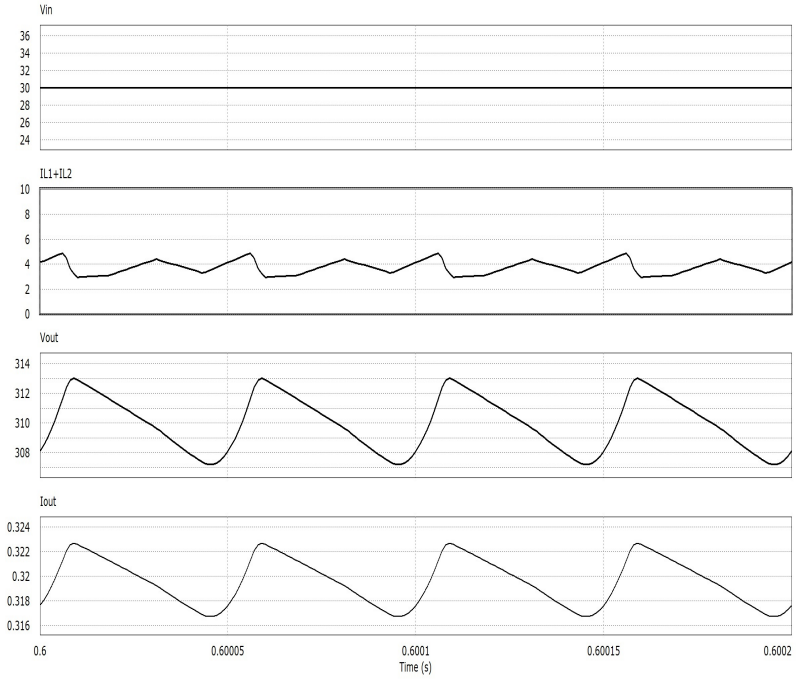

Figure 12. Simulation of input voltage, input current, output voltage and output current.

Figures 13 and 14 show the hardware and simulation waveforms of the output voltage during startup. In the simulation waveform, the output voltage rises to a steady-state value within 400 ms. Practically, it can be seen that the output voltage rises to a steady-state value within 100 ms. This is within acceptable variation limits. It is also seen that the converter does not have any peak overshoot.

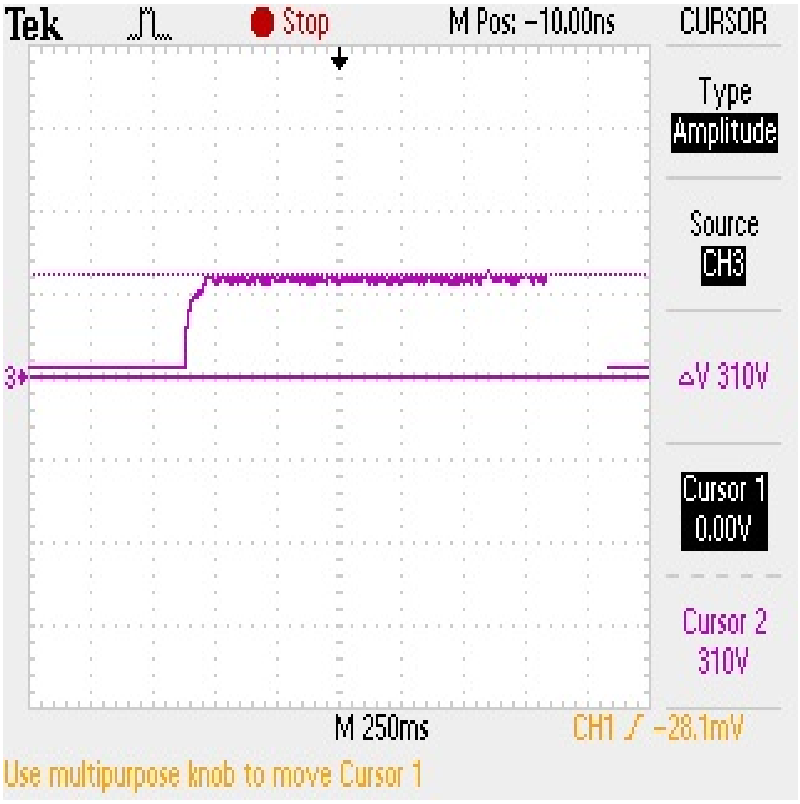

Figure 13. Output voltage vs. time.

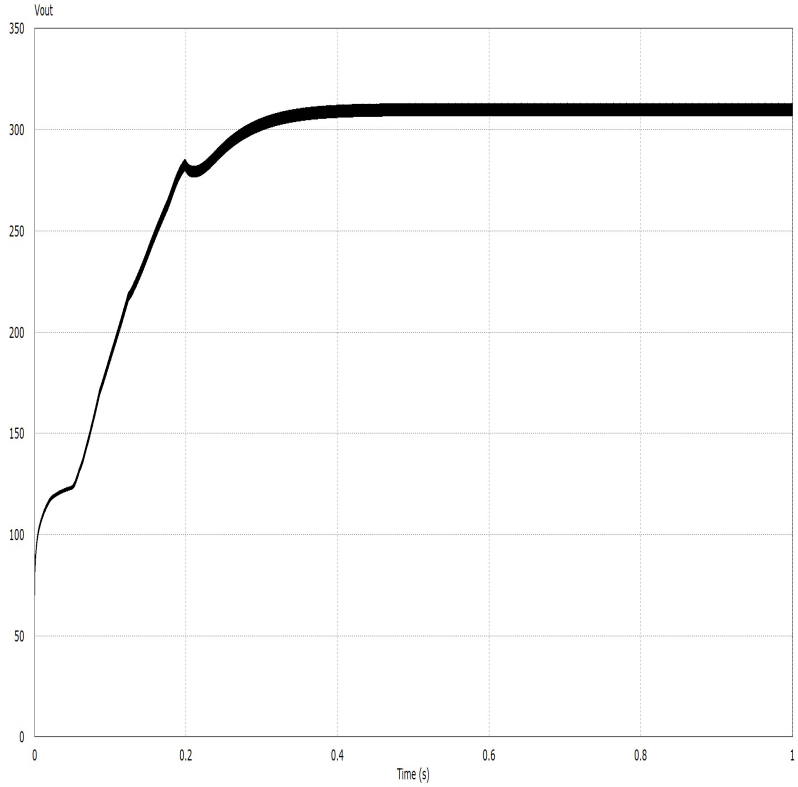

Figure 14. Simulation of output voltage vs. time.

5. Conclusions

A novel, non-isolated high gain boost converter is presented. The proposed converter has an interleaved input stage and provides considerable voltage gain using voltage-lift capacitor techniques and a switched-capacitor network. The features of the converter are a high gain without an extreme duty ratio and a continuous input current. The prototype of the proposed converter operates at an output voltage of 310 V while delivering 100 W at an efficiency of 92.88%. The results of the simulation and hardware testing indicate that the proposed converter has low peak overshoot, fast settling time and good efficiency.

Author Contributions: Conceptualization, G.G.R.; investigation, G.G.R.; methodology, G.G.R.; project administration, N.U.; resources, N.U.; software, G.G.R.; supervision, N.U.; validation, G.G.R.; visualization, G.G.R.; writing—original draft, G.G.R.; writing—review and editing, G.G.R. All authors have read and agreed to the published version of the manuscript.

Funding: This research received no external funding.

Institutional Review Board Statement: Not Applicable.

Informed Consent Statement: Not Applicable.

Conflicts of Interest: The authors declare no conflict of interest.

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