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The Modeling of the LC Divergence Oscillation Circuit of a Superconducting DC Circuit Breaker Using PSCAD/EMTDC

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Abstract: We proposed a superconducting DC circuit breaker that can reliably cut off the fault currents in preparation for the DC system. It consists of a superconducting element and a mechanical DC circuit breaker. The mechanical DC circuit breaker is connected in parallel with a mechanical high-speed switch, an LC divergence oscillation circuit, and a surge arrester. This provides stable cutoff operation due to the fault-current-limiting operation of the superconducting element and the artificial current zero point of the mechanical DC circuit breaker. In this paper, the operating principle of the LC divergence oscillation circuit that creates an artificial current zero point was reviewed based on the theory. We used experimental data to model the time constant of the initial fault current, the arc model generated by the mechanical high-speed switch, and the experimental equipment. As a result, the LC divergence oscillation circuit was confirmed in the simulation, and simulation modeling was reviewed based on the theoretical principle of generation.

Keywords: DC circuit breaker; LC divergence oscillation circuit; superconducting element; PSCAD/EMTDC program



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1. Introduction

In many countries, HVDC, MVDC, and LVDC level systems are being operated, with different purposes of use, depending on each system level. HVDC has the purpose of power transmission of large-capacity renewable energy generation and power connection between countries [1,2]. MVDC consists of ships, subways, and a small power source and consumers of DC electricity in small islands; it is aimed for independent operation with the existing AC system [3]. LVDC is mostly operated by small-scale solar power plants and wind farms [4]. In the DC system of the future, when DC systems of various levels are integrated into one system, the grid stability will be as high as the existing AC system. Accordingly, the breaking capacity of the system also increases; therefore, a circuit breaker suitable for DC characteristics must be developed [5]. Unlike AC, DC fault current does not have a cutting-off zero point; therefore, there is difficulty in breaking it at a high current level. Currently, in the HVDC system, the hybrid DC cutoff technology has been commercialized and is in operation [6–9]. This is typically a structure in which a power semiconductor or superconducting current-limiting element is combined with a mechanical DC circuit breaker (MCB). In the solid-state type DC circuit breaker where the power semiconductor and MCB are combined [10–12], current flows through the mechanical DC circuit breaker in the normal state, and the power loss is occurred due to the heat of the power semiconductor element (IGBT, MOSFET). Therefore, the solid-state type DC circuit breaker has conduction losses and switching (turn-on and turn-off) losses [13–15]. Additionally, power semiconductors are not easy to maintain because they are expensive and generate heat even in the transient system. In addition, the overall configuration is complicated, because a cooling auxiliary circuit is applied to solve this problem. The superconductor can maintain its superconducting state through the technology of cryogenic

refrigeration. It has no resistance in its superconducting state and, therefore, does not impede the flow of normal current. Additionally, the fault current is limited within about 2 ms through quenching when the critical point of the superconductor is exceeded by the fault current, thereby limiting the growth of the fault current [16–29]. To respond quickly and safely to DC transients, we researched superconductor and mechanical DC cutoff technology and proposed a hybrid superconducting DC circuit breaker [19–23]. An LC circuit has to be configured for a mechanical DC circuit breaker since DC does not have a frequency. The LC circuit creates an artificial current zero point in the breaking current, helping to cut off stable the fault current. After that, the fault current remaining in the circuit is stably extinguished through a surge arrester, and the interruption of the fault current is completed. Here, the method of using the LC divergence oscillation circuit to cut off the DC fault current is an important core technology. The LC divergence oscillation circuit generates a divergence oscillation current depending on the fault current generated in the grid transient state. However, it is possible to use it in various system environments only by understanding the operating characteristics of the passive elements L and C designed for mechanical DC circuit breakers. Up to now, the contents of the operating mechanism of the LC divergence oscillation circuit have been proposed through previous studies, and now it is necessary to study the contents for the purpose of commercialization [24–26]. In this paper, the operating characteristics according to the LC divergence oscillation circuit of the mechanical DC circuit breaker in the hybrid DC cutoff technology are reviewed. L and C of the LC divergence oscillation circuit are passive elements, and the set value must be controlled according to the unstable fault current [30–32]. Therefore, we apply the basic model of a mechanical DC circuit breaker designed using the PSCAD/EMTDC program to a single DC system. Next, we confirm the operating characteristics of the mechanical DC circuit breaker and review the model based on its basic principle.

2. Superconducting DC Circuit Breaker

2.1. Principle and Mechanism of a Superconducting DC Circuit Breaker

Figure 1 is the equivalent circuit of the superconducting DC circuit breaker. The superconducting DC circuit breaker consists of a superconducting part and a mechanical DC circuit breaker part. For superconducting parts, rare-earth barium copper oxide (REBCO) is used as a second-generation, high-temperature superconducting material [27–29]. It is utilized through various forms, and the fault current is reduced through fast quenching within about 2 ms. It reduces the fault current through fast quenching within about 2 ms. Mechanical DC circuit breaker has a structure in which mechanical circuit breaker (MCB), LC divergence oscillation circuit (LC circuit), and surge arrester (SA) are connected in parallel. The open operation of the MCB makes the divergence oscillation current of the LC circuit and helps the current in the main circuit reach the artificial current zero point. This artificial current zero point helps in stable arc extinguishing according to the opening operation of the MCB. A transient interruption voltage (TIV) is generated in the circuit when the opening operation of the MCB is completed [33,34]. The SA operates according to the occurrence of TIV, and the fault current remaining in the circuit is extinguished through the ground.

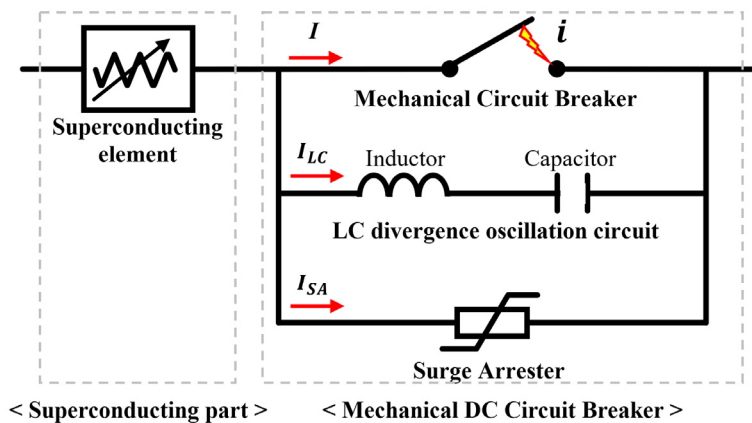


Figure 1. Equivalent circuit of superconducting DC circuit breaker.

2.2. LC Divergence Oscillation Circuit

The cutting-off technology of the above mechanical DC circuit breaker depends on the values of the inductor and capacitor of the LC divergence oscillation circuit composed of passive elements. Therefore, it has a condition to be able to control the inductor and capacitor of the passive element according to the conditions of the system. The principle of generation of LC divergence oscillation current is as follows: The fault current is reduced by the superconducting element flows through the MCB. The opening operation of the MCB starts, and a DC arc current is generated between the mechanical breaking contacts. This DC arc current (i) is generated by adding up the normal DC arc current (I) and the dynamic characteristics according to various factors, as shown in Equation (1).

$$i = I + I_m \sin \omega t \quad (1)$$

These dynamic characteristics are generated with an unspecified frequency, and the voltage–current characteristics change according to the level of the frequency. In addition, the fault current starts to flow into the LC divergence oscillation circuit as the DC arc resistance of the MCB circuit is generated. An oscillation is generated in the fault current. The principle of generating LC divergence oscillation current is as follows: The current flowing into the LC divergence oscillation circuit should consider the components occurring in each element according to Equation (2), based on Kirchhoff's voltage law [35,36].

$$L \frac{di}{dt} + Ri + \frac{1}{C} \int i dt + e_a = 0 \quad (2)$$

where e_a is the instantaneous value of the arc voltage.

If this is differentiated with respect to time and induced and replaced with the voltage equation for arc, Equation (3) is obtained.

$$L \frac{d^2 i}{dt^2} + \left(R + \frac{de_a}{di} \right) \frac{di}{dt} + \frac{i}{C} = 0 \quad (3)$$

As shown in Equation (4), it is possible to obtain a condition to become 0 through the sum of dc_a/di and R , which are average slopes of voltage–current characteristics according to the DC arc current (i) changes.

$$R + \frac{de_a}{di} = 0 \quad (4)$$

Therefore, Equation (3) becomes Equation (5) by Equation (4).

$$L \frac{d^2 i}{dt^2} + \frac{i}{C} = 0 \quad (5)$$

The L and C components remain in the LC divergence oscillation circuit, and the sum of the energies of the two components becomes 0. This is explained by the magnetic energy and electrostatic energy of Equations (6) and (7).

$$w_L = L \int I_{LC} di \quad (6)$$

$$w_C = C \int v_c dv \quad (7)$$

where I_{LC} is current flowing in LC divergence oscillation circuit, and v_c is the voltage of the capacitor.

The equation according to the impedance of each component can be expressed as Equation (8). It can be confirmed by Equation (8) that the phases of each component are opposite.

$$j\omega L = \frac{1}{j\omega C} \quad (8)$$

The natural frequency in the LC divergence oscillation circuit is determined, as shown in Equation (9).

$$f = \frac{1}{2\pi\sqrt{LC}} \quad (9)$$

The opening operation of the MCB starts, and an unspecified frequency is generated as a DC arc current flows between the mechanical breaking contacts. A resonance phenomenon occurs in the circuit—when this frequency becomes the same as the natural frequency of the LC divergence oscillation circuit, it has the resistance of Equation (4); that is, it is called the resonance frequency when the circuit frequency generated by the fault current and the natural frequency of the LC divergence oscillation circuit are the same. The oscillation width of the current gradually increases in this LC divergence oscillation circuit since L and C are connected in series. According to Kirchhoff's current law, the current flowing in the main circuit is equal to the sum of the MCB circuit, LC divergence oscillation circuit, and SA circuit. The fault current flowing in the MCB circuit is affected by the LC divergence oscillation circuit. Therefore, the oscillation amplitude of the fault current flowing through the MCB changes in response to the change in the current amplitude of the LC divergence oscillation circuit. After that, when the fault current flowing through the MCB reaches the current zero point, and the cutoff is completed in the MCB circuit, the normal DC arc current (I) excluding the dynamic property from the DC arc current–voltage characteristic flows to the LC divergence oscillation circuit. In addition, the impedance changes infinitely as the circuit of the MCB is opened, and transient interruption voltage (TIV), which is about twice the rated voltage, occurs in the circuit. The SA operates due to the occurrence of TIV with a high voltage rise slope. The SA completes all blocking operations by extinguishing the fault current remaining in the circuit through the ground.

3. Design of the Simulation

3.1. PSCAD/EMTDC Modeling

We designed a DC single system through the PSCAD/EMTDC program and simulated a short circuit by applying a superconducting DC circuit breaker. Figure 2 is the circuit diagram of the DC system and superconducting DC circuit breaker simulated short circuit. It is composed of an ideal DC power supply, line impedance, normal load, transient load, and superconducting DC circuit breaker. Mechanical DC circuit breaker is modeled as MCB, inductor, capacitor, and SA. L_0 is the line impedance, and I_{main} is the current flowing through the mainline. I_{MCB} is the current flowing in the mechanical circuit breaker, I_{LC} is the current flowing in the LC circuit, and I_{SA} is the current flowing in the absorption circuit. The rated voltage of the DC power supply is 500 V, the normal load is 10 Ω , and the transient load is 1 Ω . The fault time is about 100 ms, and the opening operation of the MCB is about 110 ms. The superconducting element is designed to be quenched at a critical

current of about 100 A, and the maximum resistance during quenching is about 0.5Ω . In addition, 15 μH and 66 μF were applied to the inductor and capacitor of the LC circuit, respectively. This is a value to generate an ideal divergence oscillation current to explain the principle of the LC circuit. We applied the parameters of three parts based on the data of previous studies to the modeling process, shown in Figure 3 [24–26]. They are DC initial fault current, arc model, and components of mechanical DC circuit breakers. First, the time constant of the DC initial fault current was applied to the simulation for the DC initial fault current based on the experimental equipment provided in the laboratory. Second, the arc model was modeled using data from previous studies on the arc resistance that occurs in the opening operation of the MCB. Third, the mechanical DC circuit breaker uses an MCB, an inductor, a capacitor, and a surge protection device (SPD), as shown in Figure 3. Figure 3a is a DC power supply, Figure 3b is a fault-generating system, Figure 3c is MCB and SPD, Figure 3d is an inductor and a capacitor.

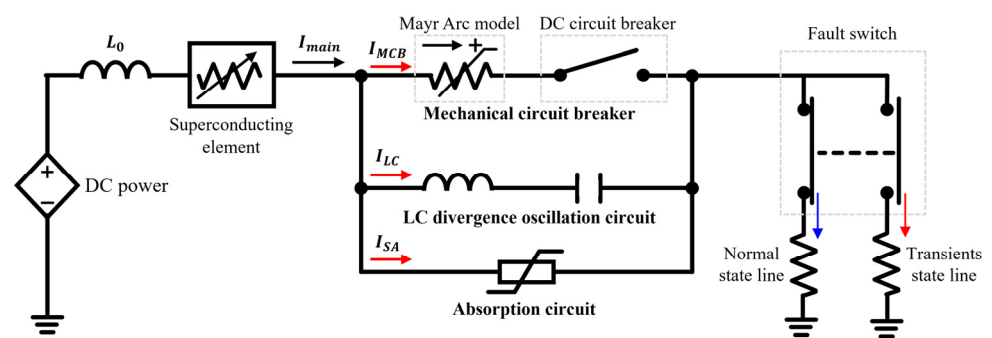


Figure 2. Configuration and circuit diagram of superconducting DC circuit breaker.

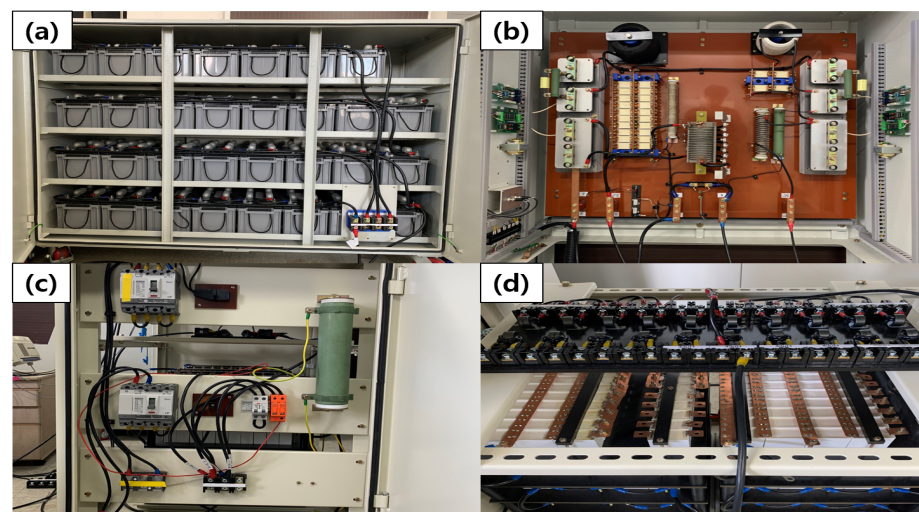


Figure 3. Laboratory equipment (a) DC power supply (150 AH-12 V lead-acid battery); (b) fault-generating system; (c) MCB and SPD; (d) an inductor (up) and a capacitor (lower).

3.2. The Modeling of DC Initial Fault Current

The time constant τ of the fault current $I_f = V/R [1 - e^{-t/\tau}]$ of the transient characteristic is important in order to model the DC initial fault current generated in the HVDC system by simulation. We conducted an experiment to set the time constant using the experimental equipment shown in Figure 3 and designed a simulation system based on the experimental result data. Figure 4 shows the graph of the fault current caused by the DC power supply of voltage of about 500 V, the normal load, and the transient load. Figure 4a is a characteristic graph of the initial fault current confirmed through the preceding experiment of Figure 3. Figure 4b is the graph of the initial fault current of the model designed based on the previous experimental data. A superconducting DC circuit breaker is not

applied to the DC system. The line fault in Figure 4a occurred at about 58.17 ms, and the maximum initial fault current was about 508.3 A at about 58.6 ms. The time constant ($0.63 I_m$) was about 0.07. The line fault in Figure 4b occurred at about 100.0 ms, and the maximum initial fault current was about 500.0 A at about 100.5 ms. The time constant τ was about 0.05.

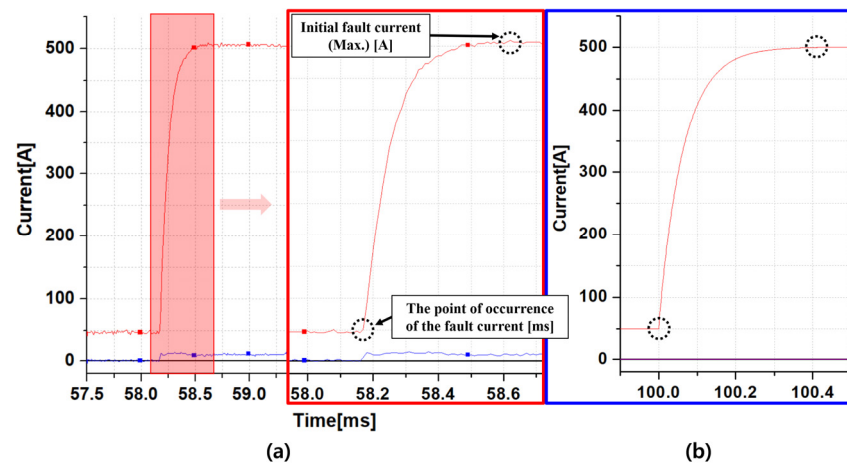


Figure 4. Graph of operating characteristics of initial fault current: (a) experimental data; (b) simulation data.

3.3. The Superconducting Element and Simulation Model

Figure 5 shows the data on the superconducting wire used in the experiment, and detailed parameters are summarized in Table 1 [37]. Figure 5a is a description of the material of 2G high-temperature superconductors (HTS) wire made by SUNAM Co., Ltd. Figure 5b shows the actual product of the superconducting wire (GdBCO) used in the experiment. The width of the superconducting wire was 4.1 mm, the height was 0.11 mm, and the critical current I_C was about 200 A. Figure 5c is a view of a superconducting element designed with a superconducting wire in a solenoid type. The length of the superconducting wire used in the experiment was about 5 m. The size of the model was about 80 mm in width and length, and 400 mm in height. Figure 5d is an equivalent circuit diagram for testing the operating characteristics of a superconductor. Through this experiment, the maximum resistance value of the superconductor required for simulation was obtained.

Table 1. Parameters of simulation model.

Parameters	Value
Operating temperature	77 K
Critical current I_C	200 A
Superconducting layer thickness	0.11 mm
Superconducting layer width	4.1 mm
Substrate	Stainless steel
Stabilizer	Copper
Coil pitch	20 mm
Size	80 × 80 × 400 mm
Total tape length	5 m
Number of coil turns	15 (Solenoid)

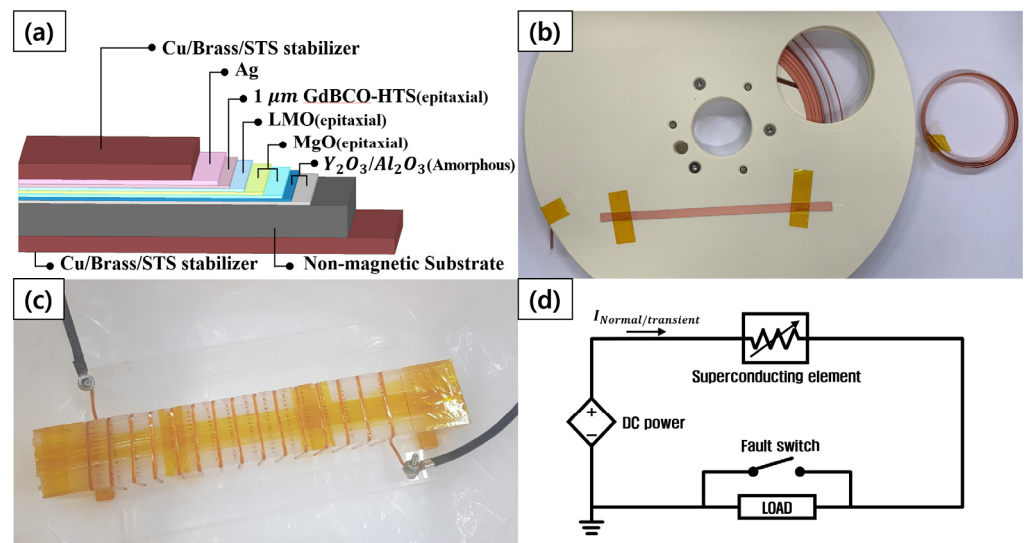


Figure 5. Experimental data of superconducting element: (a) information of 2G HTS wire; (b) superconducting wire (GdBCO); (c) proto-type of superconducting element; (d) equivalent circuit for the experiment.

Figure 6 shows the operating characteristics of the superconducting element as a graph through simulation modeling based on the experimental data. The operating characteristics of superconductors were designed based on Equation (10) [38].

$$R_{SC}(t) = \begin{cases} 0 & (t < t_{quenching}) \\ R_m \sqrt{1 - \exp\left(-\frac{t}{T_{SC}}\right)^{1/2}} & (t_{quenching} < t) \end{cases} \quad (10)$$

R_{SC} is the quenching resistance of the superconducting element. R_m is the maximum quenching resistance of the superconducting element. T_{SC} is the time constant for the operating characteristics of the fault current. Figure 6a shows the fault current about the presence or absence of the superconducting element. In addition, the maximum resistance value of the superconducting wire, and the time of occurrence are shown in a graph. The time when the fault occurred was about 100 ms, and the steady-current of about 50 A started to increase rapidly from about 100 ms. When no superconducting element was applied, the maximum fault current was about 488 A. When the superconducting element was applied, the maximum fault current was about 323 A. The maximum resistance of the superconductor was about 0.5 Ω . Figure 6b is an enlarged graph of Figure 6a to confirm the time of the quenching of the superconducting element occurred. The maximum resistance value of the superconductor was obtained through the experiment in Figure 1, and this was applied to the simulation modeling. In Figure 6b, the resistance of the superconducting element started to occur at about 101.6 ms. In addition, the characteristic of the critical current (200 A) was applied to the simulation. When the fault current reaches about 200 A, the superconducting element is designed to be quenched, and it can be confirmed through Figure 6b.

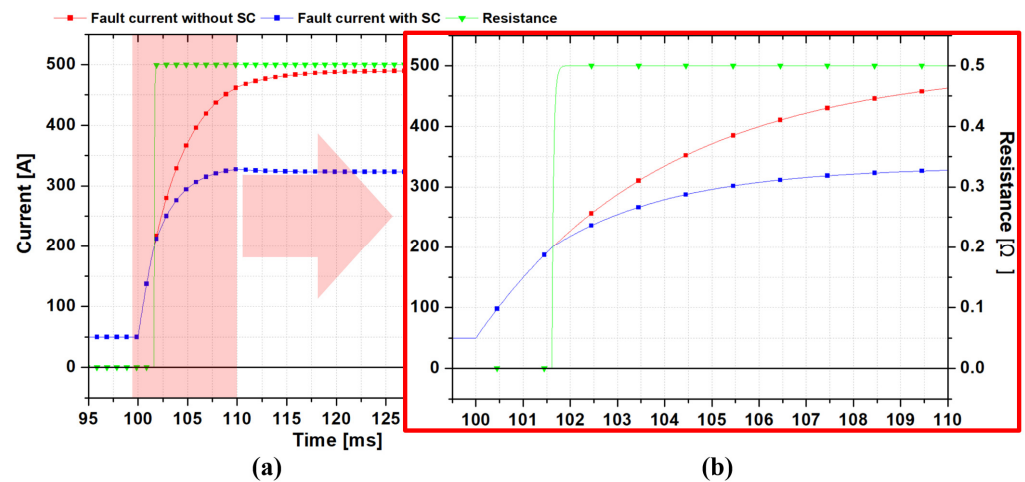


Figure 6. Simulation modeling: (a) graph of current and resistance about the presence or absence of the superconducting element; (b) graph to confirm to point the maximum resistance of superconducting wire occurs.

3.4. Arc Model

We selected the Mayr arc equation among the three arc models of Mayr, Cassie, and Schavemaker [39]. The reason is that we used the data analyzed through the experiment of the line fault of the superconducting DC circuit breaker when the power supply voltage is about 500 V. Therefore, we designed a Mayr arc model suitable for small current environments of about 8000 K or less. Figure 7 shows the modeling algorithm of arc motion characteristics in the PSCAD/EMTDC program, and the Mayr arc Equation (11) was applied [40,41]. P_0 the signal of arc operation is an element that gives a signal when the mainline changes from normal load to transient load by the fault switch. The arc model (Mayr) receiving the signal outputs the arc resistance value according to Equation (11). This model has variables of P_0 and τ , and these variables are determined from experimental data [27,41,42]. In Equation (11), G is the conductance to the arc, and τ is the time constant of the arc. In Figure 7, the arc voltage is U_{arc} , and arc current is I_{arc} . P_0 is the cooling power, and to express this in detail, it is a constant discharge power per unit volume. Since we need general arc characteristics for the operating characteristics of superconducting DC circuit breaker, we set it as follows: a cooling power of 5 kW was applied, and an arc time constant of 0.3 was applied.

$$\frac{dG}{dt} = \frac{G}{\tau} \left(\frac{U_{arc} I_{arc}}{P_0} - 1 \right) \quad (11)$$

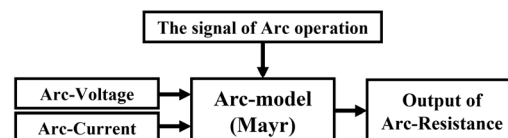


Figure 7. Arc modeling using the PSCAD/EMTDC program.

Figure 8 shows the operating characteristics generated when the model designed based on the arc equation was applied to the DC system. Figure 8a is an equivalent circuit and consists of a DC power, an arc model, a DC circuit breaker, a fault switch, and a load. This equivalent circuit generates a simulated short-circuit fault through the turn-on operation of the fault switch. The fault load was designed as 1 Ω. Figure 8b is a simulation graph for Figure 8a, and the data of voltage, current, resistance, and operating signal of the arc model. Arc voltage is the voltage applied to the arc model and is U_{arc} in Equation (11). Arc current is the current flowing through the arc model and is I_{arc} in Equation (11). Arc resistance is the output of arc resistance. The simulated short-circuit fault starts at 100 ms, and the fault current is generated at 100 ms and increases to about 488 A. The opening

operation of the DC circuit breaker occurs at 110 ms. Therefore, the trip order of the arc model was set to have a value of 1 at 110 ms. The resistance of the arc model is generated by the trip order. In this simulation, only one DC circuit breaker was applied, and it was set to fail to cut off the fault current of about 488 A.

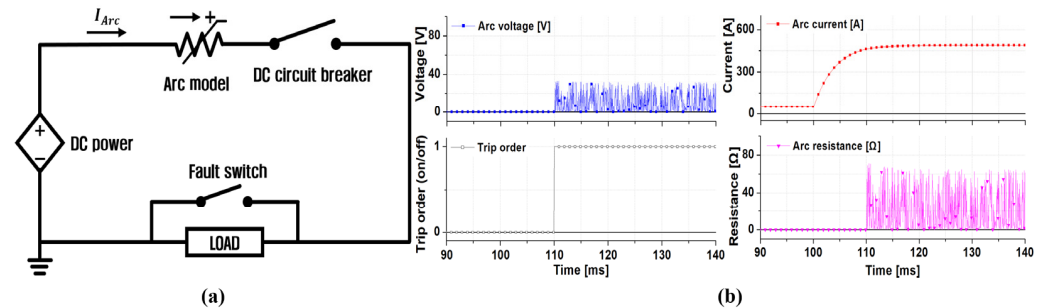


Figure 8. Operating characteristics of MCB circuit according to arc model equation: (a) equivalent circuit; (b) simulation graph.

Next, the operation of blocking the fault current through the application of a superconducting DC circuit breaker was analyzed through simulation.

4. Results of the Simulation

Figure 9 is a graph of the operating characteristics of a superconducting DC circuit breaker. $V_Mainline[V]$ is the voltage of the mainline, and $I_Mainline[A]$ is the current of the mainline. The mainline consists of a superconducting element and a mechanical DC circuit breaker. $V_MCB[V]$ and $I_MCB[A]$ are the voltage and current of the MCB circuit. $I_LC[A]$ is the current of the LC circuit, and $V_Inductor[V]$ and $V_Capacitor[V]$ are the voltages of the inductor and capacitor. $I_SA[A]$ is the current in the SA circuit.

- (a) is the time point at which the simulated short-circuit fault occurred, which was approximately 100 ms.
- (b) is the time point at which the MCB starts the opening operation, and it was about 102.0 ms.
- (c) is the time point at which the artificial current zero point of the fault current, which was approximately 103.2 ms.
- (d) is the time point when the fault current was completely cut off, and it was about 103.7 ms.

In the normal state of the line before the short circuit fault occurred, a steady current of about 50 A flowed through the mainline. Additionally, it can be checked through the $I_Mainline[A]$ and $I_MCB[A]$. A short circuit occurred at the time point (a), and the initial fault voltage and current were checked at the $V_Mainline[V]$ and $I_Mainline[A]$. If it compared with the condition without superconducting DC circuit breaker in Figure 4b, this initial fault current was limited to about 108 A from about 500 A to 392 A. Additionally, the fault current was limited by the superconducting element up to about 333 A at time (b). From point (b), the Mayr arc model operated according to the opening operation of the MCB. The arc voltage according to the arc resistance was confirmed in the $V_MCB[V]$ graph. From point (b), the fault current started to flow in the LC circuit. The amplitude of the current flowing in the LC divergence oscillation circuit increases by the inductor and capacitor connected in series, as shown in the $I_LC[A]$ graph. $I_LC[A]$ affects $I_MCB[A]$; therefore, $I_MCB[A]$ vibrates in the same way as the amplitude of $I_LC[A]$. At point (c), when the fault current of $I_MCB[A]$ reaches the artificial current zero point, the fault current of the circuit flows to the LC divergence oscillation circuit. The resonance of the $I_MCB[A]$ and $I_LC[A]$ circuits disappeared from point (c), and the voltage level of $V_Inductor[V]$ converged to zero. $V_Capacitor[V]$ has a momentarily occurred voltage peak. A maximum voltage of about 533.6 V was generated at that level, and it was quickly lowered to a voltage

level of about 500 V, the rated voltage. TIV was generated in $V_MCB[V]$ by the capacitor. The level was up to about 528 V and quickly lowered to a voltage level of about 500 V. $I_SA[A]$ operated according to the TIV occurrence time to extinguish the residual current of the circuit.

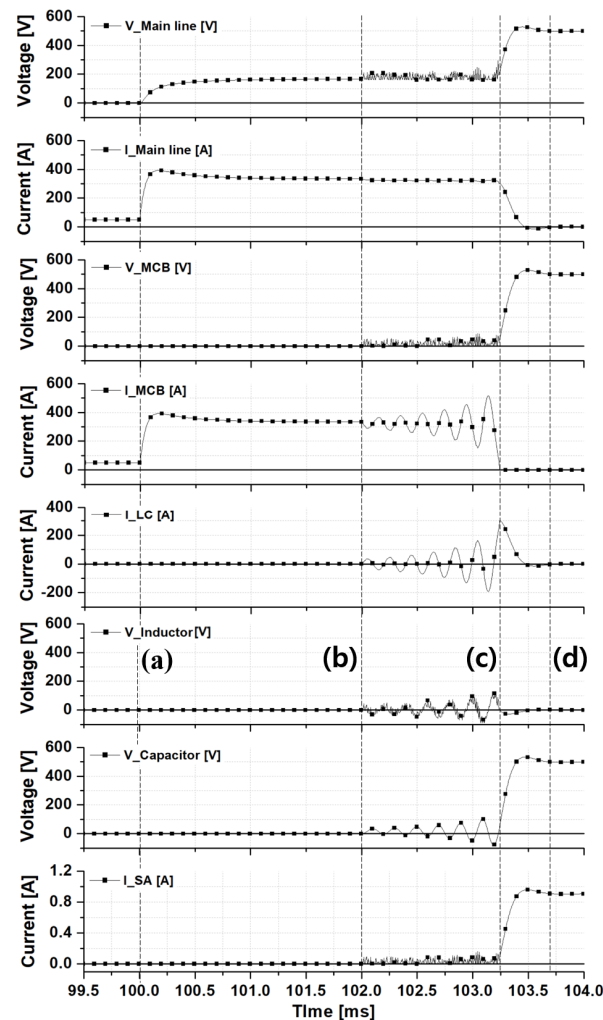


Figure 9. A graph of the operating characteristics of a superconducting DC circuit breaker.

5. Review

Figure 10 shows the graphs of the current and voltage characteristics of Figure 9 in one graph. Figure 10a shows the operating characteristics of the superconducting DC circuit breaker as a graph. Figure 10b is an enlarged graph of the operating characteristics from immediately after the opening of the MCB of the superconducting DC circuit breaker to the time when the breaking is completed. The graph was analyzed from (b), which is the opening operating point of the MCB, to (c) when the artificial current zero point was created. In the process between (b) and (c), a resonance phenomenon occurred in the circuit, and energy exchange between the inductor and the capacitor occurred. This is explained in the state of Equation (8) by Equation (5).

We divided and analyzed sections for each T_n time from T_0 to T_1 when the resonance phenomenon occurred based on $I_MCB[A]$. Table 2 summarizes the current and voltage characteristics of each element from T_0 to T_1 . Since there is no current flow of $I_SA[A]$ in the section from T_0 to T_1 , it was omitted from the analysis process.

Table 2. Simulation results of current and voltage from $T_0 \sim T_1$.

Section [ms]	T_0 [102.00]	$0.25 T_1$ [102.05]	$0.50 T_1$ [102.10]	$0.75 T_1$ [102.15]	T_1 [102.20]
I_Mainline [A]	333	325	324	324	324
I_MCB [A]	333	290	324	364	324
I_LC [A]	0	35	0	−40	0
I_SA [A]	0	0	0	0	0
V_Inductor [V]	0	−16	−33	−4	9
V_Capacitor [V]	0	16	33	13	−5

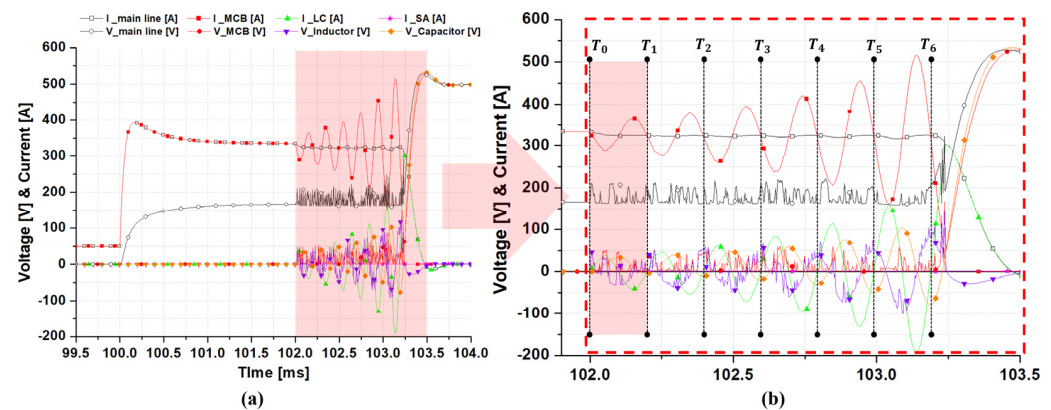


Figure 10. Current and voltage characteristic graph of superconducting DC circuit breaker (a) the operating characteristics of the superconducting DC circuit breaker; (b) an enlarged graph of the operating characteristics from immediately after the opening of the MCB of the superconducting DC circuit breaker to the time when the breaking is completed.

The fault current was flowing in the MCB circuit because it was the time when the opening operation of the MCB started at T_0 .

At $0.25 T_1$, $I_{\text{Mainline}}[\text{A}]$ decreased by about 8 A from about 333 A to about 325 A. It can be seen that the reduction of about 8 A is caused by Mayr's arc model in Equation (11). This was confirmed in the current flow of $I_{\text{MCB}}[\text{A}]$ and $I_{\text{LC}}[\text{A}]$. Since $I_{\text{MCB}}[\text{A}]$ is about 290 A and $I_{\text{LC}}[\text{A}]$ is about 35 A, the sum of the two current components is about 325 A, according to Kirchhoff's current law. $I_{\text{LC}}[\text{A}]$ can check the flow through $V_{\text{Inductor}}[\text{V}]$ and $V_{\text{Capacitor}}[\text{V}]$. $V_{\text{Inductor}}[\text{V}]$ was decreased, and the value was about −16 V. $V_{\text{Capacitor}}[\text{V}]$ was charged, and it was about 16 V.

At $0.5 T_1$, the $I_{\text{Mainline}}[\text{A}]$ decreased by about 1 A from about 325 A to about 324 A. In this section, $I_{\text{LC}}[\text{A}]$ is the point at which 0 A is generated, and $I_{\text{Mainline}}[\text{A}]$ and $I_{\text{MCB}}[\text{A}]$ are about 324 A. $V_{\text{Inductor}}[\text{V}]$ was about −33 V, and $V_{\text{Capacitor}}[\text{V}]$ was about 33 V. At this point, the capacitor was fully charged, and there was no current flow due to charging and discharging of the capacitor.

At $0.75 T_1$, $I_{\text{Mainline}}[\text{A}]$ was generated at about 324 A. In this section, $I_{\text{LC}}[\text{A}]$ with the current −40 A occurred, and about 364 A of $I_{\text{MCB}}[\text{A}]$ occurred. $V_{\text{Inductor}}[\text{V}]$ was about −4 V, and $V_{\text{Capacitor}}[\text{V}]$ was about 13 V. At this point, the capacitor was discharged, and the discharged current of the capacitor and $I_{\text{MCB}}[\text{A}]$ were generated together.

At T_1 , $I_{\text{Mainline}}[\text{A}]$ was generated at about 324 A. In this section, about 0 A of $I_{\text{LC}}[\text{A}]$ occurred, and about 324 A of $I_{\text{MCB}}[\text{A}]$ occurred. $V_{\text{Inductor}}[\text{V}]$ was about 9 V, and $V_{\text{Capacitor}}[\text{V}]$ was about −5 V. At this point, the capacitor was completed to discharge, and there was no flow of $I_{\text{LC}}[\text{A}]$.

Table 3 shows the simulation results of current and voltage in the period T_0 to T_6 . In $I_{\text{Mainline}}[\text{A}]$, a fault current of about 333 A occurred at T_0 , and the result was decreased by about 2.7% at T_1 , and after that, about 324 A was maintained. $I_{\text{MCB}}[\text{A}]$ showed the same result as the $I_{\text{Mainline}}[\text{A}]$. The reason is that the value of $I_{\text{LC}}[\text{A}]$ was 0 at the time

T_n , and the capacitor at this time is the time when the discharge is completed. The value of $V_{\text{Inductor}}[\text{V}]$ and $V_{\text{Capacitor}}[\text{V}]$ showed increasing results. This is because the inductor and the capacitor are connected in series; therefore, energy amplification by the resonant frequency occurred.

Table 3. Simulation results of current and voltage from $T_0 \sim T_6$.

Section [ms]	T_0 [102.00]	T_1 [102.19]	T_2 [102.39]	T_3 [102.59]	T_4 [102.79]	T_5 [102.99]	T_6 [103.18]
I_Mainline [A]	333	324	324	323	324	324	324
I_MCB [A]	333	324	324	323	324	324	324
I_LC [A]	0	0	0	0	0	0	0
I_SA [A]	0	0	0	0	0	0	0
V_Inductor [V]	0	9	44	27	38	73	83
V_Capacitor [V]	0	−5	−11	−20	−32	−51	−80

6. Conclusions

We researched a cutoff technology to quickly and safely cut off the fault current that occurs in the transient state, and we proposed a superconducting DC circuit breaker that combines a superconducting element and a mechanical DC circuit breaker. This cutoff method reduces the initial fault current through quenching of the superconducting current-limiting element and creates an artificial current zero points through a mechanical DC circuit breaker so that it can be cut off safely. Creating an artificial current zero point by the LC divergence oscillation circuit is a very important core technology. We sought to examine this technique based on theory through PSCAD/EMTDC simulation. We applied the initial fault current characteristics modeled based on the experimental data to the simulation, and proceeded with the modeling of Mayr's arc model and superconducting DC circuit breaker. In addition, the simulation results were analyzed based on the principle of the LC divergence oscillation circuit. As a result, we were able to verify the degree of current limiting of the initial fault current by the superconducting element and the operating characteristics of each circuit of the mechanical DC circuit breaker through theoretical principles. In addition, we could theoretically confirm the result of generating an artificial current zero point by influencing the fault current as a resonance phenomenon occurring in the circuit through the LC divergence oscillation circuit. This process was reviewed based on the theory, and the data from these results serve as points of reference in the study of commercialization of the LC divergence oscillation circuit.

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References

1. Sapkota, R.; Kolluri, S.; Adhikari, J.; Panda, S.K. MMC based multi-terminal HVDC subsea power transmission system with the integration of offshore renewable energy. In *IEEE Innovative Smart Grid Technologies-Asia (ISGT-Asia)*; IEEE: Piscataway, NJ, USA, 2017; pp. 1–6. [\[CrossRef\]](#)
2. Ahmed, N.; Norrga, S.; Nee, H.P.; Haider, A.; Hertem, D.; Zhang, L. HVDC SuperGrids with Modular Multilevel Converters—The Power Transmission Backbone of the Future. In *Proceedings of the 9th International Multi-Conference on Systems, Signals and Devices*, Chemnitz, Germany, 20–23 March 2012; pp. 1–7. [\[CrossRef\]](#)
3. Le Metayer, P.; Paez, J.; Toure, S.; Buttay, C.; Dujic, D.; Lamard, E.; Dworakowski, P. Break-even distance for MVDC electricity networks according to power loss criteria. In *Proceedings of the 23rd European Conference on Power Electronics and Applications (EPE'21 ECCE Europe)*, 6–10 September 2021; pp. 1–9.
4. Hafez, O.; Bhattacharya, K. Optimal Break-Even Distance for Design of Microgrids. In *IEEE Electrical Power and Energy Conference*; IEEE: Piscataway, NJ, USA, 2012; pp. 139–144. [\[CrossRef\]](#)
5. Parker, M.A.; Holliday, D.; Finney, S.J. DC protection for a multi-terminal HVDC network including offshore wind power, featuring a reduced DC circuit breaker count. *J. Eng.* **2019**, *17*, 4511–4515. [\[CrossRef\]](#)
6. Mitra, B.; Chowdhury, B.; Manjrekar, M. HVDC transmission for access to off-shore renewable energy: A review of technology and fault detection techniques. *IET Renew. Power Gener.* **2018**, *12*, 1563–1571. [\[CrossRef\]](#)
7. Ahmad, M.; Wang, Z. A Hybrid DC Circuit Breaker with Fault-Current-Limiting Capability for VSC-HVDC Transmission System. *Energies* **2019**, *12*, 2388. [\[CrossRef\]](#)
8. Nadeem, M.H.; Zheng, X.; Tai, N.; Gul, M. Identification and Isolation of Faults in Multi-terminal High Voltage DC Networks with Hybrid Circuit Breakers. *Energies* **2018**, *11*, 1086. [\[CrossRef\]](#)
9. Khalid, S.; Raza, A.; Alqasemi, U.; Sobahi, N.; Yousaf, M.Z.; Abbas, G.; Jamil, M. Technical Assessment of Hybrid HVDC Circuit Breaker Components under M-HVDC Faults. *Energies* **2021**, *14*, 8148. [\[CrossRef\]](#)
10. Marroqui, D.; Blanes, J.M.; Garrugós, A.; Gutiérrez, R. Self-powered 380 V DC SiC solid-state circuit breaker and fault current limiter. *IEEE Trans. Power Electron.* **2019**, *10*, 9600–9608. [\[CrossRef\]](#)
11. Li, H.; Yu, R.Z.; Yi, Z.; Yao, R.; Liao, X.L.; Chen, X.P. Design of 400 V miniature DC solid state circuit breaker with SiC MOSFET. *Micromachines* **2019**, *5*, 314. [\[CrossRef\]](#)
12. Ludin, G.A.; Amin, M.A.; Matayoshi, H.; Rangarajan, S.S.; Hemeida, A.M.; Takahashi, H.; Senjyu, T. Solid-State DC Circuit Breakers and Their Comparison in Modular Multilevel Converter Based-HVDC Transmission System. *Electronics* **2021**, *10*, 1204. [\[CrossRef\]](#)
13. Grenzheuser, J.; Lee, C.K. Power loss analysis of five-level inverters for grid tie photovoltaic system. In *Proceedings of the 2013 5th International Conference on Power Electronics Systems and Applications (PESA)*, Hong Kong, China, 11–13 December 2013; IEEE: Piscataway, NJ, USA, 2013; Volume 12, pp. 1–6. [\[CrossRef\]](#)
14. Grgić, I.; Vukadinović, D.; Bašić, M.; Bubalo, M. Calculation of Semiconductor Power Losses of a Three-Phase Quasi-Z-Source Inverter. *Electronics* **2020**, *9*, 1642. [\[CrossRef\]](#)
15. Hafezi, H.; Faranda, R. A New Approach for Power Losses Evaluation of IGBT/Diode Module. *Electronics* **2021**, *10*, 280. [\[CrossRef\]](#)
16. Liang, S.; Tang, Y.; Xia, Z.; Ren, L.; Chen, L.; Xu, Y.; Wang, Z.; Yan, S. Study on the Current Limiting Performance of a Novel SFCL in DC Systems. *IEEE Trans. Appl. Supercond.* **2017**, *27*, 1–6. [\[CrossRef\]](#)
17. Li, B.; Wang, C.; Wei, Z.; Xin, Y.; Li, B.; He, J. Technical Requirements of the DC Superconducting Fault Current Limiter. *IEEE Trans. Appl. Supercond.* **2018**, *28*, 1–5. [\[CrossRef\]](#)
18. Xiang, B.; Luo, J.; Gao, L.; Wang, J.; Geng, Y.; Liu, Z.; Ding, T. Protection schemes using resistive-type superconducting fault current limiters with mechanical DC circuit breakers in MMC-MTDC grids. *IET Gener. Transm. Distrib.* **2020**, *14*, 3422–3432. [\[CrossRef\]](#)
19. Xiang, B.; Gao, L.; Luo, J.; Wang, C.; Nan, Z.; Liu, Z.; Geng, Y.; Wang, J.; Yanabu, S. A CO₂/O₂ Mixed Gas DC Circuit Breaker with Superconducting Fault Current-Limiting Technology. *IEEE Trans. Power Deliv.* **2020**, *35*, 1960–1967. [\[CrossRef\]](#)
20. Xiang, B.; Cheng, N.; Yang, K.; Liu, Z.; Geng, Y.; Wang, J.; Yababu, S. SF₆ passive resonance DC circuit breaker combined with a superconducting fault current limiter. *IET Gener. Transm. Distrib.* **2020**, *14*, 2869–2878. [\[CrossRef\]](#)
21. Song, W.J.; Pei, X.O.; Xi, J.W.; Zeng, X.W. A novel helical superconducting fault current limiter for electric propulsion aircraft. *IEEE Trans. Electrif.* **2021**, *3*, 276–286. [\[CrossRef\]](#)
22. Lee, H.Y.; Asif, M.; Park, K.H.; Mun, H.M.; Lee, B.W. Appropriate Protection Scheme for DC Grid Based on the Half Bridge Modular Multilevel Converter System. *Energies* **2019**, *12*, 1837. [\[CrossRef\]](#)
23. Lee, J.I.; Dao, V.Q.; Dinh, M.C.; Lee, S.J.; Kim, C.S.; Park, M.W. Combined Operation Analysis of a Saturated Iron-Core Superconducting Fault Current Limiter and Circuit Breaker for an HVDC System Protection. *Energies* **2021**, *14*, 7993. [\[CrossRef\]](#)
24. Park, S.Y.; Choi, H.S. Operation Characteristics of Mechanical DC Circuit Breaker Combined with LC Divergence Oscillation Circuit for High Reliability of LVDC System. *Energies* **2021**, *14*, 5097. [\[CrossRef\]](#)
25. Park, S.Y.; Kim, S.H.; Choi, H.S. Analysis of Simulation Operation Characteristics of Superconducting DC Circuit Breaker According to L and C Elements of LC Divergent Vibration Circuit. In *Proceedings of the IEEE International Conference on Applied Superconductivity and Electromagnetic Devices (ASEMD)*, Tianjin, China, 16–18 October 2020; pp. 1–2. [\[CrossRef\]](#)
26. Park, S.Y.; Choi, H.S. Characteristics of a Superconducting DC Circuit Breaker According to L and C Elements of LC Divergent Oscillation Circuit. *IEEE Trans. Appl. Supercond.* **2021**, *31*, 1–4. [\[CrossRef\]](#)

27. Xiang, B.; Junaid, M.; Gao, L.; Liu, Z.; Geng, Y.; Wang, J.; Yanabu, S. Effects of Short Circuit Currents on Quench and Recovery Properties of YBCO Tapes for DC SFCL. *IEEE Trans. Appl. Supercond.* **2019**, *29*, 1–6. [\[CrossRef\]](#)
28. Zha, W.; Qiu, Q.; Cao, S.; Wang, H. Quench and Recovery Characteristics of Solenoid and Pancake SFCLs Under DC Impact Current. *IEEE Trans. Appl. Supercond.* **2020**, *30*, 1–6. [\[CrossRef\]](#)
29. Matsushita, N.; Yanai, S.; Angkoolpakdeekul, T.; Shirai, Y.; Shiotsu, M. Recovery Characteristics of GdBCO Series-Connected Non-Inductive Coil in Pressurized Liquid Nitrogen for a Resistive SFCL. *IEEE Trans. Appl. Supercond.* **2020**, *31*, 1–5. [\[CrossRef\]](#)
30. Mayr, O. Beiträge zur Theorie des statischen und des dynamischen Lichtbogens. *Arch. Elektrotech.* **1943**, *37*, 588–608. [\[CrossRef\]](#)
31. Mayr, O. Über die Theorie des Lichtbogens und seiner Löschung. *Elektrotech. Z. Jahrg.* **1943**, *64*, 645–652.
32. Schavemaker, P.H.; Van der Sluis, L. An Improved Mayr-Type Arc Model Based on Current-Zero Measurements. *IEEE Trans. Power Deliv.* **2000**, *15*, 580–584. [\[CrossRef\]](#)
33. Mo, Y.; Bao, L.; Jia, S.; Shi, Z.; Qin, Y.; Cai, W. The Influence of Transient Interrupting Voltage on the Residual Plasma Dissipation in a 10 kV Mechanical DC Vacuum Circuit Breaker. In Proceedings of the 29th International Symposium on Discharges and Electrical Insulation in Vacuum (ISDEIV), Suzhou, China, 18–23 September 2021; pp. 286–289. [\[CrossRef\]](#)
34. Jia, S.; Tang, Q.; Shi, Z. Review on HVDC circuit-breaker tests. In Proceedings of the 4th International Conference on HVDC, Xi'an, China, 6–9 November 2020; pp. 808–814. [\[CrossRef\]](#)
35. Pauli, B.; Mauthe, G.; Ruoss, E.; Ecklin, G.; Poter, J.; Vithayathil, J. Development of a high current HVDC circuit breaker with fast fault clearing capability. *IEEE Trans. Power Deliv.* **1988**, *3*, 2072–2080. [\[CrossRef\]](#)
36. Nakao, H.; Nakahoshi, Y.; Hatano, M.; Koshizuka, T.; Nishiwaki, S.; Kobayashi, A.; Murao, T.; Yanabu, S. DC Current Interruption in HVDC SF6 Gas MRTB by Means of Self-Excited Oscillation Superimposition. *IEEE Trans. Power Deliv.* **2001**, *16*, 62. [\[CrossRef\]](#)
37. Shen, B.; Chen, Y.; Li, C.; Wang, S.; Chen, X. Superconducting fault current limiter (SFCL): Experiment and the simulation from finite-element method (FEM) to power/energy system software. *Energy* **2021**, *234*, 121251. [\[CrossRef\]](#)
38. Zheng, F.; Deng, C.; Chen, L.; Li, S.; Liu, Y.; Liao, Y. Transient Performance Improvement of Microgrid by a Resistive Superconducting Fault Current Limiter. *IEEE Trans. Appl. Supercond.* **2015**, *25*, 6. [\[CrossRef\]](#)
39. Parizad, A.; Baghaee, H.R.; Tavakoli, A.; Jamali, S. Optimization of Arc Model Parameters Using Genetic Algorithm. In Proceedings of the International Conference on Electric Power and Energy Conversion Systems (EPECS), Sharjah, United Arab Emirates, 10–12 November 2009; pp. 1–7.
40. Van der Sluis, L.; Rutgers, W.R.; Koreman, C.G.A. A physical arc model for the simulation of current zero behavior of high-voltage circuit breakers. *IEEE Trans. Power Deliv.* **1992**, *7*, 1016–1022. [\[CrossRef\]](#)
41. Panousis, E.; Bujotzek, M.; Christen, T. Arc cooling mechanisms in a model circuit breaker. *IEEE Trans. Power Deliv.* **2014**, *29*, 1806–1813. [\[CrossRef\]](#)
42. CIGRE Working Group 13.01. *Applications of Black Box Modelling to Circuit Breakers*; Electra: Florence, Italy, 1993; pp. 41–71.