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Comparative Analysis of PI and ADRC Control through CHIL Real Time Simulations of a DC-DC DAB into a Multi-Terminal MVDC/LVDC Distribution Network

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Abstract: This article presents a deep theoretical analysis of the Active Disturbance Rejection Control (ADRC) regulator for the control of first-order systems, directly compared to a "traditional" Proportional Integral (PI) regulator. To complete the theoretical study, ADRC and PI are implemented into the model of a single-phase Dual Active Bridge (DAB) converter to regulate the voltage of a Direct Current (DC) network. Facing different types of disturbances and DC network parameters variations, strengths and weaknesses of the two controllers are highlighted. ADRC and PI controls are discretized and implemented in Control Hardware In the Loop (CHIL) simulations of a single-phase DAB converter to regulate the voltage of a node of multi-terminal and multi-level DC network. By changing the DAB connection points along the MVDC network, the controlled system is stressed with different disturbances, extending the result of single-terminal network software simulations.

Keywords: ADRC control; real-time simulation; CHIL; MVDC grid; dual active bridge converter; microcontrollers; distribution of electrical energy; converter control

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1. Introduction

This work assesses the impact of innovative control algorithms in DC distribution networks. In particular, the activity is focused on the analysis of the Active Disturbance Rejection Control (ADRC) method to handle DC power converters into a multi-terminal grid, to face heavy load disturbances and smooth voltage oscillations. The ADRC control is compared to traditional control strategies such as Proportional, Integral, or PI control.

At the very beginning, analysis of the scientific literature has been conducted on the ADRC method [1–5]; later on, ADRC has been compared to "traditional" control strategies, specifically Proportional, Integral, or PI [6]; the result was a formal mathematical equivalence between the two algorithms, and the development of a classical tuning technique. In this way, ADRC and PI could be tested and compared through common off-line software simulations.

The simulation case study was represented by the control of a Dual Active Bridge (DAB) converter [7–11] supplied by a simple Medium Voltage Direct Current (MVDC) network for the derivation of a Low Voltage Direct Current (LVDC) sub-network. To focus on comparison between control algorithms, rather than on modulation techniques optimization, Single Phase Shift (SPS) has been chosen; due to its relative simplicity, SPS has been implemented on a commercial, general-purpose microcontroller board. This helped in streamlining the research project.

With respect to other works [2,12], in which the approach was mainly theoretical (mathematical and by means of software simulations) or focused on small scale converters [1], this project involves several power devices into an electrical network. Moreover, software simulations results have been validated through real-time Control Hardware In the Loop (CHIL) tests. DAB control was implemented on a commercial, general-purpose

microcontroller board, while the converter itself and the grid have been modeled through an OPAL-RT simulator. The real-time implementation of a multi-terminal, multi-level DC distribution network is another element of novelty, and this led us to properly stress the response of the real controllers into a more realistic operative scenario.

As a result, the activity allowed to extend the theoretical/simulative considerations that identify ADRC control as a possible alternative to PI control for a power system connected to an MVDC network, also tackling the issues related to physical implementation of digital ADRC control into CHIL simulations. The article is then structured as follows:

- Section 2 shows the methodology used to perform the research in object; it also provides a brief description of the used equipment;
- Section 3 introduces ADRC control; the frequency response of the ADRC controller is formalized in a mathematical form suitable for comparison with the classical PI structure. This section also presents the general formulas necessary to guarantee the equivalence of the control action of the ADRC controller with that of a given PI;
- Section 4 briefly introduces the circuital models used for the simulations and, finally, a DAB voltage controller with ADRC algorithm is developed and tuned;
- Section 5 shows simulation and test results according to previous section theory; at first, the theoretical framework for the discretization of the two continuous algorithms (ADRC and PI) is provided, then the implementation in a physical microcontroller-based control board is described. The MVDC grid equivalent model is progressively extended to give a more accurate representation of the power network and of the phenomena that may arise. The regulators (ADRC and PI) are then evaluated not only by the DAB output voltage regulation effectiveness, but also by input voltage oscillation suppression. Finally, this section shows CHIL simulation results for a complete multi-terminal MVDC grid, with the DAB converter feeding an LVDC network. Robustness to network disturbances of both control architectures (ADRC and PI) is compared, following previous sections synthesis procedures;
- Section 6 provides a discussion about key simulation results, with direct comparison between different cases;
- As a conclusion (Section 7), beyond showing the performance improvement obtained with ADRC, it is confirmed that the ADRC control, even if discretized and implemented on a digital microcontroller, is a valid alternative to PI control for a power system connected to an MVDC network.

2. Materials and Methods

The paper summarizes several years of research, in which the topic has been faced with a bottom-up approach [13–19].

The study is based onto reference implementations in off-line simulation environments of all the main components, such as controller architecture, electric network and power converters. The two chosen environments for the time-domain electromagnetic-transient simulations are ATPDraw (ATP-EMTP) and MATLAB/Simulink (ML/SL). The latter was selected to have an intermediate step in model transposition for the CHIL simulation implementation: since the chosen real-time environment (OPAL-RT by RT-Lab) uses MATLAB/Simulink models to describe the circuit and to run code for power converters control, it was then possible to achieve easier implementation and faster validation.

The real-time simulator setup is composed by two modules: the FPGA module and the CPU. The first one can simulate fast dynamics, then it is used to model the power converter to be controlled by the external (physical) controller and the electric network around. The CPU module is able to execute complex code, but it is slower; it is used to implement the controls of every other device represented in the network.

About the Hardware (HW) platform used to physically implement control algorithms into CHIL tests, a family of widespread and commonly available general-purpose microcontrollers based on ARM® Cortex®-M7 chip (ST NUCLEO-F767ZI) has been selected. The advantages of this choice are straightforward: the board itself is cheap and reliable, it does

not require specialistic equipment for the configuration and programming and it provides a good amount of hardware resources and native compatibility with low-level MicroPython programming language [20]. On the other hand, if compared with more sophisticated DSP or FPGA implementation, it falls short in computation times. For the present work, anyway, this has proven not to be an issue, since it was possible to develop an implementation strategy that fits both the real-time constraints and the HW/SW resources available.

The approach is based on step-by-step correspondence between off-line simulations and CHIL tests, including discrete implementation of the control and validation tests on a benchmark system. After positive result of control implementation and performance comparisons, CHIL real-time simulation has been developed to achieve the needed size and complexity (multi-terminal MVDC power grid).

The correspondence between the complete system responses to the same load change is evaluated by comparing the obtained waveforms of key network nodes, both in off-line and real-time implementations. Of special interest are the control variable and regulated voltage of the power converter directly interfaced with the external (physical) controller.

By doing this, and by weighing the effects of the non-idealities introduced by the physical implementation of the control algorithm, it was possible to validate the effectiveness of the CHIL simulation setup.

3. Background: ADRC and PI Control

3.1. ADRC Control Overview

Active Disturbance Rejection Control (ADRC) is a control strategy that exploits optimal control theory. Employing an Extended State Observer (ESO), it can estimate system variables, allowing for disturbance rejection, as theorized by Professor Han in [6].

In recent times, ADRC has seen both theoretical [2,6,21] and applicative interest [1,3–5]. The control is versatile as it combines the Proportional Integral (PI) simple structure with modern approach based on state observers. Compared to classical PI control, ADRC can reach superior setpoint tracking performances and good disturbance rejection [2].

ADRC control architecture of interest for this work is the first-order scheme. The analysis starts with the linear continuous-time case, describing the mathematical steps at the basis of the theoretical considerations made. While many articles introduce second-order ADRC, here the first-order case will only be considered, due to its implementation in a system that exhibit a dominating first-order behavior. Also considering the goal to compare it with the first-order PI control, both performance-wise and complexity-wise, it is fair to have structures that can be completely defined by the same numbers of parameters (in this case, two).

Consider a simple SISO (Single Input Single Output), first-order process (P), with a DC gain (K), and a time constant (τ).

In Laplace domain, $P(s)$ transfer function is then:

$$P(s) = \frac{Y(s)}{U(s)} = \frac{K}{\tau s + 1}. \tag{1}$$

In time-domain it then becomes:

$$\dot{y}(t) = \frac{K \cdot u(t) - y(t)}{\tau}. \tag{2}$$

Adding to the process a general input disturbance d and introducing the b coefficient, we obtain:

$$\dot{y}(t) = \frac{-y(t) + d(t)}{\tau} + b \cdot u(t), b = \frac{k}{\tau}. \tag{3}$$

As explained in detail in [2] it is then possible to further divide b into a known part (b_0) and an unknown modeling error (Δb). By combining all components of (3) that does not depend on the input u with the unknown modeling error to a so-called generalized

disturbance *f*, the model for the simple first-order process changes from a low-pass type to an integrator one:

$$\dot{y}(t) = f(t) + b_0 \cdot u(t), \tag{4}$$

$$f(t) = \frac{-y(t) + d(t)}{\tau} + \Delta b \cdot u(t). \tag{5}$$

By re-combining the above (4) into a state-space representation, we have:

$$\begin{bmatrix} \dot{x}_1(t) \\ \dot{x}_2(t) \end{bmatrix} = \overset{\text{A}}{\begin{bmatrix} 0 & 1 \\ 0 & 0 \end{bmatrix}} \cdot \begin{bmatrix} x_1(t) \\ x_2(t) \end{bmatrix} + \overset{\text{B}}{\begin{bmatrix} b_0 \\ 0 \end{bmatrix}} \cdot u(t) + \begin{bmatrix} 0 \\ 1 \end{bmatrix} \cdot \dot{f}(t), \tag{6}$$

$$y(t) = \overset{\text{C}}{[1 \quad 0]} \cdot \begin{bmatrix} x_1(t) \\ x_2(t) \end{bmatrix}. \tag{7}$$

The base principle for ADRC control is to implement an extended state observer (ESO), to provide an estimate of the generalized disturbance *f*, since it cannot be measured.

In this case, the observer must provide an estimate of the state vector:

$$\begin{bmatrix} \hat{x}_1(t) \\ \hat{x}_2(t) \end{bmatrix} = \begin{bmatrix} y(t) \\ f(t) \end{bmatrix}. \tag{8}$$

The observer operates in parallel to the controlled process and it can be built only by acquiring the input and output values *u(t)* and *y(t)*.

For the desired linear ADRC, a Luenberger observer (*L*) can be used [22]. The observer is mathematically modeled on the process itself, keeping the characteristic matrices and the system order.

Figure 1 briefly shows how ESO operates in the generalized control scheme; Equations (9) and (10) below provide the state-space description of the Luenberger extended state observer.

$$\begin{bmatrix} \dot{\hat{x}}_1(t) \\ \dot{\hat{x}}_2(t) \end{bmatrix} = \overset{\text{A}}{\begin{bmatrix} 0 & 1 \\ 0 & 0 \end{bmatrix}} \cdot \begin{bmatrix} \hat{x}_1(t) \\ \hat{x}_2(t) \end{bmatrix} + \overset{\text{B}}{\begin{bmatrix} b_0 \\ 0 \end{bmatrix}} \cdot u(t) + \overset{\text{L}}{\begin{bmatrix} l_1 \\ l_2 \end{bmatrix}} \cdot [y(t) - \hat{x}_1(t)], \tag{9}$$

$$\begin{bmatrix} \dot{\hat{x}}_1(t) \\ \dot{\hat{x}}_2(t) \end{bmatrix} = \overset{\text{A-LC}}{\begin{bmatrix} -l_1 & 1 \\ -l_2 & 0 \end{bmatrix}} \cdot \begin{bmatrix} \hat{x}_1(t) \\ \hat{x}_2(t) \end{bmatrix} + \overset{\text{B}}{\begin{bmatrix} b_0 \\ 0 \end{bmatrix}} \cdot u(t) + \overset{\text{L}}{\begin{bmatrix} l_1 \\ l_2 \end{bmatrix}} \cdot y(t). \tag{10}$$

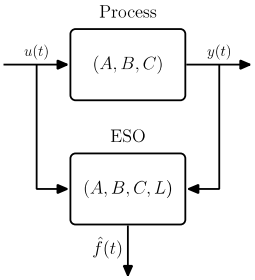

Figure 1. ESO conceptual operation.

Using the bandwidth parametrization technique [21], *L* matrix parameters (l_1 and l_2) can be derived as functions of the observer bandwidth (ω_o); the ESO eigenvalues (observer poles) are computed as a function of the chosen observer bandwidth:

$$det[sI - (A - LC)] = (s + \omega_O)^n, \tag{11}$$

where *n* represents the state variables multiplicity (2 for the first-order ADRC).

With chosen parametrization, Equation (11) becomes:

$$s^2 + l_1 \cdot s + l_2 = s^2 + 2 \cdot \omega_O \cdot s + {\omega_O}^2, \tag{12}$$

and then the Luenberger matrix parameters are defined as:

$$\begin{cases} l_1 = 2 \cdot \omega_O \\ l_2 = {\omega_O}^2 \end{cases}. \tag{13}$$

Starting from the observer state-space Equations of (9) and (10), first-order ESO is then described in Laplace domain by:

$$\begin{cases} \hat{x}_1 = \frac{l_1 \cdot (y - \hat{x}_1) + \hat{f} + b_0 \cdot u}{s} \\ \hat{f} = \frac{l_2 \cdot (y - \hat{x}_1)}{s} \end{cases}. \tag{14}$$

A graphical representation for the observer structure is given by the block diagram of Figure 2.

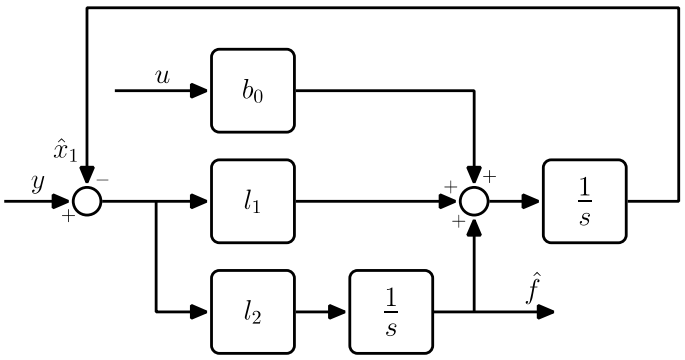

Figure 2. ESO structure block scheme.

Manipulating (4) and considering the observer estimate $\hat{x}_2$ as the value for the generalized disturbance $\hat{f}$, it can be written:

$$u(t) = \frac{\dot{y}(t) - \hat{f}(t)}{b_0} = \frac{\dot{y}(t) - \hat{x}_2(t)}{b_0}. \tag{15}$$

The model can now be considered as an integrator if it holds true that the $\hat{x}_2$ estimate is equal to the generalized disturbance *f*. The process can then be controlled by a simple proportional controller (K_A), with $\dot{y}$ being re-written as the difference between the system set-point q and the output y:

$$\dot{y}(t) \approx u_0(t) = K_A \cdot [q(t) - y(t)]. \tag{16}$$

by using the calculations of (15) and (16), an equivalent control loop structure for the SISO, first-order ADRC is given (Figure 3).

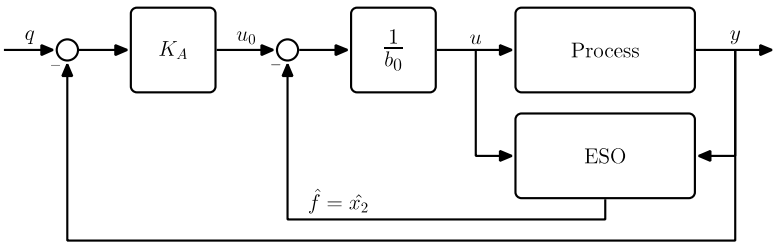

Figure 3. Control loop structure with ADRC for a first-order process.

Following the frequency domain analysis described in [23], it is then possible to trace back the input-output transfer function of the linearized first-order ADRC and process feedback loop (as presented in Figure 3) to the simplified scheme of Figure 4. In this configuration, the control action is separated in a pre-filter action *GF(s)* and a pure feedback controller *GC(s)*. This, if compared with a classical PI regulator control loop, is a first major differentiating factor.

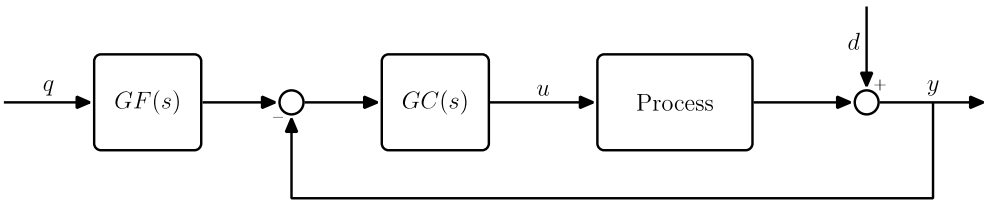

Figure 4. Input-output control loop block scheme in frequency domain.

The structure and transfer functions for the two blocks of Figure 4 can be obtained by simple manipulations and combining the ESO state-space equations with (13) and (15). In Laplace domain it results:

$$\begin{cases} GC(s) = \frac{1}{b_0 \cdot s} \cdot \frac{K_A s^2 + \left(\omega_0{}^2 + 2K_A\omega_0\right)s + K_A \cdot \omega_0^2}{s + 2\omega_0} \\ GF(s) = \frac{K_A \cdot (s+\omega_0)^2}{K_A s^2 + (\omega_0{}^2 + 2K_A\omega_0)s + K_A \cdot \omega_0^2} \end{cases}. \tag{17}$$

In a classical PI control scheme, the regulator is placed in the same position of *GC(s)* of Figure 4. As a result, ADRC and PI equivalence theory presented in next section assesses comparison and parametrization between the PI regulator and *GC(s)*.

3.2. ADRC and PI Equivalence (Theory, Background)

Consider the classic control structure of a PI regulator, *R(s)* in (18), defined throughout its proportional and integral coefficients (k_p, k_i):

$$R(s) = \left(k_p + \frac{k_i}{s}\right) = k_i \frac{1 + s\left(\frac{k_p}{k_i}\right)}{s}. \tag{18}$$

The ratio k_p/k_i, in (18), allows to define the time constant of the zero (and consequently the critical pulsation). Considering *GC(s)* expression in (17), two poles can be easily identified.

One pole is in the origin, while its only non-zero pole is:

$$s_{p1} = -2\omega_0. \tag{19}$$

The same transfer function also possesses two zeroes. In order to tune the loop transfer function to the same shape of the PI control in (18), it is necessary to place one of those zeroes in correspondence to the pole (19). This allows for a pole-zero cancellation and, provided that it is possible to place the remaining zero in correspondence to the PI regulator one, to obtain a perfect "PI equivalent" ADRC setting. A qualitative representation of *GC(s)* frequency response magnitude equivalent to a known PI controller is plotted in Figure 5.

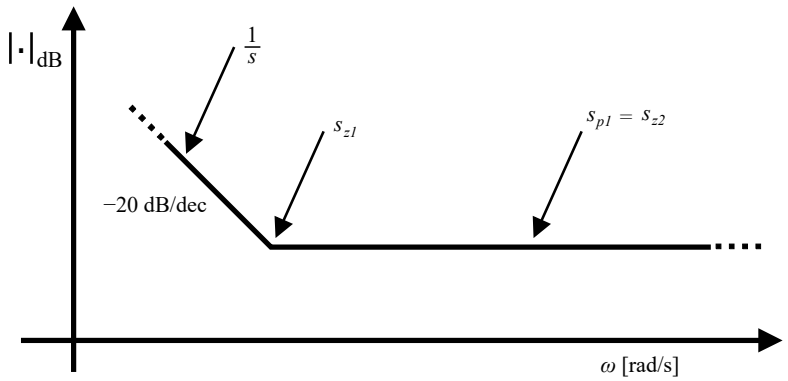

Figure 5. Bode magnitude plot of *GC(s)* with tuning equivalent to a PI regulator.

Applying the already mentioned constraints to *GC(s)* poles and zeroes and introducing a coefficient functional to the algebraic calculations (α), the following system can be obtained:

$$\begin{cases} s_{z2} = s_{p1} = -2\omega_0 \\ s_{z1} = -\alpha \end{cases}. \tag{20}$$

The generalized *GC(s)* expression can then be modified as follows:

$$GC(s) = \alpha \frac{K_A}{b_0} \frac{\left(1 + \frac{1}{\alpha}s\right)}{s} \frac{(s + 2\omega_0)}{(s + 2\omega_0)}. \tag{21}$$

By comparing *GC(s)* numerators of (17) and (21) it gives:

$$K_A s^2 + (\omega_0^2 + 2K_A\omega_0)s + K_A\omega_0^2 = K_A(s + 2\omega_0)(s + \alpha) = K_A s^2 + (K_A\alpha + 2K_A\omega_0)s + 2K_A\omega_0\alpha; \tag{22}$$

and pairwise equating the first and last term of (22) gives:

$$\begin{array}{l} \begin{cases} K_A\alpha + 2K_A\omega_0 = {\omega_0}^2 + 2K_A\omega_0 \\ 2K_A\omega_0\alpha = K_A \cdot \omega_0^2 \end{cases} \\ \begin{cases} K_A\alpha = {\omega_0}^2 \\ 2\alpha = \omega_0 \end{cases} \\ K_A\alpha = 4\alpha^2 \\ \frac{K_A}{\alpha} = 4\,,\ \forall\omega_0 > 0 \end{array} \tag{23}$$

From (23) it is possible to briefly define the procedure to obtain a linear first-order ADRC setting equivalent with a known PI regulator:

1. α is set, based on the PI regulator zero:

$$\alpha = \frac{k_i}{k_p}. \tag{24}$$

2. ω_o and K_A are calculated as a function of α, and consequently as a function of k_p and k_i:

$$\omega_0 = 2\alpha = 2\frac{k_i}{k_p} \cdots, \cdots K_A = 2\omega_0 = 4\alpha = 4\frac{k_i}{k_p}. \tag{25}$$

3. b_0 is chosen as to keep *GC(s)* gain equal to the PI gain (k_i):

$$b_0 = \alpha\frac{K_A}{k_i} = \frac{k_i}{k_p}4\frac{k_i}{k_p}\frac{1}{k_i} = 4\frac{k_i}{k_p^2}. \tag{26}$$

This last Equation (26) can be obtained by comparing the expressions of DC gains in (18) and (21).

Equation (23) also highlights another remarkable result: equivalence of *CG(s)* with a classical PI controller is always possible, without limitations over the observer bandwidth value. Furthermore, (25) establishes that there is a well-defined value of ω_0 that achieves, together with the other parameters (24) and (26), equivalence with a specific PI tuning. Nevertheless, the dynamic behavior of the ADRC controller, made equivalent to a PI, is independent of the value of the observer bandwidth, which in fact is simplified in the *GC(s)* formula. This result should not be surprising, since ω_o is not within the tuning parameters of a PI controller.

The same dynamic behavior, however, is not found in *GF(s)*, where the value of ω_o does not simplify:

$$GF(s) = \frac{(s+\omega_0)^2}{(s+2\omega_0)(s+\alpha)} \tag{27}$$

It follows that the system with ADRC regulator equivalent to a known PI regulator will have two different dynamic behaviors:

- one related to the variation of the input (so-called setpoint tracking);
- another related to disturbances rejection.

This approach allows for an easy tuning of ADRC starting from a given PI. On the other hand, it limits ADRC performances, as it excludes the presence of a pole and a zero that could instead be somehow exploited in the control. This strategy is anyway useful and necessary to critically compare the performance of two physical implementations of the ADRC and PI controllers.

In the next section, the control approach of a Dual Active Bridge (DAB) converter will be introduced, and the described technique will be extensively used to tune both ADRC and PI regulators. In order to present such results, the models used in simulations will also be briefly described.

4. First Off-Line Comparison: Simulations and Controller Tuning

4.1. DAB and DC Network Equivalent Model for Simulations

DC-DC Dual Active Bridge converter (DAB) is a very promising technology to connect Medium Voltage DC (MVDC) grids to Low Voltage DC (LVDC). Besides its bidirectional operation easiness, modular structure, and competitive efficiency [9], DAB converter can provide the needed voltage scaling.

DAB topology adopted for the analysis in this section (Figure 6) has been extensively used in so-called Solid State Transformers (SST) topologies [24–26]; it is made by two H-bridge converters, back-to-back connected with a leakage inductor (L) responsible for power transfer. As stated before, the two H-bridges are driven in SPS (Single Phase Shift) modulation: both bridges are controlled in square wave mode and power flow is modulated by changing their relative time shift T_φ. Such solution, even if relatively simple, led to keep modulation technique as fast as possible, and focus on control algorithms behavior.

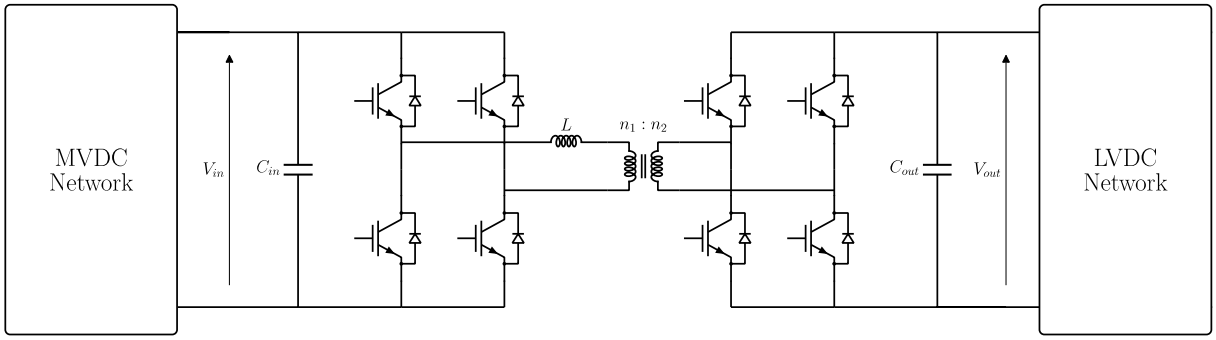

Figure 6. DAB model topology.

DAB converter used in the following simulations has been sized in previous works [15,17,19]; its main parameters are shown in Table 1.

Table 1. DAB main parameters.

Quantity	Value	Notes
V_{in}	2000 V	Rated input voltage
V_{out}	750 V	Rated output voltage
P_n	1 MW	Rated power
$T_{\varphi n}$	25 µs	Rated time-shift
P_{MAX}	1.3 MW	Maximum power
ΔV_{MAX}	±1.25% V_{out}	Maximum ripple
f_s	5 kHz	Switching frequency
T_s	200 µs	Switching period
L	0.075 mH	Leakage inductance
C_{in}	10,000 µF	Input capacitance
C_{out}	10,000 µF	Output capacitance
$n = n_1/n_2$	0.375	Transformer ratio

To tune the regulators and support this article analyses, the DAB equivalent circuit static relationships are described: the system is supposed linear and stationary in the range of the nominal operating point to compute the main transfer function in Laplace domain. This method is derived from literature [11] and leads to a first-order DAB transfer function with a DC gain and a single time constant.

This approach leads anyway to useful results: one is interested in having a meaningful but simplified representation. Starting from a "first-order linearized equivalent" it is left the controller itself the ability to "compensate" the discrepancies in that model.

The linearized and simplified dynamic model of the DAB converter is obtained from an ATPDraw simulation, trying to replicate the practical characterization process of an "unknown" system through simple tests. DAB converter has been modeled with:

- complete topological configuration as shown in Figure 6;
- ideal DC power supply, at rated voltage (V_{in} = 2000 V);
- rated resistive load (R_{load} = 0.5625 Ω), sized to absorb rated power (P_n = 1 MW) at rated output voltage (V_{out} = 750 V), with rated time-shift ($T_{\varphi n}$ = 25 µs).

In this set-up, the system is controlled in open-loop, operating directly on the time-shift T_φ between the two H-bridges voltages. Starting from zero time-shift, at 0.1 s, a step exactly equal to $T_{\varphi n}$ was applied. The output voltage of the converter has been then brought to the nominal value V_{out}, following the dynamics of the device in the chosen configuration.

In practice, the test structured in this way allows to inspect the transfer function of the uncontrolled system: it is therefore possible to determine its nature and peculiar characteristics. From the analysis of the output transient, we obtain the "natural" settling time T_{setDAB} of the system, which can be defined as the time needed by V_{out} to reach the 98% of the voltage nominal value (750 V). The simulation result is reported in Figure 7.

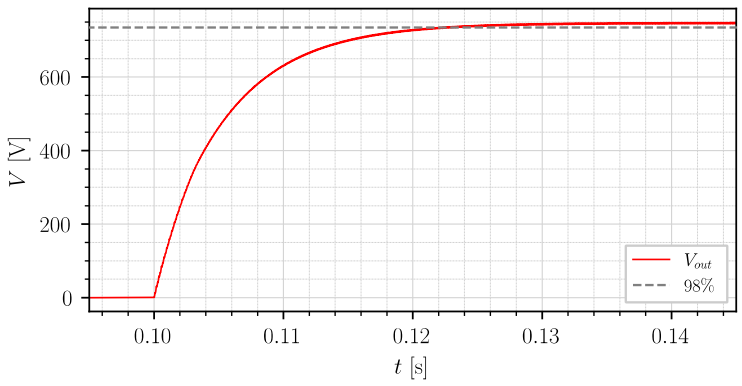

Figure 7. Output voltage (V_{out}) trend (red) and reference line for the 98% of the rated voltage (grey dashed) with DAB converter in open-loop mode.

Based on the V_{out} trend in Figure 7, it is deducted that the DAB behavior, in nominal conditions, is comparable to a first-order system whose time constant (τ_{DAB}) is:

$$T_{setDAB} = 22\,\text{ms} \cdots \rightarrow \cdots \tau_{DAB} = \frac{T_{setDAB}}{4} = 5.5\,\text{ms}. \tag{28}$$

Knowing both the value of $T_{\varphi n}$ (25 µs), and of the voltage V_{out} (750 V), it can be determined the gain (K_{DAB}) of the transfer function $P_{DAB}(s)$:

$$K_{DAB} = \frac{V_{out}}{T_{\varphi n}} = 3 \cdot 10^7 \ \frac{\text{V}}{\text{s}}. \tag{29}$$

The complete DAB transfer function results to be:

$$P_{DAB}(s) = \frac{K_{DAB}}{1 + s \cdot \tau_{DAB}} = \frac{3 \cdot 10^7}{1 + s \cdot 5.5 \cdot 10^{-3}}. \tag{30}$$

For what concerns the following simulations, the DAB has been connected:

- on the MVDC side, to a single-terminal network;
- on the LVDC side, to a constant power load.

More in detail, the MVDC network is made by the π-model shown in Figure 8, whose electrical parameters are summarized in Table 2.

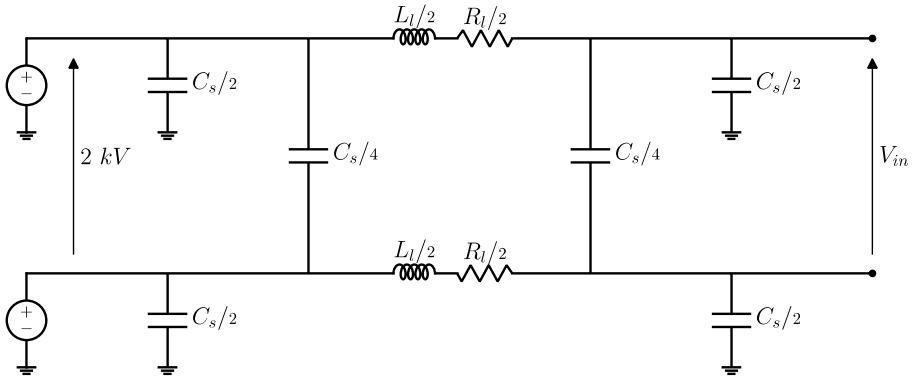

Figure 8. Electric network topology.

Table 2. List of grid parameters.

Parameter	Value
Number of cable lines	2
Line length (l)	1 km
Line resistance (R_l)	0.0283 Ω
Line inductance (L_l)	0.8 mH
Service capacitance (C_s)	0.92 µF

The LVDC network is represented by a Constant Power Load (CPL) which is directly connected to the DAB output port; the model of the load (Figure 9) is made of a boost DC-DC converter (chopper), capable to step up the input LVDC grid voltage (750 V) to 1000 V, supplying a resistive load (R = 1 Ω) sized to absorb 1 MW at 1000 V.

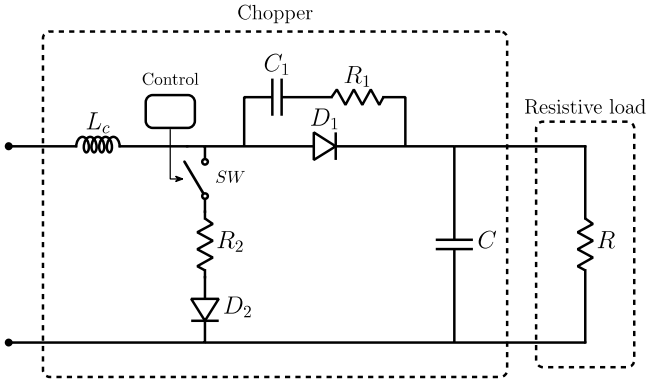

Figure 9. Constant Power Load (CPL) model.

The purpose of the chopper control is to keep the power absorbed from the LVDC side constant by measuring the input voltage; the control algorithm is based on a hysteresis band regulation of the current flowing in the L_c inductance.

The characteristic parameters of the load are listed in Table 3.

Table 3. List of load parameters.

Parameter	Value
Nominal constant power	1 MW
Nominal voltage V_{out}	750 V
Nominal current I_n	1333 A
Current hysteresis band	10% I_n
Switching frequency	10 kHz
Inductance L_c	0.5 mH
Capacitance C	500 µF
Resistive load R	1 Ω
Snubber circuit	R_1 = 20 Ω, C_1 = 10 µF
Switch resistance R_2	10 mΩ

An example of power electronic components suitable for a physical implementation of the equipment is shown in Table 4; full data list is available on datasheets [27,28].

Table 4. Power electronics components suitable for equipment implementation.

DAB MVDC Side	DAB LVDC Side and Chopper	Parameter	Unit
IHM-B module	IGBT- Module	Description	-
2400	3600	Continuous DC rated current	A
4800	7200	Repetitive peak collector current (for 1 ms)	A
3300	1700	Collector emitter voltage	V
6000	4000	Insulation test voltage	V

For the DAB stability under CPL conditions, the following brief analysis applies. Since CPL model is nonlinear, and has a negative impedance characteristic, it is common practice to linearize it in a voltage operating point V_{out} [29]. In this case, CPL nominal voltage and power correspond to DAB ones, thus the linearized model is basically equal to resistive load value presented above.

Based on further approach in literature [12], DAB cascaded power electronic converter with CPL can be reduced to a linearized transfer function equal to (30). In this way, PI preliminary tuning can be performed by using a "classical" control approach based on phase and gain margins.

4.2. First Off-Line Comparison between ADRC and PI Controllers

Having briefly described the base network topology used in the upcoming elaborations, it is possible to present a comparison between the two regulators implementation (ADRC and PI) in off-line simulations. The structure shown in Section 3.1 is used. No intentional discretization process has been applied to the base equations composing both the PI and linear first-order ADRC regulators. The obtained implementations will then be referenced to as quasi-continuous since the chosen simulation environments for such comparisons (ATPDraw) does not allow for continuous-time simulation. The implicit discretization—and the accompanying approximation—due to the intrinsically discrete-time nature of the numerical integration algorithm used in this implementation [30] can be anyway mitigated by selecting an appropriate time-step. In this case, 1 µs time-step has been chosen, many times smaller than the faster dynamics to be investigated and two order of magnitude less than half of the controlled converter switching period (T_s).

The first comparison involves a reference PI regulator whose parameters are presented in Table 5 and the ADRC counterpart obtained by the "PI-equivalent" setting procedure described in Section 3.2 (also in Table 5).

Table 5. Regulator setting parameters.

Regulator	Parameter	Value
PI	k_p	3.33×10^{-7}
	k_i	6.06×10^{-5}
ADRC	b_0	2.18×10^{9}
	K_A	727.27
	l_1	727.27
	l_2	1.32×10^{5}

The simulation test setup has been arranged to compare regulators responses facing grid disturbances. Events are organized as follows:

- $t < 0.1$ s: the DAB regulates, at no load, the voltage (750 V), no power transfer from MVDC to LVDC side;
- $t = 0.1$ s: constant power load is connected to DAB LVDC side. DAB must keep LVDC voltage stable;
- $t = 0.5$ s: load is disconnected; DAB must handle the load rejection keeping LVDC voltage regulated.

Key results of the comparison between PI and ADRC regulators are in the following pictures. It is important to underline that, for graphical reasons, an intentional displacement between tracks has been added in every figure (1 or 2 ms, as detailed in each caption).

The signals of interest are DAB power profile (Figure 10), DAB input voltage V_{in} (Figure 11) and DAB output voltage V_{out} and control variable T_φ (Figure 12).

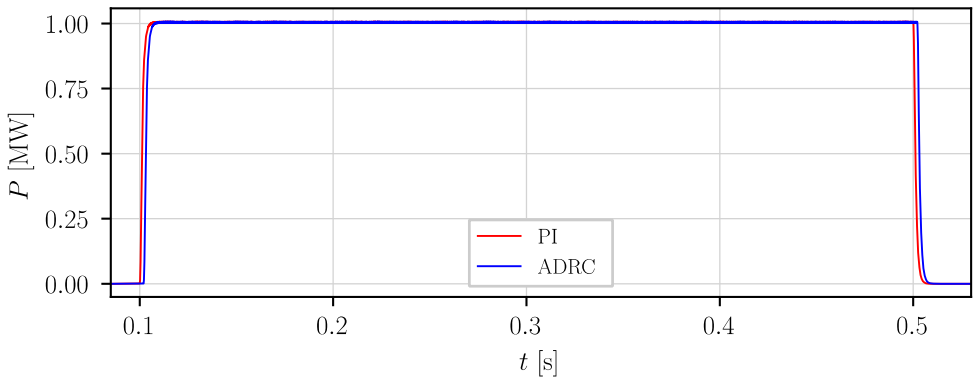

Figure 10. DAB output power. The two tracks are horizontally displaced by 2 ms for graphical reasons.

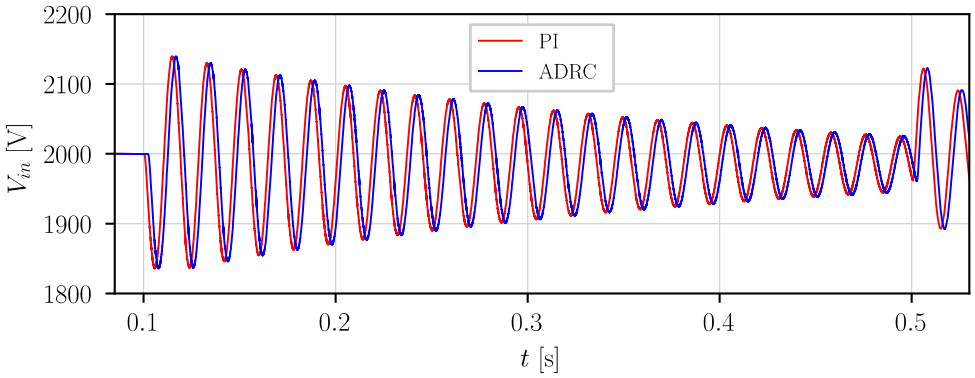

Figure 11. DAB input voltage (V_{in}). The two tracks are horizontally displaced by 2 ms for graphical reasons.

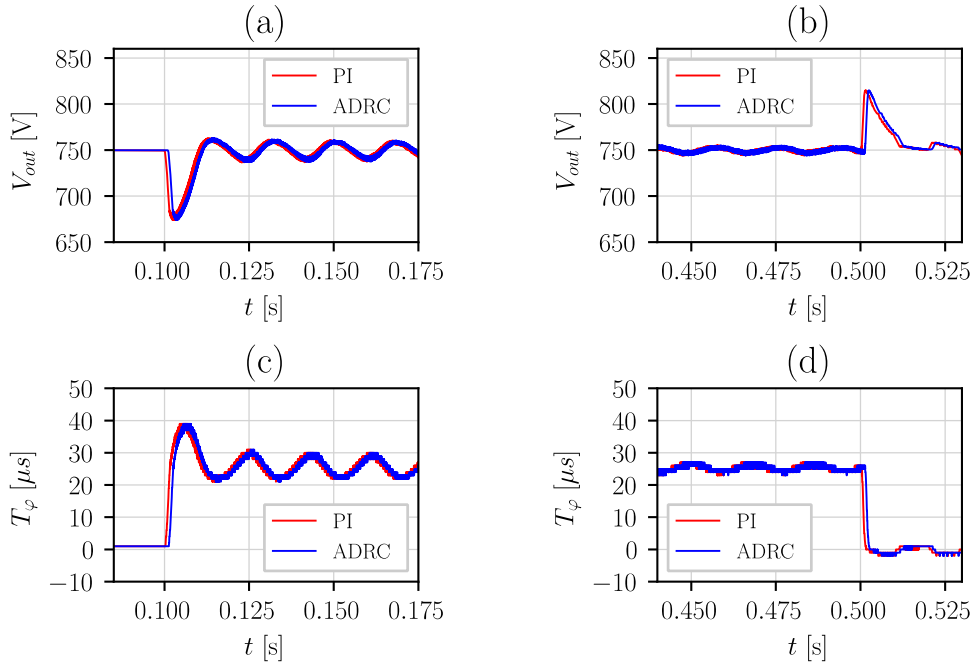

Figure 12. DAB output voltage V_{out} and control variable T_φ at loading (**a**,**c**) and unloading (**b**,**d**). The two tracks are horizontally displaced by 1 ms for graphical reasons.

The comparison between the reference PI and the corresponding "PI-equivalent" ADRC results in a striking resemblance in each track. The equivalence is made more evident also by the analysis of Figure 12: both the DAB control variable T_φ (that is the control action $u(t)$ of the respective regulator implementation) and the regulated voltage V_{out} (that is the feedback-measure $y(t)$) have the exact same response.

4.3. ADRC Re-Tuning and Comparison with PI

Looking at input voltage of Figure 11, it is evident that the load connection excites a network resonance, causing extensive stresses and potentially harmful operating conditions. It is then important to investigate the possibility to partially mitigate this phenomenon by simple control parameters tuning, avoiding power hardware modifications.

Recalling the conclusion of Section 3.2, where it was pointed out that the strict PI-equivalence imposes limits to ADRC structure, a possible way to achieve this is to exploit the pole and zero that were cancelled out. This new ADRC setting is then characterized by an implicit design trade-off: to limit the network resonance excitation, a voltage regulation performance degradation may be necessary. Here, the more flexible ADRC structure, when compared to a classical PI, can make the difference.

Before reviewing the new ADRC regulator tuning process, it is important to summarize some key assumptions:

1. the bandwidth parametrization introduced in Section 3.1 is preserved. Thus, the ADRC structure is not "completely free" but the *GC(s)* expression of (17) is still valid;
2. a straightforward countermeasure to limit the resonance excitation would be to reduce the open loop transfer function gain, operating on PI regulator gain. Unfortunately, this reduced-gain PI would then proportionally lose dynamic performances up to a point where it would not be suitable anymore to properly regulate LVDC voltage;
3. the new linear first-order ADRC setting should exploit the open loop transfer function analysis, referring the new tuning to the original PI controller and to the reduced-gain one, combining the advantages of each;
4. the synthesized controller shall provide the controlled system with the same expected critical angular frequency (ω_c^*) as the original PI controller and a reduction in amplitude of the resonant peak. Then, overall system damping will be increased without excessively sacrificing the dynamic performance.

The above considerations translate into a system whose open loop transfer function should have the asymptotic form of Figure 13. In the same graph, it is also compared with the asymptotic Bode plots of the reference PI controller and the reduced-gain one.

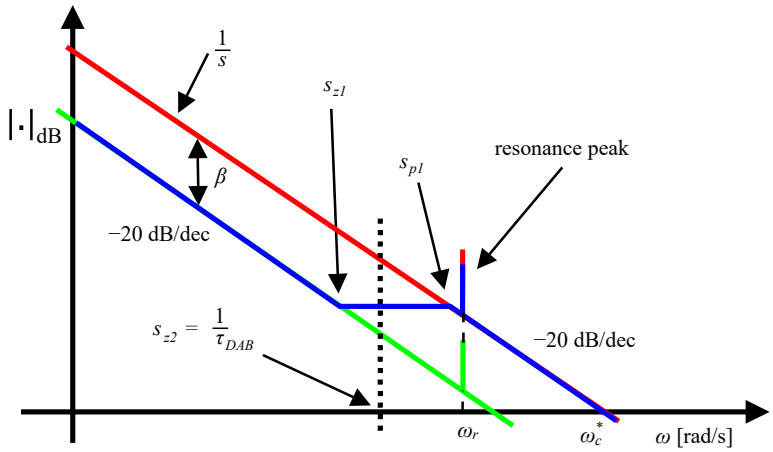

Figure 13. Asymptotic Bode plots of the open loop transfer function requirements for the new ADRC setting (blue). Reference PI (red) and reduced-gain one (green).

The constraints summarized in Figure 13 can be translated in a set of requirements over the *GC(s)* poles and zeroes location. By recalling the general expression of (17), an explicit poles-zeroes expression of *GC(s)* is:

$$GC(s) = \frac{\mu_{ADRC}}{s} \cdot \frac{(1 + s \cdot \tau_{z1})(1 + s \cdot \tau_{z2})}{(1 + s \cdot \tau_{p1})}, \tag{31}$$

where μ_{ADRC} is the DC gain and τ_{p1}, τ_{z1} and τ_{z2}, are poles-zeroes time-constant. The open loop transfer function can be then expressed as:

$$L_{ADRC}(s) = \frac{\mu_{ADRC}}{s} \cdot \frac{(1 + s \cdot \tau_{z1})(1 + s \cdot \tau_{z2})}{(1 + s \cdot \tau_{p1})} \cdot \frac{K_{DAB}}{1 + s \cdot \tau_{DAB}}, \tag{32}$$

having introduced the linearized DAB transfer function expression of (30).

It is necessary to cancel the DAB linearized transfer function pole with one of the zeroes of *GC(s)*. The location of the "fast" zero (the one with a lower time constant) is then determined by the DAB pole location τ_{DAB}:

$$\tau_{z2} = \tau_{DAB}. \tag{33}$$

The only *GC(s)* non-zero pole can then be placed at an angular frequency slightly smaller than the system resonance frequency.

The main reason behind this choice is to introduce an attenuation in the resonance peak, incorporating the advantage of the reduced-gain PI. The exact positioning is a design choice and, in this case, τ_{p1} has been selected as:

$$\omega_{p1} = \frac{1}{\tau_{p1}} = \frac{\omega_r}{\sqrt{2}}, \tag{34}$$

where ω_r is the network resonance angular frequency. Then, recalling (19), it is possible to find the expression for the desired ω_o:

$$\omega_0 = \frac{\omega_{p1}}{2} = \frac{1}{2 \cdot \tau_{p1}}. \tag{35}$$

The remaining zero placement is then univocally determined by the bandwidth parametrization chosen for the ESO formulation. To get the complete system of equations that determines the new ADRC tuning, it is necessary to manipulate (17) and (31) as follows:

$$\begin{aligned} GC(s) &= \frac{1}{b_0 \cdot s} \cdot \frac{K_A s^2 + \left({\omega_0}^2 + 2K_A\omega_0\right)s + K_A \cdot \omega_0^2}{s + 2\omega_0} = \\ &= \frac{K_A\omega_0}{2b_0 \cdot s} \cdot \frac{\frac{1}{\omega_0^2}s^2 + \left(\frac{\omega_0 + 2K_A}{K_A\omega_0}\right)s + 1}{\frac{1}{2\omega_0}s + 1}, \end{aligned} \tag{36}$$

$$\begin{aligned} GC(s) &= \frac{\mu_{ADRC}}{s} \cdot \frac{(1 + s\cdot\tau_{z1})(1 + s\cdot\tau_{z2})}{(1 + s\cdot\tau_{p1})} = \\ &= \frac{\mu_{ADRC}}{s} \cdot \frac{\tau_{z1}\tau_{z2}s^2 + (\tau_{z1} + \tau_{z2})s + 1}{1 + s\cdot\tau_{p1}}. \end{aligned} \tag{37}$$

Pairwise equating the last members of (36) and(37), while considering (35), we get a system of equations determining the new ADRC setting parameters:

$$\begin{cases} \frac{1}{{\omega_0}^2} = \tau_{z1} \cdot \tau_{z2} \\ \frac{\omega_0 + 2K_A}{K_A \cdot \omega_0} = \tau_{z1} + \tau_{z2} \\ \mu_{ADRC} = \frac{K_A \cdot \omega_0}{2 \cdot b_0} \end{cases}. \tag{38}$$

The system can be solved for the desired K_A and b_0 imposing that around the critical angular frequency (${\omega_c}^*$) the ADRC and reference PI must have the same asymptotic behavior (see Figure 13). This can be translated as:

$$[L_{ADRC}(s)]_{\omega=\omega_c^*} \propto [L_{PI}(s)]_{\omega=\omega_c^*} = \frac{\omega_c^*}{s} = \frac{k_i \cdot K_{DAB}}{s}, \tag{39}$$

$$\mu_{ADRC} = \frac{\omega_c^*}{K_{DAB}} = k_i. \tag{40}$$

The newly determined ADRC parameters are presented in Table 6, together with the reference PI (un-modified if compared to Table 5). As the bandwidth parametrization still holds valid, the Luenberger matrix coefficients (l_1 and l_2) are computed by (13).

Table 6. Regulator setting parameters.

Regulator	Parameter	Value
PI	k_p	3.33×10^{-7}
	k_i	6.06×10^{-5}
ADRC—new setting	b_0	2.82×10^{9}
	K_A	997.22
	l_1	250
	l_2	1.56×10^{4}

It is then useful to repeat the comparison between these PI and ADRC settings (Table 6) using the same simulation structure as previously done. Consequently, the signals of interest are the same as before:

- DAB power profile (Figure 14);
- DAB input voltage V_{in} (Figure 15);
- DAB output voltage V_{out} and control variable T_{φ} (Figure 16).

The regulated voltage V_{out} profile (Figure 16a,b), although showing obvious differences in the first part of the dynamic response, exhibits an overall comparable performance both for the reference PI and the new ADRC setting. The average response profile is conserved, with a first-order exponential envelope. Similar considerations can be repeated for the DAB control variable (Figure 16c,d). The steady-state value is clearly identical, both for V_{out} and T_{φ}. When looking at the converter output power (Figure 14), no significative performance reduction for the supplied load can be identified.

As a final remark, converter input voltage V_{in} (Figure 15) is the major difference between the two implementations. Comparing these two tracks also with Figure 11 nothing has changed in terms of resonance frequency. Anyway, MVDC voltage oscillation now exhibits higher damping, leading to a shorter overall transient. New ADRC setting successfully manages to limit the resonance excitation by giving shape to the aforementioned design trade-off involving voltage regulation performance degradation.

After successful re-tuning of ADRC control, the next section introduces a further step to compare PI and ADRC regulators in a CHIL real-time simulation: control algorithms are discretized to be programmed into a microcontroller board and interfaced with the simulation environment.

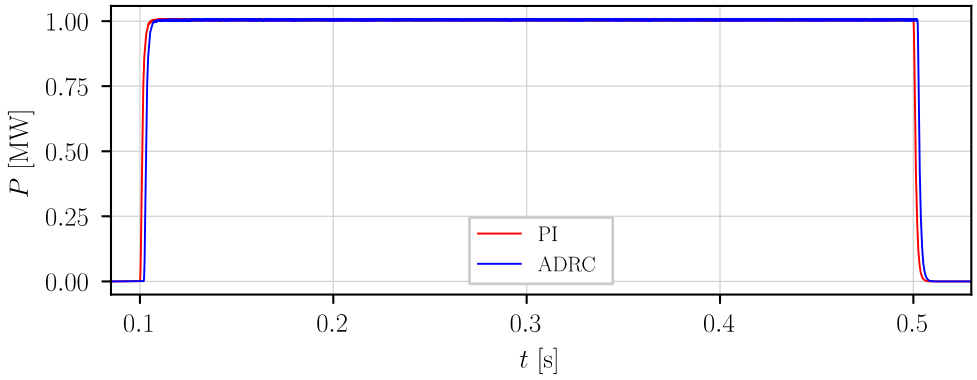

Figure 14. DAB output power. The two tracks are horizontally displaced by 2 ms for previous comparison consistency.

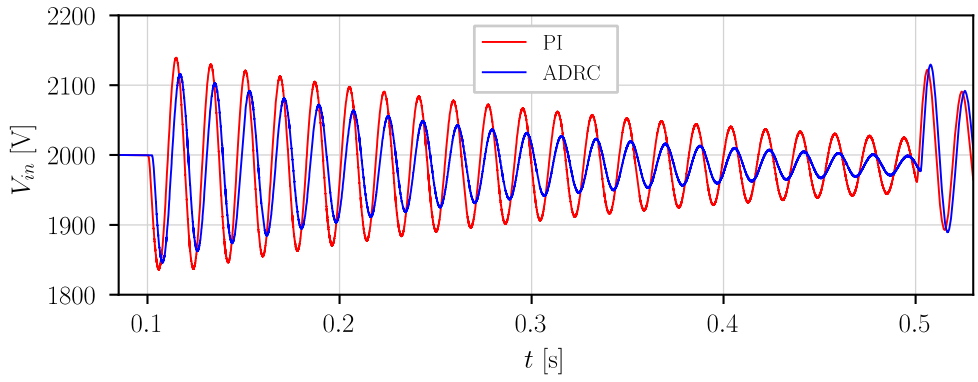

Figure 15. DAB input voltage (V_{in}). The two tracks are horizontally displaced by 2 ms for previous comparison consistency.

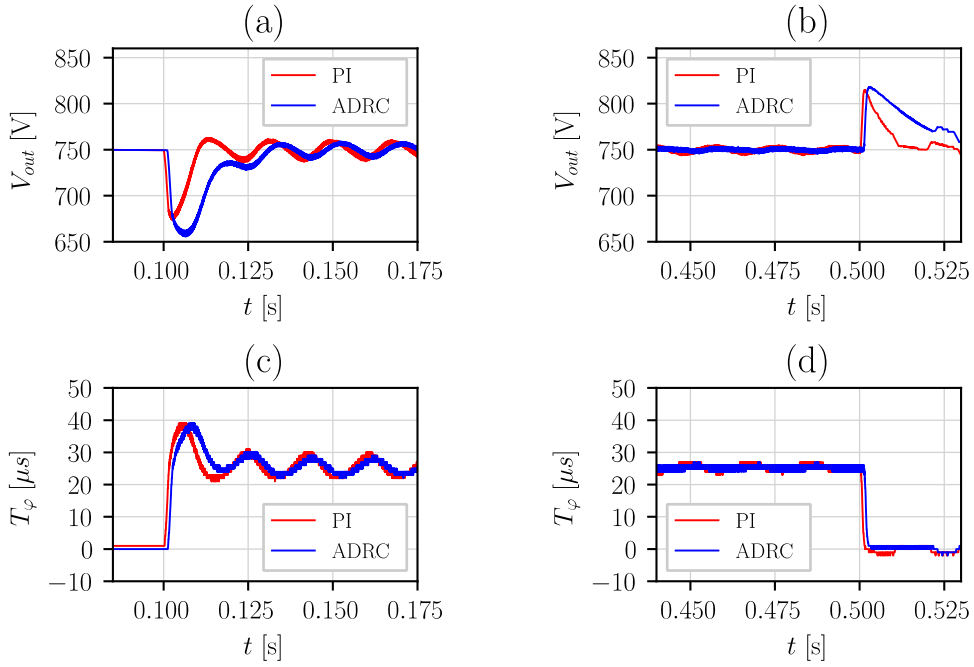

Figure 16. DAB output voltage V_{out} and control variable T_φ at loading (**a**,**c**) and unloading (**b**,**d**). The two tracks are horizontally displaced by 1 ms for previous comparison consistency.

5. Results

5.1. Controller Discretization

The comparative analysis of the two control algorithms (ADRC and PI), used as DAB output voltage regulators, evolves toward the implementation on microcontroller boards to study their behavior in the CHIL real-time simulations. To achieve this result, it is necessary, as an intermediate step, to discretize the regulators considering microcontrollers key peculiarities. A brief theoretical introduction follows for consistency.

The methodology adopted for the discretization of the algorithms analyzed in Section 3 is based on the classical bilinear (or Tustin) transformation [31], whose general formulation, for variable substitution from the s-plane to the z-plane, is given by:

$$s = \frac{2 \cdot (z-1)}{T_s \cdot (z+1)}, \tag{41}$$

where T_s is the sampling period. In literature, it is described the validity of this discretization method as the negative half-plane in s is placed in biunivocal correspondence with the points z of the unit circle. This formulation is derived from appropriate mathematical elaborations carried out from the trapezoidal integration operation [32]:

$$y(n) = y(n-1) + \frac{T_s}{2} \cdot [x(n) + x(n-1)]. \tag{42}$$

Equation (42) defines $y(n)$ as the integral of a generic function $x(n)$ at step n, obtained as the sum of the function calculated at the previous step $y(n-1)$ and the area of the trapezoid subtended by the function $x(n)$. The area of the trapezoid, constructed on the function $x(n)$ between two sequential steps, is obtained by multiplying half the sampling period T_s, (the height of the trapezoid), by the sum of the values of $x(n)$ and $x(n-1)$ (the bases of the trapezoid).

The procedure is described graphically in Figure 17.

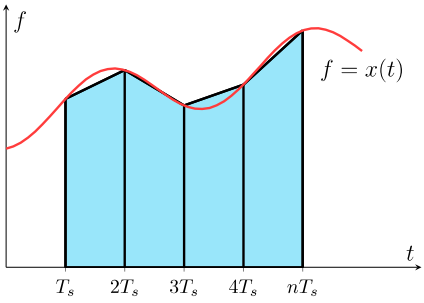

Figure 17. Discrete integration of a generic continuous function f sampled with period T_s using the trapezoid method.

Based on previous theoretical analysis, PI and ADRC algorithms has been implemented both in the following off-line simulations and on the microcontroller firmware for the real-time simulations, employing the formulation of (42) for processing the integral operations expressed as $1/s$ in Laplace formulation. Besides, to account for the specific CHIL real-time requirements described in the next few sections, two different sampling periods (T_s) have been set in off-line simulations:

- 300 µs for DAB controller (to be referenced as microcontroller discretization period $T_{s\mu c}$);
- 20 µs for all other DC/DC and AC/DC converters controllers.

In Sections 5.2 and 5.3, the discretization effect over control strategies (PI and ADRC) will be discussed to validate the model before the actual CHIL real-time implementation. To achieve that, each regulator will be analyzed separately, comparing the results obtained from ATPDraw and MATLAB/Simulink simulations.

5.2. Off-Line DAB Simulations

At this stage, it is useful to verify the performances of each discretized regulator implementation (PI and ADRC) using the same model structure as previously done with ATPDraw only (Section 4.2). This allows for a first validation of the whole model transposition in MATLAB/Simulink as an intermediate step for the desired CHIL real-time realization. The regulator settings employed here are listed in Table 6.

The signals of interest are:

- DAB power profile (Figure 18 for PI and Figure 19 for ADRC);
- DAB output voltage V_{out} and control variable T_φ (Figure 20 for PI and Figure 21 for ADRC);
- DAB input voltage V_{in} (Figure 22 for PI and Figure 23 for ADRC).

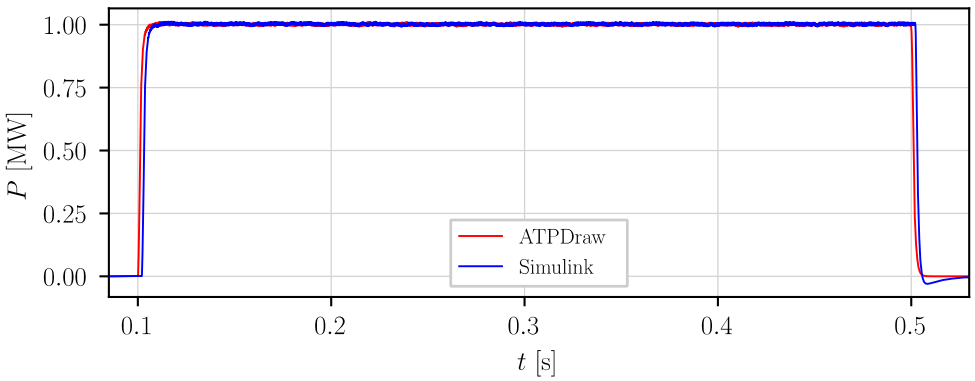

Figure 18. DAB output power with PI regulator. The two tracks are horizontally displaced by 2 ms for graphical reasons.

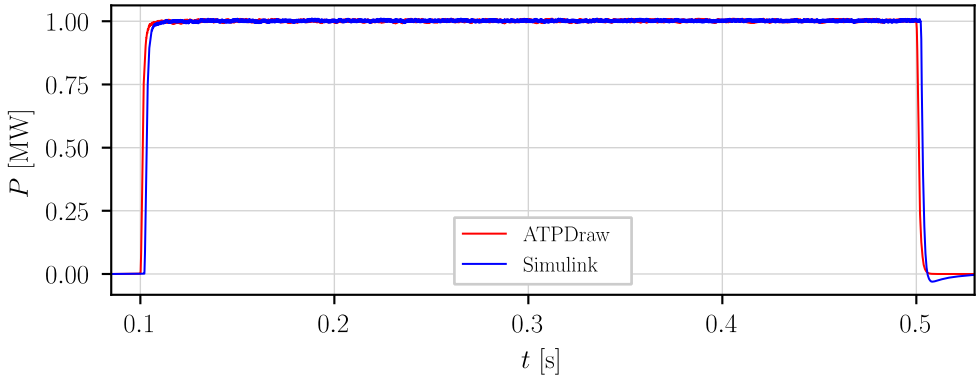

Figure 19. DAB output power with ADRC regulator. The two tracks are horizontally displaced by 2 ms for graphical reasons.

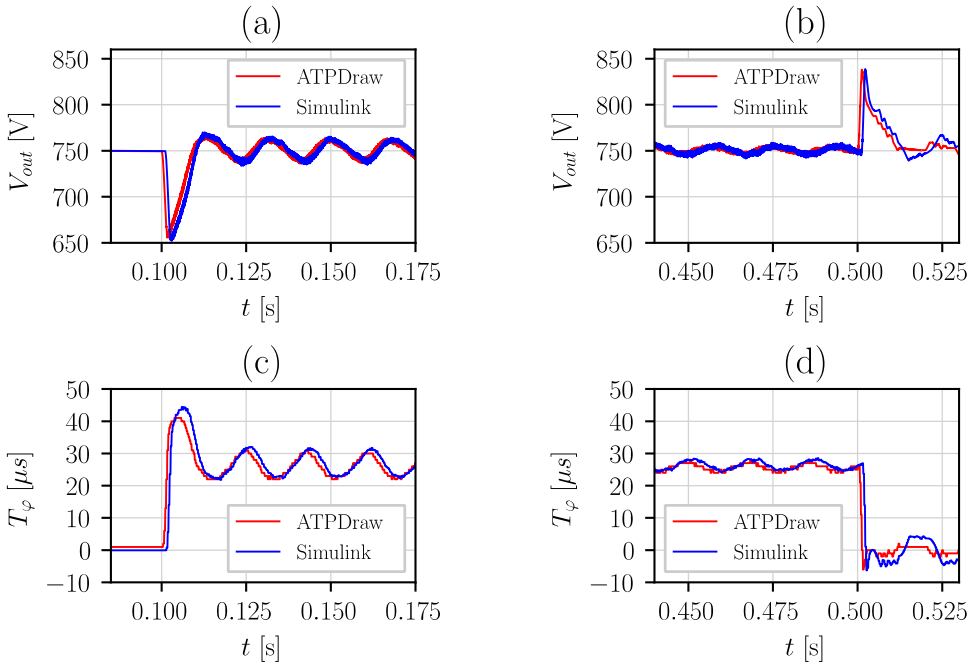

Figure 20. DAB output voltage V_{out} and control variable T_φ at loading (**a**,**c**) and unloading (**b**,**d**) with PI regulator. The two tracks are horizontally displaced by 1 ms for graphical reasons.

From the observation of the simulation results, it is possible to carry out an analogous analysis for both the control strategies (PI and ADRC). The output voltages V_{out} (Figures 20 and 21a,b), the input voltages V_{in} (Figures 22 and 23) and the converter output powers (Figures 18 and 19) respect the profiles observed in Section 4.2.

The discretization also introduced a delay in control loops. Consequently, if compared to the quasi-continuous case, the control variables T_φ (Figures 20 and 21c,d) take more time to compensate the loading and unloading operations. This aspect has a direct impact on the output voltages V_{out} which drop to lower values during transient evolution. The MATLAB/Simulink models show a higher delay on the control variables T_φ, if compared to the equivalent models in ATPDraw, this is due to a different internal design of the switch components between the simulation environment libraries [30,33].

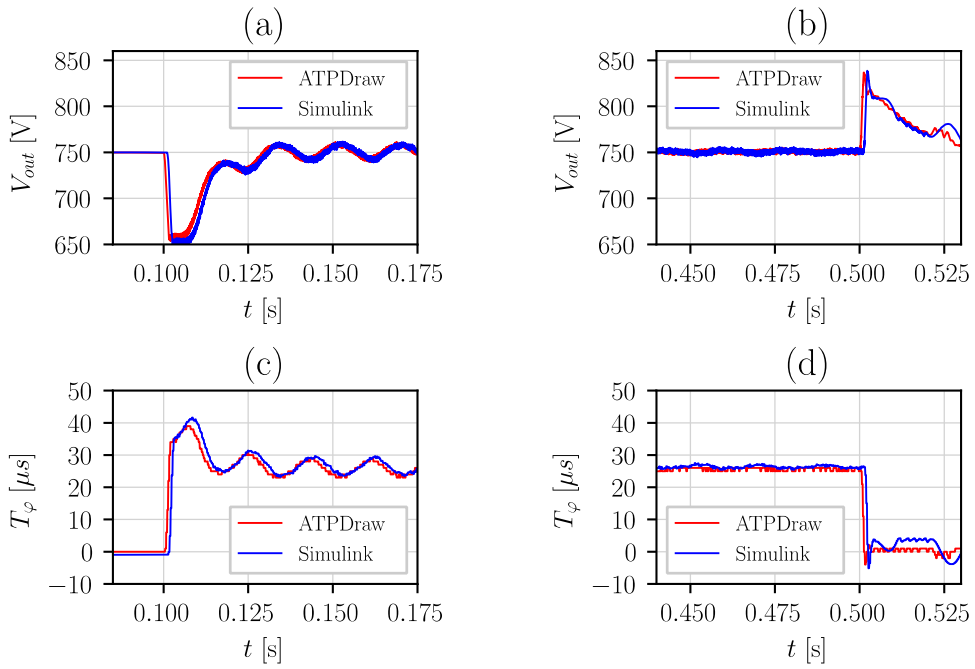

Figure 21. DAB output voltage V_{out} and control variable T_φ at loading (**a**,**c**) and unloading (**b**,**d**) with ADRC regulator. The two tracks are horizontally displaced by 1 ms for graphical reasons.

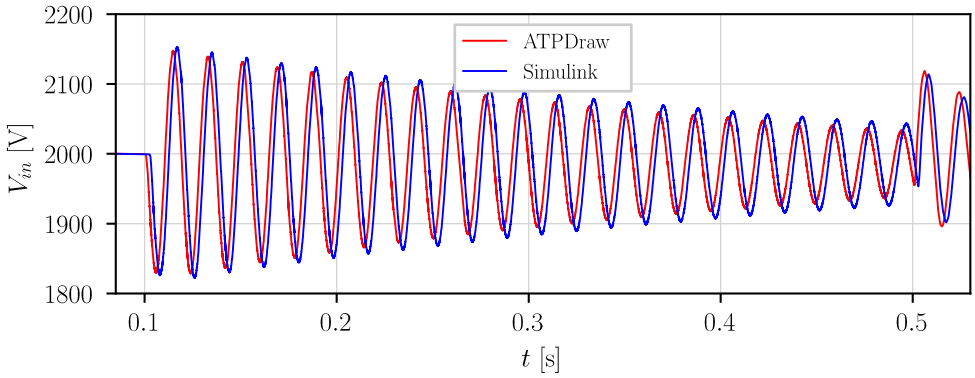

Figure 22. DAB input voltage (V_{in}) with PI regulator. The two tracks are horizontally displaced by 2 ms for graphical reasons.

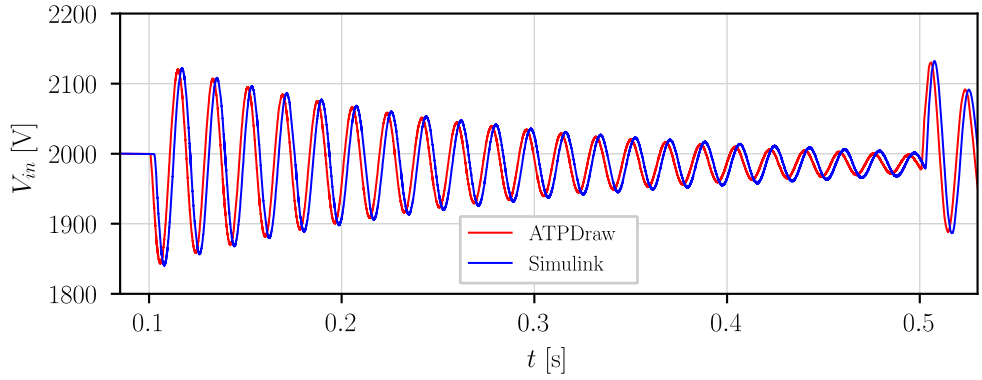

Figure 23. DAB input voltage (V_{in}) with ADRC regulator. The two tracks are horizontally displaced by 2 ms for graphical reasons.

5.3. Off-Line Multi-Terminal MVDC Extension

PI and ADRC regulators study conducted so far focuses on their implementation as a DAB output voltage control system. The results showed peculiarities of each control

strategy with only a specific model topology: DAB converter transfers power from a single-terminal MVDC network to a constant power load (on the LVDC side). At this point, the analysis can be extended, verifying the performances of the converter connected in a more complex MVDC network.

Figure 24 shows the structure of the three-terminal MVDC grid adopted both in the off-line and CHIL real-time simulations. The network has a nominal (pole-to-pole) voltage of 2 kV and interconnects three model equivalent MVDC/MVAC converters, each of them sized for a nominal power of 5 MW.

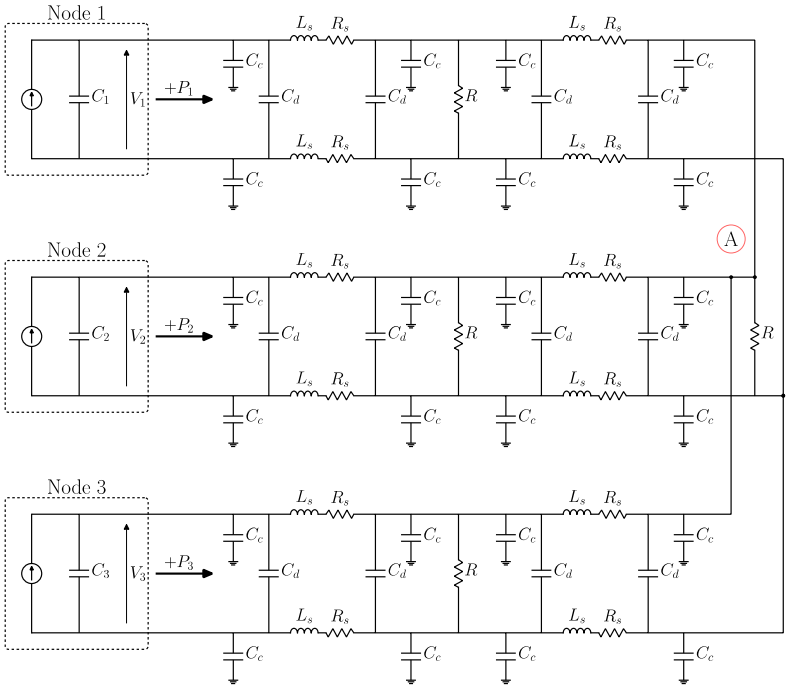

Figure 24. Three-terminal MVDC network model topology.

The three nodes are interconnected at the network central point through three lines of equal length. Each line is divided in two equivalent sections (1 km) defined by the π-model. Medium-voltage loads, represented by resistors (R), are connected at the end of each section. The value of R (4 Ω) is calculated to absorb 1 MW at the nominal grid voltage; unless there are local voltage variations, the total distributed load is about 4 MW. The parameters of the modeled components are listed in Table 7.

Table 7. Three-terminal network parameters.

Parameter	Value
Equivalent MVAC/MVDC converters	
Nominal DC voltage	2 kV
Nominal power	5 MW
Capacitance ($C_{1,2,3}$)	100 mF
MVDC Network	
Total line length	2 km
Single section length	1 km
Series resistance (Rs)	0.0094 Ω
Series inductance (Ls)	0.22 mH
Pole to ground capacitance (C_c)	1.38 µF
Pole to pole capacitance (C_d)	0.69 µF

The analysis is strictly aimed at the interaction between the MVDC network and DAB converter, without investigating the dynamics of a complete inverter model. For this reason,

three equivalent MVAC/MVDC converter models have been employed, consisting of a controlled current generator in parallel to a capacitance ($C_{1,2,3}$). Each node performs a different grid function, in particular:

- Nodes 1 and 3 carry out the P-V droop control, through the active power exchange regulation with the MVDC network. Current model power control system set-point values are $P_1{}^* = 5$ MW and $P_3{}^* = 1$ MW, which means that both converters inject active power into the MVDC network;
- Node 2 regulates the output voltage (V_2) at the nominal value (2 kV).

The control structure of Node 1 is shown in Figure 25: the current reference $I_d{}^*$ of the controlled current generator is calculated by a PI controller acting on the measured DC voltage error. Depending on the node type, the voltage reference $V_{cc}{}^*$ can be:

- constant value (2 kV) (control loop for Node 2);
- the PI output value of the external control loop for the power regulation (control loop for Node 1 and Node 3).

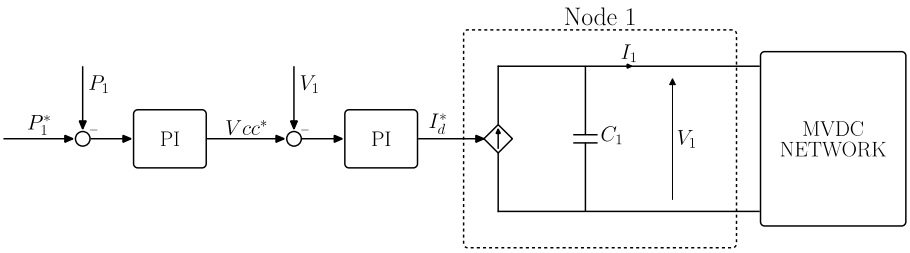

Figure 25. Example of piloted current generator control loop for Node 1.

For the following simulation test setup, a DAB converter has been connected to the central point of the MVDC network (identified with A in Figure 24). The events are organized as follows:

- $t < 1$ s: the DAB regulates, at no load, the voltage (750 V), no power transfer from MVDC to LVDC side. In the MVDC network, Nodes 1 and 3 inject respectively 5 MW and 1 MW meanwhile Node 2 regulates the nominal voltage (2 kV);
- $t = 1$ s: constant power load is connected to DAB LVDC side. DAB must keep LVDC voltage stable;
- $t = 2$ s: load is disconnected; DAB must handle the load rejection keeping LVDC voltage regulated.

Key results of the comparison between ATPDraw and MATLAB/Simulink models for each regulator are in the following pictures, the signals of interest are:

- DAB output voltage V_{out} and control variable T_φ (Figure 26 for PI and Figure 27 for ADRC);
- DAB input voltage V_{in} (Figure 28 for PI and Figure 29 for ADRC).

The analysis of the DAB converter connected to central point of the new network structure has confirmed the control responses observed with a single-terminal model. Although both the controllers operate with input voltage values V_{in} (Figure 28 for PI and Figure 29 for ADRC a and b) higher than the nominal one (2 kV), they are able to regulate the output voltages V_{out} (Figure 26 for PI and Figure 27 for ADRC, a and b) respecting the profile designed in the previous sections. Besides, with the MATLAB/Simulink models, the control variables T_φ (Figure 26 for PI Figure 27 for ADRC, c and d) show a slightly delayed response compared to the ATPDraw cases, just like the previous network structure (single terminal).

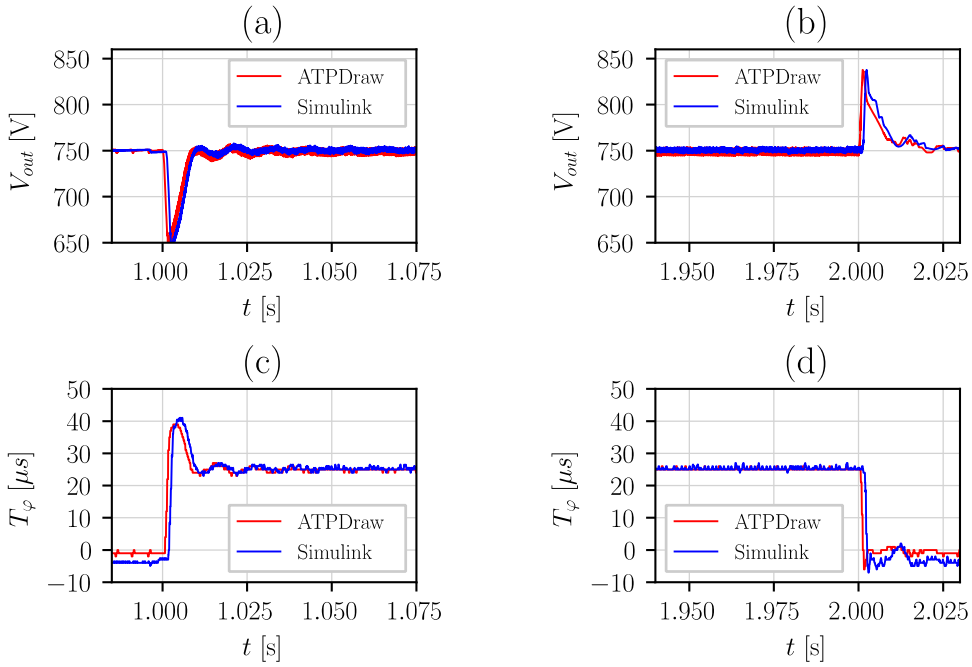

Figure 26. DAB output voltage V_{out} and control variable T_φ at loading (**a**,**c**) and unloading (**b**,**d**) with PI regulator. Tracks are horizontally displaced by a total of 2 ms for graphical reasons.

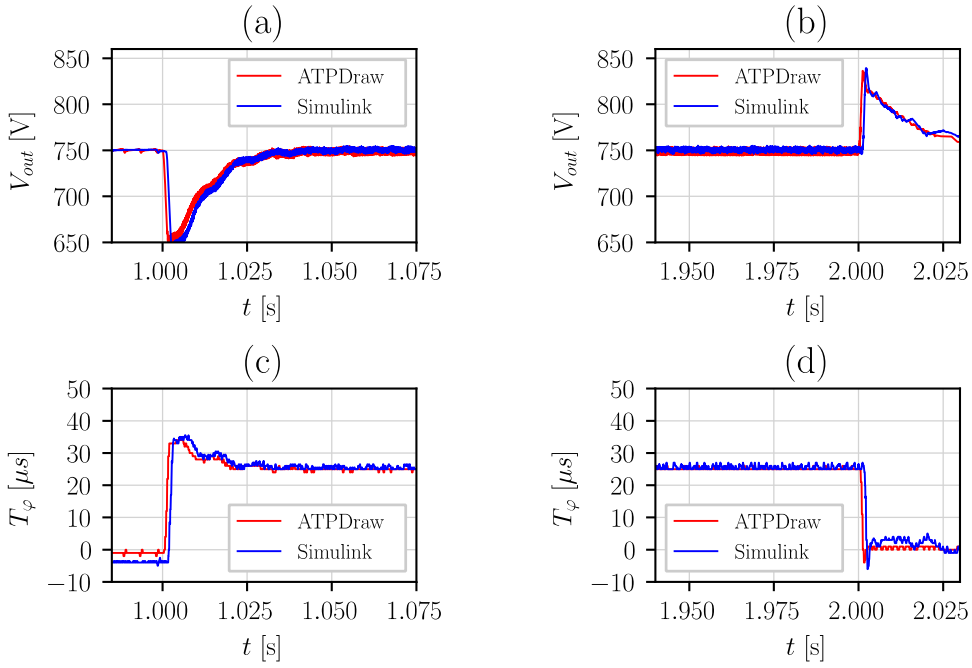

Figure 27. DAB output voltage V_{out} and control variable T_φ at loading (**a**,**c**) and unloading (**b**,**d**) with ADRC regulator. Tracks are horizontally displaced by a total of 2 ms for graphical reasons.

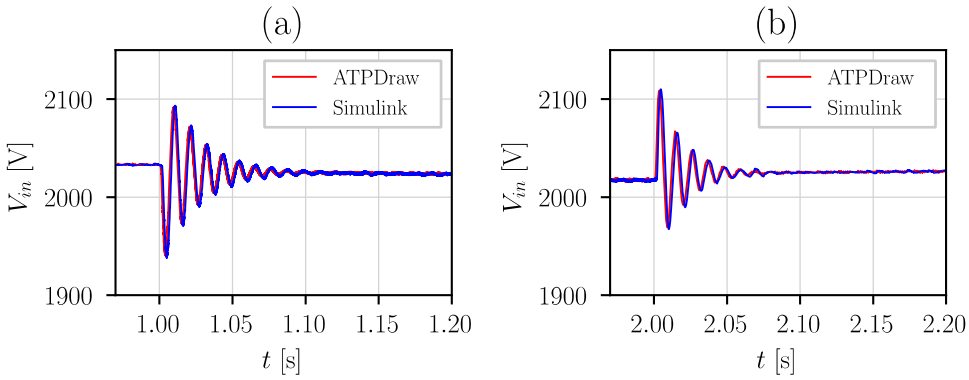

Figure 28. DAB input voltage (V_{in}) at loading (**a**) and unloading (**b**) with PI regulator. Tracks are horizontally displaced by a total of 2 ms for graphical reasons.

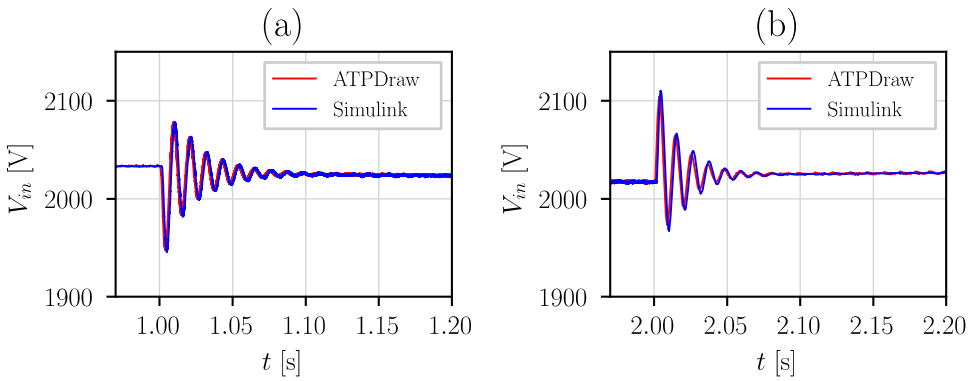

Figure 29. DAB input voltage (V_{in}) at loading (**a**) and unloading (**b**) with ADRC regulator. Tracks are horizontally displaced by a total of 2 ms for graphical reasons.

5.4. CHIL and Real-Time Aspects

To successfully implement a CHIL simulation it is of paramount importance to make sure that any of the hard real-time constraints are not systematically violated by any component. For the structure presented here it is necessary to carefully evaluate the capability of the general-purpose microcontroller board to timely execute both regulator implementations. In a real-time system it is easy to understand how this time, called control cycle (or period) T_c, cannot be greater than the discretization period $T_{s\mu c}$ of the regulator algorithm. Otherwise, the control system would go into over-runs, or would not be able to "keep up" with the inputs and outputs speed of the system to be controlled). Therefore, $T_{s\mu c}$ selection (as mentioned in Section 5.1) requires careful estimation of the whole regulator algorithm execution cycle by timings multiple runs.

Two of the major challenges to obtain a stable and quasi-deterministic T_c are to manage the periodical control variable update and to synchronize regulator code execution. Both those two results are achieved by exploiting the hardware resources of the ST NUCLEO-F767ZI board, in particular, high-precision hardware timers rising interrupts, as visualized in Figure 30.

It is important to note that a residual (idle) time is then introduced to realize an outputs update at the end of $T_{s\mu c}$. This is useful to achieve a discretized system coherent with the work of Section 5.1. The control signals generation via microcontroller ISR (Interrupt Service Routine) capabilities minimizes jitter and latency, typical of software-based generation. This powerful implementation relies on microcontroller hardware capabilities (natively managing four PWM channels necessary to control the DAB in SPS mode), yet the code is kept simple thanks to the high-level abstraction layer provided by MicroPython programming language.

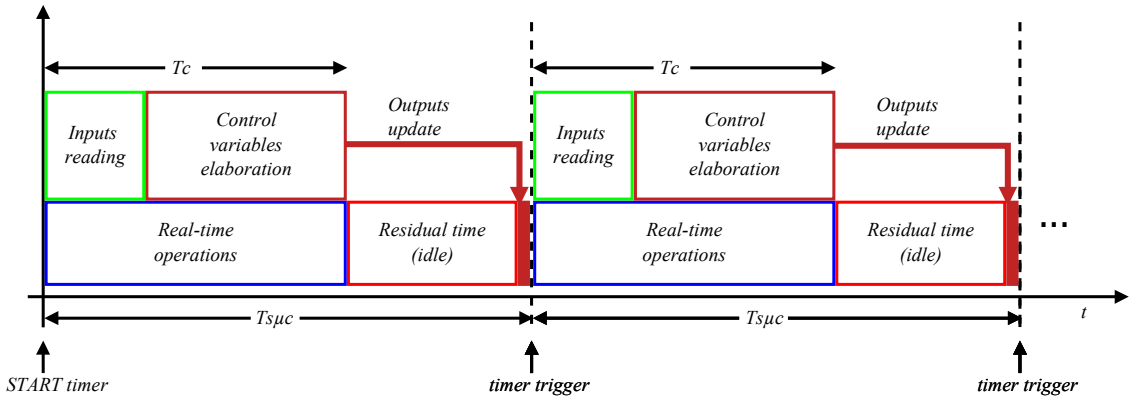

Figure 30. Time diagram of the control cycle execution.

In a CHIL simulation, the physical controller is interfaced to a simulated model via different I/O channels. The simulated model itself is divided between a CPU and FPGA module, working according to the high-level scheme of Figure 31.

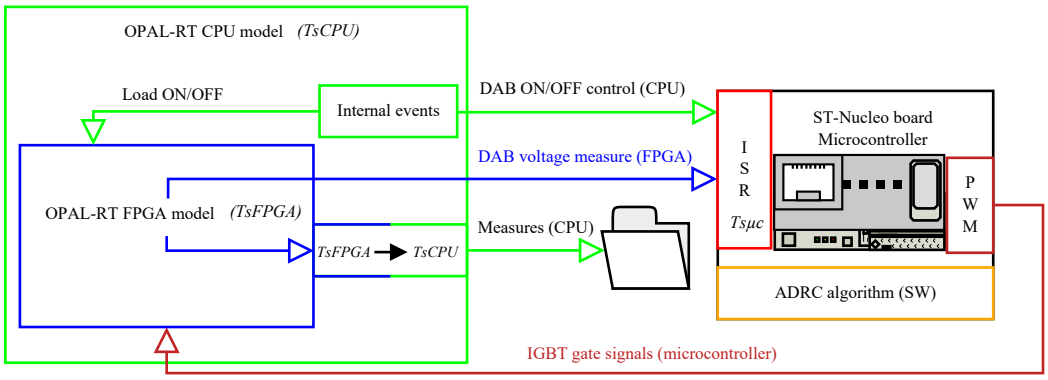

Figure 31. CHIL simulation structure, composed by systems having different discretization periods: OPAL-RT CPU module (green), OPAL-RT FPGA module (blue) and ST-Nucleo microcontroller (orange). Code execution is scheduled by an ISR system (red), PWM signals generation (brown) is managed by microcontroller hardware resources.

Simulation results can then be stored in two ways: either by logging quantities through CPU resources (depicted in Figure 31), or by sampling FPGA outputs. In this work, the only measure obtained through the second strategy is T_{φ} control variable, not readily available at the microcontroller output.

Factoring in model complexity (as presented in Section 5.3) and available real-time simulator capability, it is possible to have a complete overview of the various modules' execution times. Also adding the results of $T_{s\mu c}$ timing tests, across both PI and ADRC implementations, the different time steps can be summarized as:

$$\begin{aligned} T_{sCPU} &= 20\,\mu s \\ T_{sFPGA} &= 1\,\mu s \\ T_{s\mu c} &= 300\,\mu s \end{aligned} \tag{43}$$

By this selection it is then possible to represent in FPGA all critical electrical components, relegating in CPU the ones responsible for "slower" dynamics or complex controls. By simulating the ones giving rise to "fast" dynamics with the same time-step as off-line simulation (1 μs), a significant comparison between off-line and real-time simulations is possible.

The last major phenomenon that must be considered when performing a comparison between off-line and real-time simulations is, at the very least, measurements quantization

introduced by microcontroller ADCs (Analog-to-Digital Converters). In CHIL setup of Figure 31, the microcontroller samples the DAB output voltage V_{out} directly from FPGA module. This measure realizes the feedback loop of both PI and ADRC implementations, it is then evident how the regulator response can be impacted (with heavy differences only in case of badly implemented setups). Since it is easy to give a simplified representation of this phenomenon in ATPDraw and MATLAB/Simulink environments, it was chosen to include it in both, for the benefit of a more significant comparison. The simplest model for uniform quantization introduced by the ADC is:

$$d = \frac{\Delta V_{MAX}}{2^N - 1} \cdot round\left(\frac{2^N - 1}{\Delta V_{MAX}} y\right), \tag{44}$$

with d being the quantized signal, y the input signal from the sampling stage, N the bit resolution of selected hardware, ΔV_{MAX} the measurable range.

In theory, the same phenomenon occurs also for the input/output modules of the real-time simulator. It has anyway not been considered since the simulator employs more sophisticated hardware with higher resolution [34] than the chosen microcontroller (that can rely on 12-bit ADCs [35], so its contribution is negligible.

5.5. CHIL Multi-Terminal MVDC/LVDC DAB Simulations

In this last section, the final comparison between reference off-line and real-time CHIL simulations is presented. The base structure of Section 5.3 is implemented across all three simulation environments (ATPDraw, MATLAB/Simulink and OPAL-RT). A CHIL simulation of a multi-terminal multi-level DC distribution network is then successfully validated against known reference implementations, as presented in the following. The regulator settings employed here are listed in Table 6. The most significant comparisons involve:

- DAB input voltage V_{in} (Figure 32 for PI and Figure 33 for ADRC);
- DAB output voltage V_{out} and control variable T_φ (Figure 34 for PI and Figure 35 for ADRC).

Although an analysis of the results is to be deferred to the next section, it is important to mention that all tracks are horizontally displaced for graphical reasons. MATLAB/Simulink results have 1 ms positive offset, while OPAL-RT ones have a negative offset of the same entity with respect to the red ATPDraw line.

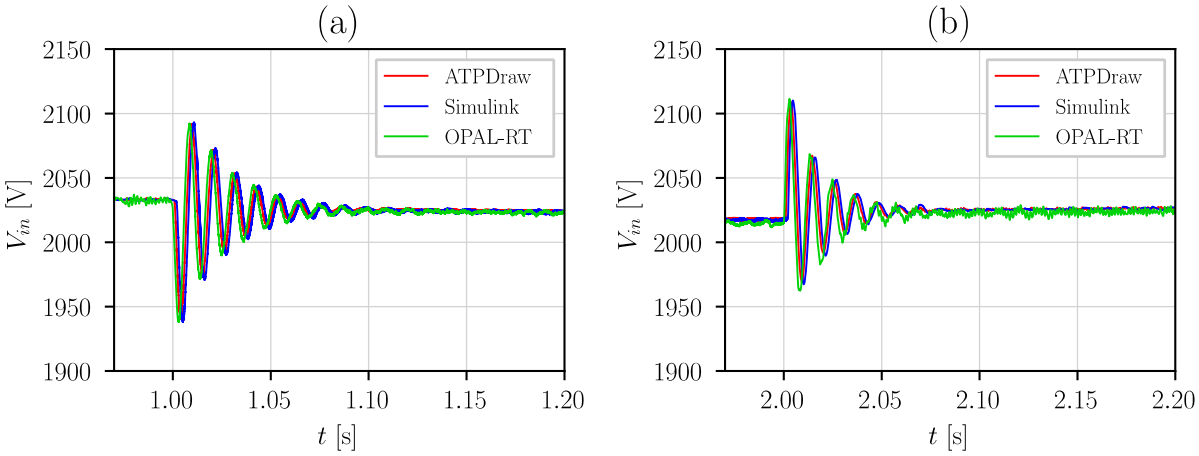

Figure 32. DAB input voltage (V_{in}) at loading (**a**) and unloading (**b**) with PI regulator. For graphical reasons, Simulink and OPAL-RT tracks are horizontally displaced respectively by ±1 ms in relation to ATPDraw.

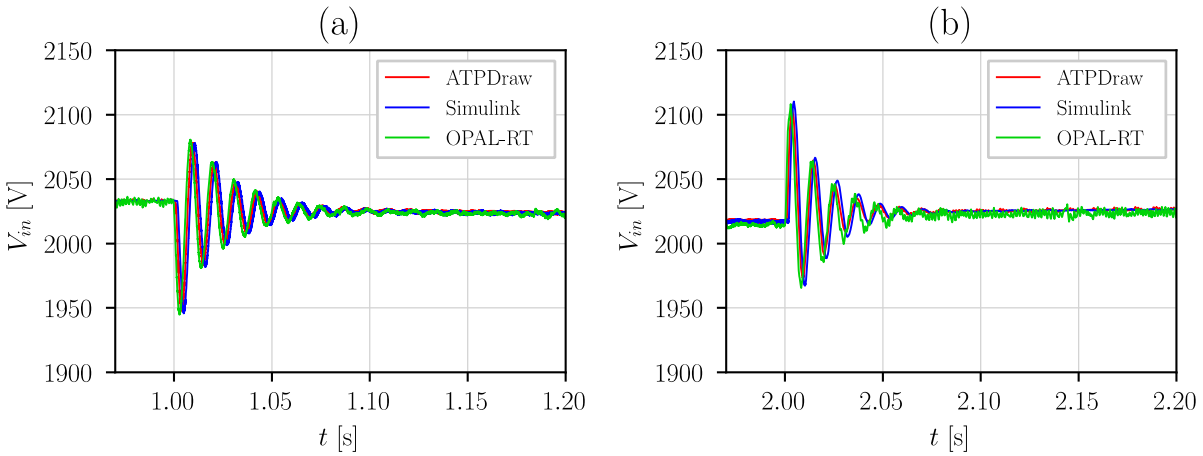

Figure 33. DAB input voltage (V_{in}) at loading (**a**) and unloading (**b**) with ADRC regulator. For graphical reasons, Simulink and OPAL-RT tracks are horizontally displaced respectively by ±1 ms in relation to ATPDraw.

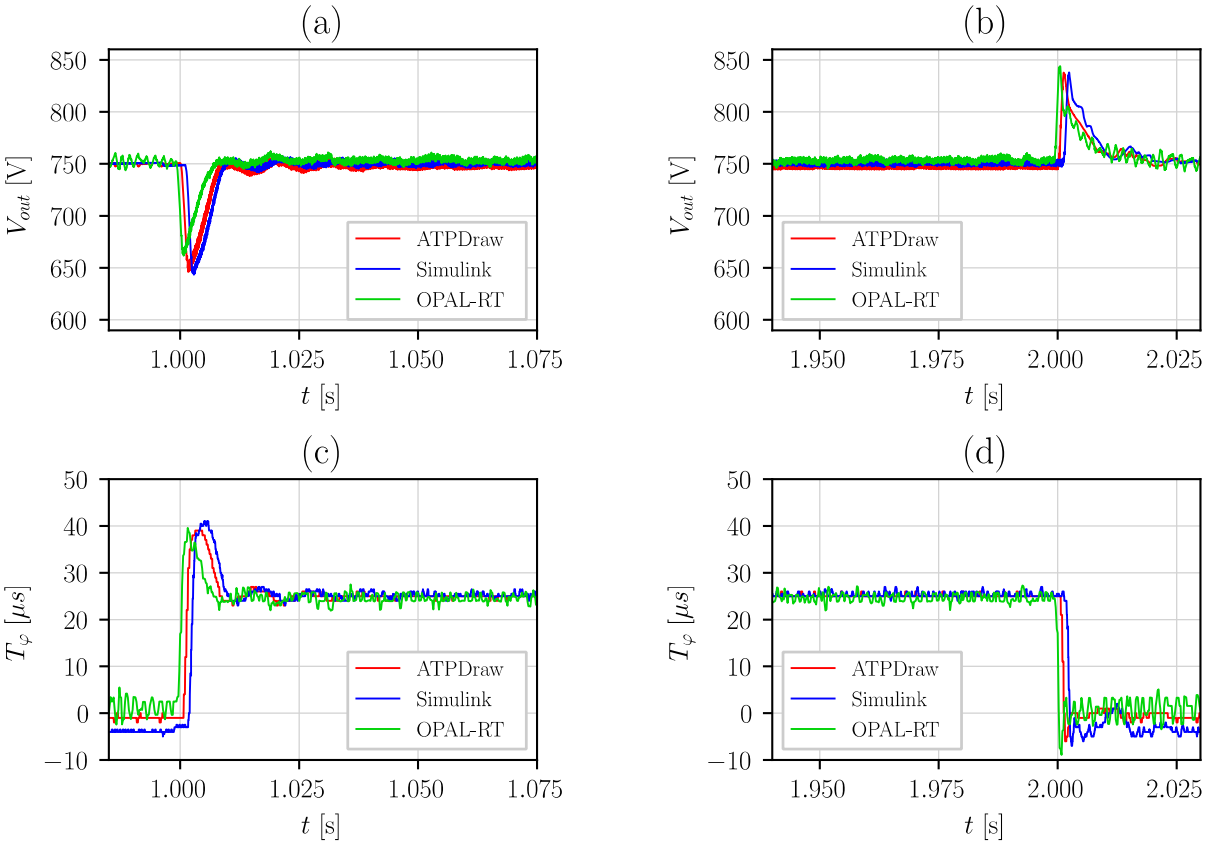

Figure 34. DAB output voltage V_{out} and control variable T_φ at loading (**a**,**c**) and unloading (**b**,**d**) with PI regulator. For graphical reasons, Simulink and OPAL-RT tracks are horizontally displaced respectively by ±1 ms in relation to ATPDraw.

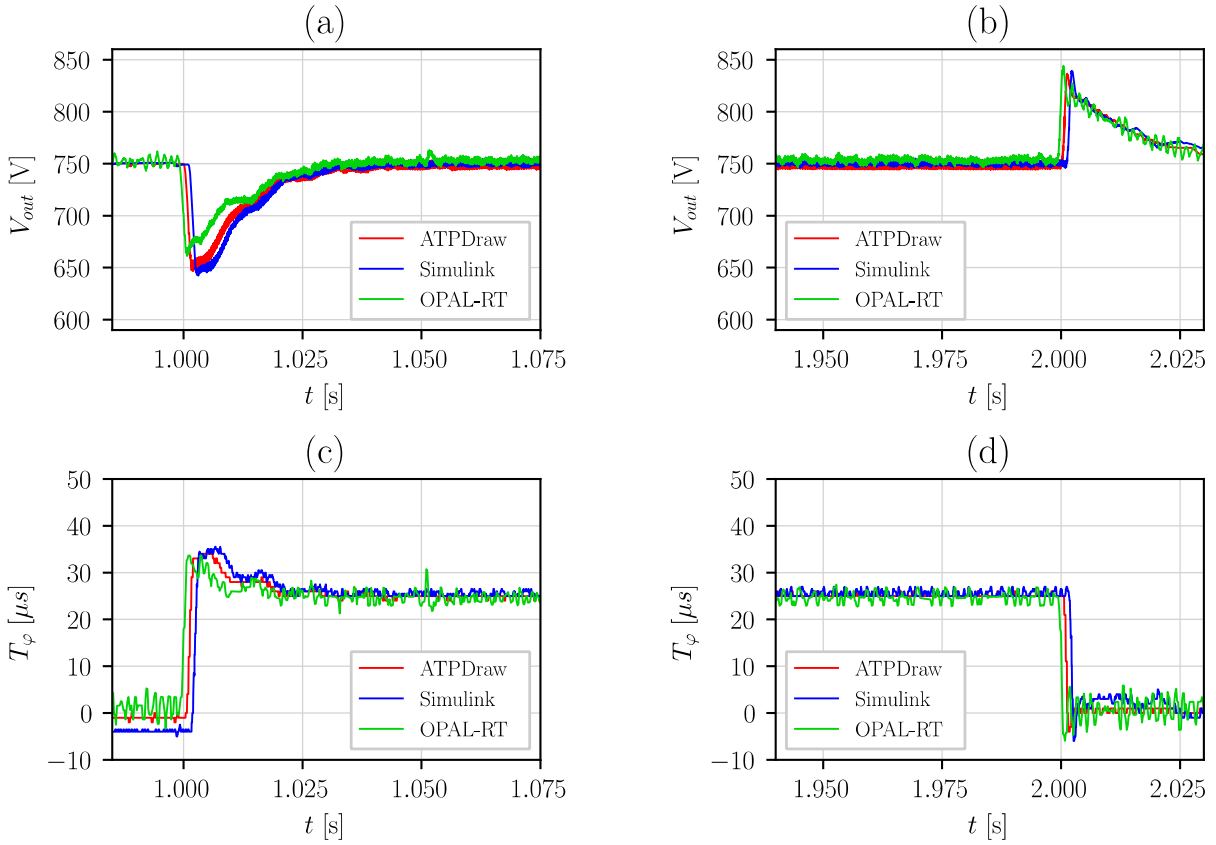

Figure 35. DAB output voltage V_{out} and control variable T_φ at loading (**a**,**c**) and unloading (**b**,**d**) with ADRC regulator. For graphical reasons, Simulink and OPAL-RT tracks are horizontally displaced respectively by ±1 ms in relation to ATPDraw.

6. Results Discussion

In this section, the key CHIL real-time results presented above are discussed. In all three simulating environments, DAB input voltage (V_{in}) is very precisely described (Figures 32 and 33). This is mainly a direct consequence of the multi-terminal MVDC network model selection of Section 5.3, that allows for an easy implementation in each simulation. By comparing the results of Figure 32 (obtained with PI regulator) with Figure 33 (the ones with ADRC), it is possible to retrieve the same characteristics in reduction of network resonance excitation as described in Section 4.3. Further comparison with Figure 16 made evident that the advantages in V_{in} profiles are balanced by a slower response in V_{out}. This represents a first proof that the theoretical considerations behind this new ADRC setting (presented in Table 6) still holds true when transitioning to a physical implementation.

The V_{out} regulated voltage and T_φ control variable (Figures 34 and 35) show the anticipated step variation at t = 1 s and t = 2 s, after which all regulators' implementations follow mainly the same transients. In CHIL results there is, however, a high-frequency component superimposed to T_φ profile at no load. Its effect is also tangible in V_{out} profile. Anyway, no significant impact can be seen in the general voltage regulation performance, the value being on average very close to reference off-line simulations. The existence of this high-frequency component can be explained by:

- control variable higher instability in CHIL simulations, due to the way T_φ is acquired. Since microcontroller computed value cannot be logged, T_φ is re-constructed sampling the gate signals with an external oscilloscope. No-load values are then subjected to higher errors and cannot show the ideal envelope outputted by off-line simulations;

- DAB constructive characteristic is such that at no-load small variations in control variable produce a very amplified effect over controlled variable. Although this characteristic is common to all simulations (offline and CHIL), in real-time this effect is further amplified by the non-ideality of the generated gate pulses.

The final comparisons of Section 5.5 show a good correspondence between off-line and real-time results for both regulators implementations. System response following each transient is correctly represented, with only minor discrepancies due to inevitable differences in solver setup and component modeling (e.g., Figures 34a and 35a). This does not impair the generality of the validation, confirming the absence of significant deviations across control algorithms implementations.

It is also important to further comment on the two controllers' differences, as shown along the paper. At first an ADRC equivalent to the reference PI has been introduced. In this case, the overall response (both in output voltage (V_{out}) and input V_{in} profiles) is identical—also factoring in the intentional shift of the two tracks applied for graphical reasons only. Once the re-tuning of ADRC of Section 4.3 is introduced, the overall response in output voltage (V_{out}) transient is slower as predicted by the theory behind the ADRC re-tuning, but it is more than compensated by a better V_{in} profile.

As a last consideration, it is important to focus on CHIL results over different simulation environments, since they represent the outcome of a long and careful implementation study, where each model and representation extension has been individually validated. It is then interesting to demonstrate that the system is a suitable platform for CHIL studies of a multi-terminal multi-level DC distribution network.

7. Conclusions

This work presented an implementation strategy for a CHIL real-time simulation of a DAB DC-DC converter control in a multi-terminal multi-level DC distribution network. The research has elements of novelty because it aims to unify in an organic way many different parts, both theoretical and experimental: DAB controller description, tuning, discretization, and physical implementation; in addition, a real time model of a whole electrical network has been implemented, and also CPL handling has been assessed.

All those aspects contributed to final CHIL results, and they were crucial to stress algorithms' response in a more realistic and challenging operative scenario.

Two different control strategies have been presented: a classical PI (Proportional Integral) and an ADRC (Active Disturbance Rejection Control) regulator. Beyond showing a possible theoretical ADRC setting equivalent to a given PI, a different tuning method has been proposed to exploit ADRC's more flexible structure, without abandoning bandwidth parametrization and relevant simplified frequency domain analysis.

All those considerations have been then transferred into reference off-line simulations to validate models and structures for CHIL real-time implementation. It has been than confirmed that the ADRC control, even if discretized and implemented on a digital microcontroller, can be considered a valid alternative to PI control for a power system connected to an MVDC network.

All comparisons and all simulations were positive: the proposed controls are sufficiently robust to preserve characteristics predicted by off-line simulations also in physical implementation; more in detail, besides minor differences between off-line simulations and real-time CHIL test, it was possible to:

- verify the correct discretization of the off-line simulations to make a direct and consistent comparison with the CHIL test;
- confirm with CHIL simulation the proper implementation of discrete PI and ADRC algorithm into the microcontroller board.

In conclusion, the discretization process did not introduce substantial changes to the algorithm studied in the ideal scheme of continuous time control.

Future work will continue the development of CHIL real-time simulations with multi-terminal MVDC distribution networks, to test control algorithms also in fault-grid condi-

tions; due to this, solid state breakers and current-limiting devices will be introduced on the network.

In such a scenario, overvoltage phenomenon along the line due to massive current interruptions and recovery will also be considered.

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Abbreviations

The following abbreviations are used in this manuscript:

AC	Alternating Current
ADRC	Active Disturbance Rejection Control
CHIL	Control Hardware In the Loop
CPL	Constant Power Loads
CPU	Central Processing Unit
DAB	Dual Active Bridge
DC	Direct Current
ESO	Extended State Observer
FPGA	Field Programmable Gate Array
IGBT	Insulated Gate Bipolar Transistor
ISR	Interrupt Service Routine
LVDC	Low Voltage Direct Current
ML/SL	Matlab/Simulink
MVAC	Medium Voltage Alternating Current
MVDC	Medium Voltage Direct Current
PI	Proportional Integral (Control)
PWM	Pulse-Width Modulation
HW	Hardware
SISO	Single Input Single Output
SW	Software
RSE	*Ricerca sul Sistema Energetico* (Research on Energetic System)
RT	Real-Time

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