

## Article

# A Single-Phase Compact-Sized Matrix Converter with Symmetrical Bipolar Buck and Boost Output Voltage Control

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**Abstract:** The development of single-phase symmetrical bipolar voltage gain matrix converters (MC) is growing rapidly as they find their application in power systems for dynamic restoration of line voltages, high voltage AC–DC converters, and variable frequency controllers for many industrial processes. However, the existing trend in matrix converter technology is a buck–boost operation that has inherently serious issues of high voltage and current surges or stresses. This is a big source of the high voltage and current rating of semiconductor switching devices. There is also a problem of high ripples both for voltage as well for current, requiring large size of filtering capacitors and inductors. The non-symmetrical control of the voltage gain increases the control complication. A large count of operating transistors is critical regarding their cost, size, and power conversion losses, as the space and cost required by their gate control circuits are much larger than the size and cost of the switching transistors. Thus, in this research work, a new single-phase MC is introduced only employing six fully controlled switching devices, ensuring similar operation or outputs as is obtained from the existing topologies that require the use of eight or more fully controlled switching devices, and the reduction by two or more switching transistors helps to compact the overall size and lower the overall cost. The separation in its voltage buck and boost operation enables smooth control of the voltage gain through duty cycle control. The low values of the voltage and current surges reduce the power rating and losses of the switching devices. The flow of the current in the filtering inductor is kept unidirectional to avoid the current interruption and reversal problem once the operation of the converter is abruptly switched from inverting to non-inverting and vice versa. All these factors are comprehensively detailed through the circuit’s description and comparative analysis. Simulation and practical results are presented to confirm the effectiveness of the developed circuit topology.

**Keywords:** matrix converter; frequency controller; buck and boost operation; voltage and current surges; bipolar voltage gain; fully controlled devices; non-inverted and inverted operation



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## 1. Introduction

### 1.1. Motivation

Single-phase bipolar voltage gain matrix converters find their application in various fields, such as variable speed drive systems, power systems, voltage step-up AC-to-DC converters, traction systems, and converters associated with wind turbines. The voltage variation in a power system is very critical for sensitive loads and sensitive control systems. The main source of this voltage deviation is the system’s faults, especially single line to ground. During this event, the voltage of the faulty line is decreased, and for non-faulty lines, voltage is boosted. To balance the system’s voltage, it is mandatory to add and subtract the voltage from the line voltage. This can only be possible if matrix converters

connected with the lines have abilities to produce the non-inverted and inverted regulated outputs. In the same way, single-phase matrix converters are also attractive in applications where speed variation is required in some selected discrete steps. Such applications include traction systems, grinding mills, and steel rolling mills. By viewing the preceding discussion, it is concluded that the design and development of single-phase matrix converters is an attractive research area nowadays. These features lead us to develop a compact-sized bipolar voltage matrix converter.

## 1.2. Literature Review

AC–AC converters are used in various fields, from domestic to industrial applications. Their basic role is to govern the output rms voltage and frequency per the load requirement or application [1]. These applications may include the correction of grid voltage through the dynamic voltage restorer, variable speed control system, solid-state transformer, and wind power system connected to the grid [2]. The voltage variation or fluctuation is critical for the operation of the critical load as they are very sensitive to this variation. This issue is very common in modern power systems due to the use of renewable energy resources or the presence of faults in the power system. For example, a single phase to ground fault is one of the most frequently occurring events in the power distribution system, and its rate is more than 50% compared to the other power system problems [3,4]. This problem disturbs the voltage level or profile of the three phases of the power system. The line rms voltage of the faulty phase is decreased beyond a certain level, and this phenomenon in power engineering terminology is known as voltage sag [5–8]. This created problem may be corrected by adding or injecting the voltage with the line. This only is successful if the phase angle of the injected voltage is the same as that of the line voltage. There is an increase in the voltage of the non-faulty line, called a voltage swell. The correction of this problem requires lowering the line voltage and this can only be possible by subtracting the injected voltage from the line. This characteristic of the injected voltage is made possible if the phase angle difference between the line and injected voltage is 180 degrees or both are out of phase [9,10]. The characteristics of such injected voltage can only be ensured if power-converting converters can transform the input voltage into its inverted and non-inverted versions with controllable magnitude [11–13].

There are two broad classes of AC–AC converters called indirect and direct converters. The first category may have a multistage structure involving the use of a DC link capacitor as a fundamental requirement. The basic role of the front or first-stage converter is to rectify AC voltage into DC voltage, and its structure can be in the current source bidirectional form. At the second or final stage, the conversion of DC voltage to AC is obtained by using a voltage source inverter. This converter can transform constant DC voltage into a variable voltage and frequency AC output. The regulation of the output AC voltage is gained with the control of the gain of the inverter. The control of the time period of the output governs the variation in the output frequency. Mostly, the application area of this sort of converter is frequency control for various industrial processes. But due to the use of a bulky DC-link capacitor and implementation in the multistage power conversion process, the efficiency and reliability of the system are severely affected [14,15]. The complementary switching behavior of the switching transistor connected to the inverter legs may lead to the shoot-through problem. This issue can be addressed by introducing the dead-time in the control inputs that govern the on–off states of complementary operated transistors. This may lead to a reduction in the maximum obtainable voltage gain and it increases the control complication. The operation of an indirect AC–DC–AC converter based on the use of a z-source structure is employed in [16] to address the previously stated problems. The use of a z-source network in the converter not only addresses the shoot-through issue but also helps in the adjustment of the required voltage gain. The existing topologies of the indirect AC–AC converters are reported in [17–21]. The stability analysis and several modulation schemes for a DC-link capacitor are stated in [17,18]. The power quality-related issues in AC–DC–AC converters are reported in the multilevel converter approach in [19–21]. The

DC-link capacitors employed in indirect AC–AC converters are electrolytic capacitors that are sizeable and have short operation life. Therefore, they are the big source of the low reliability in indirect AC–AC converters.

The implementation of direct AC–AC converters eliminates the use of DC-link capacitors as they can control output voltage and frequency without any intermediate power conversion process. These converters can regulate the output voltage to any required voltage level with the PWM control in its non-inverted and inverted form. But their frequency control is limited to some discrete value as outputs' waveforms for this requirement are obtained by arranging the non-inverted and inverted forms of the input voltage. These features of the output can be obtained by taking the advantage of z-source structure [22–24], but these topologies face the problem of high current surges and slow dynamic response as high-order passive components are connected in the z-source network. The other class of direct converters is developed from the modified form of the direct DC–DC converters that have voltage buck, boost, and buck–boost characteristics. The unidirectional flow of the current may be converted to bidirectional flow by replacing the unidirectional current conduction switching devices with devices that have bidirectional current flow capabilities [25–28]. This approach is simple in terms of circuit configuration and gate control mechanism. In these approaches, the required magnitude of the output voltage is adjustable with the help of PWM control. There is also a possibility to arrange the output voltage in-phase or out-of-phase with respect to the input voltage. This helps to arrange the number of positive or negative half cycles or pulses at the output as per the required value of the load frequency. There may be some power quality-related concerns both for output voltage and current as they are investigated through an analytical approach in detail as reported in [29,30]. Power factor and total harmonic distortion are the key parameters used to evaluate the input current. These factors approach their ideal value by improving the sinusoidal characteristics in the input current by lowering the effects of the generated harmonics. The sinusoidal behavior of the input current is enhanced by ensuring the continuity of the input current in some research articles, as reported in [31–33]. In these converters, the improvement in the power quality of the input currents affects the sinusoidal characteristics of the output voltage. In addition, there is no ability to regulate the output voltage, which is a mandatory requirement for industrial drive systems to avoid the core saturation of the AC motors. These problems are addressed in [34–36], but there is limited output voltage regulation for some output frequencies only. The solution proposed in these converters disturbs the power quality of the input current. The present dominant harmonics exist at low frequency and their suppression is not easily achievable as the size of the filtering components always depends on the switching frequencies. In [37], a direct AC-to-AC converter is connected at the input of the wireless power transfer system converting low line frequency to high output frequency. In switching converters, the generated harmonics are forced to shift at higher frequencies so they can be easily suppressed with the small size of the filtering components. A high switching frequency matrix converter is reported in [38]. The major issue of this topology is non-symmetrical control of the bipolar voltage gain. This nature of the problem is addressed in [28] by adding two more transistors and diodes, as in [38]. The overall impact of this solution is an increase in the overall cost and size. Further, in these two converters [28,38], there is the conduction of more solid-state devices resulting in high conversion losses. There is also a problem with power quality. The number of conducting devices is reduced in [39] but its overall volume is increased due to the use of eight switching transistors. This discussion leads toward the description of the research gap or problem statement.

### 1.3. Problem Statement

The conduction of fewer semiconductor devices and symmetric bipolar voltage gain with buck and boost outputs is obtained in the converter reported in [39]. However, the practical implementation of this topology requires the use of eight insulated bipolar junction transistors (IGBTs) or eight MOSFET-diode series-connected pairs. The use of more

switching devices, especially the transistors, is more critical as their switching operation requires gating control circuits. Such circuits are large in size and cost once compared with switching transistors. Further, there is the use of three capacitors and two inductors. A capacitor is connected at the input, and another is connected at the output terminals to eliminate the voltage variation. The third capacitor is a film capacitor connected at the intermediate stage of the two power converting stages. One inductor is connected toward the input and the other is at the output side, and there is a chance that they may connect in series. It may create a serious problem of high inductive voltage if they have different currents. The inductor connected in series with the load is also critical as there is a chance of its current interruption problem, especially in the operation where the required output frequency is greater than the input frequency. In such cases, the output voltage is abruptly changed from a positive value to a negative value and vice versa many times in one cycle of the input voltage. A summary of deficiencies in similar existing converters reported in [28,39] may be summarized as follows:

1. The overall volume is high as there is a use of more devices or components, especially gate control circuits. This leads to an increase in overall cost and conversion losses.
2. The dynamic response is slow as there is a use of a large number of energy-storing devices such as inductors and capacitors.
3. Gate control schemes have complex switching algorithms.
4. The filtering inductor connected with the load has bidirectional current conduction characteristics, leading to the problem of inductive kicks as there is an abrupt change or interruption in its current.

#### 1.4. Contribution

In viewing these constraints, a novel single-phase matrix converter is proposed in this article that performs a similar operation as in [28,39], just using six switching transistors. The elimination of two transistors helps to compact the size and reduce the overall cost as there is the use of six gate control circuits instead of eight. There is the use of only one energy storing inductor, and its current in all operating modes is unidirectional. This characteristic of inductor current avoids the current reversal problem. It also helps to solve the problem of slow dynamic response. The values of the voltage and current at which the semiconductor devices operate are low, thus helping in lowering the power rating and conversion losses to improve overall efficiency. The values of the ripple current and voltage are also low, which enhances the power quality characteristics. A summary of the salient features of the proposed circuit is listed below.

1. Only six transistors are employed to obtain the required output, eliminating the use of two gate drivers, one inductor, and one capacitor. It results in the compactness of the converter as the size of one gate driver is larger compared to the overall size of the switching transistors.
2. It also improves the dynamic response and overall conversion losses.
3. The direction of the current is kept unidirectional to tackle its current interruption or reversal problem. This characteristic also helps to simplify the feedback control schemes.
4. There is no problem with current shoot-through as the direction of the current in the transistors is ensured to be unidirectional by connecting the series diodes.
5. The same control scheme can be used to produce the non-inverted or inverted buck or boost operation.
6. The state space model for combining voltage buck and boost operation is developed.

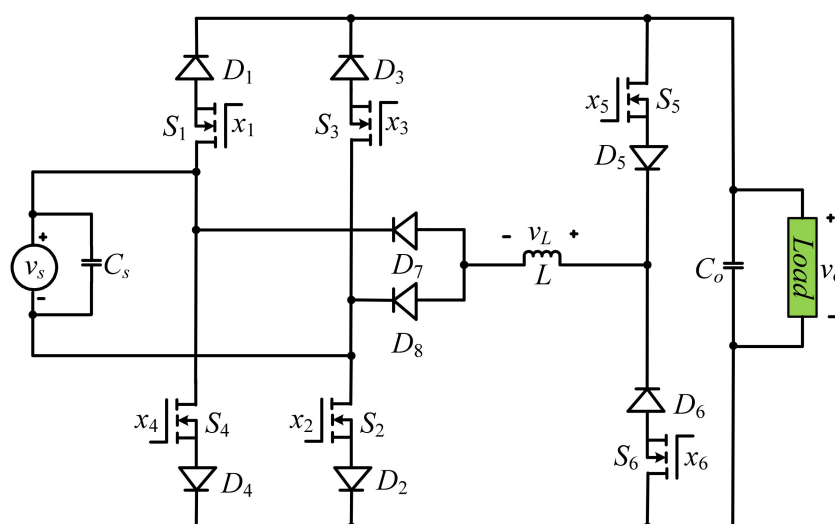
#### 1.5. Paper Organization

The manuscript is organized in various sections. The introduction of the various AC–AC converters in terms of their operating characteristics is explored in Section 1. The operation of the proposed circuit in its various working modes and exploration of the non-inverted and inverted voltage behavior are detailed in Section 2. The voltage transfer ratio in all possible modes is obtained with the help of the inductor voltage for the PWM on and

off periods. A comparative analysis in terms of various performance parameters is detailed in Section 3. Section 4 validates the operation and performance of the proposed circuit by presenting the practical and simulated results. Section 5 is reserved for the conclusion.

## 2. Working Principle and Related Operating Modes

This section helps to understand and explore the working principle with the help of all operating modes, exploring how the sinusoidal input voltage is converted to its inverting and non-inverting forms with a controllable voltage arrangement. The output voltage may have positive or negative values irrespective of the fact that the input voltage has any polarity, which means positive or negative half cycles. This characteristic facilitates arranging a group of positive and negative pulses to set the output frequency to a required value. The change in output frequency with respect to input frequency is always a discrete value that is two times or one-half, etc. The circuit diagram of the proposed topology is shown in Figure 1.



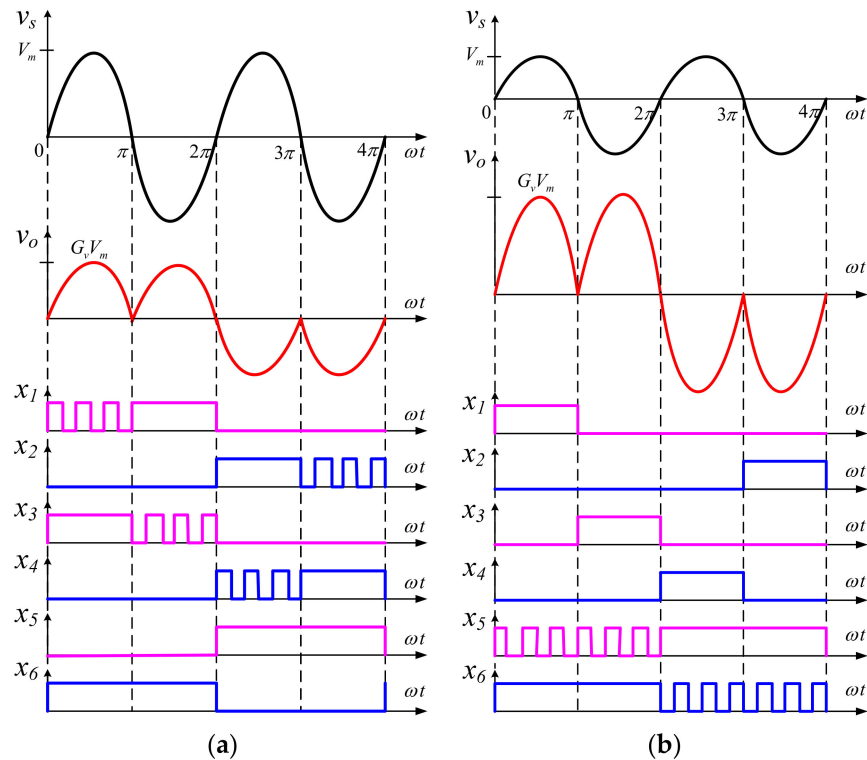
**Figure 1.** Proposed circuit.

There is the use of six transistor-diode pairs  $S_1$ - $D_1$  to  $S_6$ - $D_6$ . There is the additional use of two more diodes  $D_7$  and  $D_8$  that become forward-biased during the periods in which the input voltage ( $v_s$ ) is positive and negative, respectively. This arrangement of the switching devices avoids the possible short circuit loops formed due to the input capacitor ( $C_s$ ) and output capacitor ( $C_o$ ) or their parallel connection. The role of these capacitors is to filter the ripple in the input and output voltage. The inductor ( $L$ ) connected at the intermediate circuit stage is responsible for the storage and transfer of the input power. The direction of this inductor is always unidirectional, which is one of the attractive features of the circuit and eliminates the chance of sudden change or reversal of its current. Let us consider the worst-case switching interval in which all the six transistors are on. This event may be caused by some internal defect in the fabrication process of the switching transistors or programming errors in the control inputs. In this case, the anode voltage of diodes  $D_1$  and  $D_4$ ,  $D_2$  and  $D_3$ , and  $D_7$  and  $D_8$  have equal anode voltage, but their cathode voltages are unequal. In the same way, the cathodes of the diodes  $D_5$  and  $D_6$  are connected to the same point having equal voltage at their cathodes and unequal voltage at their anodes. These pairs of diodes cannot conduct at the same time. So, there exist no short circuit loops for the input capacitor, output capacitor, or parallel connection. In this circuit, the problem of shoot-through is eliminated inherently.

The input voltage has two half cycles, and there are four possible ways to regulate and control these half cycles at the output. That includes the non-inverted and inverted forms both for the positive and negative half cycles of the input voltage. The regulation



in the output can be step up (boost) and step down (buck). In this regard, the control inputs for voltage regulation are shown in Figure 2a,b to produce the voltage buck and boost operation.



**Figure 2.** High and low-frequency gating signals for (a) voltage buck operation and (b) voltage boost operation.

For the voltage buck operation, the peak magnitude of the output voltage is always less than the peak magnitude of the input voltage. The peak magnitude of the input is constant, but the peak magnitude of the output voltage is controllable through the regulation of duty cycle control. The high-frequency PWM control signals  $x_1$  and  $x_3$  with low-frequency control signal  $x_6$  are responsible for generating the positive pulses at the output. There is no role for the remaining signals ( $x_2$ ,  $x_4$ , and  $x_5$ ) for this operation. There is the use of high-frequency control signals  $x_2$ ,  $x_4$ , and one low-frequency control signal  $x_5$  to generate negative output pulses at the output. A complete control scheme for the operation where the output frequency is half of the input frequency is shown in Figure 2a. For voltage boost operation, the high-frequency operation of the switching transistors is performed with the control signals  $x_5$  and  $x_6$ . The generation of a group of positive and negative pulses is ensured at the output with the low-frequency operating transistors. The generation of control inputs  $x_1$  and  $x_3$  help to arrange the positive pulses at the output during the positive and negative half cycle of the input voltage, respectively. In the same way, control signals  $x_4$  and  $x_2$  are set to logic high for positive and negative input voltage, respectively. The PWM modulation of the high-frequency signals controls the gain ( $G_V$ ) of the converter.

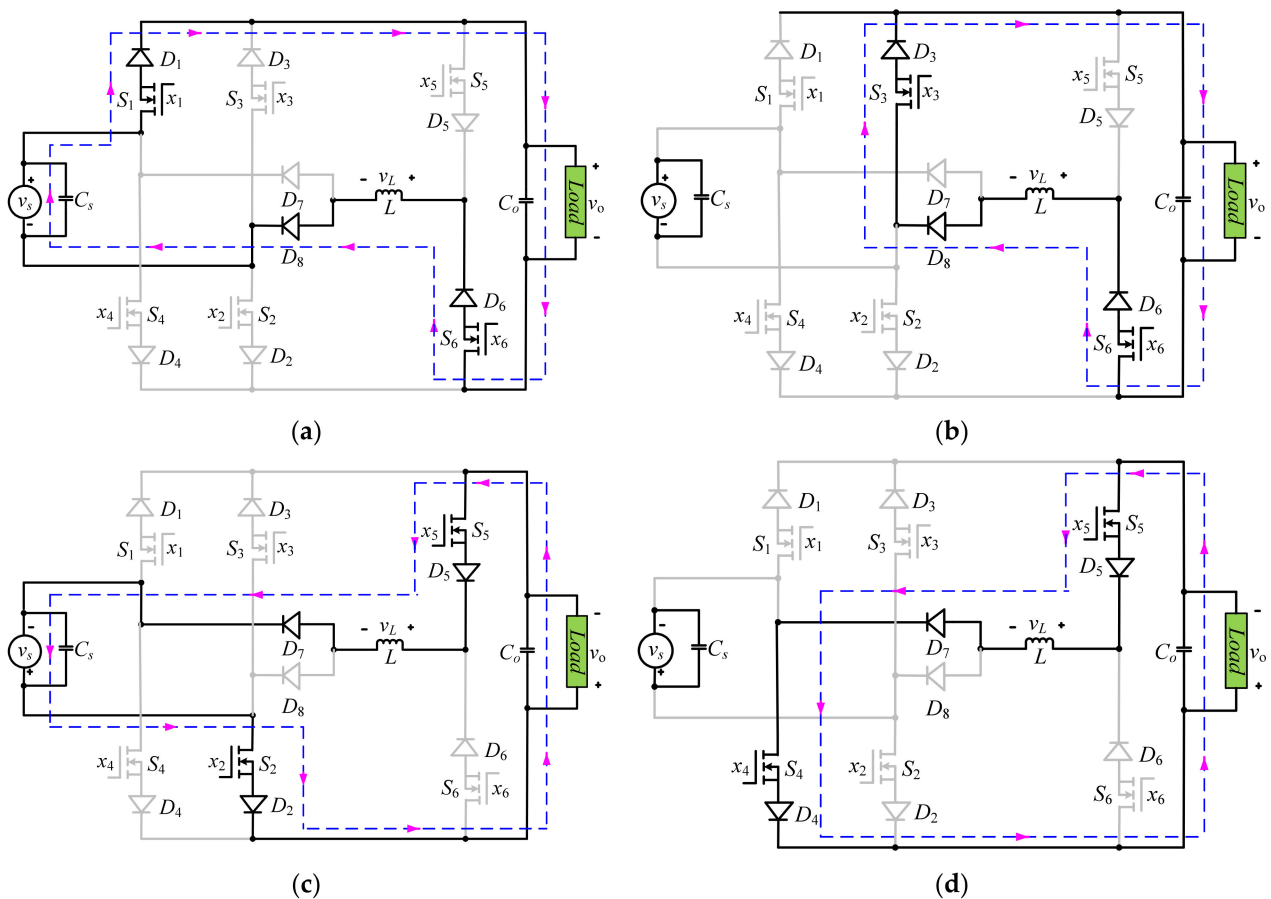
### 2.1. Generation of Non-Inverted and Inverted Voltage Buck Outputs

The regulation in the load voltage ( $v_o$ ) can be confirmed via the duty cycle or PWM control ( $d_1$ ) developed for the operating transistors. In the voltage buck operation, the variation in the load voltage is ensured from the maximum value of the input voltage to some lower value. In this operation, the input power is sent to output via an intermediate inductor by turning on all transistors in that conducting loop. This process is continued for the on-time interval ( $d_1 T$ ) of the one-control period ( $T$ ). In the off-time interval ( $(1 - d_1)T$ )

of the switching period, the source voltage is removed from the circuit, and power stored in the inductor to now transferred to the load. Voltage buck operation in its non-inverted and inverted form for the positive and negative input voltage is detailed here.

The control signals in Figure 2a help to perform the voltage buck operation. Here the output is non-inverted for the first and fourth half cycles of the input voltage. The output voltage is positive in the first half cycle of the input voltage. To produce this output during this period, the switching transistor  $S_1$  operates with high-frequency PWM control while the transistors  $S_3$  and  $S_6$  remain on until the polarity of the input voltage is changed. The series-connected diode  $D_3$  with transistor  $S_3$  is reverse-biased as its cathode is connected with the positive terminal of the source voltage once the transistor  $S_1$  is on. No current can be conducted through this branch or pair. During this interval, the load is connected with the input as shown in the highlighted loop of Figure 3a as transistors  $S_1$  and  $S_6$  are on with the forward biasing of diodes  $D_1$ ,  $D_6$ , and  $D_8$ . The value of voltage across the inductor ( $L$ ) is detected in Equation (1) by applying the KVL in the existing loop.

$$v_L(t = d_1 T) = v_s - v_o \tag{1}$$



**Figure 3.** Equivalent current-conducting loops with respect to input voltage to produce non-inverting buck operation during; (a,b) positive half cycles; (c,d) negative half cycles.

The continuity in the inductor current is granted with the turning on of the diode  $D_3$  once the high-frequency operating transistor  $S_1$  turns off. In this period  $((1 - d_1) T)$ , the energy stored in the inductor is linked to the output with the highlighted loop in Figure 3b. In this interval, the inductor becomes a current source for the output and its voltage is founded through KVK analysis as

$$v_L(t = (1 - d_1) T) = -v_o \tag{2}$$

Next, the non-inverting voltage buck operation is considered for negative input voltage. The output of this mode is produced with the help of the high-frequency switching operation of the transistors  $S_2$  and  $S_4$ . The switch  $S_5$  remains on for the period in which input voltage is negative to facilitate the conduction of continuous inductor and load currents. The current conduction loops in which the input power is stored and then transferred to the output is shown in Figure 3c,d. Here the transistors  $S_2$  and  $S_4$  operate in a complementary way. The high-frequency operation of the transistor  $S_4$  is controlled with the forward biasing and reversing of the diode  $D_4$ . The operating behavior of this diode is directly linked with the operation of the transistor  $S_2$ . There is no change in the value of the inductor voltage during the high-frequency on and off intervals as shown below.

$$v_L(t = d_1T) = v_s - v_o \quad (3)$$

$$v_L(t = (1 - d_1)T) = -v_o \quad (4)$$

The use of a high switching frequency facilitates considering the inductor voltage constant during one switching period. The balancing of the inductor volt-second principle helps to determine the voltage transfer ratio or voltage gain in terms of duty cycle control.

$$(v_s - v_o)d_1T = v_o(1 - d_1)T \quad (5)$$

$$v_s d_1 = v_o \quad (6)$$

So

$$v_o = d_1 v_s \quad (7)$$

For the inverting voltage buck operation, the polarity of the output voltage is always inverted with respect to the input voltage. The inverted outputs are observed in the second and third half cycles of Figure 2a for negative and positive input voltage, respectively. A previous approach may be employed for validation of the inverting voltage gain. This includes the current conduction loops for power transfer and the value of the inductor voltage once it stores and releases the power toward the load. These loops are demonstrated in Figure 4a,b for positive input, and in Figure 4c,d for negative input voltage. The value of the inductor voltage can be simply modified from Equations (1) and (2) by just inverting the polarity of the output voltages and may be observed from Equations (8) and (9).

$$v_L(t = d_1T) = v_s + v_o \quad (8)$$

$$v_L(t = (1 - d_1)T) = v_o \quad (9)$$

By considering the principle of volt-second behavior of the inductor for one switching period, it may be noticed as:

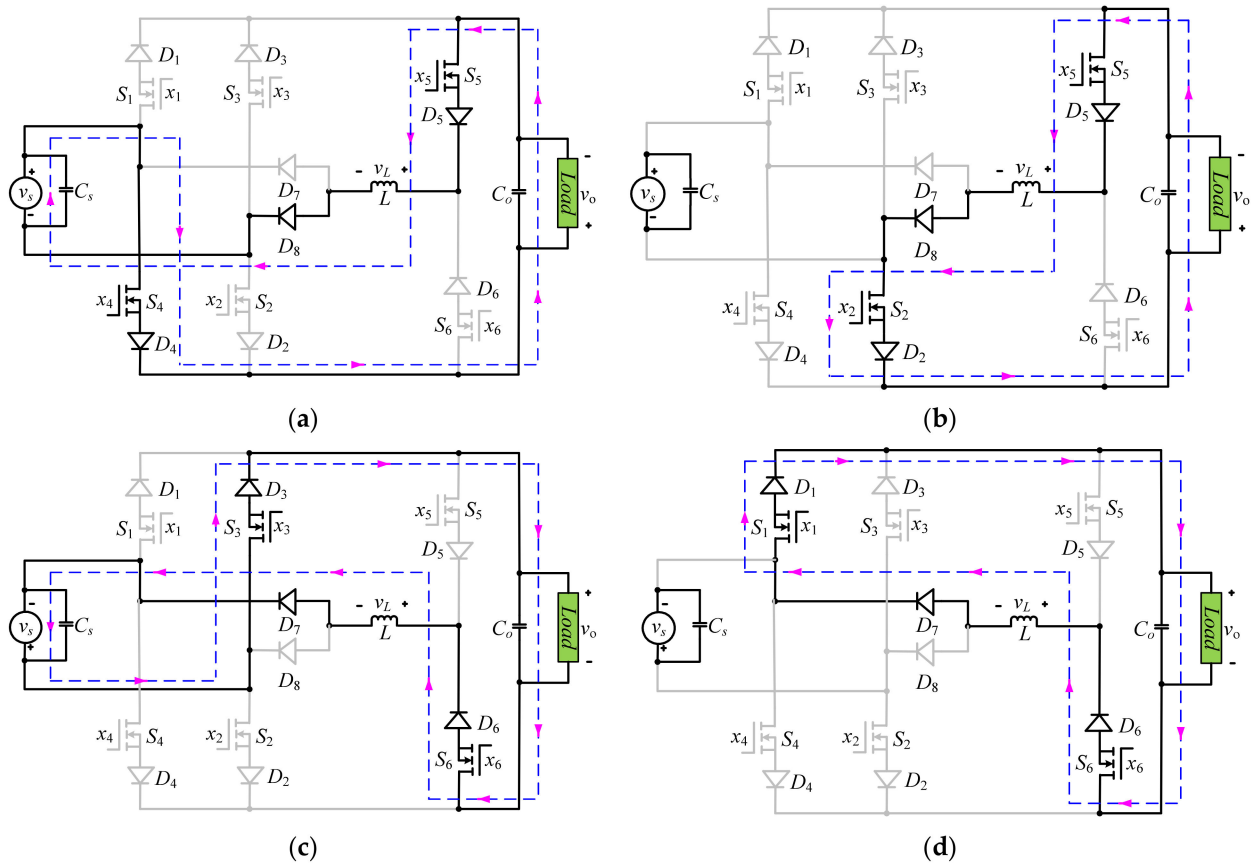
$$(v_s + v_o)d_1T = -v_o(1 - d_1)T \quad (10)$$

$$v_s d_1 = -v_o \quad (11)$$

$$v_o = -d_1 v_s \quad (12)$$

The final closed forms of Equations (7) and (12) express the non-inverted and inverted relationship between the input and output voltage, respectively. The controllability of the output voltage can be governed with the help of duty cycle control. This arrangement ensures the voltage regulation in the instantaneous output voltage from maximum input voltage to some lower values.





**Figure 4.** Equivalent current-conducting loops with respect to the input voltage to produce inverting buck operation during; (a,b) positive half cycles; (c,d) negative half cycles.

It is investigated that in all equivalent current loops, there is the conduction of two transistors with their internal resistances  $r_t$ , three diodes with their internal resistances  $r_d$ , and there is one inductor with its resistance of  $r_L$ . Therefore, the total resistance faced by the current conduction in these loops due to conducting devices and a filtering inductor can be calculated by adding their values. It can be seen as

$$R_{ind} = r_L + 2r_t + 3r_d \tag{13}$$

The state space modeling of the voltage buck operation with duty cycle control of  $d_1$  for any polarity of the input voltage based on the PWM averaging principle as reported in [40] is formulated in Equations (14) and (15) for non-inverting and inverting operation, respectively. Here inductor current ( $i_{ind}(t)$ ) and output capacitor voltage ( $v_o(t)$ ) are chosen as the state variable.

$$\frac{d}{dt} \begin{bmatrix} i_{ind}(t) \\ v_o(t) \end{bmatrix} = \begin{bmatrix} \frac{-R_L}{L} & \frac{-1}{L} \\ \frac{1}{C_o} & \frac{-1}{R_o C_o} \end{bmatrix} \begin{bmatrix} i_{ind}(t) \\ v_o(t) \end{bmatrix} + \begin{bmatrix} \frac{d_1}{L} \\ 0 \end{bmatrix} v_s(t) \tag{14}$$

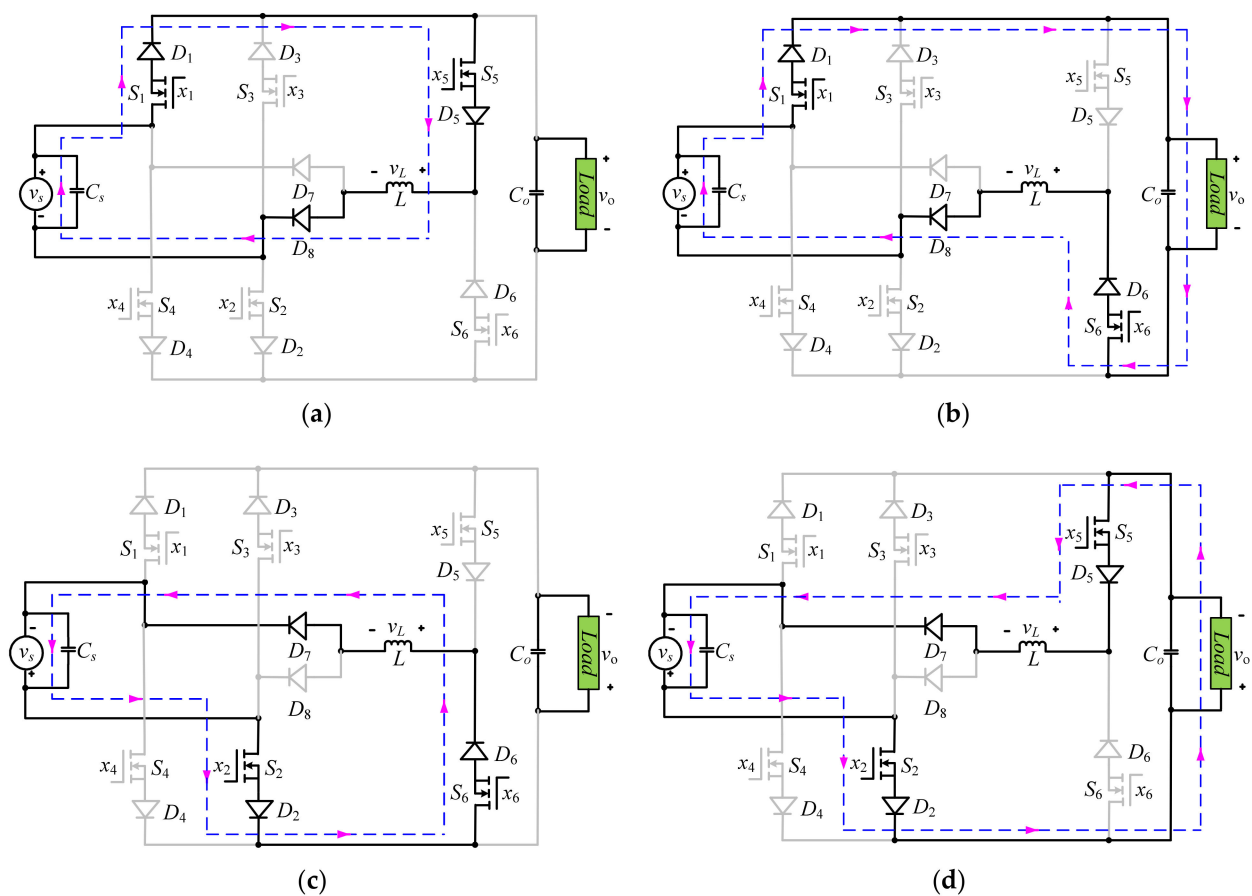
$$\frac{d}{dt} \begin{bmatrix} i_{ind}(t) \\ v_o(t) \end{bmatrix} = \begin{bmatrix} \frac{-R_L}{L} & \frac{1}{L} \\ \frac{-1}{C_o} & \frac{-1}{R_o C_o} \end{bmatrix} \begin{bmatrix} i_{ind}(t) \\ v_o(t) \end{bmatrix} + \begin{bmatrix} \frac{d_1}{L} \\ 0 \end{bmatrix} v_s(t) \tag{15}$$

### 2.2. Generation of Non-Inverted and Inverted Voltage Boost Outputs

This operation is utilized for the application where the required instantaneous output voltage is greater than the input voltage. The required voltage gain is more than unity, and this is controllable with the help of the duty cycle control ( $d_2$ ) of high-frequency switching devices, especially transistors. The voltage boost operation comprises the first storage of

the input power in the inductor. At that time, the load is completely isolated from the input source voltage, and power consumed by the load is supplied from the output capacitor. For this purpose, the size of this capacitor should be reasonable to lower the ripple in the output voltage and supply power to the load in this period. The period (that is, the known turn-on interval of a PWM control signal) in which the inductor is energized from the source voltage is directly linked with the amount of the required voltage gain. The value of the inductor voltage depends on this period. The load voltage is the sum of the input and inductor voltage in the turn-off interval of the PWM control signal. Surely this sum of the voltages is greater than the input voltage, so this operation is called a voltage boost operation. The only difference between the non-inverting and inverting processes is output voltage polarity with respect to the input voltage. The output voltage form is non-inverted and inverted if it is in-phase and out of phase with respect to the input voltage. This behavior of the output is explained in the next paragraphs.

Non-inverted and inverted voltage forms can be explained with respect to control inputs plotted in Figure 2b. Here it may notice that there are only two high-frequency control signals  $x_5$  and  $x_6$ . The non-inverted and inverted versions of the input voltage are determined from the generation of the low-frequency signals. For example, to realize the non-inverted version of the input voltage, the low-frequency control inputs  $x_1$  and  $x_2$  are set to logic high during the intervals in which the input voltage has positive and negative half cycles, respectively. The current conducting loops for this process are highlighted in Figure 5a–d for positive and negative input voltage, respectively.



**Figure 5.** Equivalent current-conducting loops with respect to the input voltage to produce non-inverting boost operation during: (a,b) positive half cycles; (c,d) negative half cycles.

The plots in Figure 5a,c show the current flowing paths to transform the input power to the inductor. In this process, the inductor voltage is equal to the input voltage as it is directly connected across the source voltage.

$$v_L(t = d_2T) = v_s \tag{16}$$

The output voltage is the sum of the input and inductor voltages once one high-frequency PWM control transistor turns off and the other turns on to keep the continuity of the inductor current. This behavior is highlighted in the plot of Figure 5b,d for positive and negative input voltage, respectively. During these intervals, the inductor voltage is the difference between input and output voltages, as can be viewed from Equation (17).

$$v_L(t = (1 - d_2)T) = v_s - v_o \tag{17}$$

The voltage-second balance of the inductor voltage during the turn-on and off intervals helps to determine the voltage transfer ratio in terms of duty cycle control.

$$v_s d_2 T = -(1 - d_2) T (v_s - v_o) \tag{18}$$

$$v_o = \frac{v_s}{1 - d_2} \tag{19}$$

Similar control signals as shown in Figure 2b can be practiced to get the inverted version of the input voltage. To achieve this target, the role of  $x_1$  and  $x_2$  is exchanged with  $x_3$  and  $x_4$ . The behavior of the high-frequency control signals remains unaltered as it is seen for a non-inverting operation. The plots of Figure 6a–d express the inverting boost operation for positive and negative input voltage, respectively. Parts ‘a’ and ‘c’ of this figure show the current conduction path that is used to transform the power from the input source to the intermediate inductor ( $L$ ). The same inductor voltages as seen for a non-inverting operation can be observed in Equation (20) by using the KVL concept in the loops of Figure 6a,c.

Equation (20) can easily be obtained by inverting the polarity of the output voltage in Equation (17). This value of the inductor voltage can also be confirmed from the highlighted loops in Figure 6b,d. These current-conducting loops show how the stored energy is recovered and sent to the output using high-frequency PWM control.

$$v_L(t = d_2T) = v_s \tag{20}$$

$$v_L(t = (1 - d_2)T) = v_s + v_o \tag{21}$$

The knowledge of the inductor volt-sec product leads to the development of the following voltage transfer ratio. This equation validates the inverted voltage response of the converter with voltage step-up features.

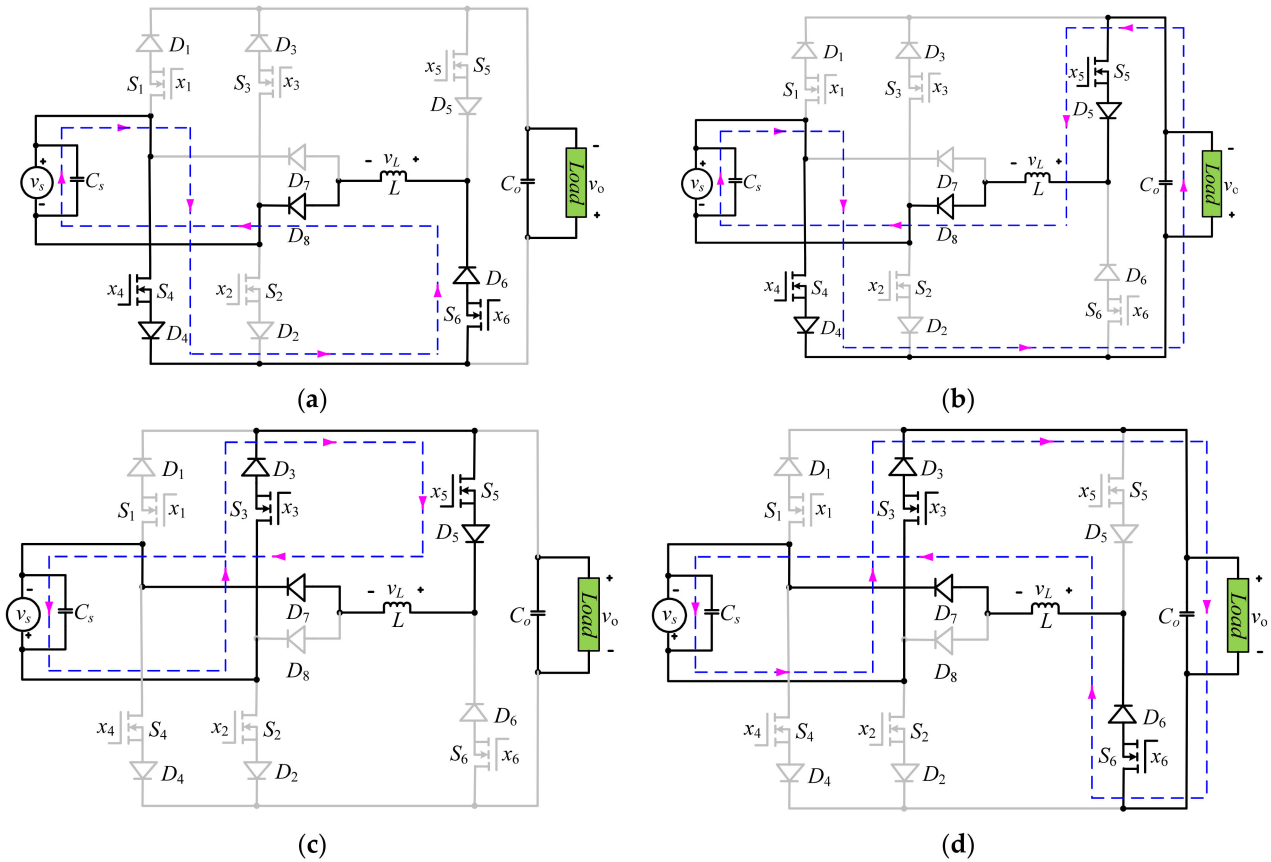
$$v_o = \frac{-v_s}{1 - d_2} \tag{22}$$

The observation of Equations (19) and (22) confirms the voltage step-up behavior. The output voltage may be a non-inverted or inverted version of the input voltage, and adjustment in the output can be attained by applying PWM control.

The state space modeling of the voltage boost operation with duty cycle control of  $d_2$  for both polarities of the input voltage that is based on the PWM averaging principle as discussed in [41] is formulated in Equations (23) and (24) for non-inverting and inverting operation, respectively.

$$\frac{d}{dt} \begin{bmatrix} i_{ind}(t) \\ v_o(t) \end{bmatrix} = \begin{bmatrix} \frac{-R_L}{L} & \frac{-(1-d_2)}{L} \\ \frac{(1-d_2)}{C_o} & \frac{-1}{R_o C_o} \end{bmatrix} \begin{bmatrix} i_{ind}(t) \\ v_o(t) \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} v_s(t) \tag{23}$$

$$\frac{d}{dt} \begin{bmatrix} i_{ind}(t) \\ v_o(t) \end{bmatrix} = \begin{bmatrix} \frac{-R_L}{L} & \frac{(1-d_2)}{L} \\ \frac{-(1-d_2)}{C_o} & \frac{-1}{R_o C_o} \end{bmatrix} \begin{bmatrix} i_{ind}(t) \\ v_o(t) \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} v_s(t) \quad (24)$$



**Figure 6.** Equivalent current-conducting loops with respect to the input voltage to produce inverting boost operation during: (a,b) positive half cycles; (c,d) negative half cycles.

The state space modeling of voltage buck and boost operation can also be merged into a single model, as may be seen from Equations (25) and (26) for non-inverting and inverting outputs, respectively.

$$\frac{d}{dt} \begin{bmatrix} i_{ind}(t) \\ v_o(t) \end{bmatrix} = \begin{bmatrix} \frac{-R_L}{L} & \frac{-(1-d_2)}{L} \\ \frac{(1-d_2)}{C_o} & \frac{-1}{R_o C_o} \end{bmatrix} \begin{bmatrix} i_{ind}(t) \\ v_o(t) \end{bmatrix} + \begin{bmatrix} \frac{d_1}{L} \\ 0 \end{bmatrix} v_s(t) \quad (25)$$

$$\frac{d}{dt} \begin{bmatrix} i_{ind}(t) \\ v_o(t) \end{bmatrix} = \begin{bmatrix} \frac{-R_L}{L} & \frac{(1-d_2)}{L} \\ \frac{-(1-d_2)}{C_o} & \frac{-1}{R_o C_o} \end{bmatrix} \begin{bmatrix} i_{ind}(t) \\ v_o(t) \end{bmatrix} + \begin{bmatrix} \frac{d_1}{L} \\ 0 \end{bmatrix} v_s(t) \quad (26)$$

The state space form shown in the above two equations represents the complete behavior of all operating modes in Figures 3–6. Equations (25) and (26), respectively, show their non-inverting and inverting behavior. For example, for non-inverting buck operation for positive input voltage, the value of  $d_2$  is kept at zero. This value ensures that the transistor  $S_5$  is kept off all the time for the above operation (see Figure 3a,b). The duty cycle control of  $d_1$  is a PWM control that regulates the output voltage per requirements. In the same way, for boost operation, the value  $d_1$  is set to '1', and now duty cycle control of  $d_2$  is a PWM control that controls the output voltage. Equation (25) represent Equations (14) and (23) by putting  $d_2 = 0$  and  $d_1 = 1$ , respectively. These values of the duty cycle control also help to converge Equation (26) to Equations (15) and (24), respectively. The developed steady-state representation may be used to find stability by designing an appropriate feedback controller.

### 3. Comparison and Analysis

The major achievement of the proposed circuit arrangement is a reduction in the switching devices. In the suggested circuit, there is the ability to govern the load voltage with the adjustment of the duty cycle, which is PWM control. The polarity of the output voltage can also be set to a positive or negative value for any polarity of the input voltage. The control in the output voltage can be settled to the required value by setting the positive and negative half cycles for the consecutive half periods of the output voltage. All these processes can be performed with the help of only six transistors and a diode. In the same way, the similar output in the existing converters uses eight transistors and diodes [28,39]. The use of gate control circuits is a fundamental need for the operating principle of switching transistors, and they require more space and have high costs. These circuits acquire a reasonable space in the total space of the switching converters. The compared parameters are listed in Table 1. The peak or rms voltage of the switching devices depends on the inductor value equal to the output and input currents for voltage buck and boost operations, respectively. In this regard, the switching voltages and currents of the proposed circuit and the existing converter [28,39] are the same. In the proposed circuit and converter in [28], there is only one energy-storing inductor and its current direction is unidirectional, which is one of the attractive features that limit the current interruption problem of the inductor current. This feature of the inductor current also helps to simplify the feedback control schemes. However, the converter of [39] has to use two energy-storing inductors. The inductor is connected to the input store and releases the energy to obtain voltage boost operation. The current flow in this inductor is bidirectional and there is no current interruption or reversal problem. However, the inductor connected toward the load side used to perform the voltage buck operation has a risk of reversal and interruption of its current. During the one operating cycle of the input voltage, there is the use of four low-frequency transistors and diodes in the proposed circuit and converter in [28,39]. These converters have equal conduction losses as listed in Table 1. In these computations,  $V_{fd}$  is the forward voltage of the diodes, and  $R_{fd}$  and  $R_{tr}$  are conducting resistances of the diodes and transistors, respectively. The converter in [39] only needs the high-frequency operations of the two transistors, so its switching losses are low, but these losses cannot significantly increase the overall conversion losses. Switching losses depend on the rise ( $t_r$ ) and fall ( $t_f$ ) times of the switching transistors, and their values in the modern age lie in the nanosecond range. The proposed topology simplifies the constraints of the existing circuits and increases the effectiveness or potency of application in various industrial drives.

**Table 1.** Comparison with existing circuit topologies.

Parameters	Proposed Circuit	Converter in [28]	Converter in [39]
Peak switching currents	$I_{L(\max)}$	$I_{L(\max)}$	$I_{L(\max)}$
Peak switching voltage	$V_{o(\max)}$	$V_{o(\max)}$	$V_{o(\max)}$
Number of transistors	6	8	8
Number of diodes	6	8	8
Number of gate control circuits	6	8	8
Inductor current interruption	No	No	Yes
Number of capacitors	2	2	3
Number of inductors	1	1	2
Directional of inductor current	Unidirectional	Unidirectional	Bidirectional
Conduction losses	$\frac{4V_{fd}I_{L(p)}}{\pi} + I_{L(p)}^2 \left( R_{fd} + \frac{R_{tr}}{2} \right)$	$\frac{4V_{fd}I_{L(p)}}{\pi} + I_{L(p)}^2 \left( R_{fd} + \frac{R_{tr}}{2} \right)$	$\frac{4V_{fd}I_{L(p)}}{\pi} + I_{L(p)}^2 \left( R_{fd} + \frac{R_{tr}}{2} \right)$
Switching losses	$\frac{4f_{sw}V_{o(p)}I_{L(p)}}{6} (t_r + t_f)$	$\frac{4f_{sw}V_{o(p)}I_{L(p)}}{6} (t_r + t_f)$	$\frac{2f_{sw}V_{o(p)}I_{L(p)}}{6} (t_r + t_f)$

### 4. Results and Discussion

To examine the performance and operational features of the proposed circuit, various test platforms are employed, including the simulation approach and practical results

obtained from real circuits. In this section, one output frequency is chosen to test the regulation in the voltage and inverted or non-inverted output with respect to a given source voltage. In these test results, the magnitude (180 V) and frequency (50 Hz) of the input voltage are kept constant. The frequency and magnitude of the load are regulated through switching signals. The low-frequency switching signals adjust the load frequency in some selected discrete steps, for example, one-half or one-third of the constant input frequency. On the other hand, the high-frequency PWM or duty cycle control governs the variation in the magnitude of the output voltage. For any required output frequency value, Table 2 shows the required value of the duty ratio control to obtain the peak output voltage of 50 V, 80 V, and 200 V from an input peak voltage of 180 V.

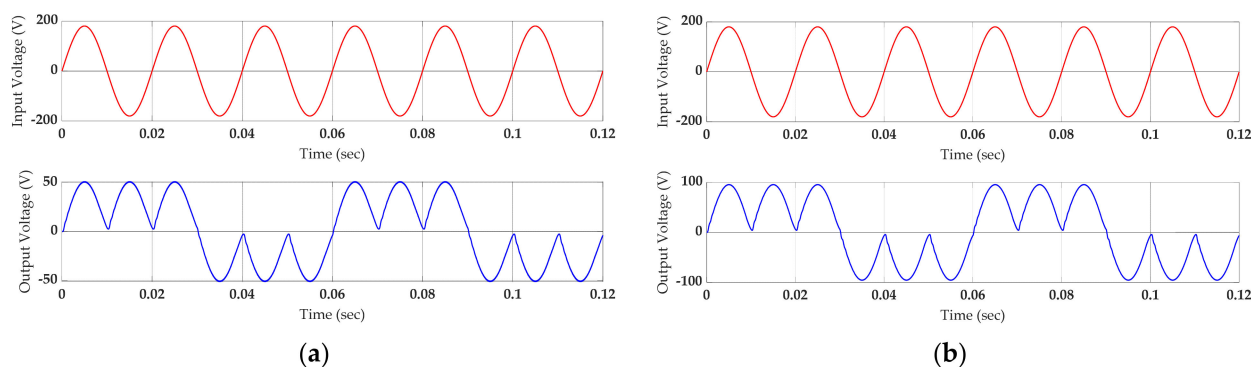
**Table 2.** Required voltage gain or duty cycle ratio to obtain the required output.

Input Voltage	Output Voltage	Voltage Gain	Duty Ratio Control
180 V	50 V	0.28	0.28
180 V	80 V	0.55	0.55
180 V	200 V	1.12	0.107

The variation in the output voltage may be adjusted to any required value below 180 V and above 180 V with the proper setting of the duty ratio control.

#### 4.1. Simulated Results

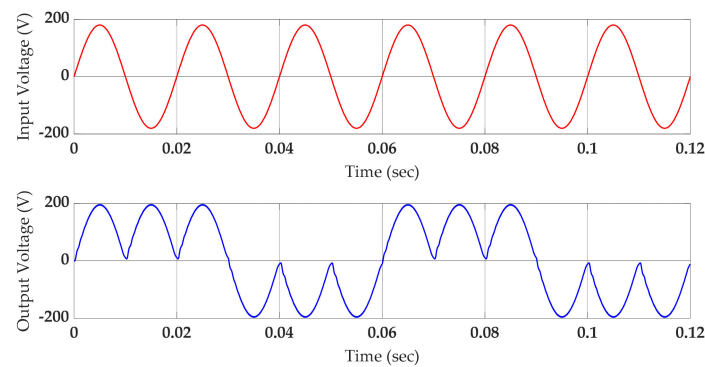
One of the attractive approaches is to test the outputs of the proposed circuit on a computer simulation before it is moved toward practical implementation. It is simple and easy to analyze the switching converters in this environment because there is no need for detecting or sensing the polarity of the input voltage. In this effort, the values of the designed components for practical realization are used to test the outputs. The modeling of the switching devices is developed with respect to the internal parameters of the transistors and diodes that are designed for practical setup. The role of the microcontroller is modeled by employing the pulse generators. A load of 100  $\Omega$  is connected to the output as a load to test its outputs. The purpose of this environment is to test the non-inverted and inverted voltage buck and boost operation with voltage regulation capabilities. For this purpose, the input peak voltage of 180 V is converted to 50 V and 100 V peak voltage, ensuring a voltage gain of 0.28 and 0.55, respectively, for voltage buck operation. The simulated output with these required values is plotted in Figure 7a,b.



**Figure 7.** Simulation results for output frequency step-down process with a voltage gain of (a) 0.28; (b) 0.55.

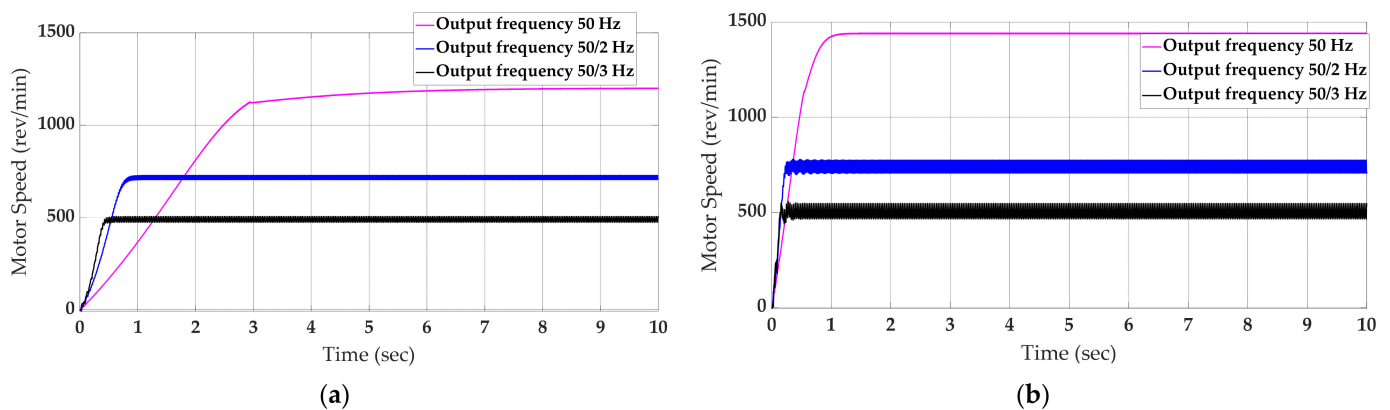
The output frequency of the output voltage is lowered to three times the input frequency. The voltage boost operation is also explored at the same frequency, and its output is presented in Figure 8 in simulation form.





**Figure 8.** Simulation results for output frequency step-down process with a voltage gain of 1.12.

These test results prove the required operation of the proposed converter. The observation of these figures indicates that the output voltage is a regulated form of the input voltage. This output can be converted into the non-inverted and inverted versions of the input voltage. These features of the output voltage enable variation in the load frequency to govern the output speed of the single-phase induction motors. For this purpose, a 180 W single-phase capacitor start induction motor is connected to the output as a load. The output speed variation of this motor is observed at three frequencies (50, 25, and 17 Hz) with various output voltage levels. The values of the input frequency and peak voltage are 50 Hz and 180 V, respectively. The values of the peak output voltage for these output frequencies are adjusted to 50 V and 80 V with the settings of duty ratio control of 0.28 and 0.55, respectively. Figure 9 shows the variation in the speed of the single-phase induction motor with respect to the variation in its voltage and frequency.

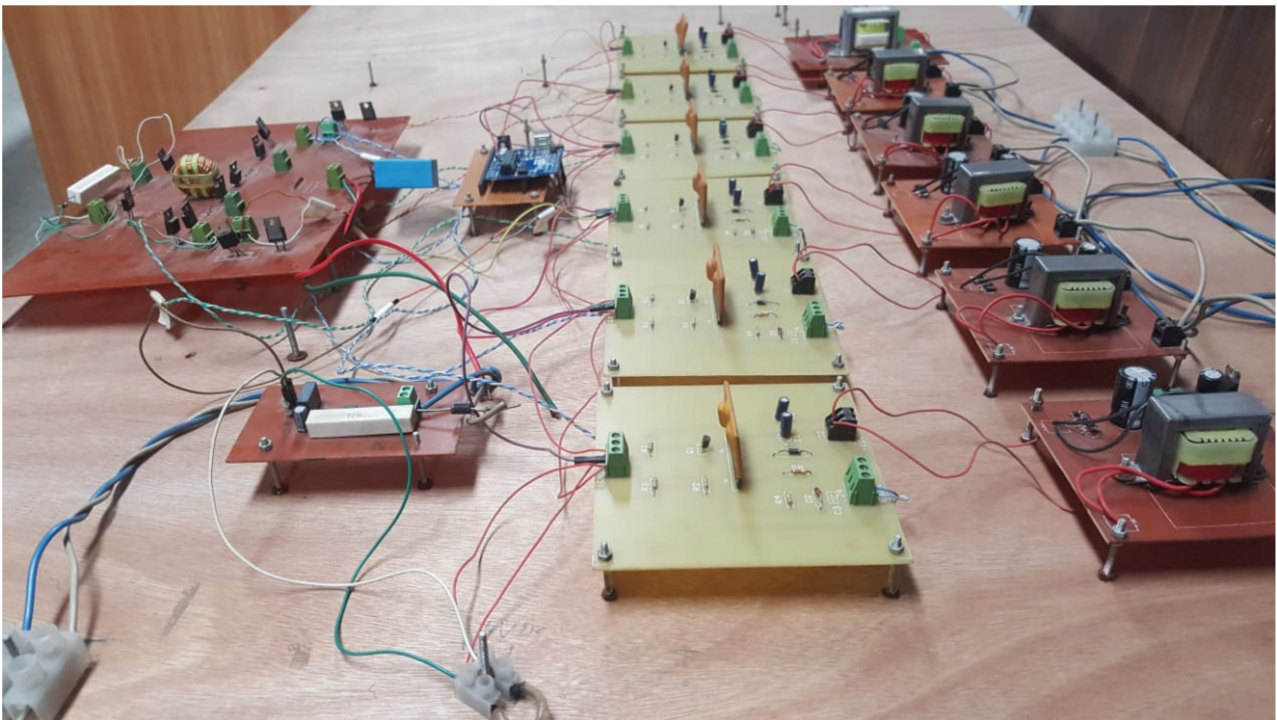


**Figure 9.** Simulation results for motor output speed for various output frequencies with a voltage gain of (a) 0.28 and (b) 0.55.

It is observed that for 50 Hz frequency operation, there is no change in the output frequency with respect to input; the waveform quality of the output voltage is almost similar to the input voltage. There is a low ripple in its speed at this frequency compared to the 25 Hz and 17 Hz output frequencies. The variable frequency outputs always contain harmonics, which are investigated in [28,30]. Most of the effects of these harmonics are tackled by the inductance of the motor winding but there is a generation of some ripples in its output speed. The speed of the induction motor inversely varies with respect to the frequency, which means that at low frequencies, the motor speed is low, and it is high at higher frequencies. The variation in the speed is also directly proportional to the magnitude of the supplied voltage.

#### 4.2. Practical Results

This section aims to convert the constant magnitude and frequency sinusoidal input (grid) voltage into various forms, that is, its non-inverting and inverting shapes with controllable magnitude and frequency. Some distortion may be added to the input voltage due to high switching frequency operation; one low-value capacitor ( $1\ \mu\text{F}$ ) can be connected to the input side. In the successful operation of the switching converters, there is always a need for an energy-storing inductor. In this regard, an inductor of  $1\ \text{mH}$  is used. The role of this inductor is to store and transfer the input energy to output with the high-frequency operation of the switching devices. The value of this inductor and switching frequency determines the amount of ripple in its current. The ripples and power quality directories of the output voltage also require the use of one output capacitor ( $4.7\ \mu\text{F}$ ). The photograph of this practical setup is shown in Figure 10. On the right side of this figure, six isolated DC supplies and six gate drivers are shown in two vertical rows. The RHRG3040 and IRF840 are used as high-frequency diodes and transistors, respectively. The EXB840 hybrid chip is used in the gate control circuit to increase the voltage level of the generated signal generator. Normally, the voltage level of the control signals lies in the range of  $0\ \text{V}$  to  $5\ \text{V}$ , but the required voltage value for the effective operation of the transistor IRF 840 may exceed  $20\ \text{V}$ . All the control signals generated by the micro-controller have the same reference voltage level. However, in switching converters, the voltage reference level of all control inputs should be isolated. This needs the isolated DC value of  $20\ \text{V}$ . For this purpose, a stepdown transformer in each isolated DC power supply ensures the required DC voltage and the electrical isolation between all outputs of the DC power supplies. The output of the microcontroller is supplied to the gate control circuit to isolate the reference points of all control signals and to set their magnitude to the required  $20\ \text{V}$  level. A voltage-detecting circuit is also required to determine the polarity of the input voltage. The output of this circuit ensures the alignment of all control signals with respect to the input voltage, having a peak voltage of  $180\ \text{V}$ .



**Figure 10.** Practical test circuit.

The inverted and non-inverted arrangement of the voltage buck and boost operation with various output voltages are shown in Figures 11 and 12, respectively. These outputs

are the recorded forms obtained from the Rigol oscilloscope. The input and output voltage waveforms of figures are represented with red and blue colors for their differentiation. Two cycles of the output voltage during the six cycles of the input voltage are investigated from these waveforms. One period of the output voltage contains three periods of the input voltage, so the output frequencies of these waveforms are one-third the frequency of the input voltage. It is also observed that during one period of the output, four pulses (first, third, fourth, and sixth) are in the non-inverted form of the input voltage while two pulses (second and fifth) are present in the inverted form of the input voltage. For the results of voltage buck operation as demonstrated in Figure 11a,b, the voltage gains of the power converting system are 0.3 and 0.55, as the peak values of these pulses are approximately 60 V and 100 V, respectively. The output of Figure 12 shows the voltage of the boost operation with the peak value of the output voltage at approximately 200 V. The results show in these waveforms that output voltage and frequency can be effectively produced with simple control schemes.

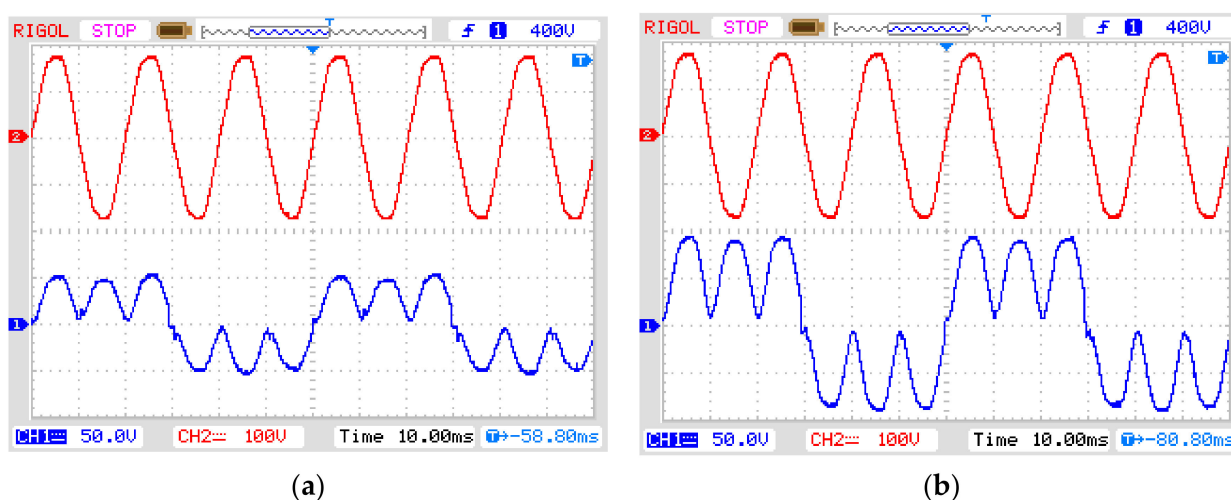


Figure 11. Real value results for output frequency step-down process with a voltage gain of (a) 0.3 and (b) 0.55.

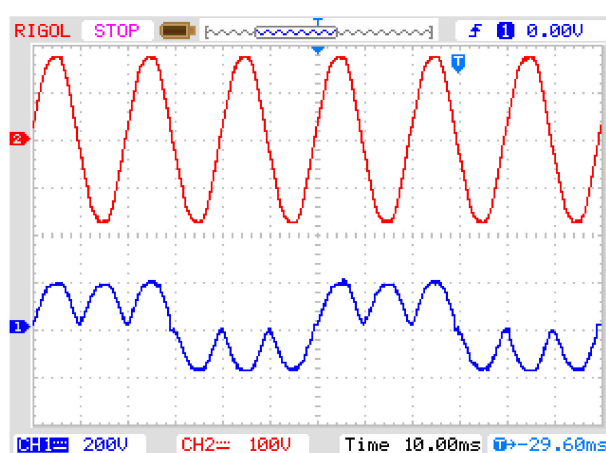


Figure 12. Real value results for output frequency step-down process with a voltage gain of 1.12.

## 5. Conclusions

The present research is related to developing a compact-sized AC–AC converter that can produce controllable output in non-inverted and inverted voltage buck and boost forms. The value of the output can be set to any desired value with the PWM control. These output voltage features are used to obtain the required variable output frequency

with the proper arrangement of positive and negative pulses. The independent voltage buck and boost operation enhance the controllability and flexibility through PWM control. This operation ensures low values of the voltage and current stresses for the components and semiconductor devices. There are also low values of the peak ripple currents and voltage; smooth variations in output voltage, output current, and input current are the main factors of the improved power quality. The regulation in the output voltage and frequency is obtained just by using six transistors and six diodes as compared to eight transistors and eight diodes in existing converters. The reduction in semiconductor devices lowers the size, losses, and overall cost. The major achievement in these values is due to the elimination of two transistors, as the size and cost of their control circuit are much larger with respect to their cost and size. There is also the use of only one filtering inductor and two filtering capacitors. The direction of this current is ensured to be continuous and unidirectional to tackle its interruption and reversal problem. Otherwise, there is a chance for the induction of high inductive voltage kicks, which may require complex switching arrangements. The details of all operating modes are highlighted indicating the non-inverting and inverting voltage operation both for the positive and negative input values. The proposed topology can vary the output frequency in step-down and step-up modes, so this can be effectively operated with unity and non-unity power factor loads. The simulation environment and practical setup circuit are developed to test its output for variable frequency operation with controllable voltage capabilities. These results confirm the usefulness of the developed circuit.

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