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Hysteresis Based Quasi Fixed Frequency Current Control of Single Phase Full Bridge Grid Integrated Voltage Source Inverter

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Abstract: The traditional Fixed Band Hysteresis Current Control (FB-HCC) though being widely used for the current control of grid integrated voltage source inverter (GI-VSI), has the drawback of variable switching frequency. To overcome this drawback, Complex Programmable Logic Device (CPLD) based switching scheme is proposed in this paper. The proposed method calls for a single reference wave and the control concept is to terminate the rising and falling inductor current (i_L) either by the comparator or by the CPLD, based on the nature of its slope. Termination of the i_L with steeper slope by the comparator ensures lower current ripple, whereas the CPLD ensures constant switching frequency (f_{sw}). However, the i_L obtained with the proposed logic has a DC offset, which is corrected by modifying the reference. The basic concept, switching logic, and reference correction are thoroughly detailed. MATLAB/Simulink results are included to verify the proposed concept. The constant frequency operation of the proposed method is also validated in a 2 kW, 230 V, 50 Hz GI-VSI prototype.

Keywords: complex programmable logic device; constant switching frequency; hysteresis current control; grid integrated voltage source inverter

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1. Introduction

Even as the economy sunk under the COVID-19 lock downs in 2020, renewable energy sources (RES) especially solar, continued to flourish and has been recognised as the most promising among the various RES [1]. Due to the volatility and incompatibility of the solar photovoltaic (SPV) power, additional circuits are necessary for its effective interface to the utility grid. Thus, an inverter plays a key role in interfacing as well as inverting the SPV power. The inverter can be of current source or voltage source. Voltage Source Inverter (VSI) is preferred to Current Source Inverter (CSI) in grid connection as the size, weight and cost of dc link capacitor are lower compared to the dc link inductor of comparable rating [2]. The VSI can be line-commutated or self-commutated. However, self-commutated switches are preferred in high frequency and grid applications, as the gate terminal has the complete control of the switch [3]. To ensure the stability and quality requirements of the power system, it is necessary to have the proper control of the inverter which can be voltage/current mode [4]. Current mode control is preferred in grid connection as it exhibits better transient response and results in improved power factor with simple control circuit [5]. The current control techniques can be linear or nonlinear; however, the nonlinear

controllers based on natural reference frame outperforms the linear controllers under dynamic conditions [6–8]. Furthermore, the pulse width modulators are not necessary for their operation. There are several nonlinear current controllers such as Sliding Mode Controller (SMC), Model Predictive contoller (MPC) and Fixed Band Hysteresis Current Controller (FB-HCC) developed in the past few decades. Reference [9] presents an SMC scheme for a single phase grid connected VSI, which exhibits excellent performance in terms of dynamic response, robustness and low THD. The proposed scheme reduces the wide variation in switching frequency, though it does not guarantee the constant switching frequency. An SMC with double band hysteresis scheme is proposed in [10], for a cascaded two-level inverter (CTLI) based grid connected/stand-alone photovoltaic (PV) system. Reference [11] proposes a digitally implemented SMC that runs at a fixed switching frequency. Here a hysteresis comparator realises the SMC, and the outer control loop regulates the switching frequency by modifying the hysteresis bandwidth. Model Predictive Control (MPC) is another control strategy proposed in [12] which uses a model-based system to predict the future behaviour of the variables over a time horizon. This method possesses features like fast dynamic response and easy inclusion of system constraints and nonlinearities [13]. However, it has drawbacks, such as variable switching frequency and high computational burden. A simplified Finite Control Set Model Predictive Controller (FCS-MPC) algorithm is proposed in [14] for power converters to reduce the computation time while maintaining the control performance. Additionally, another nonlinear current controller called Fixed Band Hysteresis Current Control (FB-HCC) is found in the literature because of its simplicity and easy implementation [15,16]. It also gives a fast response and has a natural peak current limiting capability [17]. However this controller exhibits uneven switching within a fundamental period and may result in device damage due to the excessive switching of the power devices. The filter design is also challenging as the harmonics are distributed throughout the fundamental period and these drawbacks reduce the acceptance of FB-HCC [18]. A control strategy which combines the benefits of HCC and SVPWM is proposed in [19]. The switching frequency is significantly reduced with this method, making it suitable for high power application.

Extensive work has been conducted by many researchers to overcome the drawback of variable switching frequency of a FB-HCC and one of the approaches is by using variable hysteresis band [20–25]. Reference [20] proposes an HCC with a modulated band to maintain the constant switching frequency. The implementation complexity of this method is high, as the hysteresis band width needs to be calculated for every switching cycle. A Phase Locked Loop (PLL) based programmable HCC is suggested in [21] to restrict the inverter switching at a fixed frequency; however, the transient performance of this controller is poor. In [22], a Sinusoidal Band-HCC is proposed in which the average and maximum switching frequencies are higher compared to traditional FB-HCC. Here a lockout circuit is mentioned to limit the switching frequency at the expense of increased current ripple and harmonic factor. An analog prediction of hysteresis band along with PLL control is proposed in [23] to ensure constant switching frequency. Reference [24] presents a computationally intensive approach in which the hysteresis band is calculated in real time for every switching period from the system state variables. Another notable work is the analog controlled constant switching frequency HCC of grid connected VSI without hysteresis band [25]. The analog controllers discussed in [20–25] have a fast transient response but have limitations such as (i) increased component count (ii) hardware complexity and (iii) need of circuit modification in case of controller reconfiguration [26]. Also, the constant switching frequency operation of the inverter is not guaranteed in [20], when it is working under the influence of noise and disturbance [27].

A Digital HCC (DHCC) with constant switching frequency is proposed in [28] where the sampling period is adjusted online. The digital controllers outperform the analog controllers in the real time implementation of the advanced control algorithms. However, the performance of the digital controllers depend greatly on the sampling/switching frequency and it requires high speed microcontroller for the realization [29]. The digital

controllers with low sampling frequency will have low switching frequency, resulting in higher current ripple and Total Harmonic Distortion (THD). The problem of higher THD while using digital controllers can be resolved by using advanced controllers such as Field Programmable Gate Array (FPGA)/Complex Programmable Logic Devices (CPLD) with a higher sampling frequency [30–34]. Table 1 compares the proposed method with advanced control strategies like SMC and MPC. [13].

Table 1. Comparison of advanced control strategies with the proposed method.

MPC	SMC	QFFHCC
(1) Non-linear controller (2) No modulation needed (3) Handle system constraints in an intuitive way (4) Can include non-conventional control objectives	(1) Robustness to parameter variations (2) Fast transient response (3) Reduction in system order	(1) Non-linear controller (2) Easy to implement (3) No modulators are used (4) Very fast transient response (5) Robust (6) Offers fixed switching frequency (7) Works well with advanced controllers like FPGA/CPLD
(1) Variable switching frequency (2) High computational burden	(1) Chattering effect (2) Variable switching frequency	(1) Performance depends on the controller used (2) Current feedback is needed

This paper proposes a CPLD based control strategy for the Quasi Fixed Frequency Hysteresis Current Control (QFFHCC) of a single phase full bridge GI-VSI.The proposed method does not compute switching time; instead, it uses event-based switching. The digital controller can eliminate the noise caused by analogue implementation [30,35]. The unique feature of the proposed control method is its single reference wave without any hysteresis band. Here the fixed switching frequency operation is achieved by partially relaxing the upper/lower bounds of the FB-HCC.

Following this section, the principle of operation, switching logic and the flowchart are described in Section 2, along with the reference correction. Section 3 discusses the simulation results, while the experimental verification of the proposed method is discussed in Section 4. Finally, Section 5 summarizes the result drawn.

2. Principle of Operation

Figure 1 shows the schematic of GI-VSI, where the CPLD dictates the switching scheme based on the half cycle information (P) and the comparator output (C).

The conventional FB-HCC has two physical bands to limit the i_L, whereas the proposed method uses only a single reference wave ($i_L{}^*$) without any hysteresis band. The phase-locked loop (PLL) implemented using the microcontroller, senses the grid voltage (v_g) and generates the synchronized $i_L{}^*$ and the P. The control concept is to terminate the rising and falling i_L either by the comparator or by the CPLD, based on the nature of its slope. In either half cycle, the comparator terminates the i_L with a steeper slope, whereas the CPLD controls the other. The switching states $S+$ and $S-$ during the positive half cycle ($P = 1$) of v_g are given in Figure 2a,b, respectively. The state $S+$ refers to the ON state of S_1, S_4 and the OFF state of S_2, S_3. Similarly, the OFF state of S_1, S_4 and the ON state of S_2, S_3 is referred as $S-$.

The slope of i_L during the $S+$ state can be expressed as

$$\left(\frac{\mathrm{d}i_L}{\mathrm{d}t}\right)_{rise} = \frac{V_{dc} - v_g}{L} \tag{1}$$

whereas the slope of i_L in the $S-$ state is given by

$$\left(\frac{\mathrm{d}i_L}{\mathrm{d}t}\right)_{fall} = -\left(\frac{V_{dc} + v_g}{L}\right) \tag{2}$$

where V_{dc} is the supply voltage and L is the inductance.

From (1) and (2), it is clear that the slope of i_L is relatively steep during the $S-$ state compared to the $S+$ state in the positive half cycle. During the negative half cycle ($P = 0$), the nature of the i_L slope is different, wherein it is steeper during the $S+$ state compared to the $S-$ state, as v_g is negative.

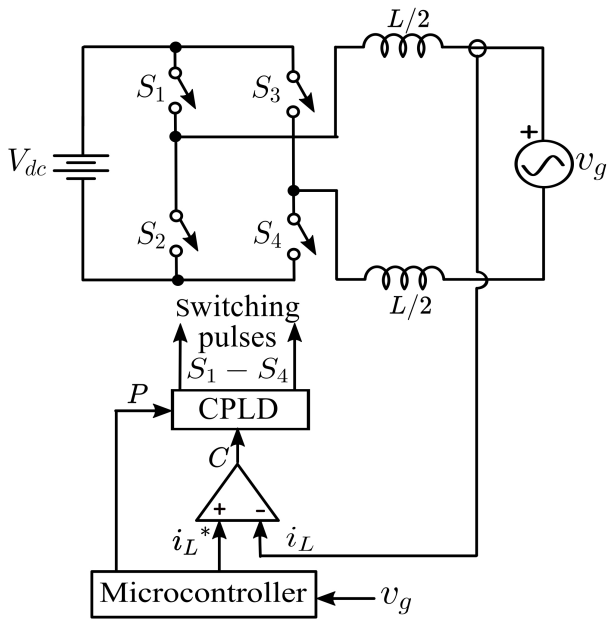


Figure 1. Schematic of the single phase full bridge grid integrated inverter with the proposed logic.

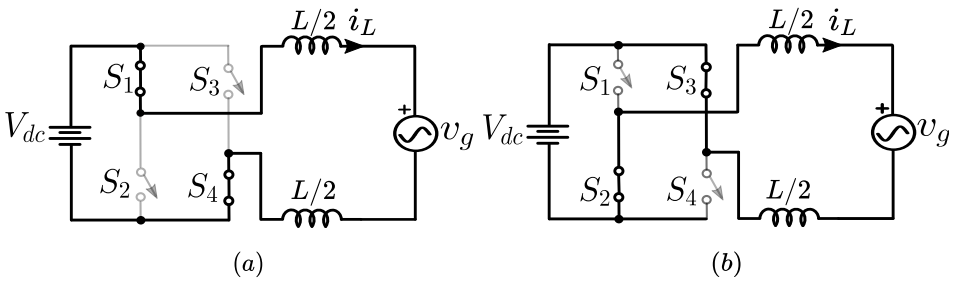


Figure 2. The switching states (**a**) $S+$ and (**b**) $S-$ during the positive half cycle.

2.1. Switching Logic

Figure 3 illustrates the nature of i_L over a switching cycle with the proposed logic.

2.1.1. Positive Half Cycle

Figure 3a demonstrates the nature of i_L for the $S+$ and $S-$ states during positive half cycle. As the slope of i_L is comparatively steeper during the $S-$ state, it is regulated by the comparator. The CPLD regulates the $S+$ state by ensuring a time period of 50 µs between two consecutive $S-$ states. The termination of the i_L with a steeper slope by the comparator offers lower current ripple, whereas the CPLD ensures constant switching frequency (f_{sw}) of 20 kHz. The peak to peak inductor current ripple (Δi_{Lpp}) during the positive half cycle is calculated using the instant t_2, where the difference between i_L and ${i_L}^*$ is maximum over a switching cycle.

Hence at t_2,

$$\Delta i_{Lpp} = i_L(t_2) - {i_L}^* \tag{3}$$

However,

$$i_L(t_2) = i_L(t_1) + \left(\frac{V_{dc} - v_g}{L}\right) t_{on(n)} \tag{4}$$

Also, $i_L = {i_L}^*$ at t_1.

By substituting (4) in (3) and rearranging, the Δi_{Lpp} during the state $S+$ can be obtained as

$$\Delta i_{Lpp} = \left(\frac{V_{dc} - v_g}{L}\right) t_{on(n)} \tag{5}$$

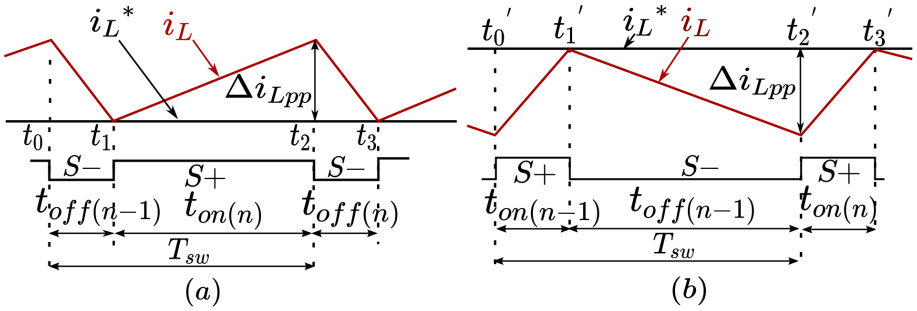


Figure 3. Sketch of inductor current over a switching cycle (**a**) Positive Half Cycle. (**b**) Negative Half Cycle.

Similarly, the Δi_{Lpp} in the $S-$ state can be expressed as

$$\Delta i_{Lpp} = \left(\frac{V_{dc} + v_g}{L}\right) t_{off(n)} \tag{6}$$

By combining (5) and (6), the expression for the Δi_{Lpp} over a switching period during the positive half cycle can be obtained as

$$\Delta i_{Lpp} = \frac{{V_{dc}}^2 - {v_g}^2}{2 f_{sw} L V_{dc}} \tag{7}$$

where $f_{sw} = 1/T_{sw}$

2.1.2. Negative Half Cycle

Figure 3b depicts the activation logic of $S+$ and $S-$ states in the negative half cycle, wherein the state is changed to $S-$ on a negative edge at the comparator output and the CPLD activates the state $S+$. Here the 50 µs period separates the two adjacent $S+$ states with the ${i_L}^*$ acting as the upper boundary. The expression for the peak to peak i_L in the negative half cycle remains the same as that of the positive half cycle.

Figure 4 depicts the flow chart of the proposed logic, where the f_{sw} is limited to 20 kHz.

2.2. Reference Correction

The current injected into the grid must be sinusoidal and should be in phase with v_g to ensure unity power factor. To achieve this, the i_L must be distributed evenly on either side of the ${i_L}^*$. It is observed in Figure 3a that the i_L lies above the ${i_L}^*$ during the positive half cycle with its lower peaks touching the ${i_L}^*$ and thus resulting a positive DC offset. During the negative half cycle, the i_L is below the ${i_L}^*$, with the upper peaks of the i_L touching the ${i_L}^*$ and thereby leading to a negative DC offset. These DC offsets in either half cycle cause distortion in the i_L as shown in Figure 5.

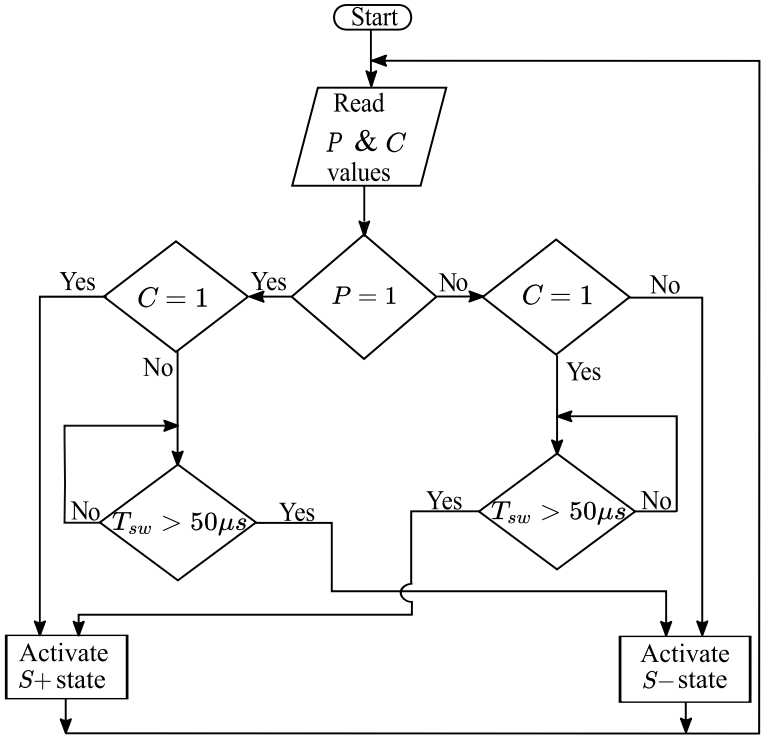


Figure 4. Flowchart of the proposed logic implemented in CPLD.

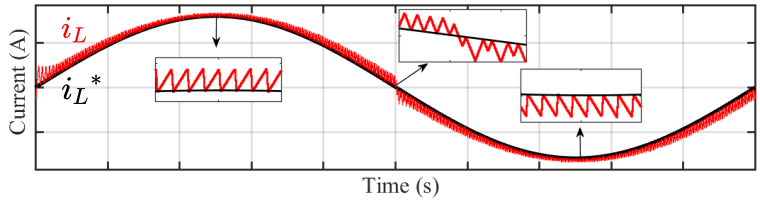


Figure 5. Sketch of inductor current over a line cycle with the sinusoidal reference current.

To correct this DC offset in either half cycle, the $i_L{}^*$ is corrected by (8) and (9).

$$i_{Lnew}^{*}+ = i_L{}^* - k \tag{8}$$

$$i_{Lnew}^{*}- = i_L{}^* + k \tag{9}$$

where $i_{Lnew}^{*}+$ and $i_{Lnew}^{*}-$ represent the positive and negative half cycles of the corrected reference (i_{Lnew}^{*}) and k is the offset correction factor.

Figure 6 demonstrates the DC offset correction over a switching cycle by correcting the reference as i_{Lnew}^{*}. It is seen that the i_L is evenly dispersed on either side of the $i_L{}^*$, after the correction. Figure 7a depicts the distorted current obtained with the sinusoidal reference shown in Figure 7a. The corrected reference and the sinusoidal current thus obtained are shown in Figure 7b, respectively.

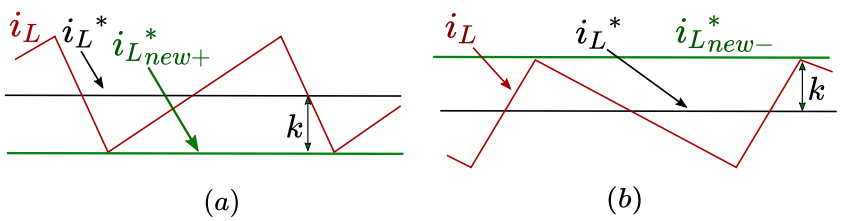


Figure 6. Pictorial representation of reference correction over a switching cycle (**a**) Positive half cycle. (**b**) Negative half cycle.

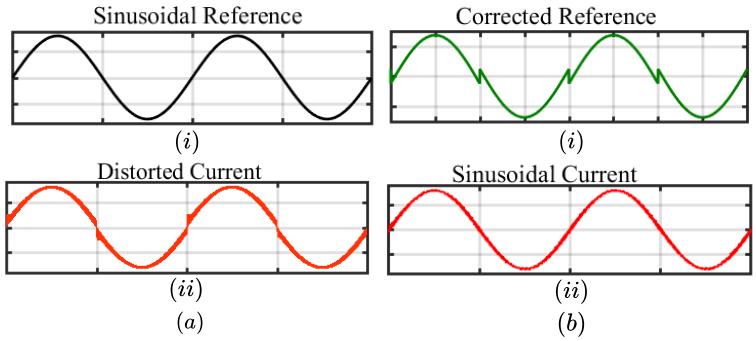


Figure 7. Sketch of inductor current over a line cycle with (**a**) Sinusoidal reference. (**b**) Corrected reference.

The amplitude of Δi_{Lpp} obtained by (7) is not the same throughout the line cycle, but varies with v_g as shown in Figure 8, where it is highest at zero-crossing of v_g and the lowest at v_g peak.

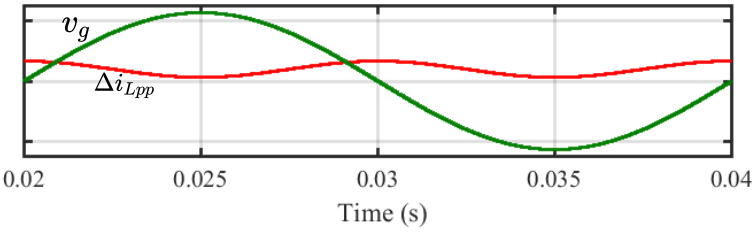


Figure 8. Variation in the amplitude of the inductor current ripple with the grid voltage.

Hence, the k needed to correct the offset also varies and is half the current ripple at that instant $\left(k = \dfrac{\Delta i_{Lpp}}{2}\right)$.

From (7), the expression for the maximum amplitude of Δi_{Lpp} is

$$\Delta i_{Lpp_{max}} = \left(\frac{V_{dc}}{2 f_{sw} L}\right) \tag{10}$$

The correction factor (k) corresponding to the maximum current ripple is

$$\left(\frac{\Delta i_{Lpp_{max}}}{2}\right) = \left(\frac{V_{dc}}{4 f_{sw} L}\right) \tag{11}$$

The $i_L{}^*$ is modified by (12) and (13), for the fixed offset correction of maximum current ripple as,

$$i_{L_{new}}^{*} += i_L{}^* - \left(\frac{\Delta i_{Lpp_{max}}}{2}\right) \tag{12}$$

$$i_{L_{new}}^{*} -= i_L{}^* + \left(\frac{\Delta i_{Lpp_{max}}}{2}\right) \tag{13}$$

Figure 9 shows the $i_L{}^*$ and the reference corrected $\left(i_{L_{new}}^{*}\right)$ by (12) and (13). The i_L waveform over a line cycle with the reference corrected by a fixed offset is given in Figure 10.

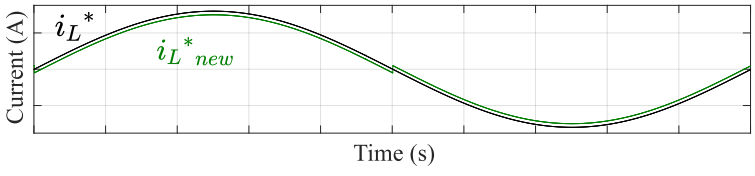


Figure 9. Sinusoidal reference and the reference corrected by fixed offset.

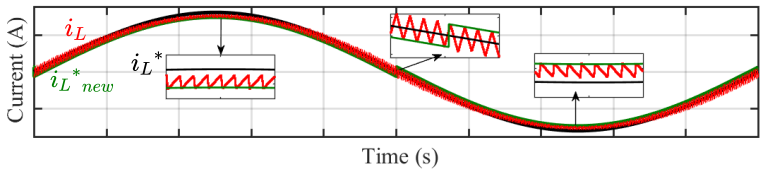


Figure 10. Inductor current obtained with the fixed offset corrected reference.

The DC offset is corrected at the zero crossing while it is over-corrected at other points in the waveform. Hence, to remove the DC offset completely and to improve the i_L waveform further, the $i_L{}^*$ is modified by a variable offset given by Equations (14) and (15).

$$i_{Lnew}^{*}+ = i_L{}^* - \left(\frac{\Delta i_{Lpp}}{2}\right) \tag{14}$$

$$i_{Lnew}^{*}- = i_L{}^* + \left(\frac{\Delta i_{Lpp}}{2}\right) \tag{15}$$

where $\frac{\Delta i_{Lpp}}{2} = \frac{V_{dc}{}^2 - v_g{}^2}{4 f_{sw} L V_{dc}}$, is the DC offset correction factor used for variable offset correction.

The sinusoidal $i_L{}^*$ and the reference corrected by (14) and (15) is given in Figure 11, while Figure 12 shows the i_L waveform obtained with the variable offset corrected reference. As observed in Figure 12, the i_L is distributed on either side of the $i_L{}^*$, and thus the DC offset is corrected completely.

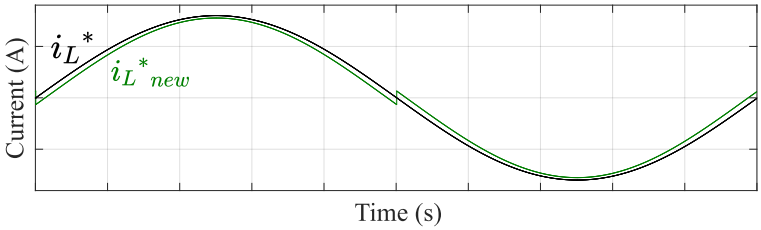


Figure 11. Sketch of sinusoidal reference and the reference corrected by variable offset.

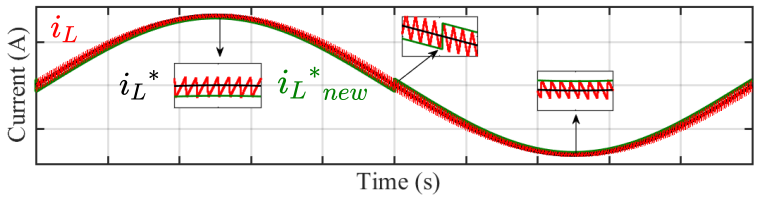


Figure 12. Sketch of Inductor current obtained with the variable offset corrected reference.

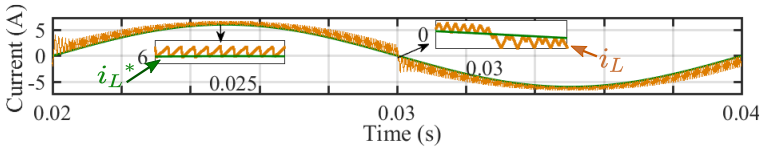
3. Simulation Results

Table 2 lists the system parameters used in the MATLAB simulation for the implementation of the proposed logic.

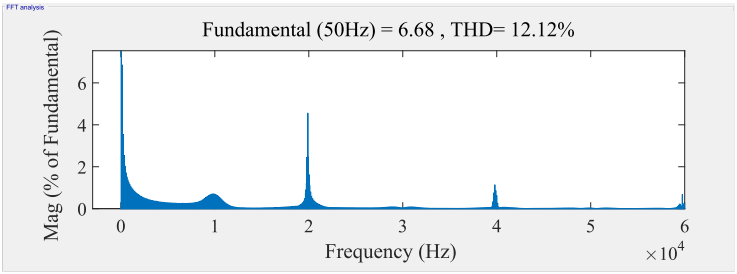
Table 2. System Parameters.

Parameter	Value
V_{dc}	400 V
f_o	50 Hz
$v_{g_{rms}}$	230 V
f_{sw}	20 kHz
L	5 mH
$i_L{}^*{}_{peak}$	6 A

Figure 13a shows the i_L waveform obtained with sinusoidal $i_L{}^*$, where the i_L tracks the $i_L{}^*$ well. However there is a DC offset as discussed in Section 2.2. The THD is 12.12% as shown in Figure 13b, which is more than the permissible limit of 5% as per IEEE 519, IEEE 1547, and IEC 61727 [36–39]. The following section discusses the methods to correct the DC offset and improve the THD.



(*a*)



(*b*)

Figure 13. (**a**) Inductor current waveform obtained with the Sinusoidal reference. (**b**) Frequency spectrum of inductor current obtained with the Sinusoidal reference.

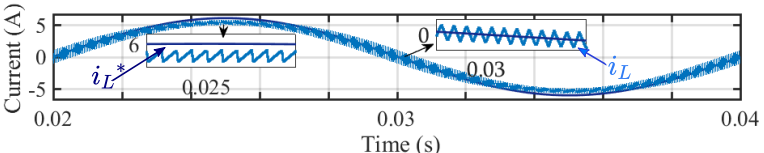
3.1. Methods to Correct the DC Offset and Curb the THD

3.1.1. Modifying the Reference Current

The $i_L{}^*$ is modified by various offset correction factors (k) as given below.

- Fixed offset

  The $i_L{}^*$ is modified by the k, equivalent to half the maximum amplitude of inductor current ripple $\left(\frac{\Delta i_{Lpp_{max}}}{2}\right)$ given by (11) and the resulting waveform is in Figure 14a. Here the distortion at the zero-crossing is corrected completely, while the rest of the quarter-wave is over-corrected as observed in the zoomed view of the positive peak shown in Figure 14a. The THD is within the limit as shown in Figure 14b. To remove the DC offset error completely, a variable offset correction is suggested.



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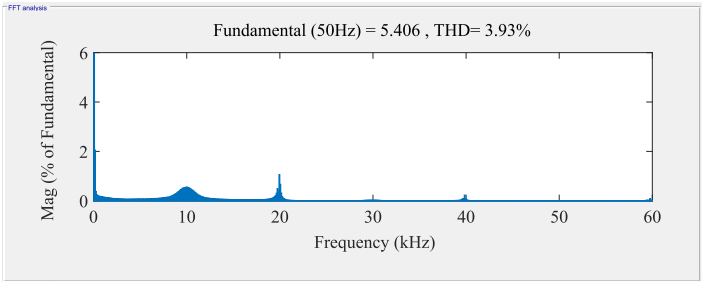

(*b*)

Figure 14. (**a**) Inductor current waveform obtained with fixed offset correction ($k = \frac{\Delta i_{Lpp_{max}}}{2}$). (**b**) Frequency spectrum of inductor current obtained with fixed offset correction.

- Variable Offset
  For a given condition, the Δi_{Lpp} in (7) varies with the instantaneous values of v_g while the other parameters are kept constant. Hence, the k needed to correct the offset also varies and is half the current ripple at any instant ($k = \Delta i_{Lpp}/2$). Figure 15a shows the i_L waveform corrected by the variable offset, and its frequency spectrum is given in Figure 15b. It shows that the DC offset error is corrected completely and the THD is improved even further.

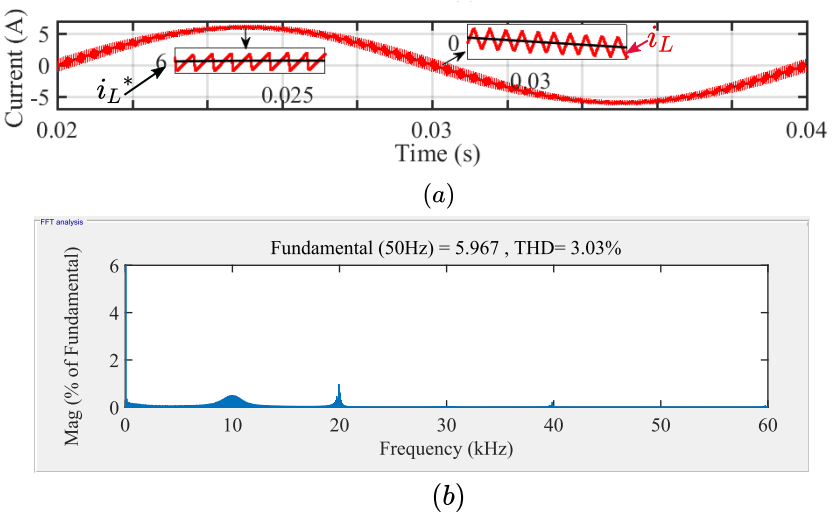

Figure 15. (**a**) Inductor current waveform obtained with variable offset correction ($k = \frac{\Delta i_{Lpp}}{2}$). (**b**) Frequency spectrum of inductor current obtained with variable offset correction.

3.1.2. Increasing the Inductance

Alternatively, the THD can be improved by increasing the inductance (L) without modifying the reference. Figure 16 shows the plot of THD vs L obtained by simulating the proposed logic with the sinusoidal $i_L{}^*$ for various L values. It shows that the THD of 12.12% with the sinusoidal $i_L{}^*$ is reduced to 5% by increasing the L from 5 mH to 13 mH at the expense of increased size and cost of the inductor.

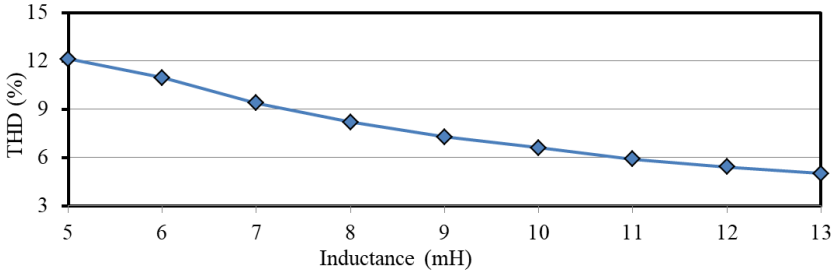

Figure 16. THD vs. Inductance plot.

3.2. Sensitivity Analysis

Variation in the amplitude of Δi_{Lpp} with the supply voltage is analyzed here. Figure 17a shows the step rise in the V_{dc} from 400 to 460 V at 0.023 s. The response of inductor current is shown in Figure 17b while its zoomed view is given in Figure 17c. It is observed that the amplitude of Δi_{Lpp} rises instantaneously with the step rise in supply voltage; however, the switching frequency remains unchanged as indicated by the cursor values shown in Figure 17c.

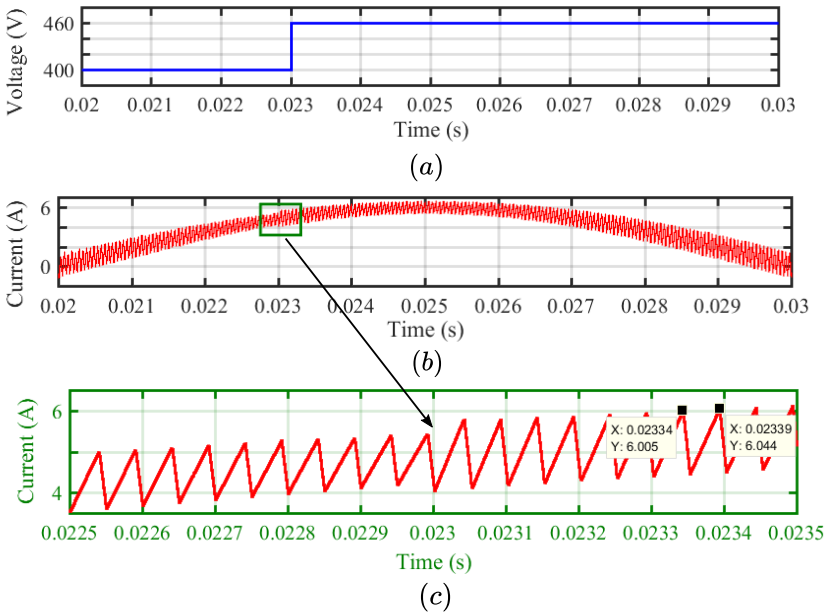

Figure 17. (**a**) Step rise in the supply voltage. (**b**) Inductor current waveform over a half cycle. (**c**) Inductor current waveform zoomed around the step change.

3.3. Switching Frequency Analysis

To compare the switching frequency variation in the case of FB-HCC and QFFHCC, both are simulated using the parameters given in Table 2. The QFFHCC method used the variable offset corrected $i_L{}^*$ and the hysteresis band used in the FB-HCC is equivalent to the average current ripple. Figure 18 shows the switching frequency variation in either case; where it varies between 17.8 kHz and 22.2 kHz in the FB-HCC, while the QFFHCC maintains the switching frequency constant at 20 kHz.

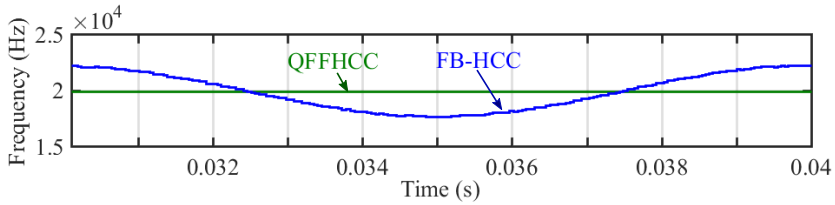

Figure 18. Comparison of switching frequencies in the case of FB-HCC and the QFFHCC.

3.4. Transient Behavior

The FB-HCC and the QFFHCC are simulated using the parameters given in the Table 2, to analyse the transient response. A step change of $1A$ is given to the $i_L{}^*$ to compare the transient response of QFFHCC with the FB-HCC, where the proposed system used the $i_L{}^*$ modified with the variable offset. As depicted in Figure 19, the transient response of QFFHCC is equally good as that of the FB-HCC.

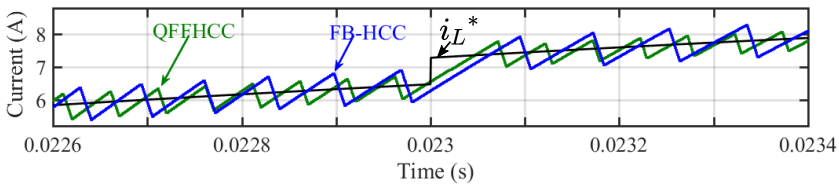

Figure 19. Comparison of transient response in the case of FB-HCC and the QFFHCC.

3.5. Comparison with a Similar Control Scheme

To check the superiority of the proposed method, it is compared with a similar work mentioned in [28] that implements the hysteresis current control without band and with

constant switching frequency. The simulation parameters used to simulate the proposed system are the same as that given in [28] and below are the results. The Figure 20a shows the steady state inductor current waveform where the inductor current tracks the reference well. The frequency spectrum is shown in Figure 20b, where the spectrum is concentrated around 10 kHz. The constant switching frequency operation is thus guaranteed. Further, the THD observed is 4.51% which is within limits. The dynamic performance of the proposed method is analyzed by stepping the reference current from 10 A to 20 A, as in [28] and the result in Figure 20c shows that the proposed method exhibits excellent dynamic behaviour.

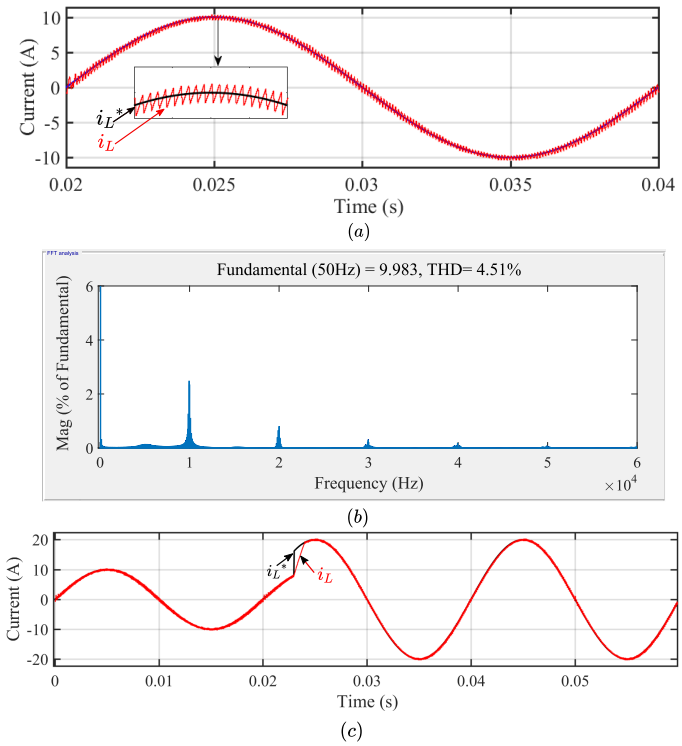

Figure 20. Waveforms obtained by simulating the proposed method with the parameters in [28]. (**a**) Steady state performance of the proposed method. (**b**) Frequency spectrum. (**c**) Dynamic response.

4. Experimental Verification

Figure 21 shows the experimental set up for validating the proposed control logic implemented in a 2 kW GI-VSI. The system parameters used for the experimental purpose are the same as that used in the MATLAB simulation. The PCB of the power circuit is designed using Altium Designer 17. It comprises four Field Stop (FS) Trench IGBTs (FGH60T65SQD) driven by optically isolated gate driver. The FS IGBT offers superior performance in switching applications with low on state voltage drop ($V_{CE(sat)}$ = 1.6 V) and minimal switching loss (E_{ts} = 327 µJ). A high precision, galvanically isolated current sensor (SI8920AC–IP) is used to feedback the i_L and an external comparator is used to compare the $i_L{}^*$ and i_L. The proposed control logic is implemented on a XC9536 CPLD with advanced CMOS 5 V Fast FLASH technology. The XC9536 is a high-performance CPLD providing advanced in-system programming and test capabilities for general purpose logic integration. It comprises eight 36V18 Function Blocks, providing 800 usable gates with propagation delays of 5 ns. The CPLD dictates the switching scheme based on the nature of the i_L slope.

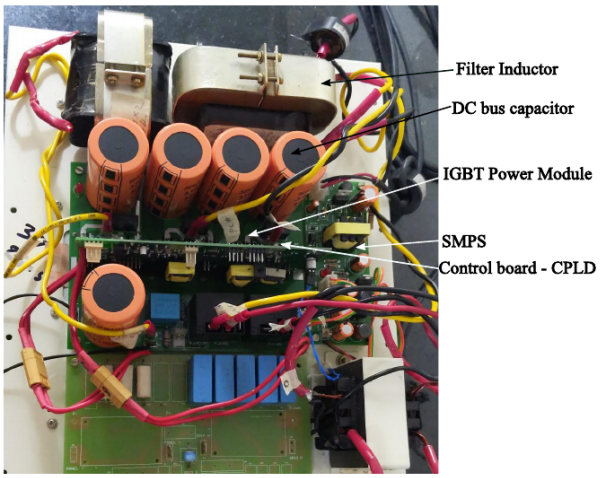

Figure 21. Experimental set up: 2 kW GI-VSI prototype.

Figure 22a depicts the i_L waveform for a sinusoidal $i_L{}^*$. The waveform has a DC offset throughout the line cycle as observed in Figure 13a. Figure 22b shows the i_L waveform obtained when the $i_L{}^*$ is modified by a correction factor which is more than the required value. To improve the i_L waveform obtained in Figure 22a,b, the $i_L{}^*$ is modified by the fixed offset of $\left(\frac{\Delta i_{Lpp_{max}}}{2}\right)$ as discussed in the Section 2.2 and the result is furnished in Figure 23. It shows that the DC offset error is corrected and the sinusoidal i_L waveform, in phase with the v_g, is delivered to the grid at 0.5 kW, 1 kW and 1.5 kW of power as shown in Figure 23a–c respectively.

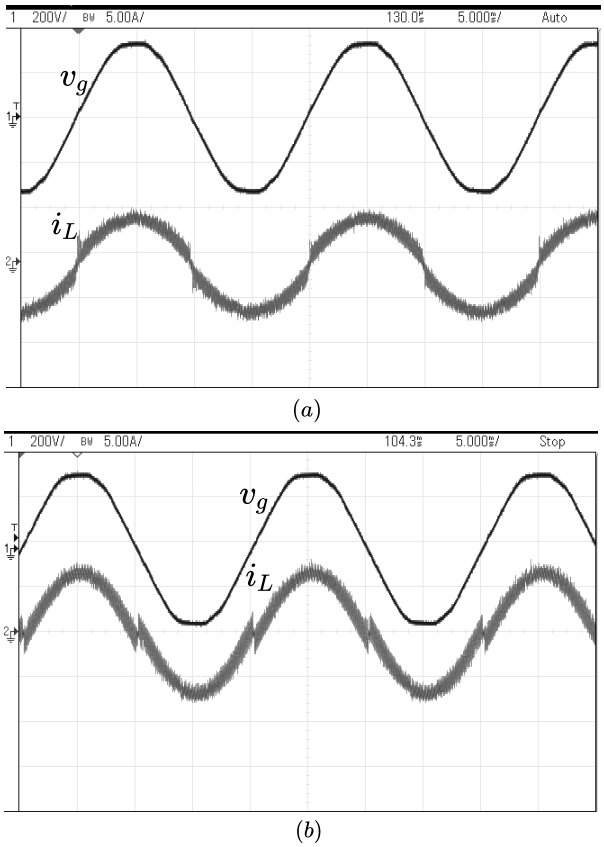

Figure 22. Inductor current obtained with (**a**) Sinusoidal $i_L{}^*$ (**b**) Over-corrected $i_L{}^*$.

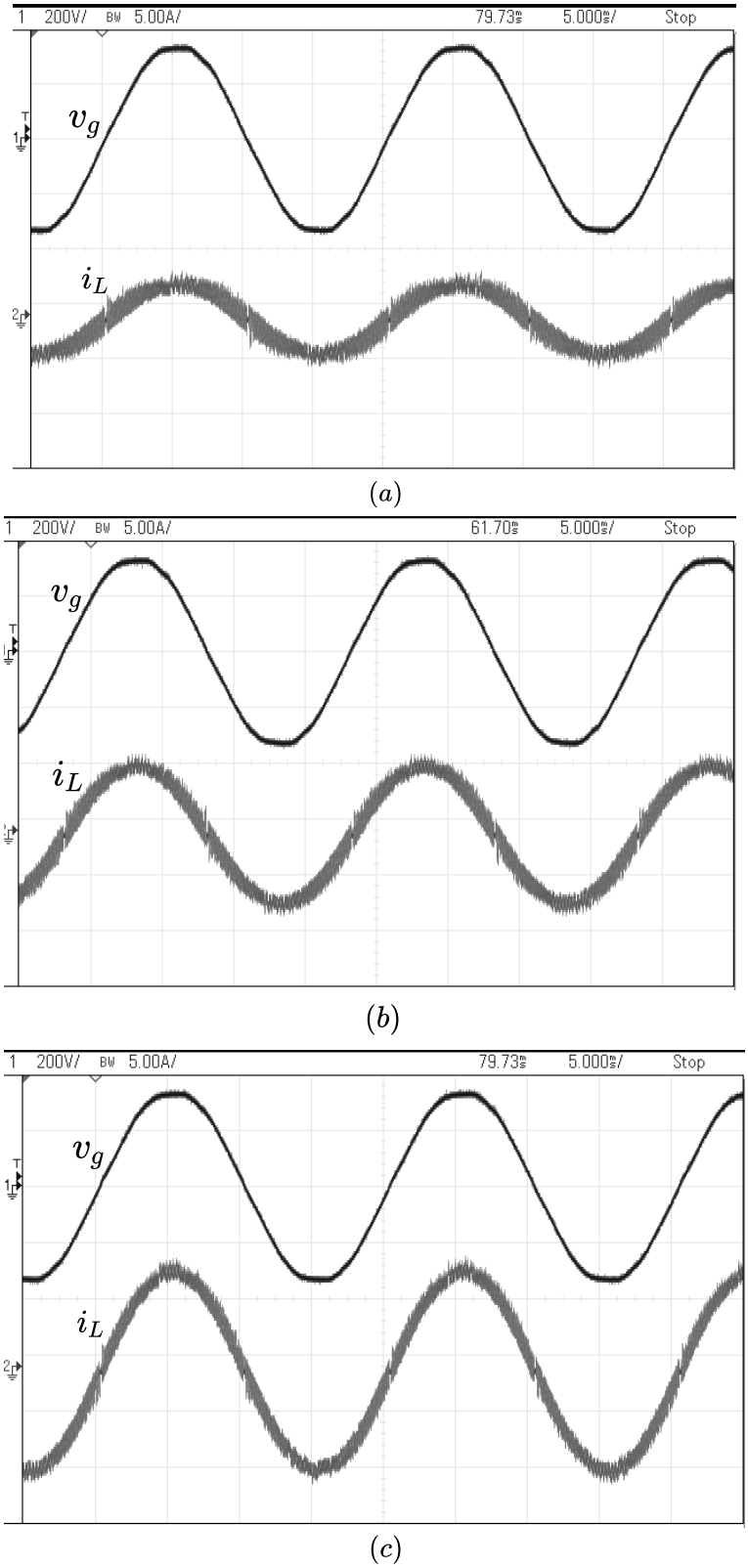

Figure 23. Synchronised operation of single phase GI-VSI delivering (**a**) 0.5 kW (**b**) 1 kW (**c**) 1.5 kW.

Figure 24 shows the zoomed view of Figure 23b over a switching cycle scale, where the i_L maintains the T_{sw} of 50 µs, ensuring a constant f_{sw} of 20 kHz. Figure 25 shows a THD of 4.04% for the i_L waveform corresponding to the Figure 23b, which is acceptable as per the standards.

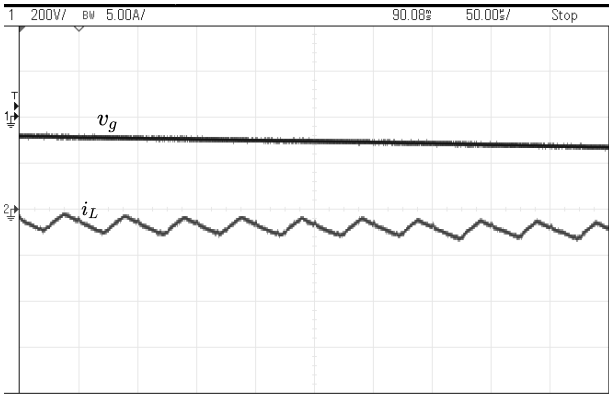

Figure 24. Zoomed view of inductor current.

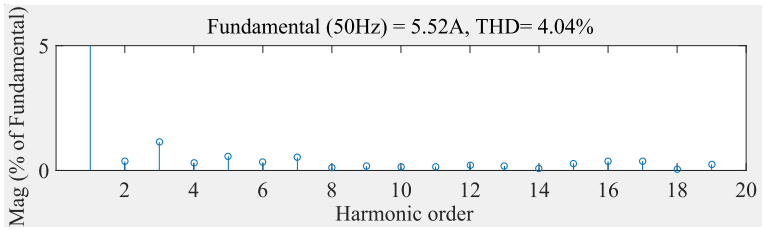

Figure 25. Harmonic spectrum of inductor current for the proposed method.

5. Conclusions

This paper proposes a fixed switching frequency current control strategy for a single phase full bridge GI-VSI. The proposed method ensures fixed switching frequency while retaining the benefits of conventional FB-HCC. The proposed QFFHCC method is analysed in MATLAB/Simulink. Further, its switching frequency and transient responses are compared with the conventional FB-HCC to prove its effectiveness. A 2 kW, 230 V, 50 Hz GI-VSI prototype is used for the experimental validation. The transient response of QFFHCC is similar to that of the FB-HCC, with a response time of 50 µs. A fixed offset correction yields an experimental THD of 4.04%, which can be further enhanced using a variable offset correction. Future scope of the proposed work is to implement the QFFHCC in a three phase grid connected system and analyse its response to the grid faults.

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