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# Design Space Analysis of the Dual-Active-Bridge Converter for More Electric Aircraft

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**Abstract:** In the literature, different DC/DC power electronic converters (PECs) have been found to interconnect high-voltage DC and low-voltage DC grids in the electric power distribution networks of aircraft. In this scenario, the dual-active-bridge (DAB) converter has been shown to be one of the most promising topologies. The main disadvantages of this PEC are the large output capacitance required to satisfy more electric aircraft (MEA) requirements and the high conduction losses produced in low-voltage power devices of (LV). Therefore, this paper proposes analytical models to determine the voltage ripple and root-mean-square (RMS) current in DC bus capacitors of DABs considering different modulation strategies. Moreover, an analysis of the design space in an MEA case study is performed to evaluate the influence of the design variables in power losses of power devices and peak-to-peak voltage ripple in DC bus capacitors. These models are useful for the design stage of this PEC, as well as to enable multi-objective optimization procedures by reducing the computational cost of these methodologies. Furthermore, the exploration of the switching frequency and limit of the modulation angle aid in reducing the resulting volume of the low-voltage DC capacitor.

**Keywords:** dual active bridge; bidirectional DC/DC power conversion; design space analysis; more electric aircraft

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## 1. Introduction

Currently, there is an increasing interest in the electrification of aircraft. The emergence of electrically supplied actuators and energy storage systems (ESS) provides the chance to develop aircraft with higher electrical power [1], which has been shown to be more efficient than traditional hydraulic, pneumatic, and mechanic systems. This increment in the electrical power installed onboard the aircraft leads to benefits in terms of efficiency and emissions when compared to the existing solutions. Therefore, different electric power distribution systems have been proposed for more electric aircraft (MEA) [2,3]. The most important parameters when considering MEA applications are efficiency, volume, and weight of the power-electronic converter (PEC) to achieve a system with high power density. In order to achieve an optimized design, every element in the PEC has to be considered, from the PEC topology to the modulation strategy, the power semiconductors, the cooling system, and/or the passive components. The large number of variables to be considered make the optimization process complex.

In the different power distribution systems proposed for MEA, isolated bidirectional DC/DC PECs are usually employed to interface high-voltage DC (HVDC) and low-voltage DC (LVDC) buses for ESS [4–7]. In this context, the dual-active-bridge (DAB) converter is one of the most promising PEC topologies. This converter, first presented in [8], has been widely studied in the literature for many applications, such as automotive [9], traction [10], and/or aircraft electrification [11]. DAB has been characterized by different modulation methods [12], as well as the utilization of wide bandgap power devices when considering MEA applications [13,14]. Furthermore, combined modulation strategies to

ensure zero-voltage switching (ZVS) in wide input and output voltage range applications [15], modulation strategies for a reduction in the conduction losses [16], and design methodologies for improving DAB performance [17] have been analyzed in detail.

However, the main disadvantage of the DAB converter found in the literature is the large LVDC capacitance needed to satisfy the strict MEA voltage ripple requirement [18]. Due to this fact, alternative topologies, i.e., the active-bridge-active-clamp converter, have been proposed in the literature in order to solve this issue. Nevertheless, this topology includes a large number of passive components in comparison to DAB, which affects the reliability of the system. Therefore, an exhaustive modeling of DAB LVDC capacitors is attached in this work to reduce the impact of this component on the converter volume. In this context, the design of the DAB LVDC is challenging due to the high circulating currents, which cause high conduction losses in the capacitors, transformer, and power devices. The optimization of these components is particularly interesting due to its impact on power losses, volume, and weight, which define the gravimetric and volumetric power density of the designed power converter [19].

To solve this issue, analytical modeling to determine voltage and current stress in PEC components is essential. These models have been proposed for the power devices of DAB converters considering different modulation methods [20–22], which are useful for exploring the design space of these components. The analysis of the design space has been widely utilized in the literature to optimize the power density of magnetic components, such as inductors [23] and/or power transformers [24], improving the resulting efficiency of these components. Moreover, many optimization routines are found for DAB based topologies in different applications [25,26].

However, an analysis of the design trade-offs of converter performance with other factors such as selected switching frequency, decoupling inductance, and/or DC bus capacitance in MEA applications has not been conducted. In this paper, analytical models of RMS current stress and voltage ripple in HVDC and LVDC bus capacitors of DAB converter are proposed. Then, the analytical models of the power devices and capacitances are combined to develop a design space analysis of these components, aiming to find the design trade-offs in the converter design. These analytical models are of huge importance because they imply a reduction in the computational cost and are applicable to different application proposals. A defined design space is employed to analyze the impact of the design variables on the resulting RMS current stress, voltage ripple, power losses, volume and weight of the power devices, heatsink, and/or DC-link bus capacitors. Furthermore, the presented equations can be utilized for design of the DAB converter considering different specifications and application purposes. A deep insight regarding the main contributions found in the literature and principal differences with this work is provided in Table 1.

This paper is structured as follows. In Section 2, a general description of the DAB converter is presented, together with the main modulation methods of this PEC. Moreover, the analytical analysis to determine the RMS current stress and voltage ripple in DC bus capacitors is described, and the resulting equations are included in the Appendix A of this work. Then, an analysis of the converter design space is performed in Section 3, where the impact of the switching frequency, limit of the modulation angle, and DC-link bus capacitance on the converter efficiency and voltage ripple on DC-link bus capacitors are presented. Finally, the main conclusions of this work are gathered in Section 4.

**Table 1.** Summary of literature contributions for DAB converter.

| Ref. | Contribution | Weakness |
|---|---|---|
| [7] | Multiport DAB converter for aircraft ESS focusing on its control. | TPS modulations. |
| [9] | Efficiency optimized DAB considering alternative modulation methods for automotive applications. | Conventional modulations. |
| [12–14] | Analysis of wide-bandgap power devices, i.e., SiC, in MEA applications. | Analytical models. |
| [15] | ZVS of DAB converter in wide input and output voltage applications. | LV and high-current DAB. |
| [16] | Control of DAB converter to minimize conduction losses. | Design procedure. |
| [17] | Efficiency optimization of DAB converter by enhancing the ZVS operation of the converter. | TPS modulations. |
| [20] | Analytical modeling of power devices considering the main modulation methods of DAB. | Control algorithm. |
| [21,22] | Analytical modeling and design of DAB converter considering SPS rectangular and EPS modulation for MEA applications. | TPS modulations. |
| This work | Analytical modeling and design space analysis of DAB converter considering the principal modulation methods for MEA applications. | Control algorithm. |

## 2. Dual-Active-Bridge Converter

A DAB converter schematic is shown in Figure 1. It is formed by two full-bridge inverter and/or rectifier stages interconnected through a power transformer. This PEC is modulated by shifting the angles between the nodes A–C ($\delta$), A–B ($\Omega_1$), and C–D ($\Omega_2$). Depending on the number of angles shifted, single-phase shift (SPS), double-phase shift, and triple-phase shift (TPS) modulation strategies can be distinguished. These strategies are commonly utilized to obtain a desired current waveform through transformer windings. In this work, SPS and TPS strategies are considered. SPS modulation is considered due to its simple and robust implementation, while TPS modulations are considered due to their improved performance, as reported in the literature.

The main current and voltage waveforms with the different modulations are presented in Figure 2. HV ($I_{\mathrm{HV}}$) and LV ($I_{\mathrm{LV}}$) currents in DC buses are described in (1):

$$I_{\mathrm{HV}} = \frac{P}{V_{\mathrm{HV}}} \ , \ I_{\mathrm{LV}} = \frac{P}{V_{\mathrm{LV}}} \ , \tag{1}$$

where $P$ is the power transferred by the converter, and $V_{\mathrm{HV}}$ and $V_{\mathrm{LV}}$ are the voltages of the HVDC and LVDC buses.

To determine the analytical models of RMS current and voltage ripple in input and output capacitors, Kirchhoff's current law is applied in the positive terminal of these components. Considering HV to LV power transfer, full-bridge inverter and rectifier stages inputs ($i_{\mathrm{in}}$) and outputs ($i_{\mathrm{out}}$), currents can be defined. Then, the corresponding definition of RMS current and voltage ripple in the input DC-link capacitor are presented in (2) and (3):

$$I_{\mathrm{C_{HV(RMS)}}} = \sqrt{\frac{2}{T_{\mathrm{SW}}} \int_0^{T_{\mathrm{SW}}/2} \left(I_{\mathrm{HV}} - i_{\mathrm{in}}\right)^2 dt} \ , \tag{2}$$

$$\Delta V_{\mathrm{C_{HV(pk-pk)}}} = \frac{\int_0^{T_{\mathrm{Charge}}} \left(I_{\mathrm{HV}} - i_{\mathrm{in}}\right) dt}{C_{\mathrm{HV}}} \ . \tag{3}$$

In (3), the definite integral of the current during the charging time ($T_{\mathrm{charge}}$) is the charge stored in the capacitor, often defined as the product of the voltage across the capacitor and capacitance. By solving these integrals, the analytical models presented in the Appendix A of this work are obtained for input capacitor. This procedure is also carried out for output

capacitor. In the following subsections, SPS rectangular, TPS trapezoidal (TPS-TPM) and TPS triangular (TPS-TRM) modulations are described in depth.

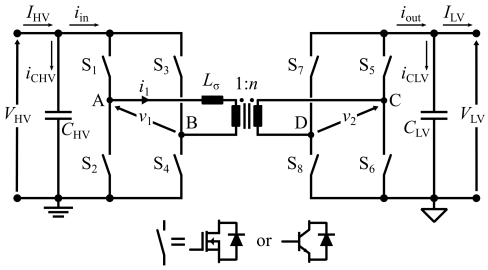



**Figure 1.** Schematic of DAB converter.

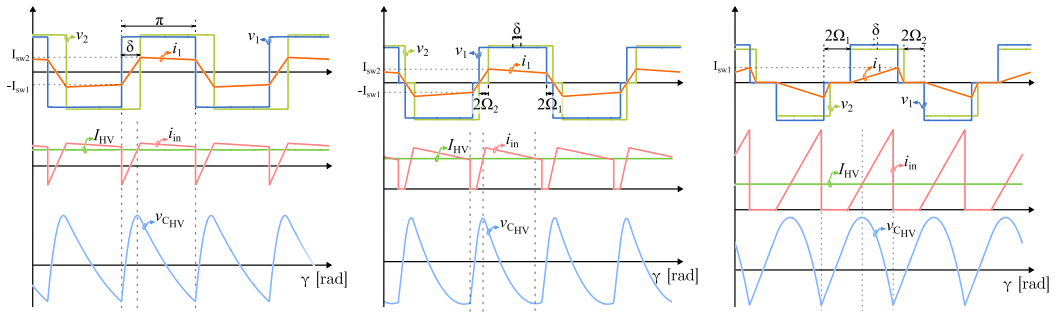



**Figure 2.** Main current and voltage waveforms of DAB converter: (**a**–**c**) are the primary and secondary voltage ($v_1$ & $v_2$) and primary current ($i_1$) in SPS rectangular, TPS-TPM and TPS-TRM, respectively, together with the input currents ($I_{HV}$ & $i_{in}$) and voltage ripple ($v_{C_{HV}}$) in these modulation methods. Forward-mode power transfer (from HV to LV).

### *2.1. Single-Phase Shift Rectangular Modulation*

SPS rectangular is the main modulation method of the DAB converter, which only modifies the $\delta$ modulation angle between $-\pi/2$ and $\pi/2$ ($\Omega_1$ and $\Omega_2$ are set to zero) to manage power flow direction and power level. Furthermore, the maximum power transfer is only achieved with this modulation when considering a specific design, i.e., output power, switching frequency, and decoupling inductance values. Mathematical development directed toward obtaining switching currents in primary and secondary power devices is described in [27,28], resulting in (4) and (5) for the switching currents referred to the primary side of the transformer with this modulation:

$$I_{sw1} = \frac{V_{HV}\,\pi + n\,V_{LV}\,(2\,|\delta| - \pi)}{4\,\pi\,f_{sw}\,L_\sigma}\ , \tag{4}$$

$$I_{sw2} = \frac{V_{HV}\,(2\,|\delta| - \pi) + n\,V_{LV}\,\pi}{4\,\pi\,f_{sw}\,L_\sigma}\ , \tag{5}$$

where $\delta$ is the modulation angle, $f_{sw}$ is the switching frequency, and $L_\sigma$ is the decoupling inductance. Depending on the switching and DC bus current, four particular cases are distinguished to determine DC buses capacitor voltage ripple in this modulation method. These cases define the resulting voltage ripple waveform of the DC buses and thus the limits to determination of each analytical model according to (3). Therefore, input and output voltage ripple are differentiated in the following cases:

- Case 1: $I_{sw1} > I_{HV}$ and $I_{sw2} > I_{HV}$ for input capacitor, $n\,I_{sw1} > I_{LV}$ and $n\,I_{sw2} > I_{LV}$ for output capacitor.
- Case 2: $I_{sw1} < I_{HV}$, $I_{sw2} > I_{HV}$ and $|\,I_{sw1}\,| > I_{HV}$ for input capacitor, $n\,I_{sw1} < I_{LV}$ and $n\,I_{sw2} > I_{LV}$ for output capacitor.

- Case 3: $I_{sw1} < 0$ and $| I_{sw1} | > I_{HV}$ for input capacitor, $n\, I_{sw1} > I_{LV}$ and $n\, I_{sw2} < I_{LV}$ for output capacitor.
- Case 4: $I_{sw1} > I_{HV}$ and $I_{sw2} < I_{HV}$, for input capacitor, and no distinction on output capacitor.

As in previous work [20], the input and/or output full-bridge rectifier currents can be defined with piecewise linear functions, resulting in the current waveforms depicted in Figure 2. To this aim, characteristic times of this modulation are determined with (6)–(8):

$$T_1 = \frac{L_\sigma}{V_{HV} + n\, V_{LV}}\, I_{sw1} \ , \tag{6}$$

$$T_2 = \frac{L_\sigma}{V_{HV} + n\, V_{LV}}\, I_{sw2} \ , \tag{7}$$

$$T_3 = \frac{T_{sw}}{2} - (T_1 + T_2) \ . \tag{8}$$

### *2.2. Triple-Phase Shift Trapezoidal and Triangular Modulations*

In TPS modulation strategies, $\delta$, $\Omega_1$, and $\Omega_2$ are modified at the same time to obtain the desired current waveform in transformer windings to transfer power to the output. The main advantage of these strategies is the extension of the ZVS operating area of the power devices when working outside unity DC gain ($n\, V_{LV}/V_{HV}$). It is important to note that TPS-TPM and TPS-TRM are typically proposed in a combined modulation method, because the working range of TPS-TRM is when it is not possible to achieve a trapezoidal current waveform through the transformer. The major benefit of TPS-TRM relies in the lower switching losses when compared to the SPS rectangular modulations and TPS-TPM. However, in TPS-TRM, it is not possible to work at $V_{HV} = n\, V_{LV}$ and the transferred power is lower.

The switching currents in power devices referred to the primary side when working with TPS-TPM are given in (9) and (10):

$$I_{sw1} = \frac{n\, V_{LV}\, (|\delta| - \Omega_2 + \Omega_1)}{2\, \pi\, f_{sw}\, L_\sigma} \ , \tag{9}$$

$$I_{sw2} = \frac{V_{HV}\, (|\delta| - \Omega_1 + \Omega_2)}{2\, \pi\, f_{sw}\, L_\sigma} \ . \tag{10}$$

Three different cases can be distinguished for the voltage ripple of the input and output capacitors working with TPS-TPM modulation:

- Case 1: $I_{sw1} > I_{HV}$ and $I_{sw2} > I_{HV}$ for input capacitors, $n\, I_{sw1} > I_{LV}$ and $n\, I_{sw2} > I_{LV}$ for output capacitors.
- Case 2: $I_{sw1} < I_{HV}$ and $n\, I_{sw2} > I_{HV}$ for input capacitors, $n\, I_{sw1} < I_{LV}$ and $n\, I_{sw2} > I_{LV}$ for output capacitors.
- Case 3: $I_{sw1} > I_{HV}$ and $I_{sw2} < I_{HV}$ for input capacitors, $n\, I_{sw1} > I_{LV}$ and $n\, I_{sw2} < I_{LV}$ for output capacitors.

The characteristic times of this modulation method are calculated with (11)–(13):

$$T_1 = \frac{L_\sigma}{V_{HV}}\, I_{sw2} \ , \tag{11}$$

$$T_2 = \frac{T_{sw}}{2} - 2\, T_{\Omega_1} - 2\, T_{\Omega_2} \ , \tag{12}$$

$$T_3 = \frac{L_\sigma}{n\, V_{LV}}\, I_{sw1} \ . \tag{13}$$

In TPS-TRM modulation, the switching currents in power devices referred to the primary side are shown in (14) for $V_{HV} < n\, V_{LV}$ ($I_{sw2}$) and $V_{HV} > n\, V_{LV}$ ($I_{sw1}$):

$$I_{sw1} = \frac{n\,V_{LV}\,|\delta|}{\pi\,f_{sw}\,L_\sigma}\ ,\ I_{sw2} = \frac{V_{HV}\,|\delta|}{\pi\,f_{sw}\,L_\sigma}\ . \tag{14}$$

Furthermore, the characteristic times of TPS triangular modulation are determined with (15) and (16) for cases 1 and case 2, respectively:

$$T_1 = \frac{L_\sigma}{V_{HV}}\,I_{sw2},\ \ T_2 = \frac{L_\sigma}{|V_{HV} - n\,V_{LV}|}\,I_{sw2}\ , \tag{15}$$

$$T_1 = \frac{L_\sigma}{|V_{HV} - n\,V_{LV}|}\,I_{sw1},\ \ T_2 = \frac{L_\sigma}{n\,V_{LV}}\,I_{sw1}\ . \tag{16}$$

The analytical expressions to determine voltage ripple and RMS current in bus capacitors when working with the main modulation methods of DAB converter are presented in the Appendix A of this work. The parameters defined in Table 2 simplify the resulting equations presented in this paper. These models have been validated based on a simulation model developed in PLECS by applying the same procedure as in previous work [20].

**Table 2.** Definition of key parameters for the simplification of the analytical models of this work (see Appendix A).

| Parameter | Value | Parameter | Value |
|---|---|---|---|
| $A_1$ | $I_{SW1} + I_{HV}$ | $A_2$ | $n\,I_{SW2} + I_{LV}$ |
| $B_1$ | $I_{SW1} + I_{SW2}$ | $B_2$ | $n\,I_{SW1} + n\,I_{SW2}$ |
| $C_1$ | $I_{SW1} - I_{HV}$ | $C_2$ | $n\,I_{SW1} - I_{LV}$ |
| $D_1$ | $I_{SW2} - I_{HV}$ | $D_2$ | $n\,I_{SW2} - I_{LV}$ |
| $E_1$ | $I_{SW1} - I_{SW2}$ | $E_2$ | $n\,I_{SW1} - n\,I_{SW2}$ |

## 3. Design Space Analysis of DAB Converter

The number of parameters that impact the volume and weight of DAB converter is large. Therefore, the selected design approach determines the resulting power density of the converter. In order to clarify the design trade-offs of this PEC, a design space analysis is carried out in this section based on the analytical models of the current stress of the power semiconductors in [20] and the DC-link capacitors presented in this work. The results of this analysis aid the design procedure, resulting in the selection of the switching frequency, the $\delta$ modulation angle limit, the decoupling inductance, and the DC-link bus capacitances.

Because SPS rectangular modulation is able to transfer the maximum power across the three modulations considered in this study, it is selected to determine the required decoupling inductance. In order to transfer 10 kW at the considered switching frequencies, the resulting decoupling inductances are computed with (17):

$$L_\sigma = \frac{V_{HV}\,n\,V_{LV}\,\delta_{lim}\,(\pi - \delta_{lim})}{2\,\pi^2\,f_{sw}\,P_{max}}\ , \tag{17}$$

where $P_{max}$ is the desired maximum power transfer and $\delta_{lim}$ is the theoretical limit of the modulation angle $\delta$, whose maximum is $\pi/2$ radians. At this angle, the maximum power of the converter is extracted for a specific $L_\sigma$ value. In this work, the decoupling inductance is determined for the nominal values of HVDC and LVDC buses, i.e., $V_{HV} = 270$ and $V_{LV} = 27$. The resulting decoupling inductances for the case studies presented in Sections 3.1 and 3.2 are given in Figure 3, First, the $\delta_{lim} = 90°$ is considered and the switching frequency is varied. Then, the switching frequency is set to the optimal value extracted in Section 3.1, and $\delta_{lim}$ is varied. The design parameters utilized for the MEA case study are listed in Table 3. These parameters are selected according to the standard of aircraft electric distribution systems (HVDC and LVDC voltages and voltage ripple) [29], the ratio between nominal operating voltages (transformer turns ratio), and typical values found in the literature for DC–DC power conversion (nominal power) [18], while the

switching frequency and limit of the modulation angle are swept to find its optimal values for the selected component technologies.

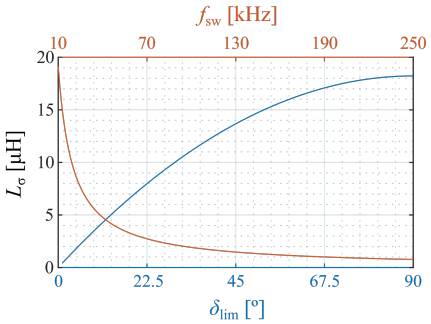



**Figure 3.** Resulting decoupling inductances versus the switching frequency and $\delta_{lim}$.

**Table 3.** Design parameters.

| Parameter | Value | Units |
|---|---|---|
| $V_{HV}$ | 270 (250–280) | V |
| $V_{LV}$ | 27 (22–29) | V |
| $n$ | 10 (270/27) | - |
| $P$ | 10 | kW |
| $f_{sw}$ | 10:1:250 | kHz |
| $\delta_{lim}$ | 1:1:90 | ° |
| $\Delta V_{HV(pk-pk)}$ | 6 | V |
| $\Delta V_{LV(pk-pk)}$ | 1.5 | V |

### *3.1. Switching Frequency*

The switching frequency of the power devices in the DAB has a relevant influence on the volume of the overall converter. On one hand, a high switching frequency can reduce the volume of the power transformer. However, the switching losses in the power semiconductor devices are also higher as a result, and thus the volume of the required heatsink increases. Therefore, the optimal switching frequency is selected considering the volume of these components.

Moreover, the current levels of power devices of the DAB converter do not vary when the switching frequency is increased in the considered case study. This is due to the fact that the required decoupling inductance in this converter increases as the switching frequency decreases, and the product of these two variables is constant when considering the same power transfer, i.e., constant switching and RMS currents. Therefore, conduction losses do not increase with the switching frequency, and the larger switching losses are due to the linear increment of the switching frequency.

In this paper, the volume of the power transformer is determined from the area product considering EE planar core geometries of N97 magnetic material [30,31].

To compute the volume of the heatsink, the required thermal resistance is calculated from (18):

$$R_{th} = \frac{(T_c - T_{amb})}{P_{tot}}, \tag{18}$$

where $T_c$ and $T_{amb}$ are the case and ambient temperatures, respectively, and $P_{tot}$ is the sum of switching and conduction losses in power devices. Then, the volume of this component is estimated to achieve the desired thermal resistance based on the cooling system performance index (CSPI) [32]. The considered power devices are C3M0045065D (SiC) and STP240N10F7 (Si) for the HVDC and LVDC sides, respectively. For LVDC, five power devices are placed in parallel to reduce the power losses per device, ensuring that the maximum junction temperature of the device is not exceeded.

In Figure 4, the estimated volume of the power transformer and heatsink are presented together when $\delta_{\text{lim}}$ is set to 10°. The crossing point between the transformer and heatsink volumes lies slightly below 50 kHz. However, the minimum of the total volume is found at this frequency. Then, the selected switching frequency is 50 kHz for the estimation of the power losses presented in this paper.

It is important to note that the switching frequency in which the minimum volume is obtained may vary when considering different $\delta_{\text{lim}}$ due to its influence on the power losses, and thus in the required heatsink. Therefore, an analysis of the power losses in switching devices for different $\delta_{\text{lim}}$ is performed in the following subsection.

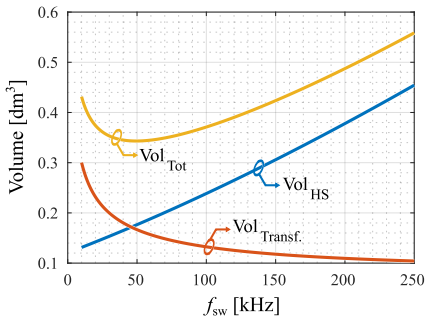



**Figure 4.** Volume of the power transformer and heatsink in DAB versus the switching frequency.

### *3.2. Limit of the Modulation Angle*

The active-to-reactive power ratio in a DAB converter strongly depends on the modulation angle $\delta$ [27] when considering low-voltage variations in DC buses. A common design choice in DAB design is to limit the maximum modulation angle $\delta$ with which the converter transfers the maximum power at nominal operating DC voltages. With this consideration, the reactive power processed by the converter is reduced to transfer the same active power level. Therefore, the resulting RMS and switching currents are lower, which determines the conduction and switching losses of the PEC. The power losses estimated in DAB are depicted in Figure 5 for SPS rectangular and combined TPS and TPM-TRM modulations.

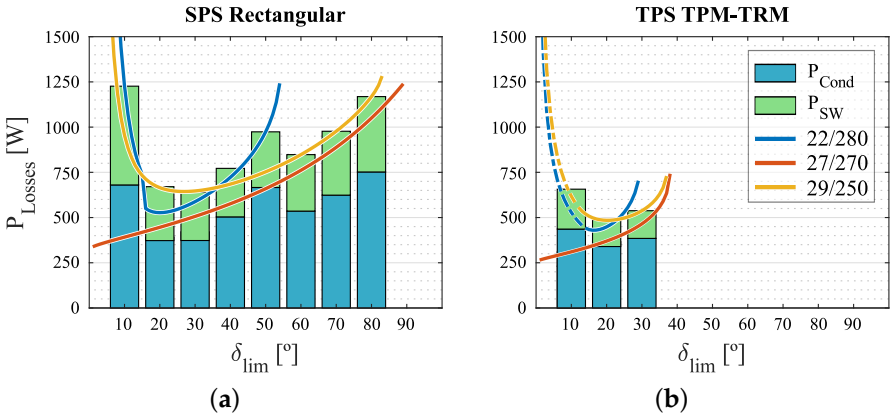



**Figure 5.** Power losses in the power devices of DAB converter for different operating DC voltages with: (**a**) SPS rectangular and (**b**) combined TPS-TPM and TPS-TRM modulations. The distribution of conduction and switching losses is depicted in the worst case.

In Figure 5a, the power losses for 10 kW of power transfer and SPS rectangular modulation are presented for different limits of the modulation angle and different input to output voltages relationship. These different input and output voltage ratios correspond to the maximum (29/250), minimum (22/280), and unity (27/270) DC gain values ($n\,V_{\text{LV}}/V_{\text{HV}}$) of the converter. The conduction and switching loss distributions are presented in the worst DC gain case at each $\delta_{\text{lim}}$, where the conduction losses are shown to be dominant in

this application due to the high circulating currents in the LVDC side. A reduction in $\delta_{\text{lim}}$ decreases the conduction losses in the DAB converter, which are critical in the design of the LVDC side of the DC/DC converter in MEA applications due to the low-voltage and high-current stress. However, this benefit is mainly found close to the nominal DC gain, and there is a trade-off between $\delta_{\text{lim}}$ and the power losses when working outside nominal operating condition. Comparing $\delta_{\text{lim}}$ at 10° and 20° in the 22/280 case, the increment in power losses is noticeable. In this case, the higher switching losses are caused by the operation in hard-switching (HS) conditions during high-power transfer, which is the main drawback of decreasing $\delta_{\text{lim}}$, whereas the conduction losses are larger due to the reactive power that flows through the converter when working outside nominal DC voltages with low modulation angles. Furthermore, it can be noted that the nominal power transfer is not achieved at the minimum DC gain for $\delta_{\text{lim}}$ above 55°. This is due to the fact that the required $\delta$ to transmit the maximum output power is above 90°, exceeding the maximum theoretical $\delta$.

In Figure 5b the study is presented for the combined TPS TPM-TRM. When $\delta_{\text{lim}}$ is set above 40° it is not possible to transfer the maximum power with this combined modulation method in the considered DC gain relationships. Below 40°, power transfer is possible in these operating conditions. As in SPS rectangular modulation, the power losses are lower when $\delta_{\text{lim}}$ is decreased at unity DC gain, which is also due to the reactive power in the converter. However, the large power losses found at low $\delta_{\text{lim}}$ values are caused by the higher RMS current levels when working with TPS TRM during high-power transfer as compared to TPS TPM. Furthermore, the required $\delta_{\text{lim}}$ to transmit the maximum power at a minimum DC gain is below 30°.

Although the variation of DC voltages in MEA applications is not wide (250–280 V in HVDC and 22–29 V in LVDC), the selection of $\delta_{\text{lim}}$ must be deeply analyzed to reduce the conduction and switching losses, improving the resulting power density. Therefore, the efficiency of the converter is determined and compared between different $\delta_{\text{lim}}$ for the modulation methods presented in this work.

### *3.3. Efficiency Analysis*

In this section, the efficiency of DAB is analyzed when $\delta_{\text{lim}}$ is set to 10°, 20° and 25°. The theoretical limit of the modulation angle is selected to be able to transfer the maximum power with the combined TPS TPM-TRM in all the operating points of the converter. Then, the efficiency of the converter is computed considering conduction and switching losses in power devices.

The efficiency maps of the DAB converter are presented in Figure 6 for the mentioned $\delta_{\text{lim}}$ and the considered modulations. These efficiency maps are obtained by computing the power losses (switching and conduction) of the switching devices at each operating point. In all cases, the highest efficiencies in the converter are found close to the nominal operating conditions defined in Table 3. This phenomenon becomes remarkable as the limit of the modulation angle $\delta$ decreases, and this is due to a reduction in the circulating reactive power in the converter when working at DC gain values close to unity. Nevertheless, the efficiency starts to decrease outside this condition as a result of the impact of DC bus voltages on the reactive power. Moreover, HS regions appear when working with SPS rectangular modulation, whose impact on the efficiency of the converter is critical.

For $\delta_{\text{lim}} = 20°$ and $\delta_{\text{lim}} = 25°$, the efficiency of the converter decreases compared with $\delta_{\text{lim}} = 10°$. In all cases, the efficiency improvement with combined TPS TPM-TRM over SPS rectangular modulation is considerable.

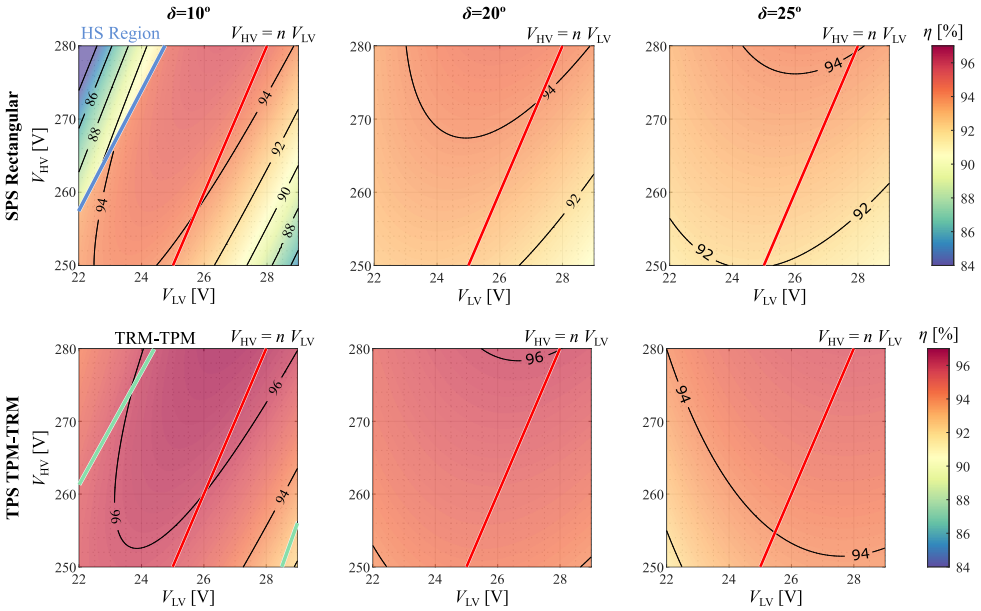



**Figure 6.** Efficiency map of the DAB converter at $P = 10\,\text{kW}$ when working with SPS rectangular (**top**) and combined TPS TPM and TRM (**bottom**) modulations for different $\delta_{\text{lim}}$: 10°, 20° and 25°.

This analysis leads to the selection of combined TPS TPM-TRM working with low $\delta$ angles. In order to examine the influence of $\delta_{\text{lim}}$ over different load conditions, the study is extended to the whole output power range considering forward (HV to LV) and backward (LV to HV) power flow direction. To this aim, the average efficiency ($\eta_{\text{AVG}}$) of the map at the different output power is defined by (19):

$$\eta_{\text{AVG}} = \frac{1}{\Delta V_{\text{LV}}\,\Delta V_{\text{HV}}} \int\int^{\Delta V_{\text{HV}},\Delta V_{\text{LV}}} \eta(V_{\text{HV}}, V_{\text{LV}}) dV_{\text{HV}}\, dV_{\text{LV}}\,, \tag{19}$$

where $\eta(V_{\text{HV}}, V_{\text{LV}})$ is the efficiency as a function of the DC bus voltages, and $\Delta V_{\text{HV}}$ and $\Delta V_{\text{LV}}$ are the DC-link voltage ranges in the HVDC and LVDC, respectively.

In order to select the best efficiency trade-off, $\eta_{\text{AVG}}$ is computed and compared for the different voltage gains, transferred power and $\delta_{\text{lim}}$, and it is presented in Figure 7. It can be noted that the average efficiency in combined TPS modulation is larger than both SPS rectangular modulation's forward and backward modes in the whole output power range when $\delta_{\text{lim}}$ is set to the considered angles. This is due to the HS operation in some operating points while working with SPS rectangular modulation. This HS region appears at low power transfer levels when $\delta_{\text{lim}}$ is increased, leading to higher $\eta_{\text{AVG}}$ at medium power transfer levels. Therefore, TPS TPM-TRM modulation seems to be the most adequate for increasing the efficiency of the converter in a wide operating region. With this modulation method, the average efficiency at high-power transfer is increased at low $\delta_{\text{lim}}$. However, the efficiency in light-load conditions is penalized. This fact is due to the operation of TPS-TRM outside nominal DC gain, which increases the RMS current stress in the power devices. Then, the best efficiency trade-off between full- and light-load operating conditions is found at $\delta_{\text{lim}} = 20°$ for the considered MEA application.

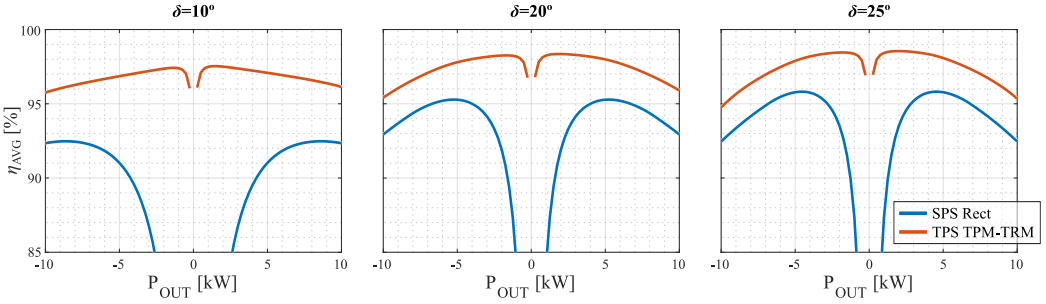
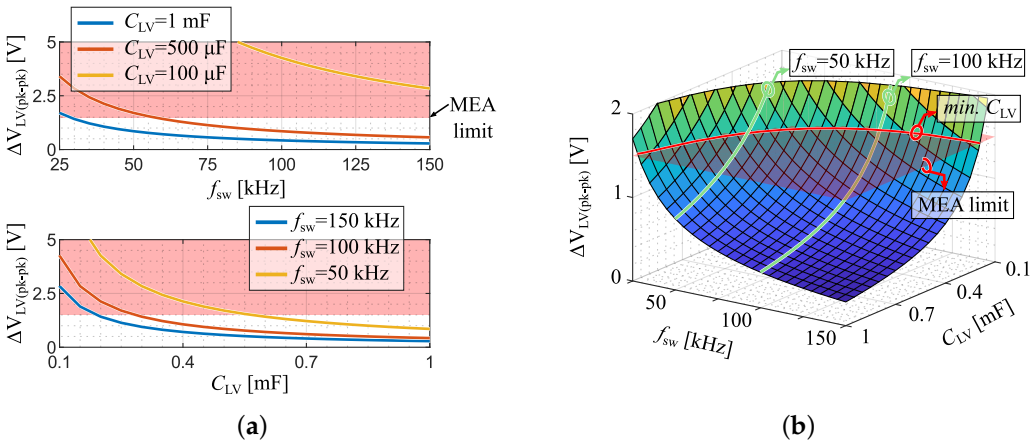



**Figure 7.** Efficiency versus output power ($P_{\mathrm{OUT}}$) in SPS rectangular and combined TPS TPM−TRM modulations for the considered $\delta_{\mathrm{lim}}$: 10°, 20° and 25°.

### *3.4. DC-Link Capacitors*

One of the critical steps in the design of DAB converter for MEA applications is the large LVDC capacitance required to satisfy the voltage ripple requirements. However, the impact of the switching frequency and LVDC bus capacitance on the voltage ripple have not yet been investigated. Because the analysis is similar for input and output capacitors, this section is focused on output capacitors.

To develop this study, the analytical models presented in the Appendix A of this work are employed to characterize the voltage ripple in LVDC capacitor regarding the selected capacitance and switching frequency. In Figure 8a, two scenarios are depicted: the influence of switching frequency variations on the peak-to-peak voltage ripple for fixed output capacitances, and the influence of LVDC capacitance variations for fixed switching frequencies. It can be noted that, for capacitance values below 100 µF, the switching frequency must be increased above 150 kHz in order to fulfill MEA requirements. As far as the capacitance is increased, the switching frequency required to meet the standard is reduced.




(**a**) (**b**)

**Figure 8.** (**a**,**b**): Influence of output capacitance ($C_{\mathrm{LV}}$) and switching frequency ($f_{\mathrm{sw}}$) on the peak-to-peak voltage ripple ($\Delta V_{\mathrm{pk-pk}}$).

Furthermore, the trend of the output capacitance required at different switching frequencies is shown. At 50 kHz of switching frequency, the minimum required capacitance is 550 µF to achieve a maximum peak to peak voltage ripple of 1.5 V. For higher switching frequencies, the impact of this capacitance is lower, and MEA limits are satisfied for capacitances above 200 µF for $f_{\mathrm{sw}} = 150$ kHz.

The impacts of both switching frequency and output capacitance are presented in Figure 8b. The minimum LVDC capacitance at each switching frequency is defined by the intersection of the LVDC peak-to-peak voltage ripple ($\Delta V_{LV(pk-pk)}$) with the MEA limit plane. This curve is defined by two asymptotic limits that theoretically tend to infinite capacitance when the switching frequency is close to zero, and an infinite switching

frequency when the output capacitance falls to zero in order to meet the MEA standard. Therefore, the best trade-offs between switching frequency and required capacitance are found in the knee of the curve, which is found between 50 and 100 kHz of the switching frequency for the MEA case study considered in this work. Furthermore, it can be noted that the safety margin regarding the MEA limit can be achieved by slightly increasing the minimum capacitance.

The RMS current level that flows through the capacitor also plays an important role in the sizing of this component. The number of capacitors set in parallel must be able to handle the required RMS current. In Figure 9, the normalized RMS current through the output capacitor is presented to find the optimal $\delta_{\text{lim}}$ for its sizing. For the limit of the modulation angle selected in this work, i.e., 20°, the RMS current is close to its minimum value. Nevertheless, the trend is increasing below 10°.

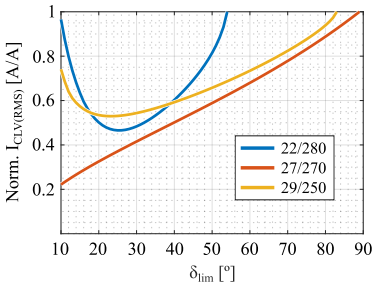



**Figure 9.** Normalized RMS current level that flows through LVDC capacitor versus $\delta_{\text{lim}}$ for minimum, nominal, and maximum DC gain voltages at maximum power transfer.

## 4. Conclusions

In this work, the analytical modeling of power devices and DC bus capacitors of DAB converter has been completed in the main modulation methods of the converter, i.e., SPS rectangular and combined TPS-TPM and TRM modulations. These models have been validated through a simulation model developed in PLECs.

Based on the presented analytical models, the sizing of power devices and DC bus capacitor is significantly simplified. Therefore, a design space analysis has been carried out in this work to determine the impact of each design variable on the performance of the converter, emphasizing the power losses in an MEA case study. In order to obtain a good trade-off between the transformer and heatsink volumes, 50 kHz is the selected switching frequency. At this frequency, the modulation angle is limited to $\delta_{\text{lim}} = 20°$ to reduce the circulating reactive power through the converter, thus reducing the high conduction losses produced in the LVDC side. In this case, combined TPS-TPM and TPS-TRM is selected due to its efficiency improvement from full- to light-load operation.

Finally, the selection of the required capacitance to fulfill MEA requirements is analyzed. Due to the high switching frequency utilized, low capacitances are required in HVDC and LVDC buses. Furthermore, the impact of the switching frequency and capacitance on the voltage ripple is studied in this work. The minimum LVDC capacitance to meet the requirement is 550 µF at 50 kHz. Below 50 kHz, the required capacitance may affect the volume of the resulting capacitor, which impacts the power density of the PEC. Above 100 kHz, the LVDC capacitance needed is lower and tends to zero for high switching frequencies. Furthermore, the optimal $\delta_{\text{lim}}$ for minimization of the RMS current stress that flows through the output capacitor lies between 20 and 30 °, which helps reduce the volume and weight of this component.

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## Appendix A. Analytical Models of the RMS Current Stress and Voltage Ripple in Bus Capacitors

In this appendix, the analytical models of the RMS currents and peak-to-peak voltage ripple in HVDC and LVDC capacitors are presented.

The equations are summarized in Tables A1–A3 for the modulation methods considered in this work. The corresponding cases in each modulation method are detailed in Section 2, where the characteristic times are also described. Furthermore, in Table 3 (Section 2), the corresponding parameters to simplify the equations included in this appendix are gathered.

These models have been validated based on a simulation model developed in PLECS applying the same procedure than in the RMS and AVG currents in power devices for the whole input and output voltage ranges at nominal power transfer [20]. The results of the validation process are presented in Figure A1. It can be noted that, regardless of the studied modulation method, the error obtained for the peak-to-peak voltage equations is below 5%. In the case of the RMS currents, the error reaches, 10 %, especially when the converter works close to a unity gain. Then, these results show a good correlation between analytical and simulation values.

**Table A1.** Voltage ripple in input and output capacitor (power transfer from HV to LV).

| Modulation | Case | $\Delta V_{C_{HV(pk-pk)}}$ | $\Delta V_{C_{LV(pk-pk)}}$ |
|---|---|---|---|
| Rectangular | 1 | $\frac{0.5\,{A_1}^2\,L_\sigma}{C_{HV}\,(V_{HV}+n\,V_{LV})}$ | $\frac{0.5\,{A_2}^2\,(L_\sigma/n^2)}{C_{LV}\,(V_{HV}/n+V_{LV})}$ |
| | 2 | $\frac{{D_1}^2\,L_\sigma\,n\,V_{LV}}{C_{HV}\left((n\,V_{LV})^2-{V_{HV}}^2\right)}$ | $\frac{0.5\,{D_2}^2\,(L_\sigma/n^2)}{C_{LV}\,(V_{LV}-V_{HV}/n)}$ |
| | 3 | $\frac{0.5\,\mid A_1\mid^2\,L_\sigma}{C_{HV}\,(n\,V_{LV}-V_{HV})}$ | $\frac{0.5\,{C_2}^2\,(L_\sigma/n^2)\,(2\,V_{HV}/n)}{C_{LV}\left((V_{HV}/n)^2-{V_{LV}}^2\right)}$ |
| | 4 | $\frac{0.5\,{C_1}^2\,L_\sigma}{C_{HV}\,(V_{HV}-n\,V_{LV})}$ | - |
| Trapezoidal | 1 | $\frac{0.5\,{D_1}^2\,(L_\sigma/V_{HV})+(0.5\,E_1+C_1)\,T_2}{C_{HV}}$ | $\frac{(0.5\,E_2+C_2)T_2+{C_2}^2\,(L_\sigma/V_{LV})}{C_{LV}}$ |
| | 2 | $\frac{0.5\,{D_1}^2\,L_\sigma\,n\,V_{LV}}{C_{HV}\,V_{HV}\,(n\,V_{LV}-V_{HV})}$ | $\frac{0.5\,{D_2}^2\,(L_\sigma/n^2)}{C_{LV}(V_{LV}-V_{HV}/n)}$ |
| | 3 | $\frac{0.5\,{C_1}^2\,L_\sigma}{C_{HV}(V_{HV}-n\,V_{LV})}$ | $\frac{0.5\,{C_2}^2\,(L_\sigma/n^2)\,(V_{HV}/n)}{C_{LV}\,V_{LV}(V_{HV}/n-V_{LV})}$ |
| Triangular | 1 | $\frac{0.5\,{D_1}^2 L_\sigma\,nV_{LV}}{C_{HV}\,V_{HV}(n\,V_{LV}-V_{HV})}$ | $\frac{0.5\,{D_2}^2(L_\sigma/n^2)}{C_{LV}\,(V_{LV}-V_{HV}/n)}$ |
| | 2 | $\frac{0.5\,{C_1}^2\,L_\sigma}{C_{HV}\,(V_{HV}-n\,V_{LV})}$ | $\frac{0.5\,{C_2}^2\,(L_\sigma/n^2)\,(V_{HV}/n)}{C_{LV}\,V_{LV}(V_{HV}/n-V_{LV})}$ |

**Table A2.** RMS Current in input capacitor (power transfer from HV to LV).

| Modulation | Case | $I_{RMS}$ |
|---|---|---|
| Rectangular | SS Case | $\sqrt{(2f_{sw})((A_1{}^2+B_1{}^2/3-A_1B_1)(T_1+T_2)+(D_1{}^2+E_1{}^2/3+D_1E_1)T_3)}$ |
| | $I_{SW1}<0$ | $\sqrt{(2f_{sw})((A_1{}^2+B_1{}^2/3-A_1B_1)T_1+(D_1{}^2+E_1{}^2/3+D_1E_1)(T_2+T_3))}$ |
| | $I_{SW2}<0$ | |
| Trapezoidal | - | $\sqrt{(2f_{sw})((I_{SW2}{}^2/3-I_{HV}D_1)T_1+(D_1{}^2+E_1{}^2/3+D_1E_1)T_2+I_{HV}{}^2T_3)}$ |
| Triangular | $V_{HV}<n\,V_{LV}$ | $\sqrt{(2f_{sw})((I_{SW2}{}^2/3-I_{HV}D_1)T_1+(D_1{}^2+I_{SW2}{}^2/3+D_1\,I_{SW2})T_2+I_{HV}{}^2T_3)}$ |
| | $V_{HV}>n\,V_{LV}$ | $\sqrt{(2f_{sw})\Big((I_{HV}{}^2+I_{SW1}{}^2/3-I_{HV}\,I_{SW1})T_1+(I_{HV})^2(T_2+T_3)\Big)}$ |

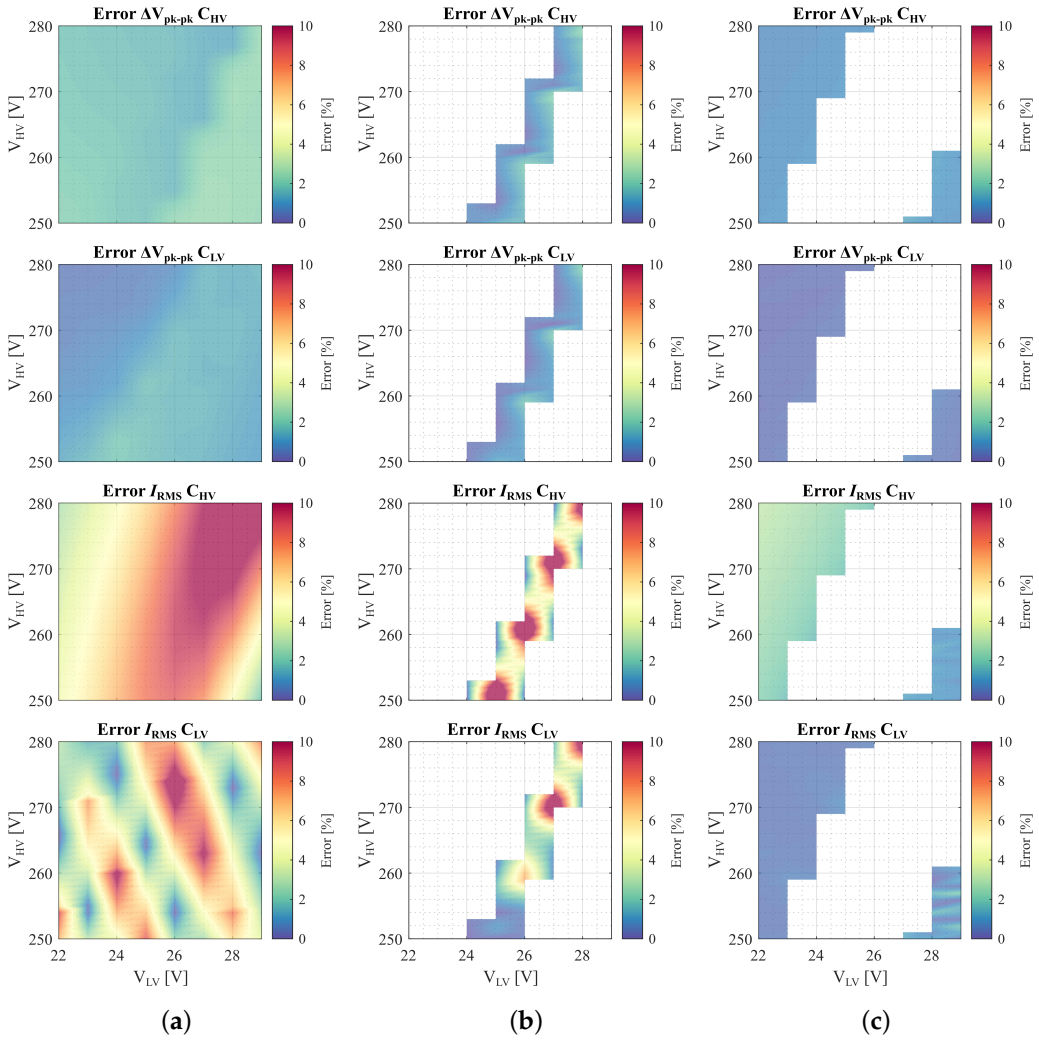


**Figure A1.** Validation of the RMS and peak-to-peak voltage ripple analytical equations presented in this work based on a simulation model developed in PLECS: (**a**) SPS rectangular modulation, (**b**) TPS-TPM and (**c**) TPS-TRM.

**Table A3.** RMS Current in output capacitor (power transfer from HV to LV).

| Modulation | Case | $I_{RMS}$ |
|---|---|---|
| Rectangular | SS Case | $\sqrt{(2f_{sw})((C_2^2+B_2^2/3-C_2B_2)(T_1+T_2)+(D_2^2+E_2^2/3+D_2E_2)T_3)}$ |
| | $I_{SW1}<0$ | $\sqrt{(2f_{sw})((C_2^2+B_2^2/3-C_2B_2)T_1+(D_2^2+E_2^2/3+D_2E_2)(T_2+T_3))}$ |
| | $I_{SW2}<0$ | |
| Trapezoidal | - | $\sqrt{(2f_{sw})\left(I_{LV}{}^2T_1+(D_2^2+E_2^2/3-D_2E_2)T_2+\left(C_2^2+(n\,I_{SW1})^2/3-C_2\,n\,I_{SW1}\right)T_3\right)}$ |
| Triangular | $V_{HV}<n\,V_{LV}$ | $\sqrt{(2f_{sw})\left(I_{LV}{}^2(T_1+T_3)+\left(D_2^2+(n\,I_{SW2})^2/3-D_2\,n\,I_{SW2}\right)T_2\right)}$ |
| | $V_{HV}>n\,V_{LV}$ | $\sqrt{(2f_{sw})\left(\left((n\,I_{SW1})^2/3-I_{LV}\,C_2\right)T_1+\left(C_2^2+(n\,I_{SW1})^2/3-C_2\,n\,I_{SW1}\right)T_2+I_{LV}{}^2T_3\right)}$ |

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