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Review

Single-Phase Fault Tolerant Multilevel Inverter Topologies—Comprehensive Review and Novel Comparative Factors

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Abstract: Multilevel inverters (MLIs) are used in a variety of industrial applications in high- and medium-voltage systems. The modularity, high-power output from medium voltages, and low harmonic content are some of the advantages of MLIs. The reliability of MLIs is quite important. The reliability is affected by different kinds of faults occurring in the MLIs. In MLI circuits, switching devices are the most vulnerable components and have a major involvement in all types of faults. As an outcome, it is necessary to take proper corrective action in the event of a fault. This work provides a comprehensive review of different fault tolerant (FT) solutions for MLIs in the event of switch fault. Moreover, various single-phase FT MLI topologies are reviewed, along with their constructional features, merits, and demerits. This work also proposes a comparison approach that integrates novel factors to account for fault tolerance quantitatively. A comparison investigation verifies the effectiveness of the proposed method. The FT operation of an existing five-level FT MLI topology is discussed, simulated, and experimentally verified.

Keywords: fault tolerant; fault-tolerant multilevel inverter; reduced device count; multilevel inverter; fault tolerance; inverters; switch faults; topology; reliability

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1. Introduction

Multilevel inverters are gaining importance in medium-voltage and high-power industrial applications [1,2]. The three MLI topologies, i.e., cascaded H-bridge (CHB), neutral point clamped (NPC), and flying capacitor (FC), are included in classical MLI topologies [3,4]. MLIs find applications in standalone or grid-connected PV systems [5–8], pumped storage power plants [9], active power filters [10,11], flexible AC transmission systems (FACTSs) [12], variable frequency drives [13], high-voltage DC (HVDC) system [14,15], etc.

Some of the merits of MLIs over two-level inverters have been discussed in the literature [1,2,16–20]. They include the following:

1. MLI provides a high-quality output voltage waveform with low harmonic content; hence, total harmonic distortion (THD) is reduced considerably.
2. Due to lower harmonic content, the need for low-frequency bulky filter requirement reduces, thereby reducing electromagnetic interference (EMI). Moreover, it has good electromagnetic compatibility (EMC).
3. MLI provides low voltage stress across switches. Hence, it enables users to generate high voltages by using low-rating semiconductor devices.

4. MLI can operate with both low frequency and a fundamental frequency modulation scheme satisfactorily. Switching losses are reduced in a low-frequency modulation scheme. Hence the efficiency of the inverter increases.
5. The reduction in overall inverter loss reduces the requirement for cooling arrangement.
6. MLI can provide FT operation under single- or multiple-switch faults.

Figure 1 depicts the fault distributions in power electronic converter components [21]. The semiconductor devices and capacitors are the most vulnerable components in MLIs. Significant failures in the semiconductor switching devices (insulated gate bipolar transistors (IGBTs) or metal oxide semiconductor field effect transistors (MOSFETs)) are open circuit (OC) faults and short circuit (SC) faults [22]. The causes of OC faults can be a loss of gating signals, thermal cycling, or the malfunctioning of gate driver circuits. The causes of SC faults can be high temperatures, avalanche stress, overvoltage, or incorrect gate voltage. The OC fault is not serious and hence does not cause damage to the system. On the other hand, the SC fault is critical and may cause severe damage to the system due to the high current flowing under faulty conditions [23]. Hence, it is recommended to remove the faulty device(s) as soon as a fault is detected in order to avoid fault propagation to other healthy switching devices. This is known as fault isolation.

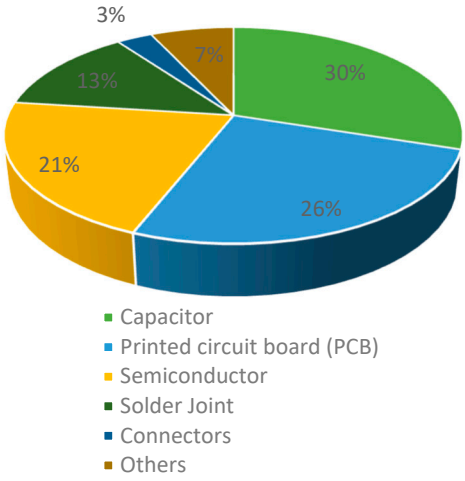

Figure 1. Distributions of faults in power electronic converter components.

As the number of voltage levels increases in conventional MLIs, the requirement for semiconductor switching devices increases. As a result, the FT operation is possible due to the presence of redundant switching states for generating the same voltage level. These redundant switches are utilized during a fault in the switch to ensure FT operation, thereby bypassing the faulty switching state [3]. The ability of an MLI to continue operation either with full or reduced power rating in case of component(s) failure is referred to as the fault tolerance of an MLI.

The conventional MLIs have the drawback of a higher number of components (semiconductor devices, DC sources, capacitors, and inductors) as the voltage level increases. Hence, MLIs result in higher costs and large sizes. Researchers are optimally reducing the active and passive components in MLIs to ensure cost reduction and modularity [1]. The focus to reduce semiconductor devices and other components as the number of level increases is reflected in "reduced device count (RDC) MLIs" was reviewed in [1,4,24–27].

In the case of switch faults in RDC MLIs, the healthy switches are utilized to generate the output voltage levels. The maximum number of voltage levels that can be generated in the case of a fault in switches depends on the available redundant states. Reducing the switches may lead to the loss of redundant states. Hence, there may be loss of output voltage level(s) [28,29]. The semiconductor switching device failure can lead to either complete shutdown of MLI or operation of MLI at reduced levels. The first option, i.e.,

complete shutdown of an MLI, may cause immeasurable economic and life losses in critical applications such as hospitals, electric vehicles, financial markets, military, PV systems, wind turbines, industries, etc. [30,31]. Low reliability is the limitation of RDC MLIs because of the loss of redundant switching states [28]. To overcome this limitation of RDC MLIs, FT MLIs are developed.

The FT MLI is one of the types of MLI that has an optimal number of switches and other components with the possibility of fault tolerance. FT MLI has the benefits of fault tolerance, as seen in conventional MLIs, and a smaller number of components, as seen in RDC MLIs [23]. The FT MLI would ensure the following [3]:

1. Tolerance to single and/or multiple OC and SC faults.
2. Uninterrupted power supply to the loads.
3. Satisfactory system efficiency.
4. Fewer switches and other components.
5. Lesser cost.

The optimal reduction of the switches and other components while preserving the output voltage levels and power in different switch faulty conditions is still a significant challenge. Several FT MLI topologies are proposed in the literature based on different FT techniques.

Figure 2 depicts the FT MLI operation in case of fault. It has four steps [22,32].

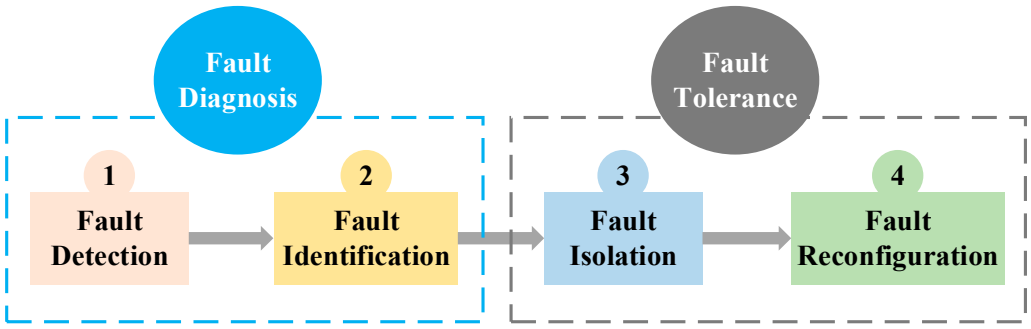

Figure 2. FT MLI operation in case of fault.

Fault diagnosis and fault tolerance are the two back-to-back processes in the FT MLI operation. The steps fault detection and fault identification come under fault diagnosis [22]. The algorithms based on fault diagnosis are reviewed in [33]. The steps fault isolation and fault reconfiguration come under fault tolerance [22]. Various fault isolation and fault reconfiguration techniques are reviewed in [30,33]. The primary goal of FT MLI operation is to avoid fault transmission and its catastrophic effects by detecting and diagnosing any type of malfunction early in order to avoid system shutdowns.

In the case of any fault, the fault detection is the first step. During this period, the fault alarm is activated, and the faulty component remains unknown. The second step is fault identification. This step helps in identifying the type (OC or SC fault) and location (which component of the MLI topology is faulty?) of the fault. The third step is fault isolation. During this period, the isolation of the faulty components takes place to avoid catastrophic failure of the healthy components and damage to the MLI. The last step is fault reconfiguration. During this period, reconfiguration of the MLI topology and/or modulation scheme takes place for uninterrupted power supply and safe operation [22]. The solutions used for MLI fault tolerance are known as MLI FT solutions.

Pre-fault is the period in which an MLI is working in normal (or healthy) conditions. During fault is the period in which the MLI may or may not work similarly to the normal condition due to the fault. Post-fault is the period in which the MLI is working after taking certain FT measures. FT MLI operation is necessary as a fault occurs to bring the MLI back in working condition.

In this paper, the authors review various recently developed single-phase FT MLI topologies. The features of the work include the following:

1. Classification of MLI FT solutions.
2. Review of single-phase FT MLI topologies with their constructional features, merits, and limitations.
3. Comparison of different single-phase FT MLI based on proposed novel factors.
4. Simulation and experimental verification of existing five-level FT MLI topology.

2. MLI FT Solutions

Different MLI FT solutions are presented in the literature. The classification is shown in Figure 3.

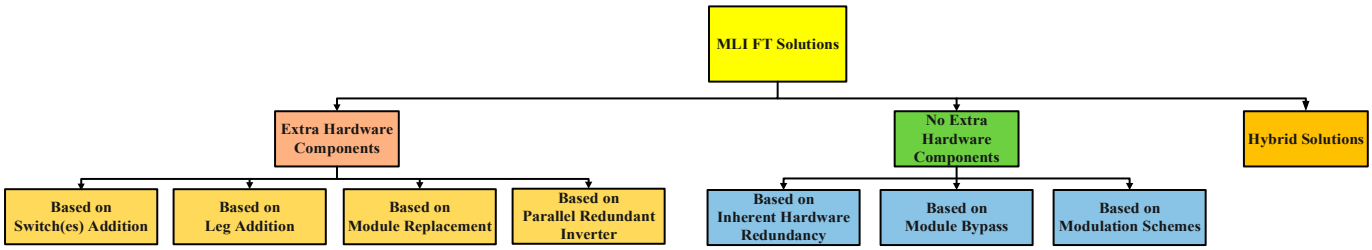

Figure 3. Classification of MLI FT solutions.

The MLI FT solutions can be classified into the following categories [22]:

1. Solution based on extra hardware components (EHC).
2. Solution based on no extra hardware components (NEHC).
3. Hybrid solutions.

2.1. MLI FT Solutions Based on EHC

In this MLI FT solution, the additional components (e.g., switching devices, power diodes, modules, relays, fuses, etc.) are added to the original MLI topology to continue supply by generating levels that are lost due to faulty switching device(s) [22]. In this solution, the process is mainly based on the use of extra hardware redundancy and FT control. The function of additional components is to add redundancy by providing conduction paths that are lost under faulty conditions in MLI topology. It also alters the modulation scheme to generate new switching angles. The MLI FT solutions based on extra hardware components can further be classified as follows [30]:

1. MLI FT solution based on switch(es) addition.
2. MLI FT solution based on leg addition.
3. MLI FT solution based on module replacement.
4. MLI FT solution based on parallel redundant inverter.

2.1.1. MLI FT Solution Based on Switch(es) Addition (SA)

In this MLI FT solution, the redundant switch(es) is added in the original MLI topology in order to provide redundant switching states. These redundant states generate voltage levels that are lost under faulty conditions. (a) The first solution is to add redundant switches, parallel or series, to the main switches. These solutions are reviewed in [30]. Higher switch count, higher conduction losses, and higher cost are the main drawbacks of the first solution. (b) The second solution is to add redundant switches in such a position that they can tolerate maximum faulty conditions. The merits of the second solution are less switches, lower cost, and single-switch fault tolerance. Reduced voltage levels and the inability to tolerate multiple-switch faults are the drawbacks of this second solution. The second solution is better than the first solution. Generally, this second solution is employed in those MLI topologies that cannot tolerate a few single-switch faults and result in a complete system shutdown. This second solution is investigated in [23,28].

2.1.2. MLI FT Solution Based on Leg Addition (LA)

In this MLI FT solution, a set of switches forming a leg (it is referred to as a redundant leg) is attached to the original MLI topology to generate redundant switching states. In case of any switch fault, these redundant paths are utilized to compensate for the lost voltage levels. Fault tolerance to single- and/or multiple-switch faults and the ability to preserve more voltage levels (as compared to the SA solution) are the merits of this solution. The main drawbacks of this solution include a greater number of switches, higher cost, and non-utilization of redundant switches under healthy conditions. This solution is reviewed in [30]. This solution is investigated in various recently developed single-phase FT MLIs [3,31,34,35] and three-phase FT MLIs [36].

2.1.3. MLI FT Solution Based on Module Replacement (MR)

This MLI FT solution is applicable to modular MLIs (MMLIs) and cascaded MLIs (CMLIs). In this solution, a faulted module is replaced with a healthy module (known as a redundant module) if a fault occurs in any module to allow for continuous power supply. The significant advantage of this solution is that it is easy to control. The major drawbacks are the higher cost and large size. This solution is reviewed in [30].

2.1.4. MLI FT Solution Based on Parallel Redundant Inverter (PRI)

This MLI FT solution is utilized in critical applications, i.e., in industries. In this solution, a similar inverter (referred to as a redundant inverter) is connected in parallel with the original inverter. This redundant inverter only works in the condition of complete failure of the original inverter. The merit of this solution is an uninterruptable power supply without causing economic losses. The drawbacks of this solution include the very high cost and greater space requirements. This solution is reviewed in [30].

2.2. MLI FT Solutions Based on NEHC

In this MLI FT solution, there is no need for extra hardware components to provide FT operation [22]. The MLI FT solutions free of additional components can further be classified as follows [22,30]:

1. MLI FT solution based on inherent hardware redundancy.
2. MLI FT solution based on module bypass.
3. MLI FT solution based on modulation scheme.

2.2.1. MLI FT Solution Based on Inherent Hardware Redundancy (IHR)

This MLI FT solution utilizes the inherent hardware redundancy of the original MLI topology without any need for additional switches. Such MLI topologies have redundant switching states for generating a particular voltage level. In the case of any switch fault, the MLI continues to deliver power through available healthy switches. The merits of this solution are 100% utilization of all switches under healthy conditions and no requirement for additional hardware components. The drawbacks of this solution include reduced voltage levels and the inability to tolerate some switch faults. This solution was investigated in various recently developed FT MLIs [31,37–42].

2.2.2. MLI FT Solution Based on Module Bypass (MB)

This MLI FT solution is applicable to MMLIs and CMLIs. In this solution, if a fault occurs in any module, the faulted module is bypassed, and the output power is supplied with the remaining healthy module(s). The merit of this solution includes no requirement for additional hardware components. The drawback of this solution is that it provides output power at reduced voltage levels. This solution is reviewed in [30].

2.2.3. MLI FT Solution Based on Modulation Scheme (MS)

This MLI FT solution is applicable in the case of three-phase MLIs. The three-phase MLI output results in an unbalanced output voltage due to a fault in one or more phases.

Hence, it results in the complete shutdown of the MLI. However, a modulation-scheme-based MLI FT solution maintains a balanced output voltage by modifying the modulation strategy under post-fault conditions. Some of the modulation schemes utilized in this technique are phase-shift pulse width modulation (PS-PWM) and space-vector PWM. The FT operation of these modulation schemes is explained and reviewed in [30,33,43,44]. The merit of this solution includes no requirement for additional hardware components. The drawbacks of this solution include complex mathematical computations and output power at reduced voltage levels.

2.3. Hybrid Solutions

Hybrid solutions may either use additional components and MS solution, MB and MS solution, or miscellaneous methods to tolerate faults. Multiple fault tolerance and higher reliability are the merits of this solution. The drawbacks of this solution include reduced voltage levels under multiple faults and complex control. These solutions are investigated in [45–47].

3. Review of Single-Phase FT MLI Topologies

In this section, several single-phase FT MLIs, with their constructional features, merits, and limitations, are reviewed and compared based on proposed novel parameters. The topologies are named from TP1 to TP53.

3.1. Single-Phase FT MLIs

3.1.1. TP1 and TP2

Other authors modified a cross-connected-sources-based MLI (CCS-MLI) and T-type MLI for FT operation in [28] by connecting switches S_1 and S_2, respectively. Both MLIs are single-phase five-level inverters. The circuit for FT CCS-MLI is shown in Figure 4a. The circuit for FT T-type MLI is shown in Figure 4b. A phase opposition disposition sinusoidal PWM (POD-SPWM) scheme is employed for generating switching pulses in both the topologies. Both the topologies use the SA FT solution for fault tolerance.

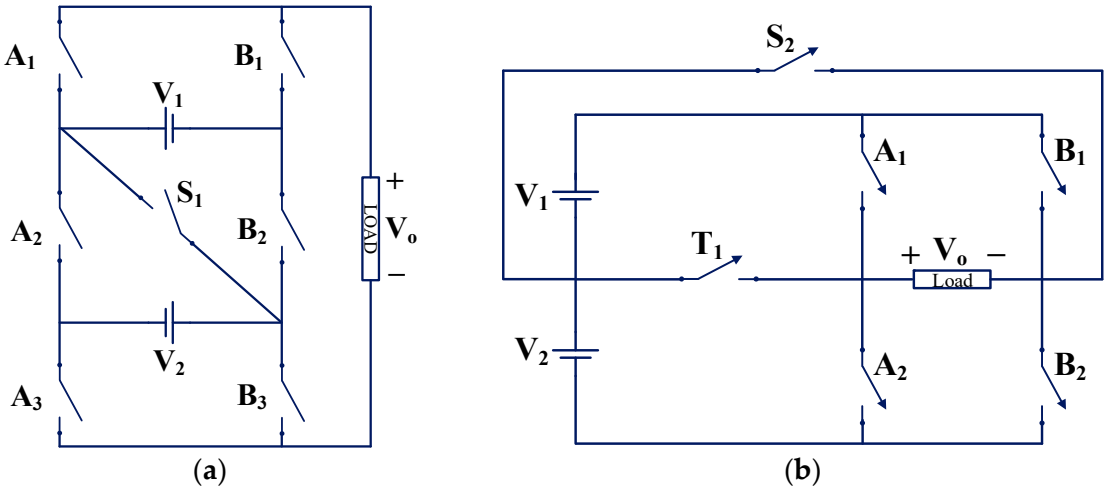

Figure 4. (**a**) Single-phase five-level modified CCS-MLI with fault tolerance capability (TP1) [28]. (**b**) Single-phase five-level modified T-type inverter with fault tolerance capability (TP2) [28].

The topology TP1, i.e., modified CCS-MLI (as shown in Figure 4a), comprises two DC sources, one bidirectional switch (S_1), and six unidirectional switches. It can generate only three levels for a single-switch OC fault in faulty conditions. This topology can tolerate a single-switch OC fault in the circuit with a loss of levels. A lower number of switches is the merit of the topology. The limitations of topology are the inability to tolerate multiple-switch faults and decreased output voltage levels under post-fault conditions.

The topology TP2, i.e., modified T-type inverter (as shown in Figure 4b), comprises two DC sources, two bidirectional switches (T_1 and S_2), and four unidirectional switches. It can generate three or five levels for a single-switch OC fault in faulty conditions. The topology can tolerate a single-switch OC fault in the circuit with a loss of levels. A lower number of switches is the merit of the topology. The limitations of topology are the inability to tolerate multiple-switch faults and decreased output voltage levels under post-fault conditions.

3.1.2. TP3 and TP4

Other authors modified a single-phase five-level Packed U-Cell MLI (PUC-MLI) and single-phase seven-level symmetrical and asymmetrical MLI topology for FT operation in [48] by connecting switches S_1 and S_2, and R_1 and R_2, respectively. The circuit for FT PUC-MLI (TP3) is shown in Figure 5a. The circuit for FT symmetrical and asymmetrical MLI (TP4) is shown in Figure 5b. A level-shifted SPWM (LS-SPWM) scheme is employed for generating switching pulses in both topologies. Both topologies use the SA FT solution for fault tolerance.

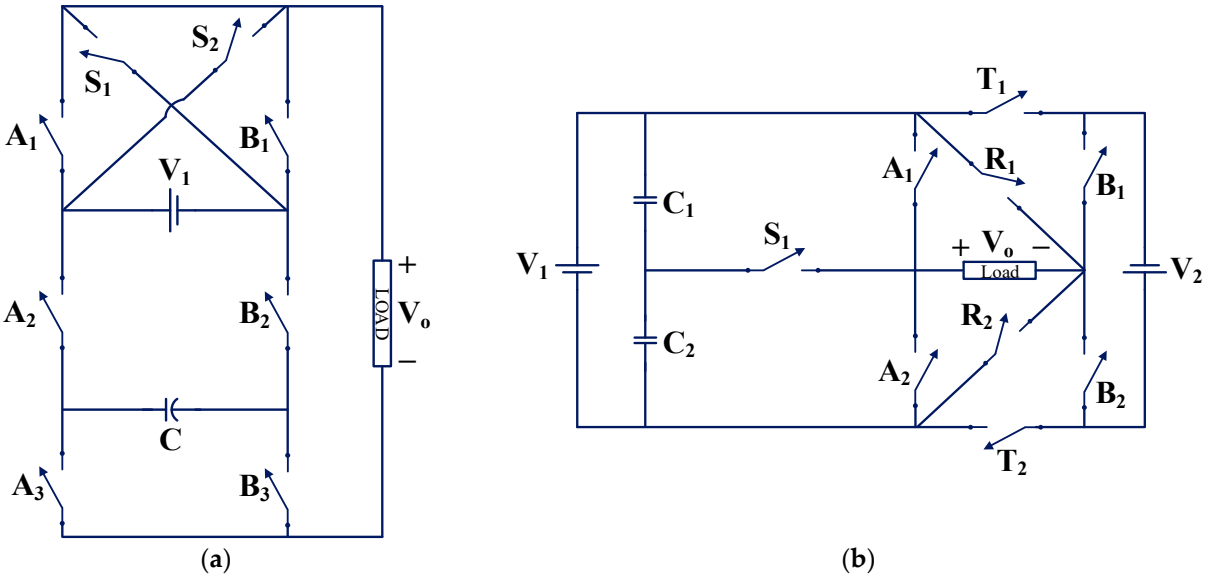

Figure 5. (**a**) Single-phase five-level modified PUC MLI with fault tolerance capability (TP3) [48]. (**b**) Single-phase seven-level modified symmetrical and asymmetrical MLI with fault tolerance capability (TP4) [48].

The topology TP3, i.e., modified PUC MLI (as shown in Figure 5a), comprises one DC source, one capacitor, and eight unidirectional switches. It can generate three or five levels for a single-switch OC fault in a faulty condition. This topology can tolerate a single-switch OC fault in the circuit with a loss of levels. A smaller number of switches is the merit of the topology. The limitations of topology are the inability to tolerate multiple-switch faults and decreased output voltage levels under post-fault conditions.

The topology TP4, i.e., modified symmetrical and asymmetrical MLI (as shown in Figure 5b), comprises two DC sources, two capacitors, three bidirectional switches, and six unidirectional switches. Switches (S_1, R_1, and R_2) are bidirectional switches. It can generate five levels for a single-switch OC fault in a faulty condition. This topology can tolerate a single-switch OC fault in the circuit with a loss of levels. A smaller number of switches is the merit of the topology. The limitations of topology are the use of bidirectional switches, the inability to tolerate multiple-switch faults, and decreased output voltage levels under post-fault conditions.

3.1.3. TP5

A single-phase five-level FT MLI topology (TP5) is proposed in [34]. The authors added a redundant leg to the full-bridge NPC inverter topology to make it FT. TP5 has a main inverter and a redundant leg. TP5 comprises two DC sources, four diodes, four fuses, and fourteen unidirectional switches. The circuit is shown in Figure 6. The LS-SPWM scheme is used for generating the gating pulses in the topology. The topology uses the LA FT solution for fault tolerance. This topology is able to generate voltage levels by using the same or a smaller number of switching devices (IGBTs). The efficiency achieved in the post-fault condition is the same or even higher than in the pre-fault condition. The topology tolerates SC faults by using fewer fuses compared to other topologies. The topology can handle single and multiple OC and SC switch faults in one or two legs of the main inverter circuit. The merits of the topology include no use of bidirectional switches, fewer conducting switches in post-fault conditions, and the preservation of all output voltage levels for all single and multiple (two switches) switch faults. No utilization of redundant legs' switches under healthy conditions is the limitation of the topology.

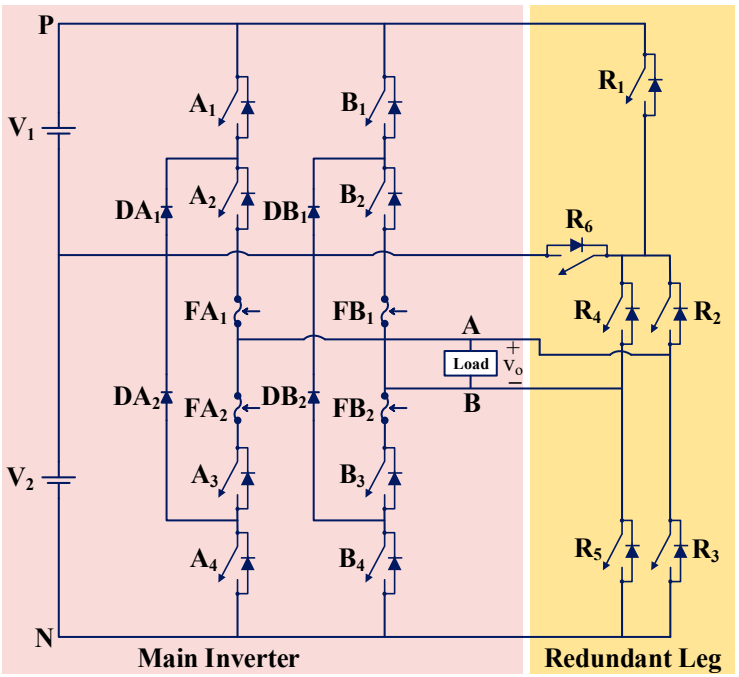

Figure 6. Single-phase five-level FT MLI (TP5) [34].

3.1.4. TP6

Another single-phase five-level FT MLI topology (TP6) is proposed in [3]. The authors combined a conventional flying capacitor (FC) leg, cascaded H-bridge (CHB) leg, and active neutral point clamped (ANPC) leg to develop FT topology. TP6 has a main inverter and a redundant leg. It comprises one DC source, one capacitor, and twelve unidirectional switches. The circuit is shown in Figure 7. The LS-SPWM scheme is employed for generating switching pulses in the topology. The topology uses the LA FT solution for fault tolerance. The topology has the ability to tolerate single- and multiple-switch OC faults in the circuit. The merits of topology include no use of bidirectional switches, the efficiency achieved in post-fault conditions being the same as the healthy operation, preservation of the output power in the faulty condition same as in the healthy operation, and self-balancing of flying capacitor voltage. No utilization of redundant legs' switches under healthy conditions is the limitation of the topology. The topology was used in [49] for more electric aircraft applications.

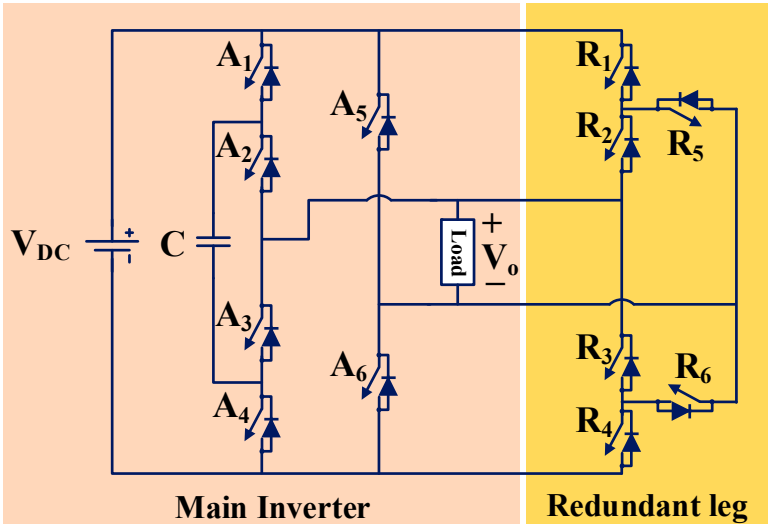

Figure 7. Single-phase five-level FT MLI (TP6) [3].

3.1.5. TP7

A single-phase nine-level FT MLI topology (TP7) is proposed in [35]. The FT MLI consists of the main inverter and the redundant leg. The main inverter is composed of two three-level flying capacitor legs. TP7 comprises two DC sources, two capacitors, and sixteen unidirectional switches. The circuit is shown in Figure 8.

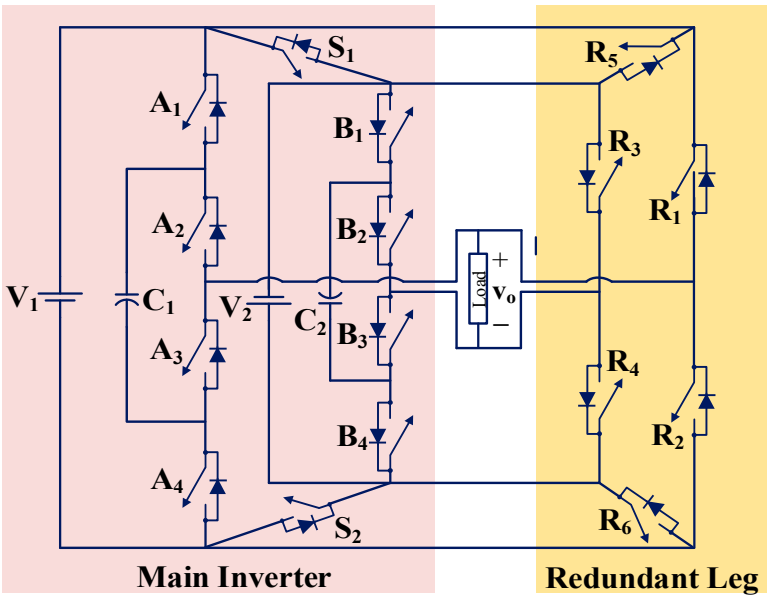

Figure 8. Single-phase nine-level FT MLI (TP7) [35].

The phase-disposition SPWM (PD-SPWM) scheme is employed for generating switching pulses in the topology. The topology uses the LA FT solution for fault tolerance. The topology does not include any bidirectional switches. The topology can generate voltage levels under single and multiple OC faults while preserving output power both in healthy and post-fault operations. The merits of this topology include the efficiency achieved in post-fault conditions being higher as compared with the healthy operation, the ability to tolerate single- and multiple-switch OC and SC faults, and the self-balancing of the flying capacitor voltage both in healthy and post-fault operation. No utilization of redundant legs' switches under healthy conditions is the limitation of the topology.

3.1.6. TP8 and TP9

A single-phase five-level FT MLI topology is proposed in [31]. Two topologies are proposed in the publication. In the first topology (TP8), there is a loss of levels in output voltage after a fault; this is termed partial fault tolerance. In the second topology (TP9), there is no loss of levels in output voltage after a fault; this is termed complete fault tolerance. The circuits for partial and complete fault tolerance are shown in Figure 9a,b, respectively. The LS-SPWM scheme is employed for generating switching pulses in both topologies. TP8 and TP9 use IHR and LA FT solutions, respectively, for fault tolerance.

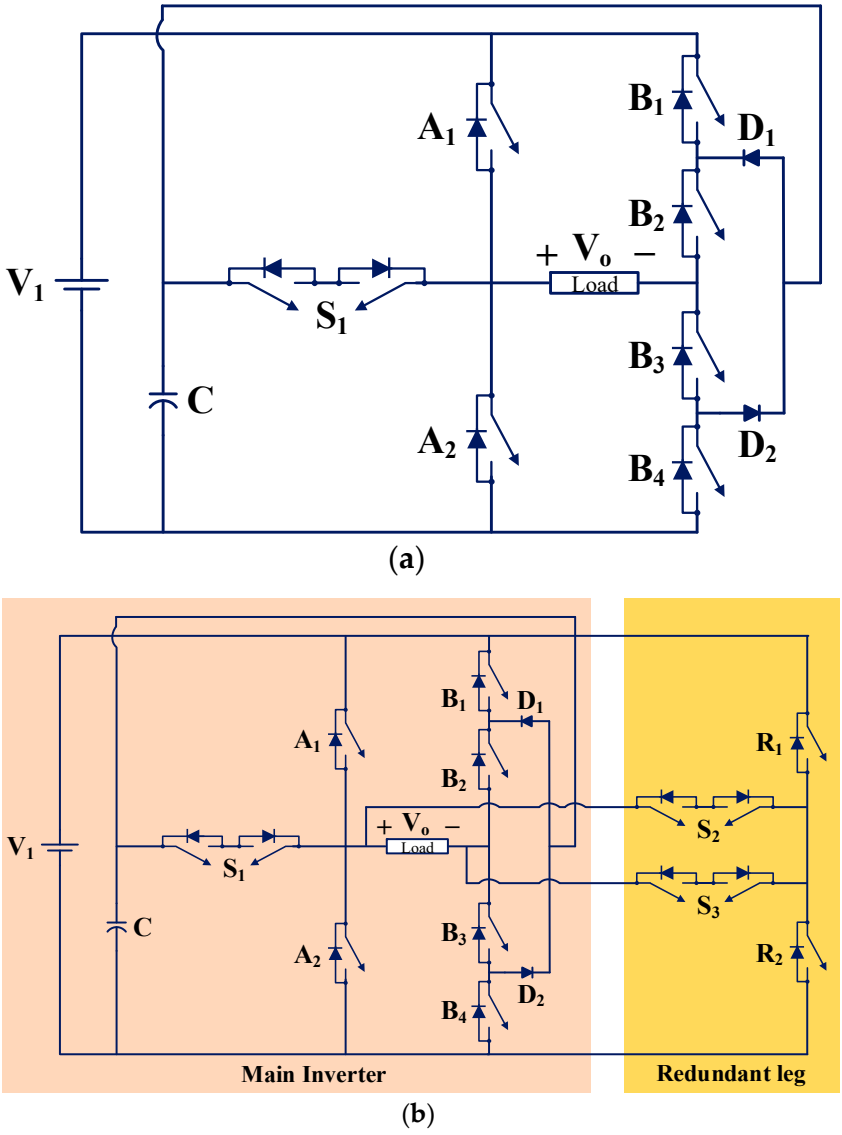

Figure 9. (**a**) Single-phase five-level MLI for partial fault tolerance (TP8) [31]. (**b**) Single-phase five-level MLI for complete fault tolerance (TP9) [31].

The first part of the publication discusses the partial solution to the faults since there are losses of levels. TP8 (as shown in Figure 9a) comprises one DC source, one capacitor, two diodes, one bidirectional switch, and six unidirectional switches. This partial solution topology can be generalized for any number of levels by cascading basic topology. The topology achieves the self-balancing of the capacitor voltage both in healthy and faulty operation. The capacitor voltage ripples increase under post-fault operation. This topology can tolerate all single-switch OC and SC faults in the circuit with loss of levels. The merits of the topology include the self-balancing of the capacitor voltage under faulty conditions,

100% utilization of all switches under healthy conditions, and FT MLI can be extended by cascading similar units depending upon the number of output voltage levels needed. The use of bidirectional switches, the inability to preserve all output voltage levels for all single-switch faults, the increase in capacitor voltage ripples under post-fault operating conditions, and the inability to tolerate multiple-switch faults are the limitations of the topology.

The second part of the publication discusses the complete solution to the faults since there is no loss of levels. TP9 (as shown in Figure 9b) has a main inverter and a redundant leg. It consists of one DC source, one capacitor, two diodes, three bidirectional switches, and eight unidirectional switches. The topology TP9 achieves the self-balancing of the capacitor voltage both in healthy and faulty operation. The capacitor voltage ripples under post-fault operation remain the same as in pre-fault operation. The topology can tolerate all single-switch OC and SC faults in the circuit without loss of levels. The redundant legs' switches are only utilized in the case of a fault. The merits of the topology include the self-balancing of the capacitor voltage under faulty conditions, no increase in capacitor voltage ripples under post-fault operating conditions, and the preservation of all output voltage levels for all single-switch faults. The use of bidirectional switches, higher cost, no utilization of redundant legs' switches under healthy conditions, higher number of conducting switches under post-fault condition (hence it results in higher switching power loss under post-fault condition), and inability to tolerate multiple-switch faults are the limitations of the topology.

3.1.7. TP10

An FT MLI topology (TP10) presented in [50] by modifying the FT MLI topology given in [31]. The authors added a novel redundant leg to the main inverter. TP10 consists of one DC source, one capacitor, two diodes, one bidirectional switch, and twelve unidirectional switches. The circuit of topology TP10 is shown in Figure 10.

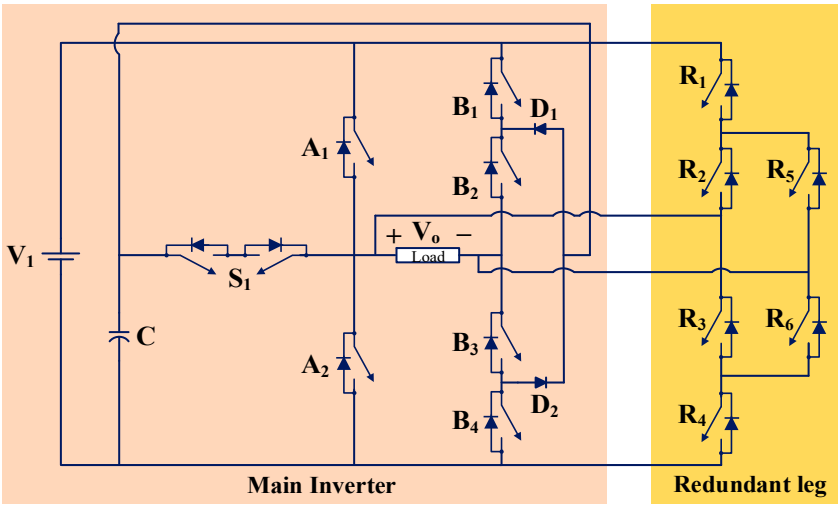

Figure 10. Single-phase five-level FT MLI (TP10) [50].

The LS-SPWM scheme is employed for generating switching pulses in the topology. TP10 uses the LA FT solution for fault tolerance. The main inverter has a drawback of lesser post-fault efficiency as compared to pre-fault efficiency. This limitation is solved in this work by proposing a novel redundant leg. The novel redundant leg provides an overload-current-sharing characteristic, which is absent in the original topology. It is capable of working at reduced voltage levels if a switch fault occurs. It can tolerate single-switch OC faults with preserved power. Overload-current-handling capability by utilizing redundant legs' switches under healthy conditions is the merit of the topology. The limitations of the topology include a higher number of conducting switches under post-fault conditions (hence, it results in higher switching power loss under post-fault conditions).

3.1.8. TP11

A single-phase five-level FT MLI topology (TP11) is proposed in [51]. The topology TP11 is capable of tolerating OC and SC faults for single and multiple switches. TP11 comprises one DC source, one capacitor, two diodes, four fuses, and twelve unidirectional switches. The circuit of the single-phase five-level FT MLI is shown in Figure 11. It consists of a main inverter and a redundant leg. The main inverter topology is constructed by using the legs of conventional three-level neutral point clamped inverter and three-level flying capacitor inverter. The redundant leg is constructed by using a conventional three-level cascaded H-bridge (CHB) inverter. The LS-SPWM scheme is employed for generating switching pulses in the topology. TP11 uses the LA FT solution for fault tolerance. The main feature of the topology is to tolerate single- and multiple-switch faults, no matter whether they are OC or SC faults. The merits of the topology include inherent capacitor voltage balancing under both single-switch and multiple-switch faults; multiple-switch faults tolerance for any pair, triplet, or quadruple of switches; and output power will remain to preserve post-fault, similar to pre-fault output power. Decreased voltage levels (leading to higher harmonic distortions of the output voltage waveform) and no utilization of redundant legs' switches under healthy operation are the limitations of the topology.

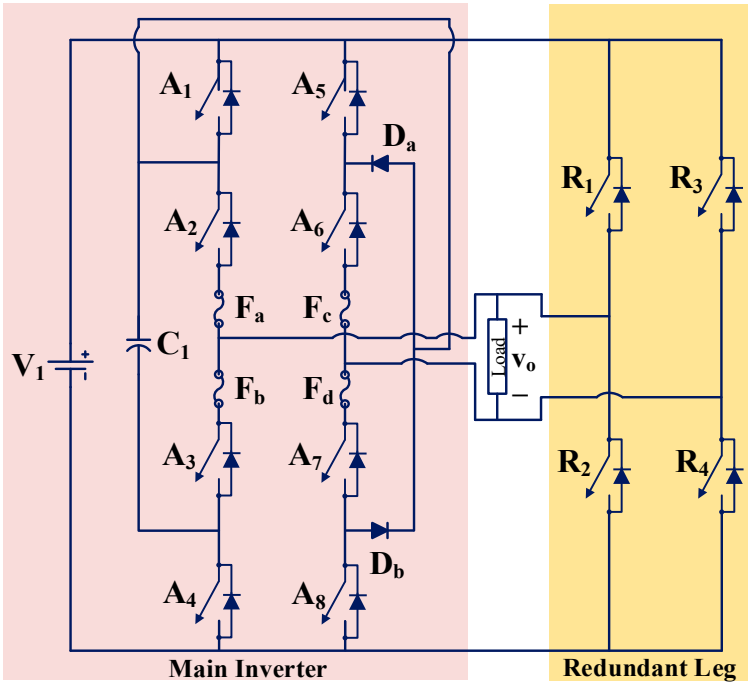

Figure 11. Single-phase five-level FT MLI (TP11) [51].

3.1.9. TP12

A single-phase five-level FT MLI (TP12) is proposed in [37]. The authors named it DITHB, i.e., developed inverter with two half-bridges. TP12 comprises two DC sources and nine unidirectional switches. The circuit for TP12 is shown in Figure 12. The LS-SPWM scheme is employed for generating switching pulses in the topology. TP12 uses the IHR FT solution for fault tolerance. In faulty conditions, the topology can generate three levels for a single-switch OC fault. This topology can tolerate a single-switch OC fault in the circuit with a loss of levels. A higher number of conducting switches under healthy and faulty conditions is the limitation of the topology. The following are the merits of the topology:

- It has switching states which can bring two sources in parallel. Due to this advantage, it is possible to maintain power in post-fault similar to the pre-fault power.
- Single unit can be connected in series depending upon the number of output voltage levels required.

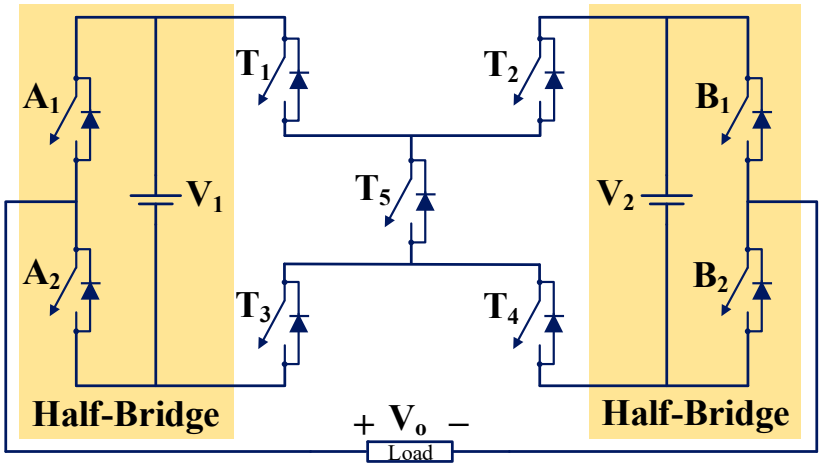

Figure 12. Single-phase five-level DITHB inverter with fault tolerance capability (TP12) [37].

3.1.10. TP13

A single-phase thirteen-level FT MLI (TP13) is proposed in [52]. TP13 comprises three DC sources, three bidirectional switches, and six unidirectional switches. The circuit for TP13 is shown in Figure 13. The nearest level control PWM (NLC-PWM) scheme is employed for generating switching pulses in the topology. TP13 uses the SA FT solution for fault tolerance. This topology can tolerate a single-switch OC fault in the circuit with a loss of levels. The merit of the topology includes the ability to tolerate all single-switch OC faults. The limitations of the topology include a higher number of bidirectional switches and the inability to tolerate multiple-switch faults.

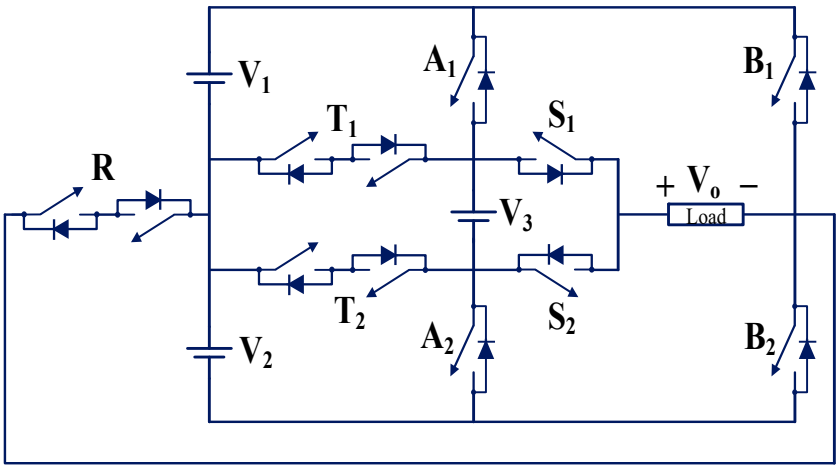

Figure 13. Single-phase thirteen-level inverter with fault tolerance capability (TP13) [52].

3.1.11. TP14

The authors of another study modified a single-phase nine-level cascaded H-bridge (CHB) inverter with an asymmetrical configuration for fault tolerance in [39]. TP14 comprises two DC sources and ten unidirectional switches. The circuit for TP14 is shown in Figure 14. A hybrid modulation technique comprising NLC and LS-PWM is employed for generating switching pulses in the topology. TP14 uses the SA FT solution for fault tolerance. It can tolerate switch OC faults. It utilizes two redundant switches, R_1 and R_2, to provide fault tolerance under faulty conditions. The merit of the topology includes the ability to tolerate all single-switch OC faults. The inability to tolerate all multiple-switch OC and SC faults is the limitation of the topology.

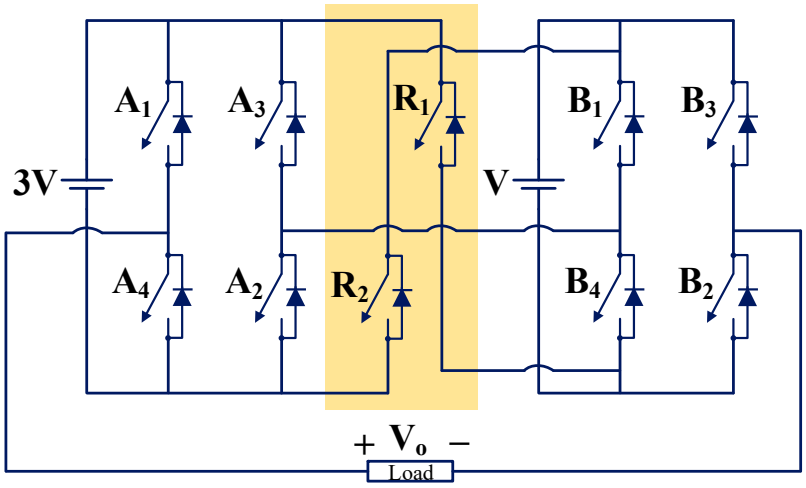

Figure 14. Single-phase nine-level CHB inverter with fault-tolerance capability (TP14) [39].

3.1.12. TP15 and TP16

A generalized single-phase FT MLI is proposed in [53]. It can work in symmetric and asymmetric modes. When all the sources are equal, the mode of operation is called symmetric, whereas when sources are different, the mode of operation is called asymmetric. The circuit of a single-phase nine-level FT MLI (TP15) is shown in Figure 15a. The circuit of a single-phase seventeen-level FT MLI (TP16) is shown in Figure 15b. TP15 and TP16 comprise four DC sources and twelve unidirectional switches. The modified level-shifted carrier PWM (LSCPWM) scheme is used for generating the gating pulses in the topology. Both topologies use the IHR FT solution for fault tolerance. The proposed topology can tolerate single- and multiple-switch OC and SC faults. The proposed topology can operate under both symmetric and asymmetric modes. The proposed topology can generate higher voltage levels with respect to its modular structure. The switches R_{1a} and R_{a2} operate only in the case of switch R_1 and R_2 failure. The ability to tolerate both source and/or switches faults and the ability to extend topology depending upon the number of output voltage levels requirement are the merits of the topology. No utilization of switches R_{1a} and R_{a2} under healthy operation is the limitation of the topology.

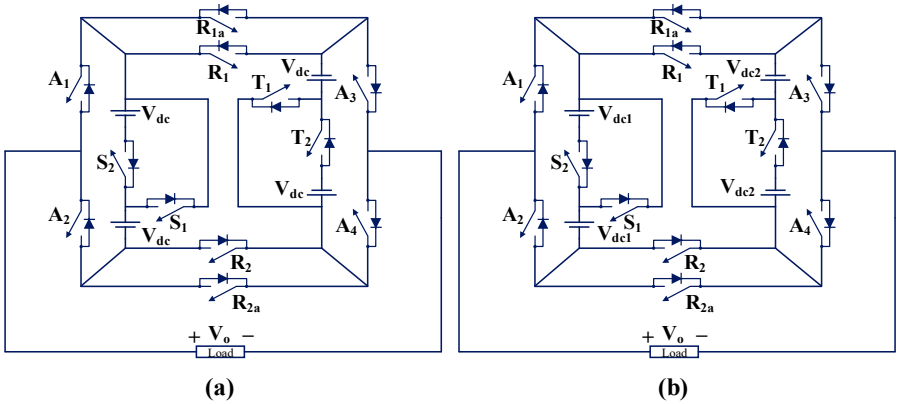

Figure 15. Single-phase symmetric FT MLI: (**a**) nine-level symmetric configuration (TP15) and (**b**) seventeen-level asymmetric configuration (TP16) [53].

3.1.13. TP17

A single-phase five-level FT MLI (TP17) is proposed in [8]. TP17 comprises two DC sources, two diodes, one bidirectional switch, and six unidirectional switches. The circuit of TP17 is shown in Figure 16. The phase-disposition sinusoidal PWM (PD-SPWM) scheme is employed for generating switching pulses in the topology. The topology uses the SA FT

solution for fault tolerance. If a fault occurs in the source and/or switch, the topology can generate three voltage levels instead of five levels. The output voltage magnitude reduces after the fault. Therefore, to maintain the rated output voltage, a transformer is used. The merits of the topology are as follows:

- TP17 topology is capable of tolerating faults caused by the failure of the source.
- TP17 reduces the uneven charging of batteries that is caused to partial shading or hotspots on one side of the PV panels due to energy-balancing between sources.

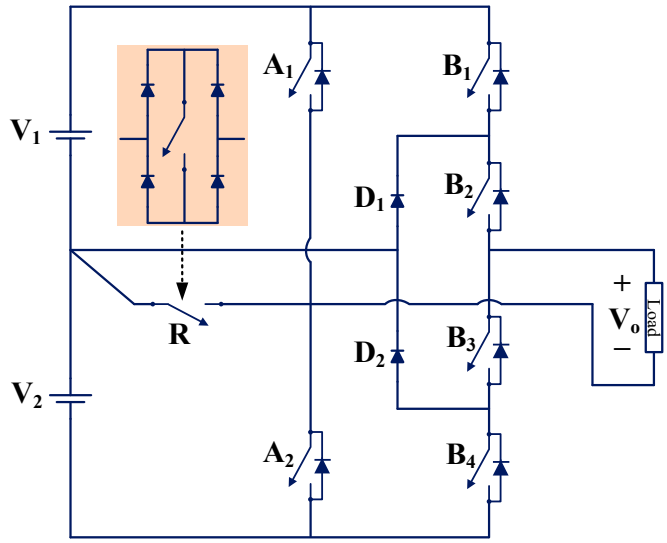

Figure 16. Single-phase five-level FT MLI (TP17) [8].

The limitations of the topology are as follows:

- Use of bidirectional switch.
- Inner leg switches in the NPC leg are not FT.
- Implementation of center-tapped transformer.

3.1.14. TP18

A single-phase nine-level FT MLI topology (TP18) is proposed in [40]. TP18 comprises two DC sources, one capacitor, three bidirectional switches, and six unidirectional switches. The circuit of TP18 is shown in Figure 17.

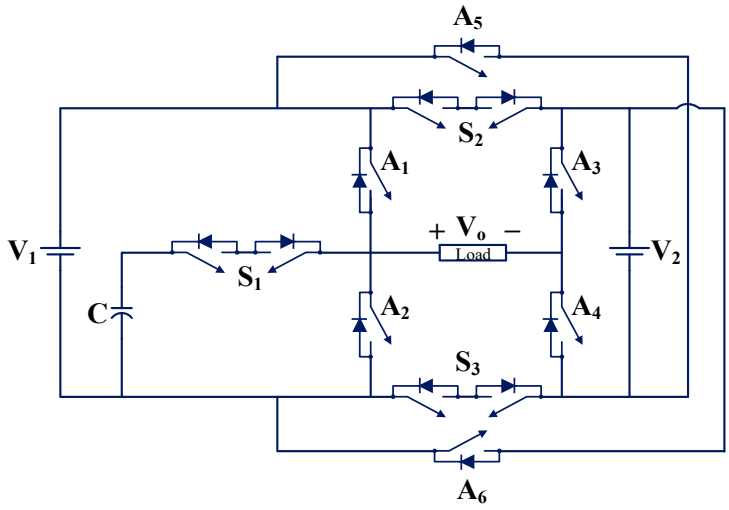

Figure 17. Single-phase nine-level FT MLI (TP18) [40].

The PD-SPWM scheme is used for generating the gating pulses in the topology. The topology uses the IHR FT solution for fault tolerance. The topology can generate nine levels, using three bidirectional and six unidirectional switches and a capacitor under healthy operation. It does not need any redundant leg or extra switches. It is capable of working at reduced voltage levels if a switch fault occurs. The merits of the topology include 100% utilization of all switches in healthy condition, and the switching scheme proposed in the work achieves the natural capacitor voltage balancing without any external circuit. The use of a higher number of bidirectional switches is the limitation of the topology.

3.1.15. TP19

A single-phase five-level FT MLI (TP19) is proposed in [54]. The proposed inverter topology is capable of tolerating both OC and SC faults on all single switches and some multiple switches. TP19 comprises two DC sources, nine fuses, three bidirectional switches, and six unidirectional switches. The circuit of TP19 is shown in Figure 18. The LS-SPWM scheme is used for generating the gating pulses in the topology. The topology uses the SA FT solution for fault tolerance. The switches A_6 and A_7 operate only under FT operation. A fast-acting switch is used in series with each switch to detect SC faults. The controller sees a short circuit as an open circuit and provides separate operations for OC and SC faults. The merits of the topology include the ability to tolerate both OC and SC faults and the ability to provide rated output voltage and power under any switch fault. The use of a higher number of bidirectional switches and no utilization of switches A_6 and A_7 under healthy conditions are the limitations of the topology.

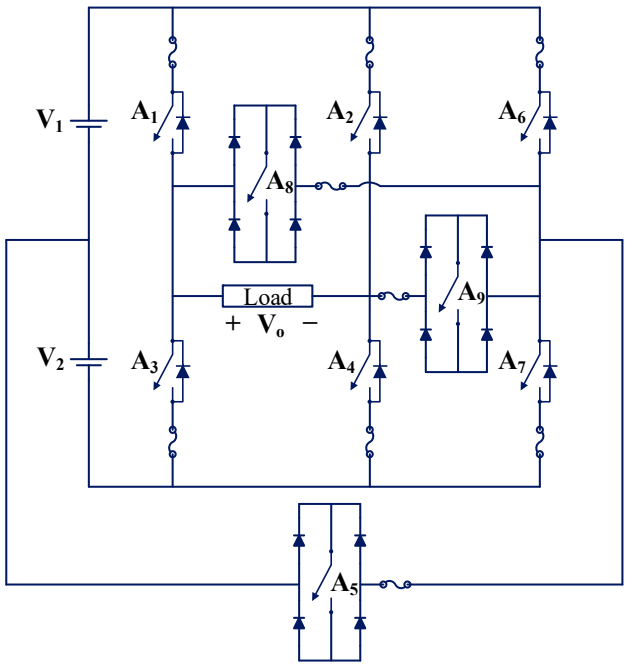

Figure 18. Single-phase five-level FT MLI (TP19) [54].

3.1.16. TP20

A single-phase nine-level FT MLI topology (TP20) is proposed in [41]. TP20 comprises two DC sources, two capacitors, three bidirectional switches, and six unidirectional switches. The circuit of TP20 is shown in Figure 19. The LS-SPWM scheme is used for generating the gating pulses in the topology. The topology uses the IHR FT solution for fault tolerance. The topology is unable to provide rated output voltage and power in some faults. A smaller number of conducting switches under post-fault conditions is the merit of the topology. The use of a higher number of bidirectional switches and the inability to tolerate fault on the

bidirectional switch connected between the capacitor and load terminal are the limitations of the topology [35,55].

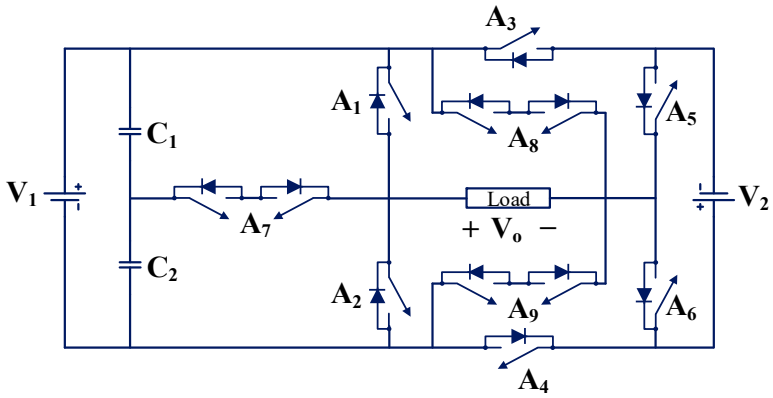

Figure 19. Single-phase nine-level FT MLI (TP20) [41].

3.1.17. TP21

A single-phase eleven-level FT MLI topology (TP21) is proposed in [56]. TP21 comprises three DC sources, three bidirectional switches, and six unidirectional switches. The circuit of TP21 is shown in Figure 20. The publication deals only with OC faults. The switches A_8 and A_9 work only under faulty conditions. The NLC-PWM scheme is employed for generating switching pulses in the topology. The topology uses the SA FT solution for fault tolerance. The ability to tolerate all single-switch OC faults and some multiple-switch OC faults is the merit of the topology. The use of bidirectional switches, no utilization of switches A_8 and A_9 under healthy conditions, and the inability to tolerate SC faults are the limitation of the topology.

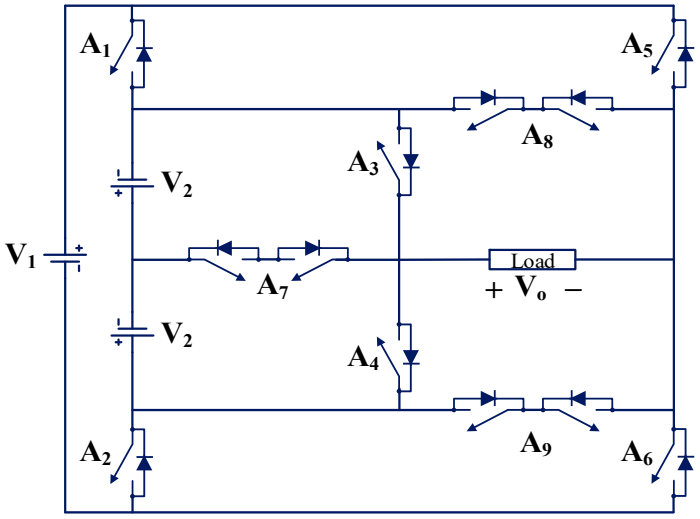

Figure 20. Single-phase eleven-level FT MLI (TP21) [56].

3.1.18. TP22

A fifteen-level FT MLI topology (TP22) is proposed in [57], and it is shown in Figure 21. TP22 comprises four DC sources, one bidirectional switch, and ten unidirectional switches. This FT MLI topology does not utilize additional hardware components to create redundancy for FT operation. It utilizes inherent hardware redundancy for fault tolerance. It is able to tolerate all single-switch OC faults. A combination of nearest level modulation (NLM) and selective harmonic elimination (SHE) is employed for generating switching pulses in the topology. The topology uses the IHR FT solution for fault tolerance. The merit

of the topology includes 100% utilization of all switches under healthy conditions. The use of a higher number of DC sources is the limitation of the topology.

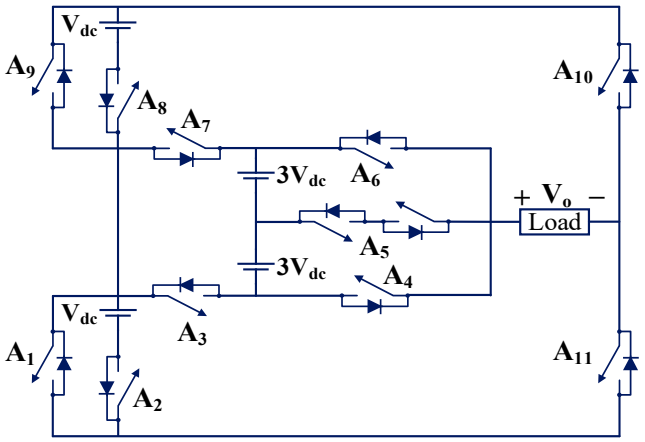

Figure 21. Single-phase fifteen-level FT MLI (TP22) [57].

3.1.19. TP23

Other authors proposed a five-level FT MLI topology (TP23) in [38] by modifying a five-level modified PUC (MPUC5) inverter topology, which is shown in Figure 22. Three redundant switches (A_7, A_8, and A_9) are added to the original MPUC5. TP23 comprises two DC sources and nine unidirectional switches. This topology can tolerate all single-switch OC faults. The NLC-PWM scheme is used for generating the gating pulses in the topology. The topology uses the SA FT solution for fault tolerance. The use of a smaller number of switches is the merit of the topology. The limitations of the topology include the inability to tolerate SC faults and multiple-switch faults.

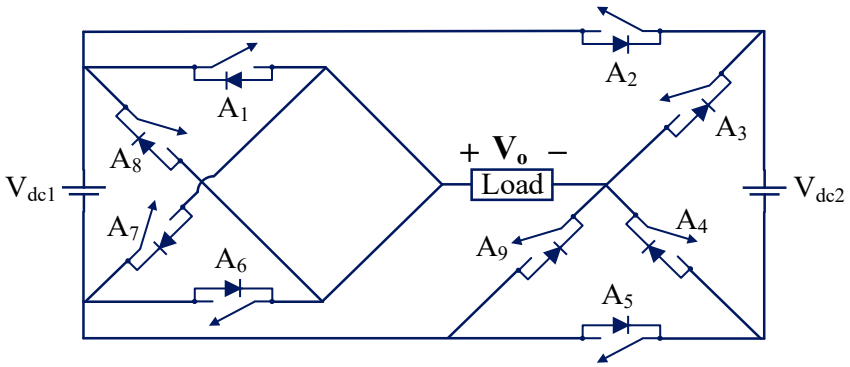

Figure 22. Single-phase five-level FT MLI (TP23) [38].

3.1.20. TP24 and TP25

The authors in [42] proposed FT MLI topologies (TP24 and TP25), and these are shown in Figure 23. Topologies TP24 and TP25 comprise four DC sources and twelve unidirectional switches. Two switches, A_{7r} and A_{8r}, are used as redundant switches. It can generate 9 levels and 17 levels of waveform depending upon the values of DC sources. The topology TP24 generates nine levels with $V_{dc1} = V_{dc2} = V_{dc3} = V_{dc4} = V$ in the symmetric mode of operation. The topology TP25 generates 17 levels with $V_{dc1} = V_{dc2} = V$, and $V_{dc3} = V_{dc4} = 3V$ in the asymmetric mode of operation. It can tolerate all single- and multiple-switch OC faults. The modified LSCPWM scheme is used for generating the gating pulses in the topology. TP24 and TP25 use the IHR FT solution for fault tolerance. The merit of the topology includes its lower total standing voltage (*TSV*). The inability to tolerate the SC fault on all switches is the limitation of the topology.

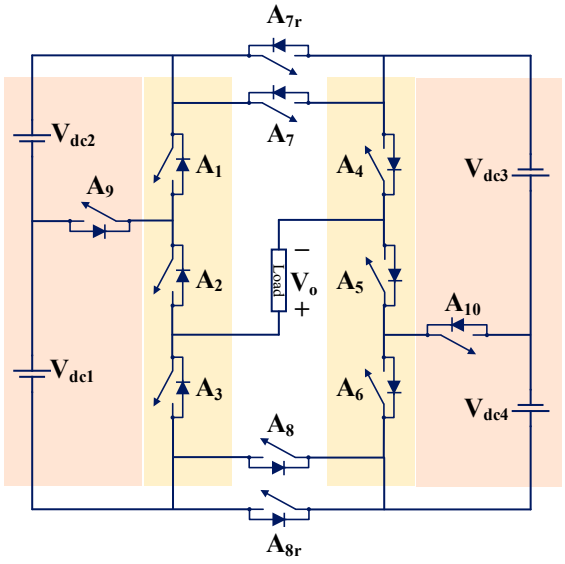

Figure 23. Single-phase FT MLI (symmetric configuration = TP24; asymmetric configuration = TP25) [42].

3.1.21. TP26

A single-phase five-level FT MLI is proposed in [58], and it is shown in Figure 24. It comprises two DC sources, two bidirectional switches, and four unidirectional switches. The POD-SPWM scheme is used for creating the gating pulses in the topology. The topology uses the IHR FT solution for fault tolerance. The topology can tolerate OC single-switch faults in all switches and some OC double-switch faults. The topology can be generalized for the "N" number of levels. This FT MLI topology can be used in solar-based charging station applications. The topology is used in [59] for wave power plant applications. The merit of the topology includes 100% utilization of all switches under healthy conditions. The use of bidirectional switches is the limitation of the topology.

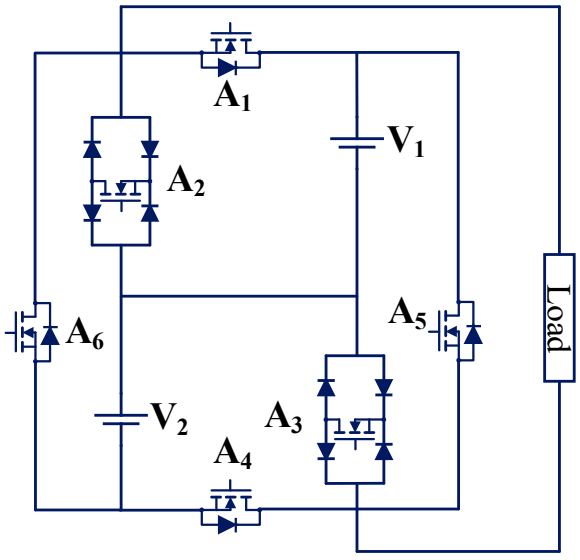

Figure 24. Single-phase five-level FT MLI (TP26) [58].

3.1.22. TP27 and TP28

A single-phase seven-level FT MLI is proposed in [60], and it is shown in Figure 25. It comprises three DC sources, five bidirectional switches, and five unidirectional switches. The topology is modular in nature. It can be generalized for the "N" number of levels. The seven-level FT MLI can be modified and made into a nine-level FT MLI by adding a module consisting

of one DC source, one bidirectional switch, and one unidirectional source. The POD-SPWM scheme is used for creating the gating pulses in the topology. TP28 uses the IHR FT solution for fault tolerance. The topology can tolerate OC single- and double-switch faults in switches and OC and SC faults in sources. The modular nature and ability to extend the topology for the "N" number of output voltage levels are the benefits of this topology.

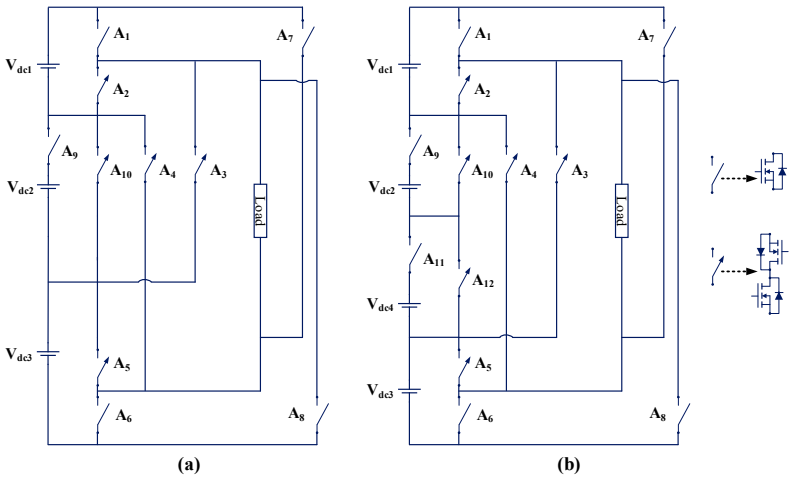

Figure 25. (**a**) Single-phase seven-level FT MLI (TP27). (**b**) Single-phase nine-level FT MLI (TP28) [60].

3.1.23. TP29

A single-phase FT MLI is proposed in [61] for multi-string photovoltaic (PV) applications, and it is shown in Figure 26. It consists of two H-bridges and comprises four DC sources, two bidirectional switches, and ten unidirectional switches. This topology can synthesize a nine-level output voltage under symmetric conditions ($V_1 = V_2 = V_3 = V_4 = V/4$). This topology can synthesize a thirteen-level output voltage under asymmetric conditions ($V_1 = V_2 = V/6$ and $V_3 = V_4 = V/3$). The PD-SPWM scheme is used for creating the gating pulses in the topology. The topology uses the IHR FT solution for fault tolerance. In the event of partial shading of PV panels, TP29 is capable of energy balancing between sources.

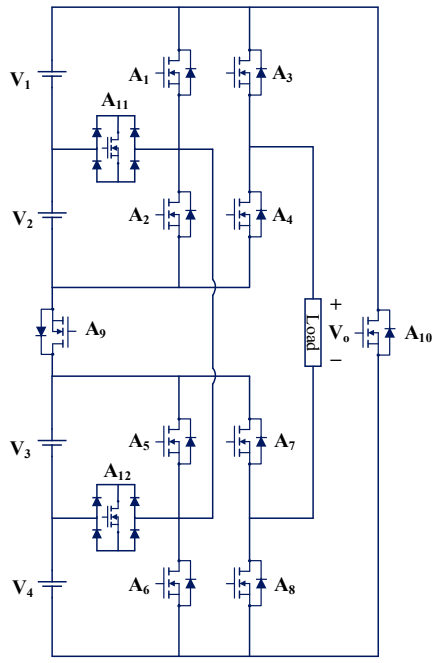

Figure 26. Single-phase FT MLI (TP29) [61].

3.1.24. TP30

A single-phase seven-level FT MLI is proposed in [62], as shown in Figure 27. It comprises three DC sources, two bidirectional switches, and eight unidirectional switches. The NLC-PWM technique is employed for generating the switching pulses in the topology. The topology uses the IHR FT solution for fault tolerance. The topology can be extended to the "N" number of output voltage levels. It can tolerate single-switch OC faults on switches.

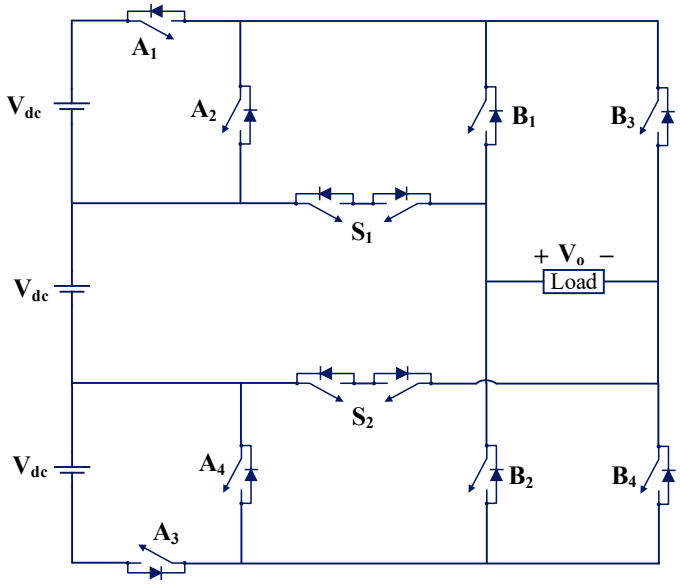

Figure 27. Single-phase seven-level FT MLI (TP30) [62].

3.1.25. TP31

A single-phase nine-level FT MLI is proposed in [63], and it is shown in Figure 28. It comprises four DC sources, three bidirectional switches, and six unidirectional switches. The POD-SPWM scheme is used for creating the gating pulses in the topology. The topology uses the SA FT solution for fault tolerance. It can tolerate single- and multiple-switch OC faults.

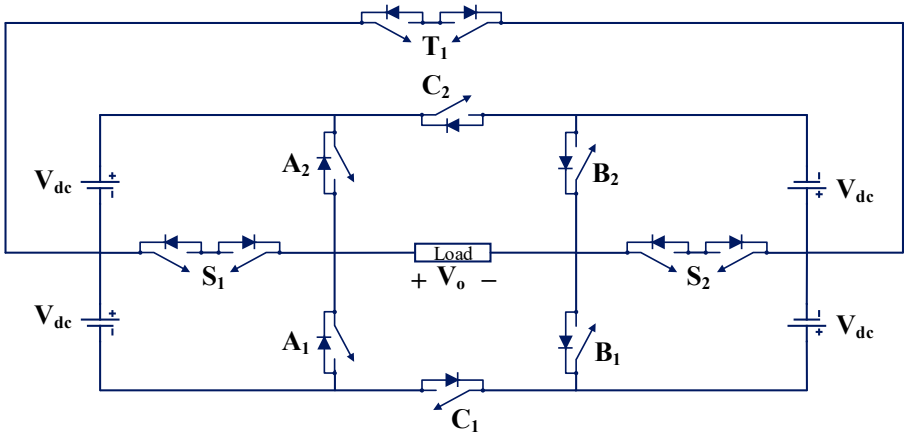

Figure 28. Single-phase nine-level FT MLI (TP31) [63].

3.1.26. TP32

A single-phase five-level FT MLI is proposed in [64], and it is shown in Figure 29. It comprises two DC sources, two bidirectional switches, and four unidirectional switches. The NLC-PWM technique is employed for generating the switching pulses in the topology. The topology uses the IHR FT solution for fault tolerance. The topology can be extended to

the "N" number of output voltage levels. TP32 can tolerate OC/SC faults in sources. It can also tolerate all single OC faults and some multiple OC faults in switches.

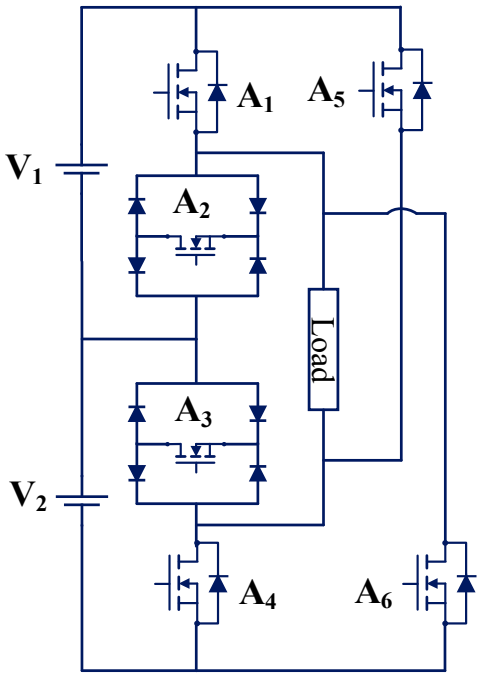

Figure 29. Single-phase five-level FT MLI (TP32) [64].

3.1.27. TP33

A single-phase FT MLI is proposed in [65], and it is shown in Figure 30. It comprises three DC sources, four bidirectional switches, and four unidirectional switches. This topology can synthesize a seven-level output voltage under symmetric conditions (same DC sources) and term it TP33A. This topology can synthesize a thirteen-level output voltage under asymmetric conditions (different DC sources) and term it TP33B. The NLC-PWM technique is employed for generating the switching pulses in the topology. The topology uses the IHR FT solution for fault tolerance. The topology can be extended to the "N" number of output voltage levels. TP33 can tolerate OC faults in all switches. A higher number of bidirectional switches is the limitation of this topology.

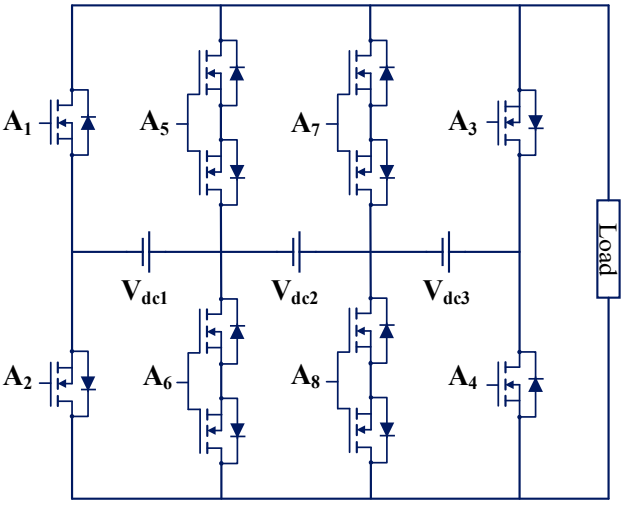

Figure 30. Single-phase FT MLI (TP33) [65].

3.1.28. TP34

A single-phase seven-level FT MLI is proposed in [66], and it is shown in Figure 31. It comprises three DC sources and eight unidirectional switches. A sine wave reference with an inverted sine carrier pulse generation scheme is used for creating the gating pulses in the topology. The topology uses the IHR FT solution for fault tolerance. It can tolerate all single-switch OC faults.

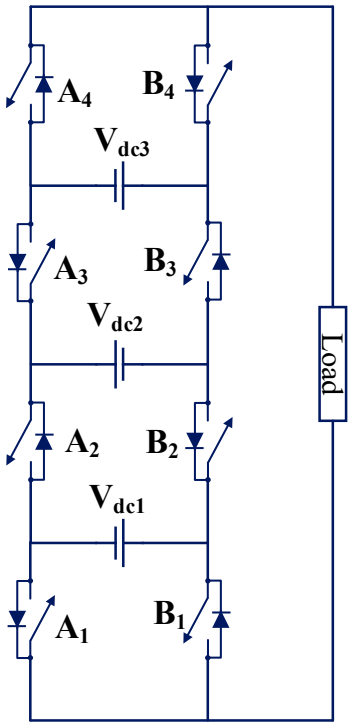

Figure 31. Single-phase seven-level FT MLI (TP34) [66].

3.1.29. TP35

A single-phase five-level FT MLI is proposed in [67], as shown in Figure 32. It comprises a single DC source, two capacitors, two bidirectional switches, and four unidirectional switches. The POD-SPWM scheme is used for creating the gating pulses in the topology. The topology uses the IHR FT solution for fault tolerance. TP35 can tolerate all single-switch OC faults. It can also tolerate any OC fault occurring in any leg of the H-bridge. This topology also achieves the self-balancing of the DC-link capacitors.

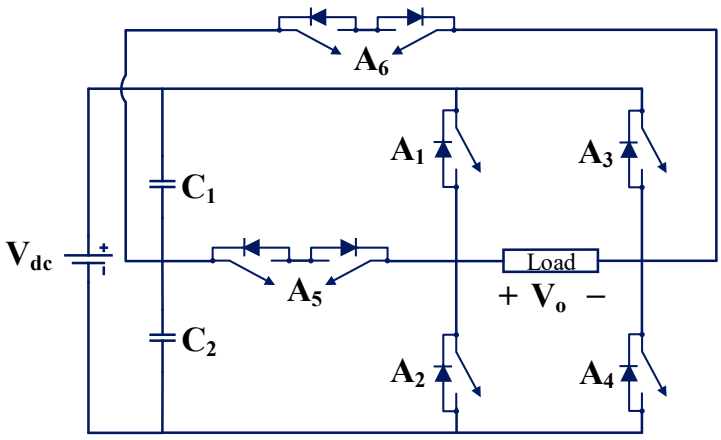

Figure 32. Single-phase five-level FT MLI (TP35) [67].

3.1.30. TP36

A single-phase seven-level FT MLI is proposed in [68], and it is shown in Figure 33. It comprises two DC sources, two capacitors, three bidirectional switches, and six unidirectional switches. The LS-SPWM scheme is used for creating the gating pulses in the topology. The topology uses the SA FT solution for fault tolerance. TP36 can tolerate all single-switch OC faults. This topology also achieves the self-balancing of the DC-link capacitors.

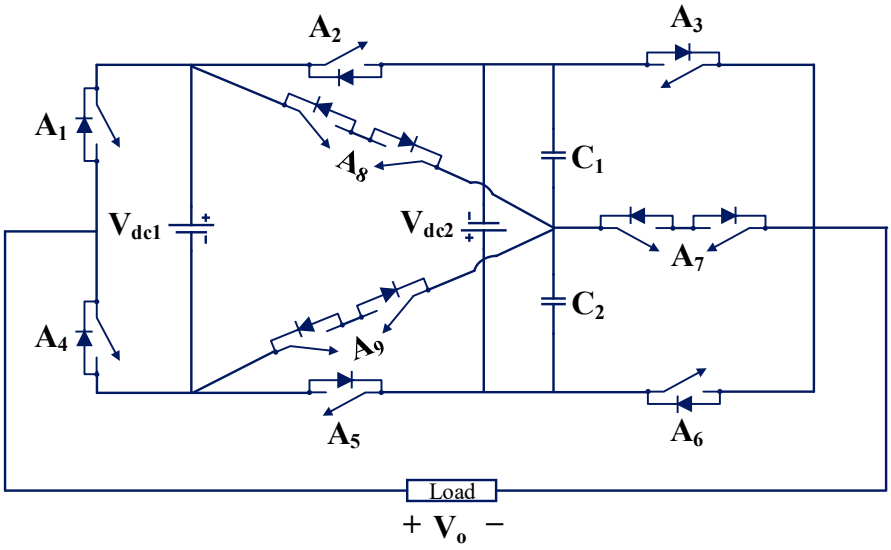

Figure 33. Single-phase seven-level FT MLI (TP36) [68].

3.1.31. TP37

A single-phase fifteen-level FT MLI is proposed in [69], and it is shown in Figure 34. It comprises a single DC source, eight capacitors, six bidirectional switches, and twenty-four unidirectional switches. The NLM-PWM scheme is used for creating the gating pulses in the topology. The topology uses the IHR FT solution for fault tolerance. TP37 can boost the input voltage seven times according to the concept of a switch capacitor. This topology can tolerate both OC and SC faults on single and multiple switches. This topology also achieves the self-balancing of the DC-link capacitors. The requirement of a single DC source is the merit of the topology.

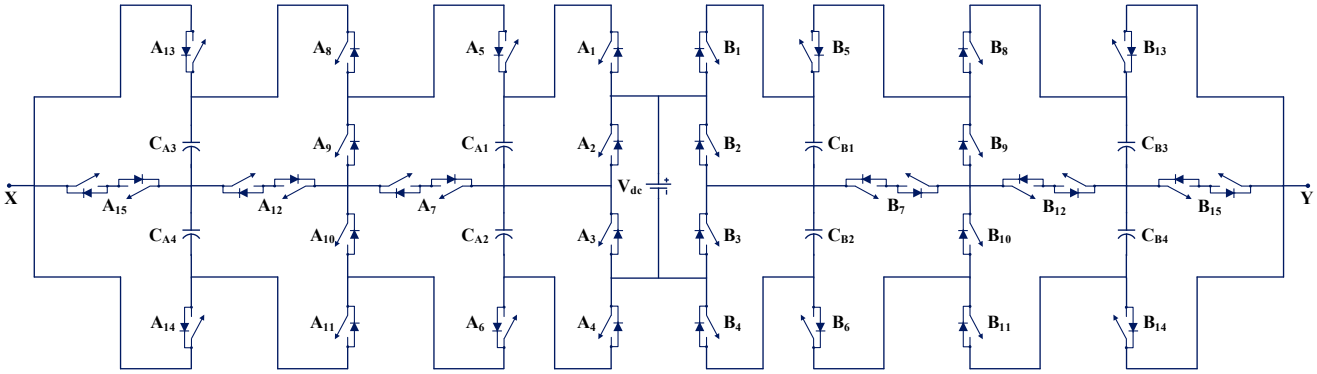

Figure 34. Single-phase fifteen-level FT MLI (TP37) [69].

3.1.32. TP38

A single-phase nine-level FT MLI is proposed in [70], and it is shown in Figure 35. It comprises four DC sources, two bidirectional switches, and eight unidirectional switches. POD-SPWM and NLC-PWM schemes are used for creating the gating pulses in the topology.

The topology uses the IHR FT solution for fault tolerance. TP38 can tolerate all single-switch OC faults. The requirement of a higher number of DC sources is the limitation of the topology.

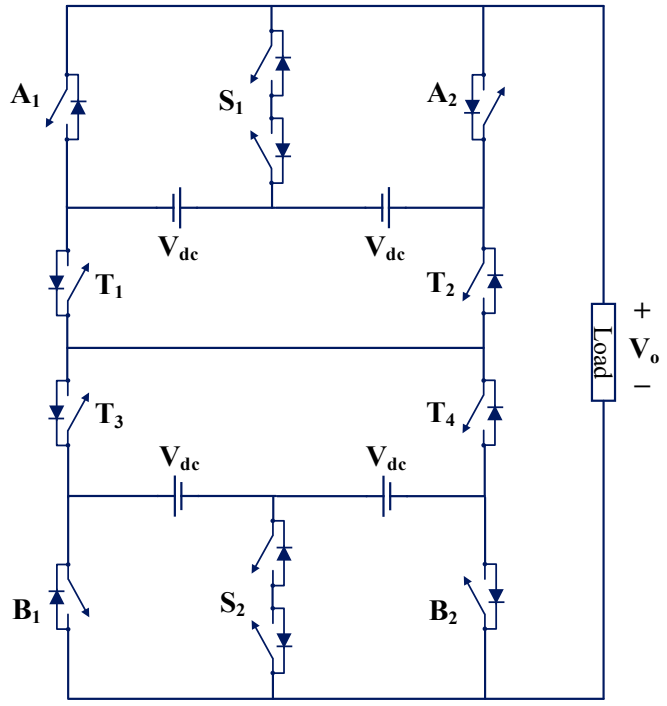

Figure 35. Single-phase nine-level FT MLI (TP38) [70].

3.1.33. TP39

A single-phase nine-level FT MLI is proposed in [71], and it is shown in Figure 36. It comprises two DC sources, two capacitors, four bidirectional switches, and six unidirectional switches. The LS-SPWM scheme is used for creating the gating pulses in the topology. The topology uses the SA FT solution for fault tolerance. TP39 achieves self-voltage balancing of DC-link capacitors under healthy and faulty conditions. The topology can tolerate both single-switch and multiple-switch faults. The use of a higher number of bidirectional switches is the limitation of the topology.

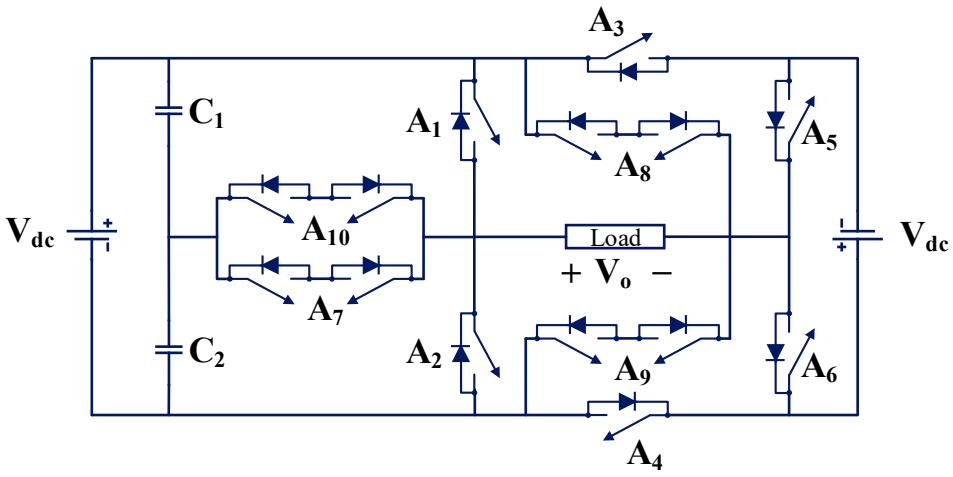

Figure 36. Single-phase nine-level FT MLI (TP39) [71].

3.1.34. TP40

A single-phase five-level FT MLI topology is proposed in [72]. The authors added a redundant leg to the conventional five-level NPC inverter to make it FT. The topology has a main inverter and a redundant leg. It comprises a single DC source, six diodes, two capacitors, and fourteen unidirectional switches. The circuit is shown in Figure 37. The LS-SPWM scheme is used for creating the gating pulses in the topology. The topology uses the LA FT solution for fault tolerance. TP40 can tolerate both single-switch and multiple-switch OC and SC faults.

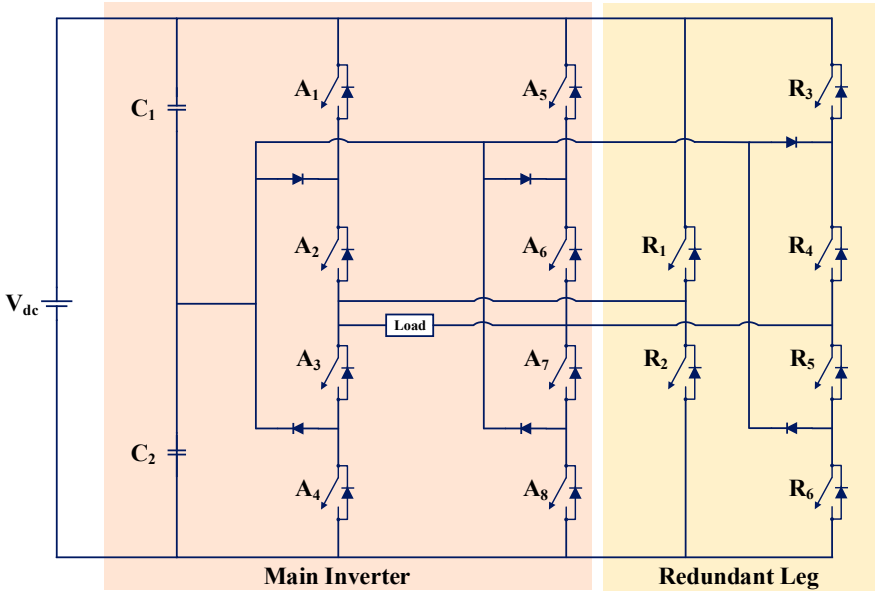

Figure 37. Single-phase five-level FT MLI (TP40) [72].

3.1.35. TP41

A single-phase seven-level FT MLI is proposed in [73], and it is shown in Figure 38. It comprises three DC sources, six relays, two bidirectional switches, and four unidirectional switches. The NLC-PWM technique is employed for generating the switching pulses in the topology. The topology uses the IHR FT solution for fault tolerance. TP41 can tolerate all single-switch OC faults.

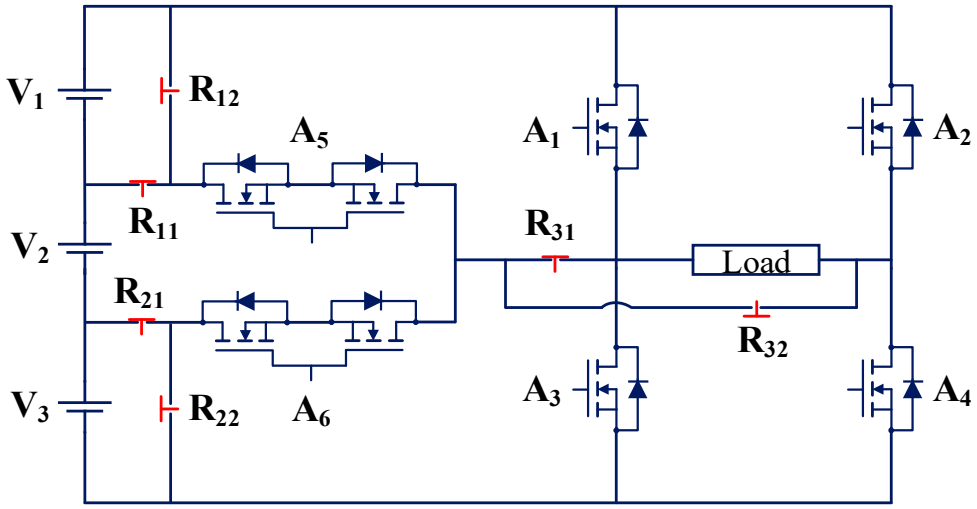

Figure 38. Single-phase seven-level FT MLI (TP41) [73].

3.1.36. TP42

A single-phase five-level FT MLI is proposed in [74], and it is shown in Figure 39. It comprises two DC sources, one bidirectional switch, and six unidirectional switches. The LS-PWM scheme is used for creating the gating pulses in the topology. The topology uses the IHR FT solution for fault tolerance. TP42 can tolerate all single-switch OC faults.

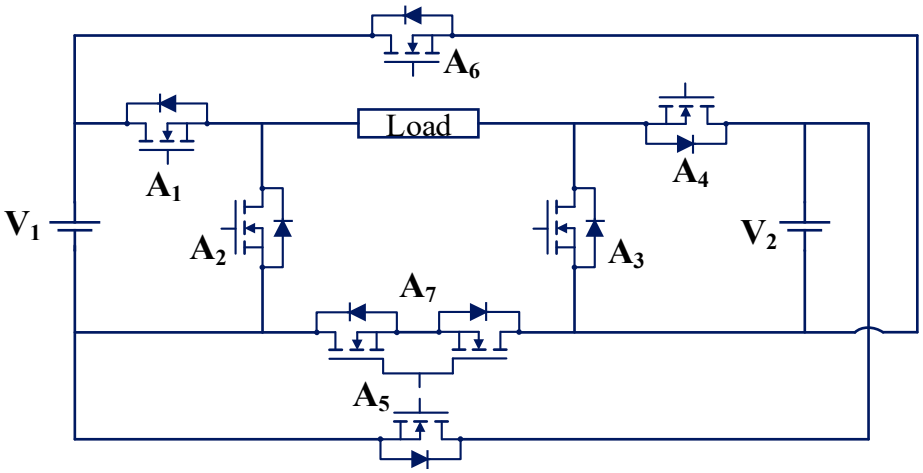

Figure 39. Single-phase five-level FT MLI (TP42) [74].

3.1.37. TP43

A single-phase nine-level FT MLI topology is proposed in [75]. The topology has a main inverter and a redundant leg. It comprises two DC sources, two capacitors, three bidirectional switches, and six unidirectional switches. The circuit is shown in Figure 40. The LS-SPWM scheme is employed for generating switching pulses in the topology. The topology uses the LA FT solution for fault tolerance. TP43 can tolerate all single-switch OC faults.

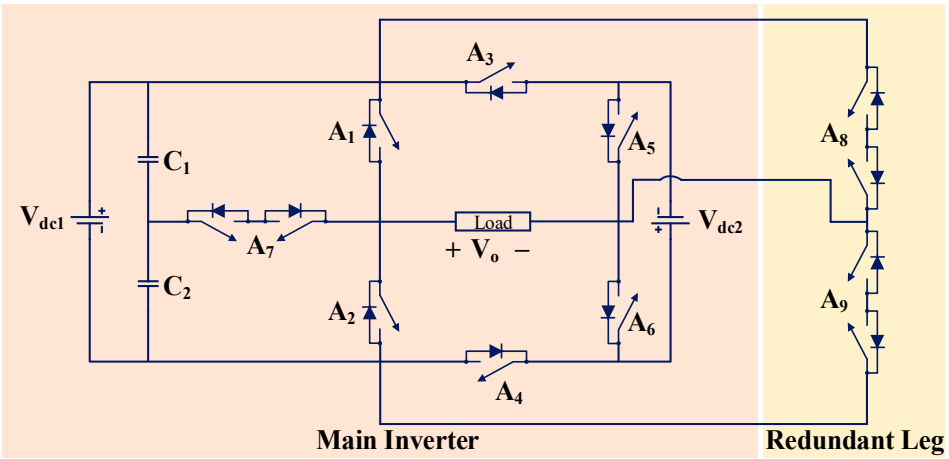

Figure 40. Single-phase nine-level FT MLI (TP43) [75].

3.1.38. TP44

A single-phase five-level FT MLI is proposed in [76], and it is shown in Figure 41. It comprises two DC sources, two relays, one bidirectional switch, and four unidirectional switches. Using relays, it is possible to bypass faulty switches and create symmetrical output voltages under faulty conditions. The LS-SPWM scheme is used for creating the gating pulses in the topology. The topology uses the IHR FT solution for fault tolerance. TP44 can tolerate all single-switch OC faults.

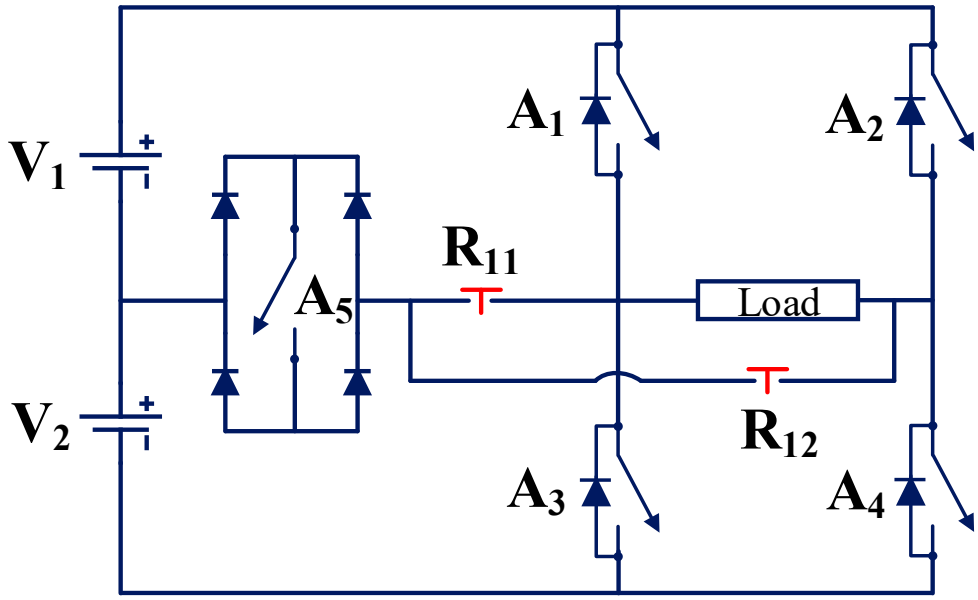

Figure 41. Single-phase five-level FT MLI (TP44) [76].

3.1.39. TP45

A single-phase nine-level FT MLI is proposed in [77], and it is shown in Figure 42. TP45 is the modified form of the topology that is proposed in [78]. It comprises two DC sources, two capacitors, and thirteen unidirectional switches. The LS-SPWM scheme is used for creating the gating pulses in the topology. The topology uses the IHR FT solution for fault tolerance. This work does not explore faults in CHB switches. TP45 can tolerate single- and multiple-switch OC faults. It achieves the self-voltage balancing of capacitors. The limitations of this topology are the inability to achieve a pre-fault voltage rating under post-fault conditions and the inability to tolerate faults on CHB switches.

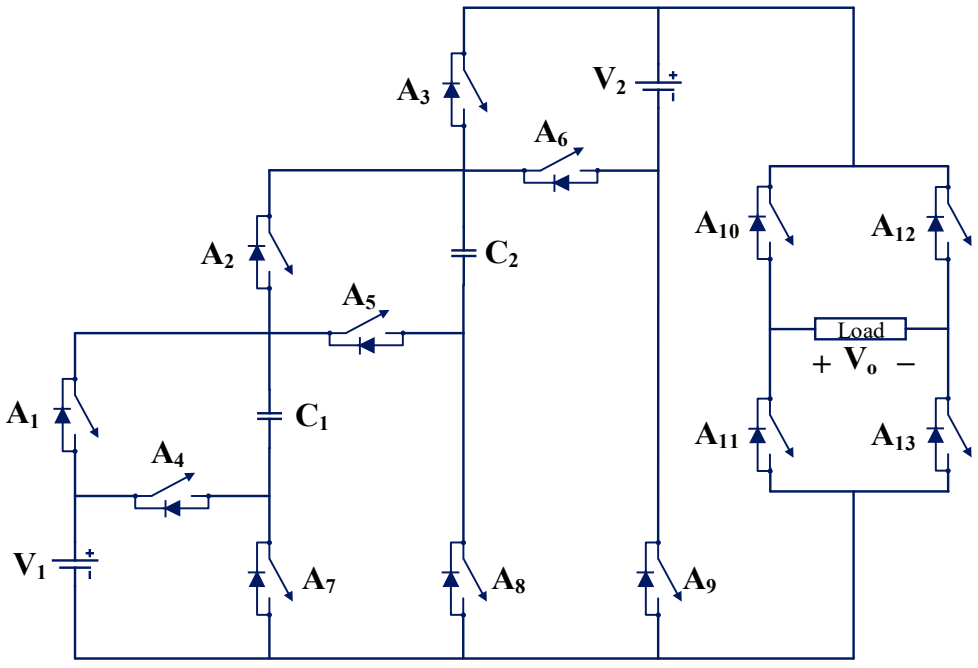

Figure 42. Single-phase nine-level FT MLI (TP45) [77].

3.1.40. TP46

A single-phase nine-level FT MLI topology is proposed in [79] for PV applications. The topology has the main inverter and the redundant leg. It comprises three DC sources, seven fuses, three bidirectional switches, and six unidirectional switches. The circuit is shown in Figure 43. A fast-acting fuse is connected to each switch in the main inverter. The LS-SPWM scheme is employed for generating switching pulses in the topology. The topology uses the LA FT solution for fault tolerance. TP46 can tolerate single- and multiple-switch OC and SC faults.

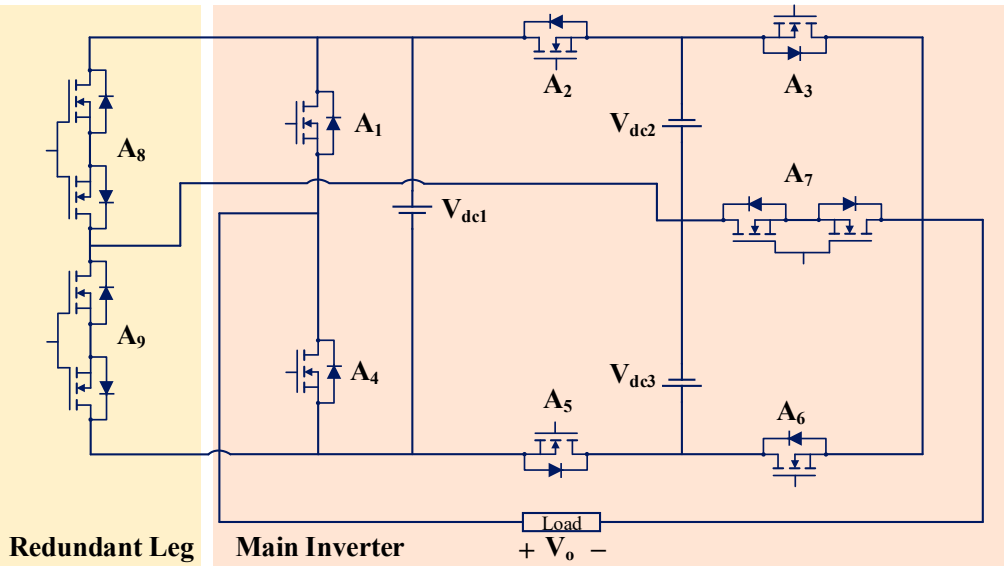

Figure 43. Single-phase nine-level FT MLI (TP46) [79].

3.2. Single-Phase FT MLIs Based on Module

3.2.1. TP47 and TP48

The authors of another study modified the CHB MLI and provided fault tolerance through their proposed scheme in [80]. The circuit of the single-phase seven-level FT MLI (TP47) (symmetric CHB, i.e., with the same sources) is shown in Figure 44a. The circuit of the single-phase fifteen-level FT MLI (TP48) (asymmetric CHB, i.e., with different sources) is shown in Figure 44b. This MLI topology consists of three CHB cells connected in cascade and one load-side H-bridge cell. The fault is removed by two relays. Each cell has one normally open (NO) and one normally closed (NC) conductor of each relay. The load-side H-bridge cell has two normally open (NO) and two normally closed (NC) conductors of each relay. The authors proposed an FT scheme for this MLI. The cascaded full-bridge CHB cells reconfigure to cascaded half-bridge CHB cells when the first fault occurs. The cascaded half-bridge CHB cells reconfigure to series-connected dc sources when a second fault occurs. This is the basic principle of this FT scheme. TP47 and TP48 use MB FT solution for fault tolerance.

The merits of the topology include the use of a smaller number of relays, low voltage stress exerted on healthy switches in case of fault, and utilization of all dc voltage sources under post-fault conditions. The limitations of the topology are as follows:

- Load side CHB cannot be made FT with fewer devices [3].
- Cannot generate pre-fault power after multiple-switch faults [35].

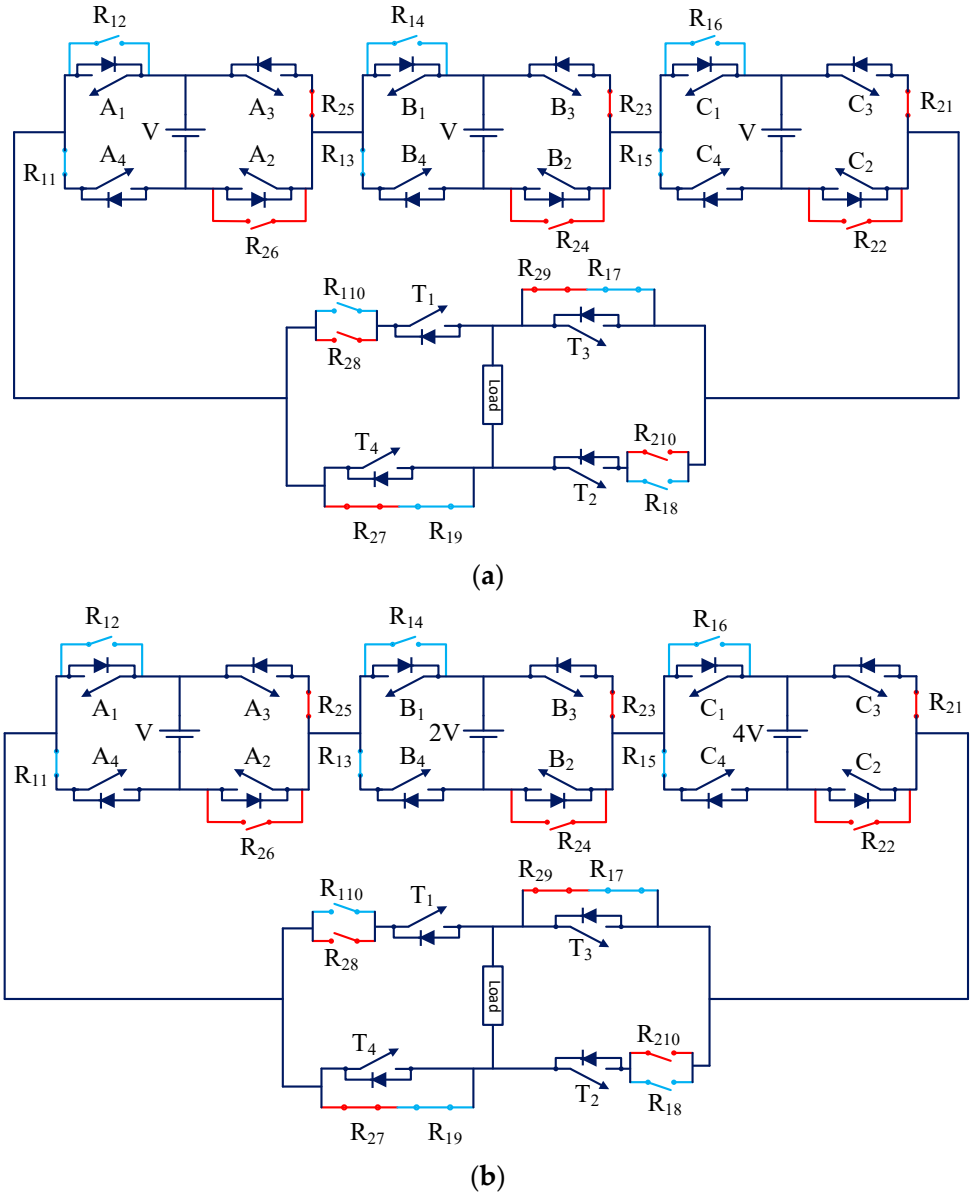

Figure 44. (**a**) Single-phase seven-level FT MLI (TP47) [80]. (**b**) Single-phase fifteen-level FT MLI (TP48) [80].

3.2.2. TP49

An FT structure and control scheme for CHB MLI are presented in [81]. The circuit diagram of the proposed single-phase seven-level FT MLI is shown in Figure 45. Each CHB module has four relays. The topology uses MB FT solution for fault tolerance. In any module's switch fault (OC or SC fault), the proposed control scheme eliminates the defected module from the circuit. The MLI continues the power supply with reduced voltage levels, with the remaining healthy modules. The merit of the topology includes the ability to tolerate both OC and SC switch faults. The limitations of the topology are as follows:

- High voltage stress is exerted on healthy switches in case of fault [80].
- Higher conduction losses.
- Higher cost.

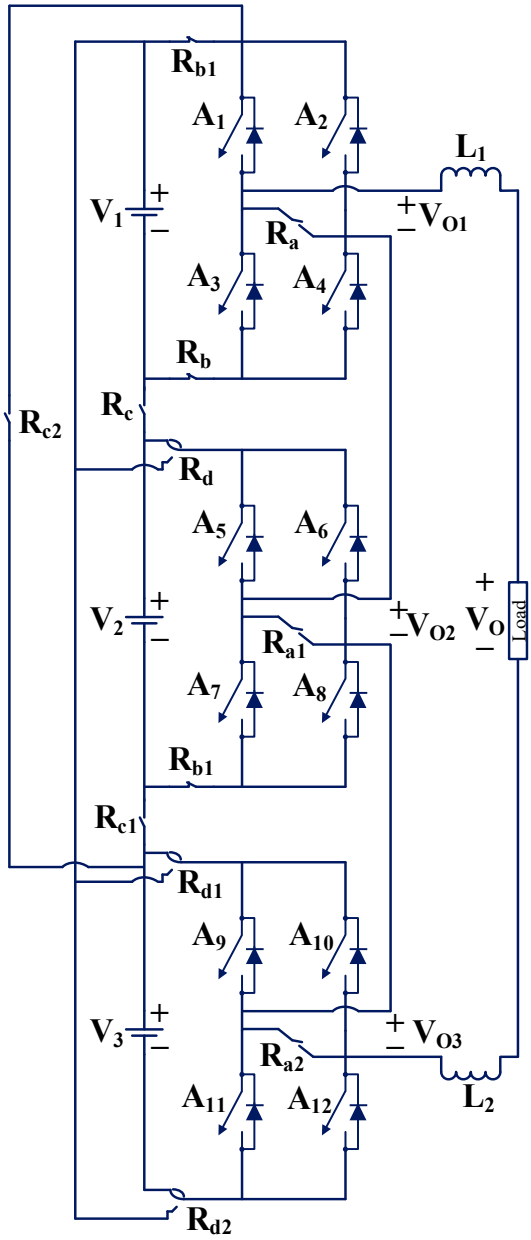

Figure 45. Single-phase seven-level FT MLI (TP49) [81].

3.2.3. TP50 and TP51

Other authors proposed a three-phase hybrid CHB FT MLI by adding an X-CHB inverter to the CHB inverter in [82]. The proposed three-phase inverter can generate an "N" number of levels. The circuit diagram of the proposed three-phase seven-level hybrid CHB inverter (TP50) is shown in Figure 46a. The circuit diagram of the proposed single-phase seven-level hybrid CHB inverter (TP51) is shown in Figure 46b. TP50 and TP51 use MB FT solution for fault tolerance. If a switch fault occurs in any H-bridge cell, the faulty H-bridge cell is bypassed and provides power from the remaining H-bridge cells and X-CHB cell. The proposed topology continues to deliver power at pre-fault voltage levels in case of OC or SC switch faults. It also provides self-balancing capacitor voltage. Battery energy storage systems (BESSs) and uninterrupted power systems are good examples of industrial applications that can utilize the topology. The merits of the topology include the ability to tolerate OC or SC faults and the ability to extend topology to an "N" number of levels. A higher device count is the limitation of the topology.

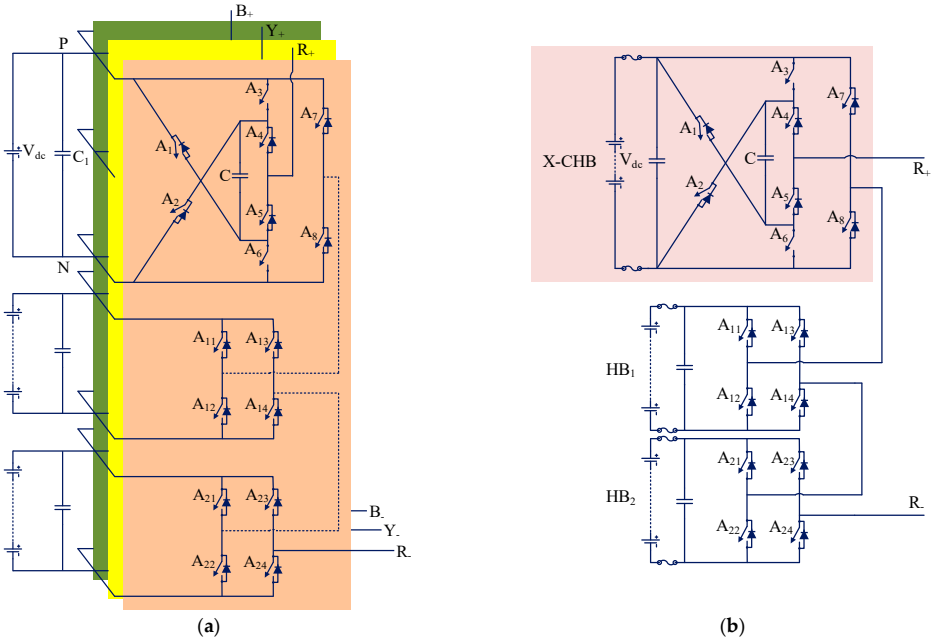

Figure 46. (**a**) Three-phase seven-level FT MLI (TP50) [82]. (**b**) Single-phase seven-level FT MLI (TP51) [82].

3.2.4. TP52

A single-phase thirteen-level FT MLI is proposed in [83], and it is shown in Figure 47. The topology consists of three modified CHB bridge modules. Each module comprises two DC sources and six unidirectional switches. One module always acts as a redundant module. Overall, the topology comprises six DC sources and eighteen unidirectional switches. The thirteen-level output is synthesized by two modules, whereas the faulty module is bypassed. The LS-SPWM scheme is used for creating the gating pulses in the topology. The topology uses the MB FT solution for fault tolerance. All the modules are equally used during normal operation. TP52 can tolerate single-switch OC and SC faults.

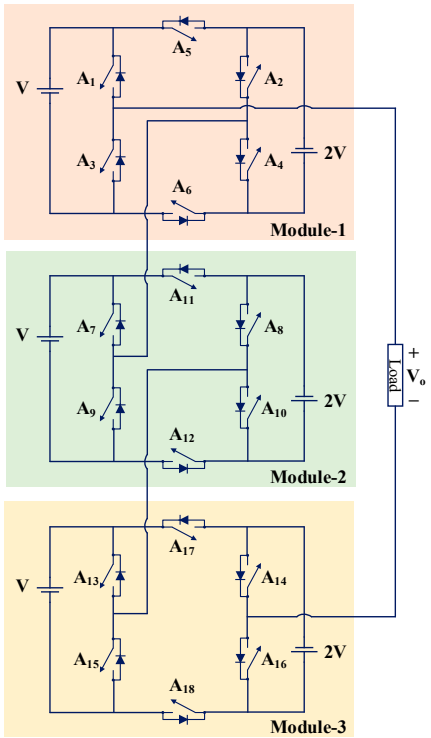

Figure 47. Single-phase thirteen-level FT MLI (TP52) [83].

3.2.5. TP53

A single-phase seven-level FT MLI is proposed in [84], and it is shown in Figure 48. It comprises three DC sources, sixteen relays, and twelve unidirectional switches. During faulty operation, relays are used to reroute conducting paths. It is important to note that T_{S1} to T_{S7} are single-pole, single-throw (SP-ST) relays, and T_{D1} to T_{D9} are single-pole, double-throw (SP-DT) relays [84]. The PD-SPWM scheme is used for creating the gating pulses in the topology. The topology uses MB FT solution for fault tolerance. When one module is faulty, the faulty module is isolated, and the faulty module's source is connected in series with one of the sources of healthy modules. If one module becomes faulty, the TP53 can continue to provide the same output voltage waveform and amplitude, as it did in the pre-fault operation. The use of a large number of relays is the drawback of this topology.

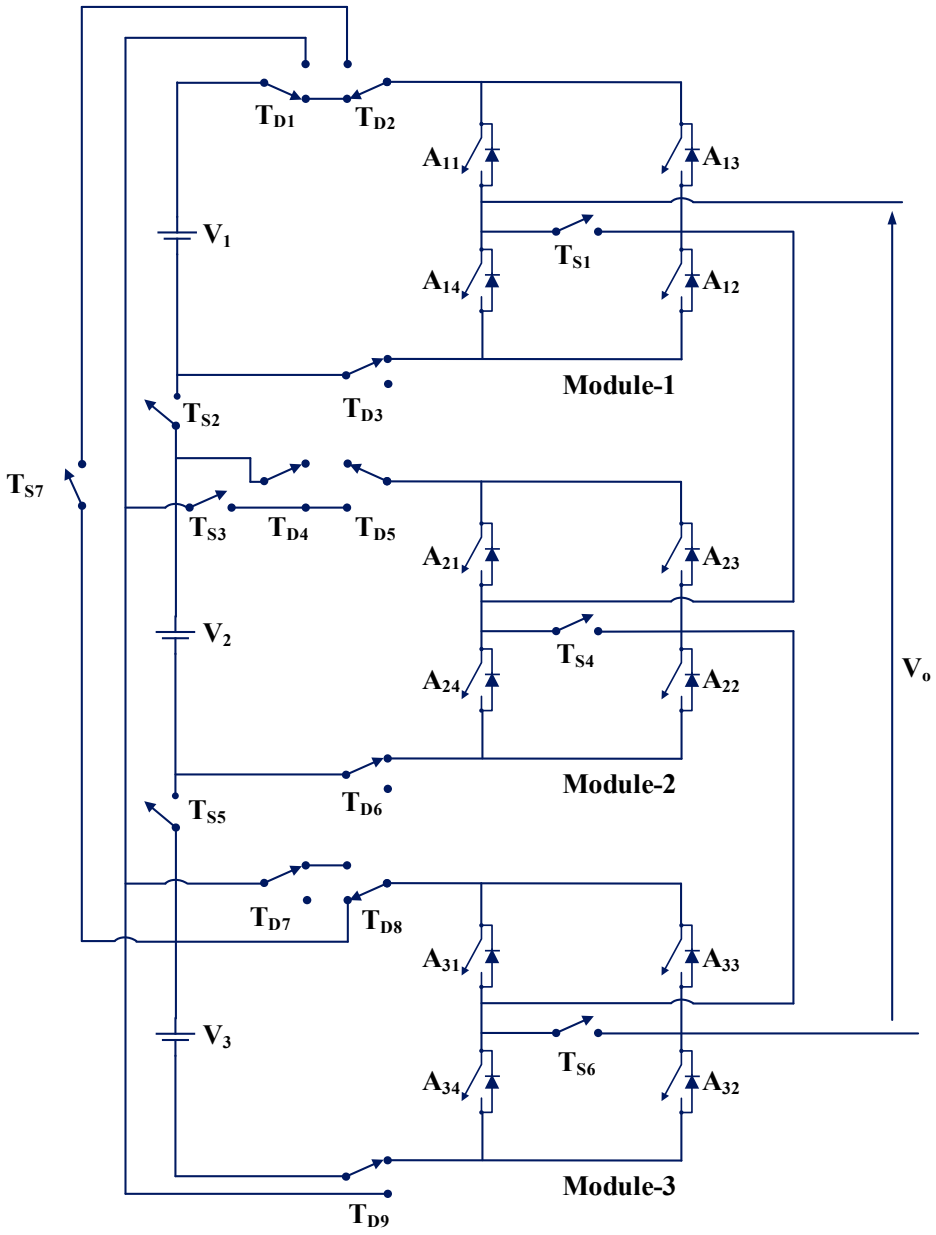

Figure 48. Single-phase seven-level FT MLI (TP53) [84].

4. Comparison of Recently Developed Single-Phase FT MLI Topologies

In the previous section, several recently developed single-phase FT MLI topologies proposed in the literature were discussed. In this section, firstly, a comparison of these

topologies based on comparative factors proposed in the literature is made. Finally, single-phase FT MLIs are compared based on proposed novel factors.

The topologies are compared based on the number of output voltage levels (X_1), number of bidirectional switches (X_2), number of DC supply (X_3), number of capacitors (X_4), total number of switches (IGBT or MOSFET devices) (X_5), number of diodes (X_6), number of fuses (X_7), maximum number of switches to operate in the healthy condition (X_8), maximum number of switches to operate in the faulty condition (X_9), number of inductors (X_{10}), number of relays (X_{11}), and number of gate driver circuits (X_{12}). It is assumed that a bidirectional switch (IGBT or MOSFET with four diodes) counts as a bidirectional switch (two IGBTs or two MOSFETs).

Single-phase FT MLI topologies are categorized into different groups according to the number of output voltage levels. The following factors are calculated for each topology.

4.1. Level to Switch Count Ratio (LSCR)

It is defined as the ratio of output voltage levels to the total switch (total IGBTs/MOSFETs) count. It was used for comparing MLIs in [85]. The higher value of *LSCR* implies better MLI topology than those with a lower *LSCR* value in terms of switch count. The *LSCR* is given as follows:

$$LSCR = \frac{X_1}{X_5} \tag{1}$$

4.2. Component Count to Level Ratio (CCLR)

It is defined as the ratio of total component counts to the output voltage levels. This factor is proposed in [86] for comparing MLIs. The lower value of *CCLR* implies better MLI topology than those with a higher *CCLR* value in terms of total component count. The *CCLR* is given as follows:

$$CCLR = \frac{(X_3 + X_4 + X_5 + X_6 + X_7 + X_{10} + X_{11} + X_{12})}{X_1} \tag{2}$$

The inverse of the *CCLR* is used in this work. It represents the level to total component count ratio (*LCCR*). The higher value of the *LCCR* implies better MLI topology than those with a lower *LCCR* value in terms of total component count. The *LCCR* is given as follows:

$$LCCR = \frac{X_1}{(X_3 + X_4 + X_5 + X_6 + X_7 + X_{10} + X_{11} + X_{12})} \tag{3}$$

4.3. Total Standing Voltage (TSV) and Cost Function (CF)

The *TSV* refers to the amount of voltage stress exerted on all power switches and power diodes. In mathematical terms, it is the sum of the maximum voltage that can be blocked by each power switch and power diode [87]. The *TSV* can be calculated as follows:

$$TSV = \sum_{i=1}^{P} (VPS)_i + \sum_{t=1}^{Q} (VPD)_t \tag{4}$$

where $(VPS)_i$ and $(VPD)_t$ are the magnitude of the maximum standing or blocking voltage for the ith power switch and tth power diode, respectively. Moreover, $i = 1, 2, 3, \ldots, P$; and $t = 1, 2, 3, \ldots, Q$. P and Q are the total number of power switches and power diodes, respectively, in the FT MLI.

The *TSV* per unit ($TSV_{P.U.}$) can be calculated by taking the ratio of *TSV* to the maximum output voltage (V_{omax}) [88]:

$$TSV_{P.U.} = \frac{TSV}{V_{omax}} \tag{5}$$

The *TSV* can be used to determine the ratings and costs of the power electronic devices that will be used in the topology, as well as the overall cost of the inverter circuit [89]. Devices with a lower voltage blocking capability will have a lower rating, which will result in a lower cost. Devices with a higher voltage blocking capability will have a higher rating, which will

result in a higher cost. The *TSV* is an essential factor in reducing the cost of MLIs. A lower *TSV* results in a lower MLI cost, while a higher *TSV* results in a higher MLI cost. Hence, different power electronic devices in an MLI should be evaluated for voltage stress [88,90].

In general, the implementation feasibility of an MLI topology is approximated by its cost function (*CF*) [91]. The *CF* can be calculated in the following manner:

$$CF = X_3 + X_4 + X_5 + X_6 + X_7 + X_{10} + X_{11} + X_{12} + (\mu \times TSV_{P.U.}) \quad (6)$$

It should be noted that μ is the weighting coefficient for the *TSV*; μ can be chosen to be greater than unity when the *TSV* needs to be given more importance. When moderate attention is paid to *TSV*, μ between 0 and 1 is chosen. In this work, μ = 1.5 is selected for the first case, and μ = 0.5 is chosen for the second case [91].

The ratio of *CF* to the number of output voltage levels, denoted by *CFLR*, is calculated in this work. The lower value of *CFLR* implies cheaper MLI topology compared to those with higher *CFLR* values [91]. The *CFLR* is given as follows:

$$CFLR = \frac{CF}{X_1} \quad (7)$$

The inverse of *CFLR* is also used in this work. It represents the level to *CF* ratio (*LCFR*). The higher value of *LCFR* implies a cheaper MLI topology than those with a lower *LCFR* value. *LCFR* is given as follows:

$$LCFR = \frac{X_1}{CF} \quad (8)$$

Table 1 compares single-phase FT MLIs in terms of *LSCR* and *LCCR*. Different topologies are divided into six groups depending upon the number of output voltage levels. Group-I, Group-II, Group-III, Group-IV, Group-V, Group-VI, and Group-VII have 5-level, 7-level, 9-level, 11-level, 13-level, 15-level, and 17-level FT MLI topologies, respectively. In Group-I, topology TP44 is the best topology for a lower component count (higher *LCCR* or *LSCR*). In Group-II, topology TP34 is the best topology regarding a higher *LSCR* value or higher *LCCR* value. In Group-III, topology TP14 is the best topology regarding a higher *LSCR* value or higher *LCCR* value. In Group-V, TP13 and TP33B have the same *LSCR* value, but TP33B is best in terms of the *LCCR* value. In Group-VI, topology TP22 is the best topology regarding a higher *LSCR* value or higher *LCCR* value. In Group-VII, TP16 and TP25 have the same *LSCR* and *LCCR* values.

Table 1. Comparison of single-phase FT MLIs in terms of *LSCR* and *LCCR*.

Group	Reference	Topology	FT Solution	X_1	X_2	X_3	X_4	X_5	X_6	X_7	X_8	X_9	X_{11}	X_{12}	*LSCR*	*LCCR*
I	[34]	TP5	LA	5	0	2	0	14	4	4	4	3	0	14	0.3571	0.1316
	[3]	TP6	LA	5	0	1	1	12	0	0	3	4	0	12	0.4167	0.1923
	[31]	TP8	IHR	5	1	1	1	8	2	0	3	3	0	7	0.6250	0.2632
	[31]	TP9	LA	5	3	1	1	14	2	0	3	4	0	11	0.3571	0.1724
	[28]	TP1	SA	5	1	2	0	8	0	0	3	4	0	7	0.6250	0.2941
	[28]	TP2	SA	5	2	2	0	8	0	0	3	3	0	6	0.6250	0.3125
	[48]	TP3	SA	5	0	1	1	8	0	0	3	3	0	8	0.6250	0.2778
	[37]	TP12	IHR	5	0	2	0	9	0	0	5	5	0	9	0.5556	0.2500
	[8]	TP17	SA	5	1 *	2	0	8	2	0	3	3	0	7	0.6250	0.2632
	[50]	TP10	LA	5	1	1	1	14	2	0	4	4	0	13	0.3571	0.1613
	[54]	TP19	SA	5	3 *	2	0	12	0	9	3	3	0	9	0.4167	0.1563
	[51]	TP11	LA	5	0	1	1	12	2	4	4	3	0	12	0.4167	0.1563
	[38]	TP23	SA	5	0	2	0	9	0	0	3	3	0	9	0.5556	0.2500
	[58]	TP26	IHR	5	2 *	2	0	8	0	0	3	3	0	6	0.6250	0.3125
	[64]	TP32	IHR	5	2 *	2	0	8	0	0	3	3	0	6	0.6250	0.3125
	[67]	TP35	IHR	5	2	1	2	8	0	0	3	3	0	6	0.6250	0.2942
	[72]	TP40	LA	5	0	1	2	14	6	0	3	3	0	14	0.3571	0.1351
	[74]	TP42	IHR	5	1	2	0	8	0	0	4	4	0	7	0.6250	0.2941
	[76]	TP44	IHR	5	1 *	2	0	6	0	0	3	3	2	5	0.8333	0.3333

Table 1. *Cont.*

Group	Reference	Topology	FT Solution	X_1	X_2	X_3	X_4	X_5	X_6	X_7	X_8	X_9	X_{11}	X_{12}	*LSCR*	*LCCR*
II	[48]	TP4	SA	7	3 *	2	2	12	0	0	3	3	0	9	0.5833	0.2800
	[62]	TP30	IHR	7	2	3	0	12	0	0	4	4	0	10	0.5833	0.2800
	[65]	TP33A	IHR	7	4	3	0	12	0	0	3	4	0	8	0.5833	0.3043
	[66]	TP34	IHR	7	0	3	0	8	0	0	4	4	0	8	0.8750	0.3684
	[68]	TP36	SA	7	3	2	2	12	0	0	4	5	0	9	0.5833	0.2800
	[73]	TP41	IHR	7	2	3	0	8	0	0	3	3	6	6	0.8750	0.3043
III	[35]	TP7	LA	9	0	2	2	16	0	0	5	5	0	16	0.5625	0.2500
	[39]	TP14	SA	9	0	2	0	10	0	0	4	4	0	10	0.9000	0.4091
	[53]	TP15	IHR	9	0	4	0	12	0	0	5	5	0	12	0.7500	0.3214
	[40]	TP18	IHR	9	3	2	1	12	0	0	3	3	0	9	0.7500	0.3750
	[41]	TP20	IHR	9	3	2	2	12	0	0	4	4	0	9	0.7500	0.3600
	[42]	TP24	IHR	9	0	4	0	12	0	0	5	5	0	12	0.7500	0.3214
	[60]	TP28	IHR	9	6	4	0	18	0	0	5	5	0	12	0.5000	0.2647
	[61]	TP29	IHR	9	2 *	4	0	14	0	0	5	5	0	12	0.6428	0.3000
	[63]	TP31	SA	9	3	4	0	12	0	0	4	5	0	9	0.7500	0.3600
	[70]	TP38	IHR	9	2	4	0	12	0	0	5	5	0	10	0.7500	0.3462
	[71]	TP39	SA	9	4	2	2	14	0	0	4	4	0	10	0.6428	0.3214
	[75]	TP43	LA	9	3	2	2	12	0	0	4	4	0	9	0.7500	0.3600
	[77]	TP45	IHR	9	0	2	2	13	0	0	3	3	0	13	0.6923	0.3000
	[79]	TP46	LA	9	3	3	0	12	0	7	3	4	0	9	0.7500	0.2903
IV	[56]	TP21	SA	11	3	3	0	12	0	0	3	3	0	9	0.9167	0.4583
V	[52]	TP13	SA	13	3	3	0	12	0	0	3	3	0	9	1.0833	0.5417
	[65]	TP33B	IHR	13	4	3	0	12	0	0	3	4	0	8	1.0833	0.5652
VI	[57]	TP22	IHR	15	1	4	0	12	0	0	4	4	0	11	1.2500	0.5556
	[69]	TP37	IHR	15	6	1	8	36	0	0	10	19	0	30	0.4167	0.2000
VII	[53]	TP16	IHR	17	0	4	0	12	0	0	5	5	0	12	1.4167	0.6071
	[42]	TP25	IHR	17	0	4	0	12	0	0	5	5	0	12	1.4167	0.6071

* Bidirectional switch = IGBT or MOSFET with four diodes.

Table 2 compares single-phase FT MLIs based on modules in terms of *LSCR* and *LCCR*. Different topologies are divided into three groups depending on the number of output voltage levels. Group-VIII, Group-IX, and Group-X have 7-level, 13-level, and 15-level FT MLI topologies, respectively. In Group-VIII, topologies (TP49 and TP53) have higher and the same *LSCR* values. TP47 is the best topology in terms of a higher *LCCR* value.

Table 2. Comparison of single-phase FT MLIs based on modules in terms of *LSCR* and *LCCR*.

Group	Reference	Topology	FT Solution	X_1	X_3	X_4	X_5	X_7	X_{10}	X_{11}	X_{12}	*LSCR*	*LCCR*
VIII	[80]	TP47	MB	7	3	0	16	0	0	2	16	0.4375	0.1892
	[81]	TP49	MB	7	3	0	12	0	2	12	12	0.5833	0.1707
	[82]	TP51	MB	7	3	4	16	6	0	0	16	0.4375	0.1556
	[84]	TP53	MB	7	3	0	12	0	0	16	12	0.5833	0.1628
IX	[83]	TP52	MB	13	6	0	18	0	0	0	18	0.7222	0.3095
X	[80]	TP48	MB	15	3	0	16	0	0	2	16	0.9375	0.4054

The *TSV*, *CF*, and *CFLR* values were calculated for all FT MLI topologies. Table 3 compares single-phase FT MLIs in terms of *TSV*, *CF*, and *CFLR*. In Group-I, topology TP44 has the lowest *CFLR* value in the case of $\mu = 0.5$, whereas TP35 has the lowest *CFLR* value in the case of $\mu = 1.5$. In Group-II, topology TP34 has the lowest *CFLR* value in both cases, i.e., $\mu = 0.5$ and $\mu = 1.5$. In Group-III, topology TP14 has the lowest *CFLR* value in the case of $\mu = 0.5$, whereas TP18 has the lowest *CFLR* value in the case of $\mu = 1.5$. In Group-VI, topology TP22 has the lowest *CFLR* value in both cases, i.e., $\mu = 0.5$ and $\mu = 1.5$.

Table 3. Comparison of single-phase FT MLIs in terms of *TSV*, *CF*, and *CFLR*.

Group	Reference	Topology	X_1	X_3	X_4	X_5	X_6	X_7	X_{11}	X_{12}	*TSV* ($\times V_{dc}$)	$TSV_{p.u.}$	*CF*		*CFLR*	
													(μ = 0.5)	(μ = 1.5)	(μ = 0.5)	(μ = 1.5)
I	[34]	TP5	5	2	0	14	4	4	0	14	22	11	43.5	54.5	8.7	10.9
	[3]	TP6	5	1	1	12	0	0	0	12	16	8	30	38	6	7.6
	[31]	TP8	5	1	1	8	2	0	0	7	10	5	21.5	26.5	4.3	5.3
	[31]	TP9	5	1	1	14	2	0	0	11	22	11	34.5	45.5	6.9	9.1
	[28]	TP1	5	2	0	8	0	0	0	7	9	4.5	19.25	23.75	3.85	4.75
	[28]	TP2	5	2	0	8	0	0	0	6	10	5	18.5	23.5	3.7	4.7
	[48]	TP3	5	1	1	8	0	0	0	8	6	3	19.5	22.5	3.9	4.5
	[37]	TP12	5	2	0	9	0	0	0	9	9	4.5	22.25	26.75	4.45	5.35
	[8]	TP17	5	2	0	8	2	0	0	7	19	9.5	23.75	33.25	4.75	6.65
	[50]	TP10	5	1	1	14	2	0	0	13	11	5.5	33.75	39.25	6.75	7.85
	[54]	TP19	5	2	0	12	0	9	0	9	13	6.5	35.25	41.75	7.05	8.35
	[51]	TP11	5	1	1	12	2	4	0	12	8	4	34	38	6.8	7.6
	[38]	TP23	5	2	0	9	0	0	0	9	7	3.5	21.75	25.25	4.35	5.05
	[58]	TP26	5	2	0	8	0	0	0	6	10	5	18.5	23.5	3.7	4.7
	[64]	TP32	5	2	0	8	0	0	0	6	12	6	19	25	3.8	5
	[67]	TP35	5	1	2	8	0	0	0	6	5	2.5	18.25	20.75	3.65	4.15
	[72]	TP40	5	1	2	14	6	0	0	14	11	5.5	39.75	45.25	7.95	9.05
	[74]	TP42	5	2	0	8	0	0	0	7	9	4.5	19.25	23.75	3.85	4.75
	[76]	TP44	5	2	0	6	0	0	2	5	9	4.5	17.25	21.75	3.45	4.35
II	[48]	TP4	7	2	2	12	0	0	0	9	19	6.33	28.17	34.5	4.02	4.93
	[62]	TP30	7	3	0	12	0	0	0	10	20	6.67	28.33	35	4.05	5
	[65]	TP33A	7	3	0	12	0	0	0	8	20	6.67	26.33	33	3.76	4.71
	[66]	TP34	7	3	0	8	0	0	0	8	12	4	21	25	3	3.57
	[68]	TP36	7	2	2	12	0	0	0	9	17	5.67	27.83	33.5	3.98	4.79
	[73]	TP41	7	3	0	8	0	0	6	6	16	5.33	25.67	31	3.67	4.43
III	[35]	TP7	9	2	2	16	0	0	0	16	16	4	38	42	4.22	4.67
	[39]	TP14	9	2	0	10	0	0	0	10	24	6	25	31	2.78	3.44
	[53]	TP15	9	4	0	12	0	0	0	12	20	5	30.5	35.5	3.39	3.94
	[40]	TP18	9	2	1	12	0	0	0	9	13	3.25	25.63	28.88	2.85	3.21
	[41]	TP20	9	2	2	12	0	0	0	9	13	3.25	26.63	29.88	2.96	3.32
	[42]	TP24	9	4	0	12	0	0	0	12	18	4.5	30.25	34.75	3.36	3.86
	[60]	TP28	9	4	0	18	0	0	0	12	33	8.25	38.13	46.38	4.24	5.15
	[61]	TP29	9	4	0	14	0	0	0	12	26	6.5	33.25	39.75	3.69	4.42
	[63]	TP31	9	4	0	12	0	0	0	9	20	5	27.5	32.5	3.06	3.61
	[70]	TP38	9	4	0	12	0	0	0	10	20	5	28.5	33.5	3.17	3.72
	[71]	TP39	9	2	2	14	0	0	0	10	14	3.5	29.75	33.25	3.31	3.69
	[75]	TP43	9	2	2	12	0	0	0	9	13	3.25	26.63	29.88	2.96	3.32
	[77]	TP45	9	2	2	13	0	0	0	13	28	7	33.5	40.5	3.72	4.5
	[79]	TP46	9	3	0	12	0	7	0	9	23	5.75	33.88	39.63	3.76	4.40
IV	[56]	TP21	11	3	0	12	0	0	0	9	18	3.6	25.8	29.4	2.35	2.67
V	[52]	TP13	13	3	0	12	0	0	0	9	13	2.167	25.08	27.25	1.93	2.09
VI	[57]	TP22	15	4	0	12	0	0	0	11	36	5.14	29.57	34.71	1.97	2.31
	[69]	TP37	15	1	8	36	0	0	0	30	46	6.57	78.29	84.86	5.22	5.66
VII	[42]	TP25	17	4	0	12	0	0	0	12	36	4.5	30.25	34.75	1.78	2.04

Table 4 compares single-phase FT MLIs in terms of *TSV*, *CF*, and *CFLR*. In Group-VIII, topology TP47 has the lowest *CFLR* value in the case of μ = 0.5, whereas TP49 has the lowest *CFLR* value in the case of μ = 1.5.

Table 4. Comparison of single-phase FT MLIs based on modules in terms of *TSV*, *CF*, and *CFLR*.

Group	Reference	Topology	X_1	X_3	X_4	X_5	X_7	X_{10}	X_{11}	X_{12}	*TSV* ($\times V_{dc}$)	$TSV_{p.u}$	*CF*		*CFLR*	
													(μ = 0.5)	(μ = 1.5)	(μ = 0.5)	(μ = 1.5)
VIII	[80]	TP47	7	3	0	16	0	0	2	16	26	8.67	41.33	50	5.90	7.14
	[81]	TP49	7	3	0	12	0	2	12	12	16	5.33	43.67	49	6.24	7
	[82]	TP51	7	3	4	16	6	0	0	16	20	6.67	48.33	55	6.91	7.86
X	[80]	TP48	15	3	0	16	0	0	2	16	56	8	41	49	2.73	3.27

4.4. Fault Tolerance Factor and Complete Fault Tolerance Factor

The factors *LSCR*, *LCCR*, *CFLR*, and *LCFR* only measure the MLI's cost and size by considering the number of components for generating "N" levels of the output waveform. These factors are good for comparing MLI topologies without fault tolerance capability. *LSCR*, *LCCR*, *CFLR*, and *LCFR* do not quantitatively measure an MLI's fault tolerance capability. This work proposes a novel factor known as the fault tolerance factor (*FTF*) to measure the fault tolerance of an MLI quantitively. It can be calculated as follows:

$$FTF = \frac{1}{G}\sum_{k}(H)_k \tag{9}$$

where G is the total number of switching devices in the MLI; H is the available number of levels for a faulty switch to synthesize output voltage waveform; k is the switching device of the original topology; and $k = 1, 2, 3, \ldots, G$. The higher value of *FTF* implies better FT MLI topology as compared to those that have a lower *FTF* value. *FTF* actually measures the fault tolerance of the MLI at the expense of the number of switches.

Let us understand with an example of a single-switch OC (SSOC) fault in a redundant leg-based MLI. For a topology (TP5) given in [34], *FTF* is calculated for faulty switches, taking one at a time. FTF_O is FTF for MLI without extra hardware (without redundant leg), and FTF_{PF} is *FTF* for an MLI with fault reconfiguration (after adding a redundant leg). It is noted that FTF_O is only calculated for MLI topologies in which some additional hardware components are added. In the case of the IHR type of FT solution, *FTF* can be calculated only for post-fault conditions, as these topologies do not add any additional hardware components. The available number of levels for faulty switch A_1, A_2, A_3, A_4, B_1, B_2, B_3, and B_4 is 3, 0, 0, 3, 3, 0, 0, and 3, respectively, during the faulty condition. Here the total number of switches (G) in MLI (before adding the redundant leg) is 8.

$$(FTF)_O = \frac{1}{G}\sum_{k=1,2,\ldots,8}(H)_k \tag{10}$$

$$(FTF)_O = \frac{1}{8}(H_1 + H_2 + H_3 + H_4 + H_5 + H_6 + H_7 + H_8) \tag{11}$$

$$(FTF)_O = \frac{1}{8}(3 + 0 + 0 + 3 + 3 + 0 + 0 + 3) = 1.5 \tag{12}$$

After adding a redundant leg to the main inverter (or original topology), the available number of levels for faulty switch A_1, A_2, A_3, A_4, B_1, B_2, B_3, and B_4 are 5, 5, 5, 5, 5, 5, 5, and 5, respectively, under post-fault condition. Here, the total number of switches (G) in MLI (after adding the redundant leg) is 14.

$$(FTF)_{PF} = \frac{1}{G}\sum_{k=1,2,\ldots,8}(H)_k \tag{13}$$

$$(FTF)_{PF} = \frac{1}{14}(H_1 + H_2 + H_3 + H_4 + H_5 + H_6 + H_7 + H_8) \tag{14}$$

$$(FTF)_{PF} = \frac{1}{14}(5 + 5 + 5 + 5 + 5 + 5 + 5 + 5) = 2.857 \tag{15}$$

For the topology TP5, without extra hardware *FTF* (FTF_O) and post-fault (or with reconfiguration) *FTF* (FTF_{PF}) are 1.5 and 2.857, respectively. It means that MLI topology after adding the redundant leg becomes 90.47% more FT compared to the original (main inverter) MLI topology for SSOC faults.

The *FTF* can be calculated for single- and multiple-switch OC and SC faults. Multiple-switch faults can be for a pair, triplet, or quadruple of switches. Table 5 compares single-phase five-level FT MLIs based on the proposed novel factor, *FTF* for a SSOC fault. To compare FT MLI from its previous version (original topology), FTF_O and FTF_{PF} values can be compared. There is an improvement of 66.67% SSOC fault tolerance capability in the case of topology TP6 by adding a redundant leg. There is an improvement of 28.55% SSOC

fault tolerance capability in the case of topology TP1 by switch addition. There is an improvement of 136.08% SSOC fault tolerance capability in the case of topology TP2 by switch addition. There is an improvement of 37.5% SSOC fault tolerance capability in the case of topology TP3 by switch addition. There is an improvement of 77.76% SSOC fault tolerance capability in the case of topology TP11 by adding a redundant leg.

Table 5. Comparison of single-phase five-level FT MLIs for SSOC faults (*TSV* is not considered).

Group	Reference	Topology	FT Solution	X_1	X_5	*LCCR*	FTF_O	FTF_{PF}	*LCCR* + FTF_{PF}
I	[34]	TP5	LA	5	14	0.1316	1.500	2.857	2.9886
	[3]	TP6	LA	5	12	0.1923	1.500	2.500	2.6923
	[31]	TP8	IHR	5	8	0.2632	-	1.500	1.7632
	[31]	TP9	LA	5	14	0.1724	-	2.500	2.6724
	[28]	TP1	SA	5	8	0.2941	2.000	2.571	2.8651
	[28]	TP2	SA	5	8	0.3125	1.200	2.833	3.1455
	[48]	TP3	SA	5	8	0.2778	2.000	2.750	3.0278
	[37]	TP12	IHR	5	9	0.2500	-	3.000	3.2500
	[8]	TP17	SA	5	8	0.2632	-	1.500	1.7632
	[50]	TP10	LA	5	14	0.1613	-	2.214	2.3753
	[54]	TP19	SA	5	12	0.1563	-	2.750	2.9063
	[51]	TP11	LA	5	12	0.1563	1.875	3.333	3.4893
	[38]	TP23	SA	5	9	0.2500	2.000	2.890	3.1400
	[58]	TP26	IHR	5	8	0.3125	-	2.750	3.0625
	[64]	TP32	IHR	5	8	0.3125	-	2.750	3.0625
	[67]	TP35	IHR	5	8	0.2942	-	2.750	3.0442
	[72]	TP40	LA	5	14	0.1351	-	2.857	2.9921
	[74]	TP42	IHR	5	8	0.2941	-	2.875	3.1691
	[76]	TP44	IHR	5	6	0.3333	-	2.500	2.8333

The *FTF* only measures the FT capability of an MLI quantitatively and does not include total component counts or cost in consideration. Hence, it cannot be used alone to compare the different FT MLIs. Therefore, another parameter, known as the complete fault tolerance factor (*CFTF*), is proposed to compare the different FT MLIs. The *CFTF* is given as follows:

(i) When *TSV* is not considered,

$$CFTF = LCCR + (FTF_{PF})_{SOCF} + (FTF_{PF})_{MOCF} + (FTF_{PF})_{SSCF} + (FTF_{PF})_{MSCF} \quad (16)$$

(ii) When *TSV* is considered,

$$CFTF = LCFR + (FTF_{PF})_{SOCF} + (FTF_{PF})_{MOCF} + (FTF_{PF})_{SSCF} + (FTF_{PF})_{MSCF} \quad (17)$$

where *LCCR* is level to total component count ratio, *LCFR* is level to cost function ratio, $(FTF_{PF})_{SOCF}$ is *FTF* for single-switch OC (SSOC) fault, $(FTF_{PF})_{MOCF}$ is *FTF* for multiple-switch OC (MSOC) fault, $(FTF_{PF})_{SSCF}$ is *FTF* for single-switch SC (SSSC) fault, and $(FTF_{PF})_{MSCF}$ is *FTF* for multiple-switch SC (MSSC) fault.

CFTF provides a complete solution for comparing FT MLIs topologies in terms of fault tolerance and the total component count or cost quantitatively. *CFTF* includes fault-type (OC or SC) and fault-number (single or multiple) information to calculate the fault tolerance of an FT MLI. The higher value of *CFTF* implies better FT MLI topology (lower component count and higher FT capability) as compared to those that have a lower *CFTF* value.

Table 5 compares single-phase five-level FT MLI topologies for SSOC faults when *TSV* is not considered. It shows that TP11 is the best single-phase five-level FT MLI topology in terms of SSOC fault tolerance and the lower total component count or cost in Group-I by using the parameter (*LCCR* + FTF_{PF}). Topology TP11, TP2, and TP12 are the best (higher *LCCR* + FTF_{PF} value) FT MLI among LA, SA, and IHR type of FT MLI, respectively.

Table 6 shows the comparison of single-phase five-level FT MLI topologies for SSOC faults when the *TSV* factor is considered. It shows that TP11 is the best single-phase five-level FT MLI topology in both cases, i.e., $\mu = 0.5$ and $\mu = 1.5$, in terms of SSOC fault

tolerance and lower cost in Group-I by using the parameter ($LCFR + FTF_{PF}$). Topology TP11, TP23, and TP12 are the best (higher $LCFR + FTF_{PF}$ value) FT MLIs among LA, SA, and IHR types of FT MLI, respectively, in both cases, i.e., μ = 0.5 and μ = 1.5.

Table 6. Comparison of single-phase five-level FT MLIs for SSOC faults (*TSV* is considered).

Group	Reference	Topology	FT solution	FTF_{PF}	*CFLR*		*LCFR*		*LCFR* + FTF_{PF}	
					(μ = 0.5)	(μ = 1.5)	(μ = 0.5)	(μ = 1.5)	(μ = 0.5)	(μ = 1.5)
I	[34]	TP5	LA	2.857	8.7	10.9	0.1149	0.0917	2.9719	2.9487
	[3]	TP6	LA	2.500	6	7.6	0.1667	0.1316	2.6667	2.6316
	[31]	TP8	IHR	1.500	4.3	5.3	0.2325	0.1887	1.7325	1.6887
	[31]	TP9	LA	2.500	6.9	9.1	0.1449	0.1099	2.6449	2.6099
	[28]	TP1	SA	2.571	3.85	4.75	0.2597	0.2105	2.8307	2.7815
	[28]	TP2	SA	2.833	3.7	4.7	0.2703	0.2128	3.1033	3.0458
	[48]	TP3	SA	2.750	3.9	4.5	0.2564	0.2222	3.0064	2.9722
	[37]	TP12	IHR	3.000	4.45	5.35	0.2247	0.1869	3.2247	3.1869
	[8]	TP17	SA	1.500	4.75	6.65	0.2105	0.1504	1.7105	1.6504
	[50]	TP10	LA	2.214	6.75	7.85	0.1481	0.1274	2.3621	2.3414
	[54]	TP19	SA	2.750	7.05	8.35	0.1418	0.1198	2.8918	2.8698
	[51]	TP11	LA	3.333	6.8	7.6	0.1471	0.1316	3.4801	3.4646
	[38]	TP23	SA	2.890	4.35	5.05	0.2299	0.1980	3.1199	3.0880
	[58]	TP26	IHR	2.750	3.7	4.7	0.2703	0.2128	3.0203	2.9628
	[64]	TP32	IHR	2.750	3.8	5	0.2632	0.2000	3.0132	2.9500
	[67]	TP35	IHR	2.750	3.65	4.15	0.2739	0.2410	3.0239	2.9910
	[72]	TP40	LA	2.857	7.95	9.05	0.1258	0.1105	2.9828	2.9675
	[74]	TP42	IHR	2.875	3.85	4.75	0.2597	0.2105	3.1347	3.0855
	[76]	TP44	IHR	2.500	3.45	4.35	0.2899	0.2299	2.7899	2.7299

Only $(FTF_{PF})_{SOCF}$ is used in this work; the $(FTF_{PF})_{MOCF}$, $(FTF_{PF})_{SSCF}$, and $(FTF_{PF})_{MSCF}$ values are not calculated in this work and are left for future analysis. This will lead to more accurate results and provide the best FT MLI topologies in fault tolerance and cost. Including the *LCFR* factor in *CFTF* provides more realistic results than the *LCCR* factor by considering the *TSV* factor.

The evaluation of reliability can be carried out in a variety of ways. Markov chain theory (MCT) is a popular method to evaluate reliability. The reliability of TP42 is found to be higher than TP17 in [74], using MCT. It can be seen that the fault tolerance capability of TP42 is higher than TP17 in Tables 5 and 6. The reliability of TP32 is found to be higher than TP17 in [64], using MCT. It can be seen that the fault tolerance capability of TP32 is higher than TP17 in Tables 5 and 6. The reliability of TP19 is found to be higher than TP8 and TP9 in [54], using MCT. It can be seen that the fault tolerance capability of TP19 is higher than TP8 and TP9 from Tables 5 and 6. Hence, the proposed factor (*CFTF*) verifies the effectiveness in evaluating fault tolerance. The proposed method provides approximately the same results as the MCT method. The proposed method uses the number of voltage levels and the component count or costs, whereas MCT uses the component failure rate to calculate reliability. The proposed method is less complex, more accurate, and easy to compare different FT MLIs. *CFTF* value gives information on component count or cost, as well as fault tolerance, whereas MCT gives only information on reliability or fault tolerance. The drawback of *CFTF* is that it does not provide reliability as a function of time because of the exclusion of the failure rate of the components.

5. Simulation and Experimental Results of a FT MLI

This paper performs and describes the FT operation of the FT MLI topology proposed in [34].

Only switch OC fault operation is analyzed in this work. The fuses were removed from the original topology because this work does not deal with SC faults. The topology is shown in Figure 49. The topology consists of the main inverter and the redundant leg.

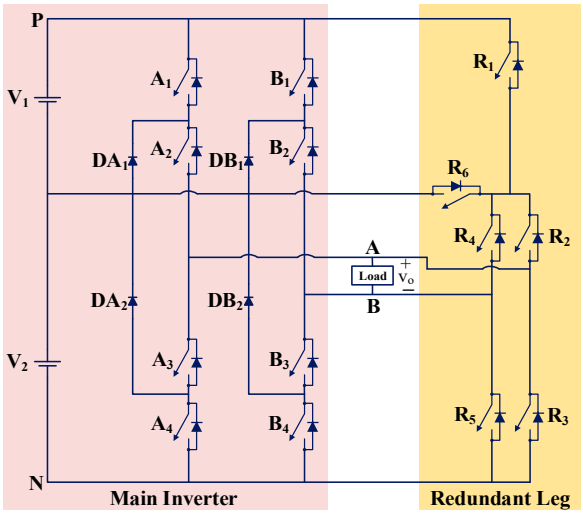

Figure 49. Single-phase five-level FT MLI [34].

The FT MLI topology consists of two dc sources ($V_1 = V_2 = E$), four clamping diodes, and fourteen switches (IGBTs). Out of fourteen switches, six switches were only utilized under faulty conditions. These six switches form a redundant leg in this FT MLI topology. This topology can generate a five-level output voltage waveform under healthy operation (or pre-fault condition).

The switching states of FT MLI under healthy operation are described in Table 7. The levels L_1, L_2, L_3, L_4, and L_5 denote output voltage amplitude 2E, E, 0, −E, and −2E, respectively. There are two switching combinations for levels L_2 and L_4, three switching combinations for level L_3, and one switching combination for levels L_1 and L_5.

Table 7. Switching states under healthy conditions.

Level	Amplitude	A_1	A_2	A_3	A_4	B_1	B_2	B_3	B_4	Path
L_1	2E	1	1	0	0	0	0	1	1	P_1
L_2	E	0	1	1	0	0	0	1	1	P_2
		1	1	0	0	0	1	1	0	P_3
L_3	0	0	1	1	0	0	1	1	0	P_4
		0	0	1	1	0	0	1	1	P_5
		1	1	0	0	1	1	0	0	P_6
L_4	−E	0	0	1	1	0	1	1	0	P_7
		0	1	1	0	1	1	0	0	P_8
L_5	−2E	0	0	1	1	1	1	0	0	P_9

1 = ON switch, 0 = OFF switch.

5.1. Nearest Level Control

Switching loss, harmonics, and filter size are all impacted by modulation methods. A fundamental frequency switching scheme is employed in this work to control the FT MLI topology. The NLC-PWM scheme is employed in this work.

For higher output voltage applications, the NLC offers the advantage of reduced switching losses and minimal low-order harmonics [92]. In the NLC, a sinusoidal signal with fundamental frequency is utilized as a reference signal, and it is compared to other carrier signals (Q_1 to Q_n) to implement each switching state. A sampled waveform can be obtained in NLC by comparing a reference sinusoidal waveform with the desired output waveform. Between the two levels, a $0.5V_{dc}$ DC loss error is generally maintained [38]. The waveform generated is then rounded off to the nearest level and compared appropriately to the switching states in Table 7 to generate gate signals for the respective IGBTs [92].

Figure 50 [93] shows a comparison of the reference sine wave with the desired output voltage levels. The NLC's working principle is depicted in Figure 51 [92].

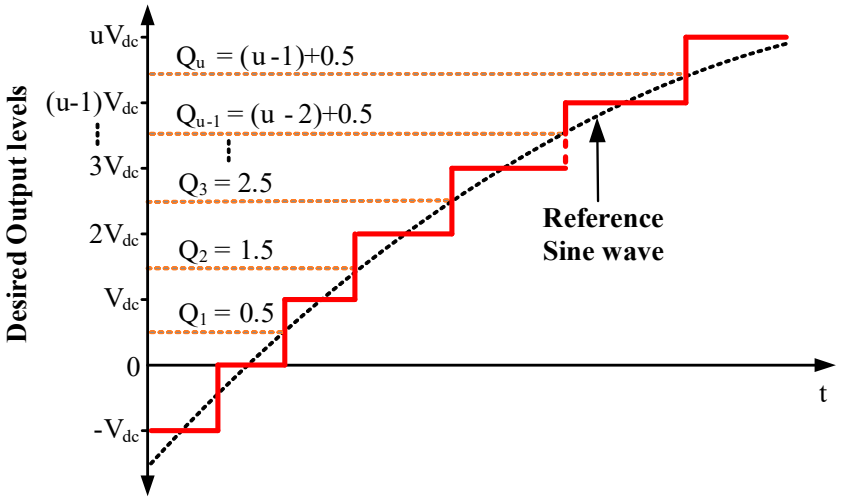

Figure 50. Sampled reference signal [93].

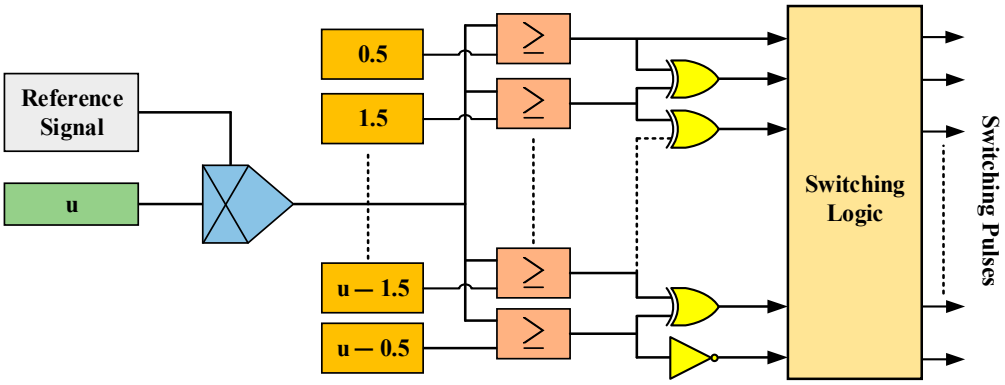

Figure 51. NLC working principle for switching pulse generation [92].

For generating N-level (N_{level}) output voltage waveform, the carrier signal is given by Table 8 [38]. Here u is given by

$$u = \frac{N_{level} - 1}{2} \tag{18}$$

Table 8. Carrier signals.

Q_1	Q_2	Q_3	Q_4	.	.	.	Q_{u-2}	Q_{u-1}	Q_u
0.5	1.5	2.5	3.5	.	.	.	(u − 3) + 0.5	(u − 2) + 0.5	(u − 1) + 0.5

In the case of conventional NLC, the switching angle is calculated as follows [94]:

$$\theta_i = M \sin^{-1}\left(\frac{i - 0.5}{u}\right) \tag{19}$$

where $i = 1, 2, 3, \ldots, u$; and M is referred to as modulation index and is stated as follows [92,95]:

$$M = \frac{V_{ref}}{V_o} = \frac{V_{ref}}{\left(\frac{N_{level}-1}{2}\right)V_{dc}} = \frac{2V_{ref}}{(N_{level}-1)V_{dc}} = \frac{V_{ref}}{uV_{dc}} \tag{20}$$

The modulation scheme is altered whenever an OC switch fault is detected to generate new switching angles [39]. This operation ensures continuous operation after a fault. The redundant leg is used for providing a conduction path in the case of a switch fault. Table 9 depicts the status of output voltage waveform levels under healthy, faulty, and post-fault conditions for all single switches and two multiple-switch pairs.

Table 9. Output voltage level status under healthy, faulty, and post-fault conditions.

Faulty Switch(es)	Levels Status Prior Fault					Levels Status during Fault					Levels Status after Fault				
	L_1	L_2	L_3	L_4	L_5	L_1	L_2	L_3	L_4	L_5	L_1	L_2	L_3	L_4	L_5
A_1	✓	✓	✓	✓	✓	✗	✓	✓	✓	✓	✓	✓	✓	✓	✓
A_2	✓	✓	✓	✓	✓	✗	✗	✓	✓	✓	✓	✓	✓	✓	✓
A_3	✓	✓	✓	✓	✓	✓	✓	✓	✗	✗	✓	✓	✓	✓	✓
A_4	✓	✓	✓	✓	✓	✓	✓	✓	✓	✗	✓	✓	✓	✓	✓
B_1	✓	✓	✓	✓	✓	✓	✓	✓	✓	✗	✓	✓	✓	✓	✓
B_2	✓	✓	✓	✓	✓	✓	✓	✓	✗	✗	✓	✓	✓	✓	✓
B_3	✓	✓	✓	✓	✓	✗	✗	✓	✓	✓	✓	✓	✓	✓	✓
B_4	✓	✓	✓	✓	✓	✗	✓	✓	✓	✓	✓	✓	✓	✓	✓
A_1 and A_4	✓	✓	✓	✓	✓	✗	✓	✓	✓	✗	✓	✓	✓	✓	✓
A_4 and B_1	✓	✓	✓	✓	✓	✓	✓	✓	✗	✗	✓	✓	✓	✓	✓

✓ = Level availability; ✗ = level unavailability.

5.2. Simulation Results and Discussion

In the case of the FT MLI topology, the output voltage and load current for the (RL) load during the pre-fault, fault, and post-fault period are simulated by using MATLAB/Simulink® 2018b environment. The OC fault is imitated by disconnecting the specified switching device's gating pulse. NLC-PWM is utilized to generate the gate triggering pulses to the switches of the FT MLI. Three different cases were chosen to evaluate the performance of FT MLI under OC fault. The three different cases include single device fault, two device faults in the same leg, and two device faults in different legs. In Table 10, all the parameters of the device that were used in the simulation are listed.

Table 10. List of simulation parameters.

DC Voltage Source 1	100 V
DC Voltage Source 2	100 V
Load Resistance (R)	70 Ω
Load Inductance (L)	140 mH
Modulation Index (M)	1
Switching Frequency	50 Hz

Based on simulation results for the FT MLI for RL load, Figure 52 illustrates the output voltage and load current for three different operating conditions, i.e., pre-fault state, faulty state, and post-fault state. An OC fault is simulated by removing gate pulses of the faulty switching device at a time of 0.442 s to know the voltage level status during an OC fault. The instance of fault (FI) means the instant at which OC fault occurs. The instance of reconfiguration (RI) represents the instant at which reconfiguration operation is made to provide fault tolerance to an FT MLI. At 0.518 s, the reconfiguration operation takes place as marked with RI. Redundant leg switches are used during reconfiguration to provide different conduction paths in order to generate voltage levels that would be lost in the event of an OC fault. This FT MLI topology's operation preserves original output voltage levels by utilizing switches present in the redundant leg.

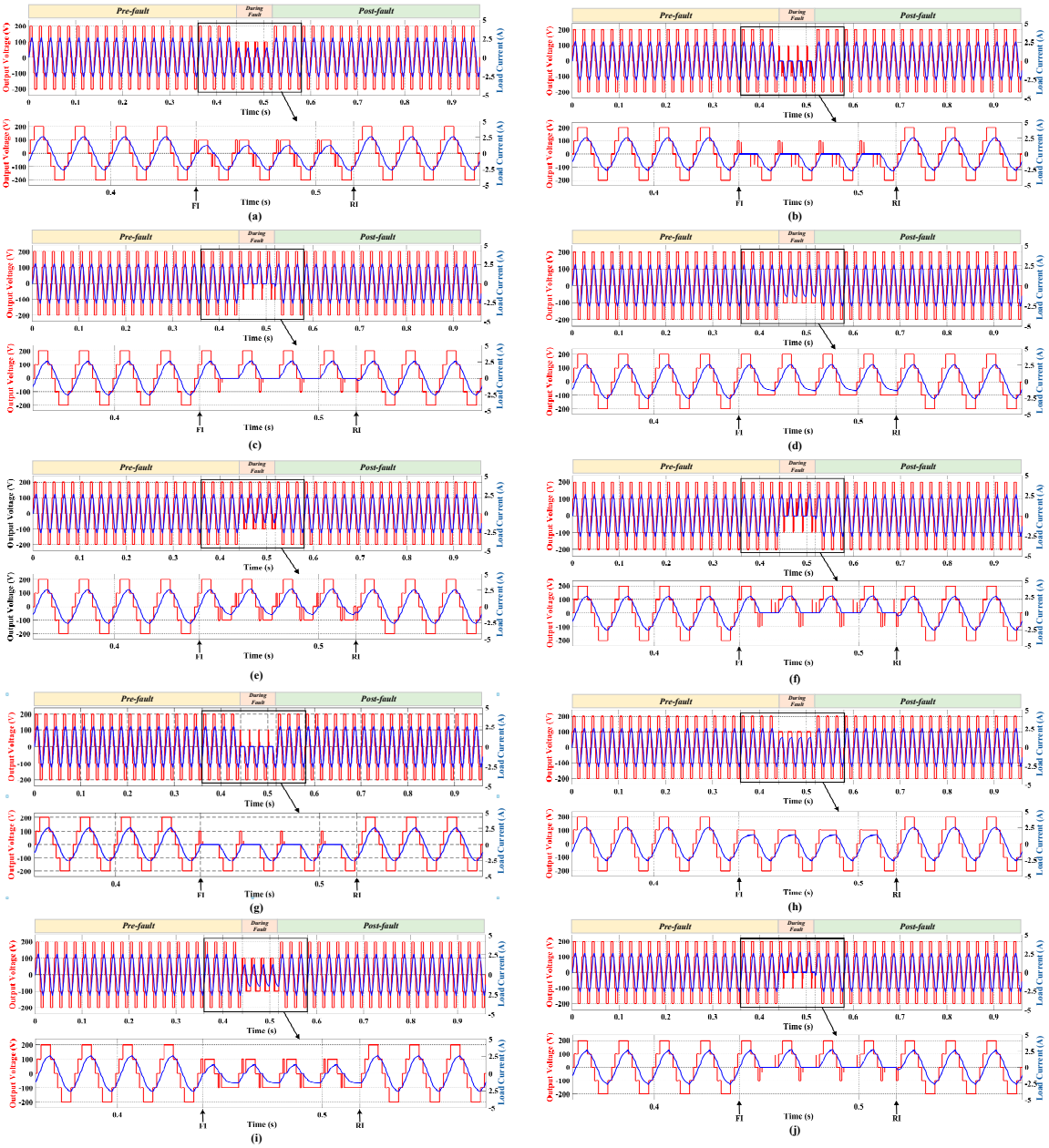

Figure 52. Simulations results (output voltage and load current) for FT operation of the topology in the case of OC single-switch fault for switch (**a**) A_1, (**b**) A_2, (**c**) A_3, (**d**) A_4, (**e**) B_1, (**f**) B_2, (**g**) B_3, and (**h**) B_4; and OC multiple-switch fault for switches (**i**) A_1 and A_4 and (**j**) A_4 and B_1.

5.2.1. Single-Switch OC Fault

The simulation results of a single-switch OC fault are shown in Figure 52a. Single-switch OC fault in switch A_1 shows the loss of L_1 voltage level. This is because of the loss of connection between point P and point A, as shown in Figure 49. A different conduction path may be provided during reconfiguration operation, using redundant leg switches R_1, R_2, and R_5 to preserve the L_1 voltage level. Consequently, the voltage waveforms remain unchanged before and after the OC fault. Similarly, Figure 52b–h show OC fault simulation results for switch A_2, A_3, A_4, B_1, B_2, B_3, and B_4, respectively.

5.2.2. Multiple-Switch OC Fault

The simulation result of multiple-switch OC faults in the same leg is shown in Figure 52i. The loss of the output voltage levels L_1 and L_5 is caused by two switch OC

faults in switches A_1 and A_4. A different conduction path may be provided during reconfiguration operation, using redundant leg switches R_1, R_2, and R_5 to preserve the L_1 voltage level and R_1, R_3, and R_4 to preserve the L_5 voltage level.

The simulation result of multiple-switch OC faults in different legs is shown in Figure 52j. The loss of the output voltage levels L_4 and L_5 is caused by two switch OC faults in switches A_4 and B_1. A different conduction path may be provided during reconfiguration operation by using redundant leg switches R_3, R_4, and R_6 to preserve the L_4 voltage level and R_1, R_3, and R_4 to preserve the L_5 voltage level.

5.3. Experimental Results and Discussion

A variety of experimental tests are conducted to examine the feasibility and robustness of the five-level FT MLI for OC faults in switching device(s). The experiment is carried out on a purely resistive (R) load. The FT MLI topology is constructed with fourteen IGBTs (FGA25N120) which act as switching devices. A gate driver circuit based on the TOSHIBA TLP-250 optocoupler is used for giving gating signals to individual IGBTs. In accordance with the NLC-PWM scheme, the gating pulses are generated by a digital signal processor (DSP) TMS320F28379D. In order to record different output waveforms, the scope coder YOKOGAWA DL1640 is used. A list of the experimental parameters utilized for performing studies on different switch faults on the FT MLI can be found in Table 11. Figure 53 shows an illustration of the experimental setup that was used in this work.

Table 11. List of experimental parameters.

DC Voltage Source 1	30 V
DC Voltage Source 2	30 V
Load Resistance	171 Ω
Switches	IGBT (FGA25N120)
DSP Kit	C2000, Texas
Switching Frequency	50 Hz

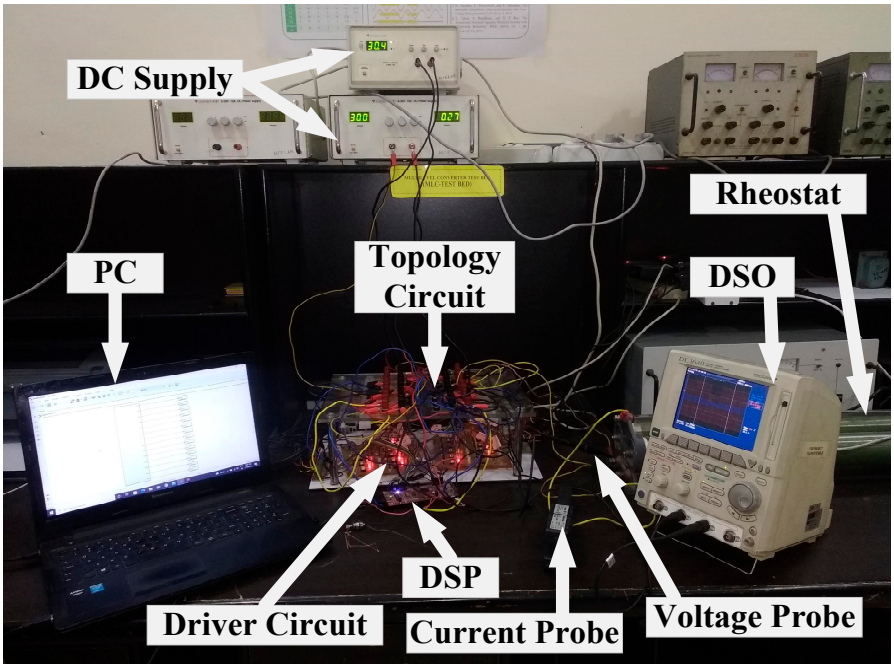

Figure 53. Experimental setup.

5.3.1. Single-Switch OC Fault

Figure 54a illustrates the experimental results obtained under the switch A_1 OC fault of the FT MLI. Under normal or healthy operating conditions, −2E, −E, 0, E, and 2E output

voltage levels are generated by using P_9, P_7, P_4, P_2, and P_1, respectively. Upon reviewing Table 9, it can be seen that the OC fault on switch A_1 results in the loss of 2E voltage level. The FI mark shows the failure of switch A_1. In the reconfiguration operation, the switching path P_1 is replaced by the path through redundant leg switches R_1, R_2, and R_5. The RI mark represents the turn-on of redundant switches. It is important to note that, in this instance, the post-fault voltage is able to regain its level and preserve the level of voltage prior to the fault. Similarly, Figure 54b–h show OC fault experimental results for switch A_2, A_3, A_4, B_1, B_2, B_3, and B_4, respectively.

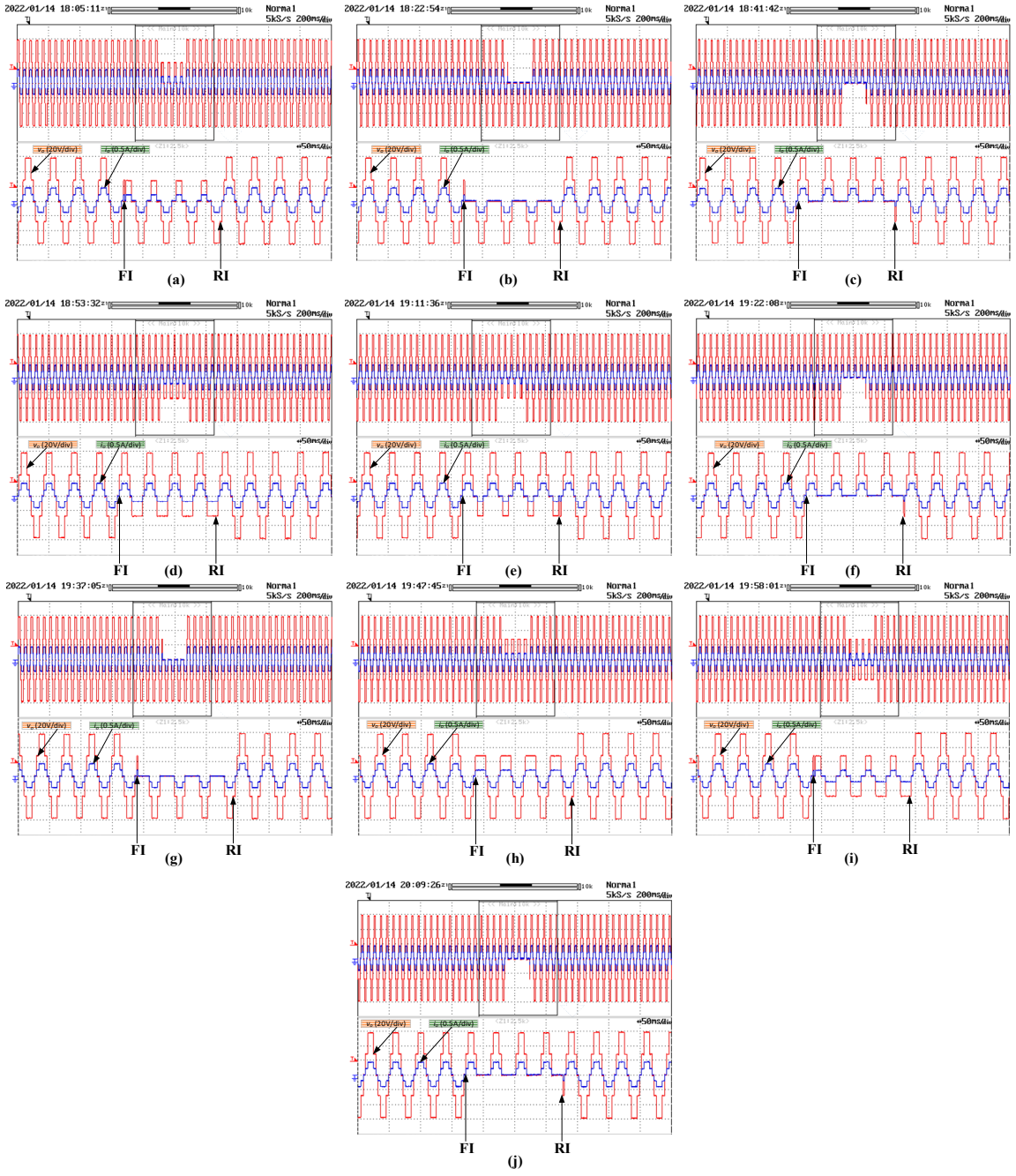

Figure 54. Experimental results (output voltage, v_o; and load current, i_o) for FT operation of the topology in the case of single-switch OC fault for switch (**a**) A_1, (**b**) A_2, (**c**) A_3, (**d**) A_4, (**e**) B_1, (**f**) B_2 (**g**) B_3 and (**h**) B_4; and multiple-switch OC fault for switches (**i**) A_1 and A_4 and (**j**) A_4 and B_1.

5.3.2. Multiple-Switch OC Fault

The experimental result of multiple-switch OC faults in the same leg is shown in Figure 54i. Two switches' OC fault in switches A_1 and A_4 displays loss of L_1 and L_5 voltage levels that are available under healthy operation, as described in Table 9. The missing voltage levels for the switches A_1 and A_4 OC faults can also be seen in Table 7. FI indicates that switches A_1 and A_4 have failed. The next is the reconfiguration stage, in which the redundant leg's switches (R_1, R_2, and R_5 to preserve the L_1 voltage level and R_1, R_3, and R_4 to preserve the L_5 voltage level) are activated accordingly in order to produce the five-level voltage waveform at the output. RI demonstrates that redundant switches are being turned ON.

The experimental result of multiple-switch OC faults in the different legs is shown in Figure 54j. Two switches' OC fault in switches A_4 and B_1 displays loss of L_4 and L_5 voltage levels that are available under healthy operation, as described in Table 9. The missing voltage levels for the OC faults of switches A_4 and B_1 can also be seen in Table 7. FI indicates that switches A_4 and B_1 have failed. The next is the reconfiguration stage, in which the redundant leg's switches (R_3, R_4, and R_6 to preserve the L_4 voltage level and R_1, R_3, and R_4 to preserve the L_5 voltage level) are activated accordingly in order to produce the five-level voltage waveform at the output. RI demonstrates that redundant switches are being turned ON.

Thus, it can be observed from the simulation, and experimental results that the five-level FT MLI topology is capable of delivering the full voltage levels at rated output power under SSOC fault, MSOC fault in the same leg, and MSOC faults in the different legs.

6. Conclusions

This paper provides a comprehensive survey of FT solutions used in MLI, as reported in the literature. Various FT solutions are explained, along with their merits and demerits. Furthermore, a comprehensive review of single-phase FT MLI topologies provides a clear picture of the current research status. There is a growing interest in fault diagnosis and fault tolerance in power electronic systems. To ensure the reliability of MLIs, their application in MLIs is of great importance. FT MLI topologies are reviewed based on their constructional features, merits, and limitations. A comparison between different proposed FT MLI topologies in terms of *LSCR*, *LCCR*, *CFLR*, and *LCFR* parameters is summarized in the tables. New comparative factors—*FTF* and *CFTF*—were introduced to compare FT MLI topologies more effectively. An *FTF*-and-*CFTF*-factors-based comparison is validated with the results from the MCT method to evaluate fault tolerance or reliability. A comparative analysis is presented to demonstrate the utility of the proposed parameters for comparing FT MLIs, allowing for a future evaluation of newer FT MLI topologies easier. The existing redundant leg-based single-phase five-level FT MLI topology is analyzed to show the FT operation in case of single- and multiple-switch OC faults. The pre-fault, during fault, and post-fault operation of this FT MLI topology are demonstrated with the help of simulation and experimental results. Based on the research, the following limitations are identified:

1. There are relatively few single-phase FT MLI topologies designed to handle multiple-switch OC and/or SC faults, owing to the fact that a majority of single-phase FT MLI topologies are only appropriate for single-switch OC and/or SC faults. The development of single-phase FT MLI topologies capable of handling multiple-switch faults is an area that requires further study.
2. It has been observed that redundant switches or redundant legs of FT MLIs have zero percent utilization under normal or healthy conditions. Hence, redundant switches remain non-operational under healthy conditions and increase the MLI cost. The development of FT MLI topologies where all switches operate under healthy conditions is an area that requires further investigation.
3. Redundant switches or redundant legs of FT MLIs only operate under faulty condition. If redundant switches were to participate during times of overload current under healthy conditions, the thermal stress on the main inverter's switches would be significantly reduced. Hence, the FT MLI topology would be more reliable and longer

lasting. Few works in the literature analyzed the overload capability characteristics of redundant-leg or redundant-switch-based FT MLIs. Further investigation can be performed on this type of MLIs.

4. Some FT MLI topologies are unable to preserve output rated voltage post-fault. Hence, topologies use a step-up transformer to maintain the output rated voltage. This will increase the cost and size of the system. The development of FT MLI topologies where output rated voltage can be achieved post-fault under the maximum number of switch fault occurrences is an area that requires further study.
5. The development of FT MLI topologies where output power and efficiency can be achieved post-fault similar to pre-fault condition is an area that requires further investigation.
6. Most of the FT MLI topologies in the literature focused on the switch fault. Very few works in the literature analyzed the capacitor and DC source failures in FT MLIs. The design of new FT MLI topologies that ensure operational continuity in the event of a capacitor and/or source failure requires further investigation.
7. Few FT MLIs that can be extended for the "N" number of voltage levels are reported in the literature. New FT MLI topologies that can be extended to higher voltage levels for high-voltage applications require further investigation.

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