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Assessment of a High-Order Stationary Frame Controller for Two-Level and Three-Level NPC Grid-Connected Inverters

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Abstract: Most grid-connected DC/AC inverters use traditional proportional–integral (PI) controllers in a synchronous frame. In addition to poor disturbance rejection capabilities, these PI controllers also exhibit steady-state errors for sinusoidal reference signals. To address these drawbacks, this article investigates the use of a high-order controller in the stationary frame and then compares it with the standard PI controller. The effectiveness of the high-order controller in the stationary frame has been examined by providing an infinite gain at a resonance frequency. In this work, the design of high-order and PI controllers and tuning instructions are given. Furthermore, both high-order and PI current-controlled two-level and three-level neutral point clamped (NPC) inverters are compared. Various operational conditions are used for the comparison. The high-order controller reduced the total harmonic distortion (THD) of the injected current by 1.15% for the two-level inverter in normal conditions as compared to the PI controller and 0.9% for the three-level NPC inverters. Furthermore, it reduced the THD in balanced abnormal conditions by 0.5% for the two-level inverter and 0.18% for the three-level NPC inverters. However, the dq controller has a lower THD during unbalance and short circuit conditions.

Keywords: grid inverter control; NPC multilevel inverter; stationary frame; synchronous frame; PI controller; tuning

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1. Introduction

Recently, there has been a rise in the demand for energy, which has resulted in various difficulties for distribution networks, including instability in the grid and power outages. Because it results in more flexibility, balance, and stability for the grids, the utilization of distributed power generating systems (DPGS) is a feasible solution for these issues. Additionally, it can enhance the management of distribution networks and lower the amount of carbon that is released [1]. Wind turbines and photovoltaic systems as well as energy storage devices such as battery banks and fuel cells as well as active filters are DPGS examples. The output voltage for these systems is typically DC, but it must be converted to AC before it can be discharged to the grid or used to power other loads [2,3].

As a result, inverters play a crucial part in grid connected DPGS because they enable the DPGS to convert the DC voltage and current to AC and then transfer it to the grid. As far as design goes, the three-phase inverter is the most basic two-level inverter. It finds widespread applicability in a diverse range of low-voltage and low-power contexts. In order for the two-level inverter to be able to endure high voltage and high current when used in high-power applications, it requires several switch connections that are connected in series and in parallel. In order to prevent overvoltage failures, all of the switches in the

series must be turned on or off at the same time. In addition to this, the two-level inverter needs the utilization of big filters for the reduction in harmonics [4].

The reliability of conventional multilevel converters has been demonstrated in a variety of high-power applications. They are most commonly categorized as neutral-point clamped (NPC), cascaded H-bridge (CHB), or flying capacitor (FC) topologies [5,6]. When compared with the conventional two-level inverters, they are capable of managing more power and voltages at lower switch voltage stress than the conventional inverters. Because of this, both the size of the output filter and the switching frequency can be lowered in a noticeable way [7].

Nevertheless, connecting inverters to the grid is critical because it causes a slew of issues, including grid instability and disturbance, if no suitable controller is in place [8]. As a result, these systems should be able to compensate for grid distortions. In this case, a high-speed controller as well as a compatibility algorithm are required. Furthermore, the controller's design is critical and significant. Active and reactive power transmission between the grid and DPGS, regulation of DC-link voltage, and grid synchronization are all critical functions of this controller [1]. The current-controlled inverter is the one that is utilized more frequently compared with the voltage-controlled inverter. The control strategy makes use of two cascade loops: an inner current loop that regulates the utility current and an outer power loop that supplies the reference current. There are two basic categories that may be used to categorize current-based controllers, namely, the non-linear control technique and the linear control technique [9].

Grid inverters have integrated non-linear controls such as sliding mode, dead-beat, hysteresis, and predictive control [10]. As one of the predictive regulators, deadbeat control mechanisms are the most commonly used control approach. When the deadbeat controller is properly tuned, it is possible to achieve near-zero tracking error in finite sample steps. When the sampling frequency is increased, this control is more susceptible to mismatches and noise [11,12]. A voltage source inverter can use the hysteresis control approach to create switching signals for inverters by comparing the output utility current to the input reference current. This control method's advantages include ease of use, independence from the loads they are supposed to control, and an excellent transient response [13]. The ability of the predictive control method in nonlinear control systems is well-known. Predictive control can achieve precise current regulation with low total harmonic distortion; however, it is often difficult to execute in practice. The inverter voltage required to force the utility current to follow a current reference is monitored using this control technique [14,15]. The sliding mode (SM) control approach is popular for non-linear and linear loads. Its remarkable performance has made SM control one of the most extensively used algorithms. High dynamic response, stability, robustness, and ease of implementation are the main advantages of this control method. However, the SM control technique has some disadvantages that are well recognized when it is employed with variable switching frequency [16]. These constraints include control imprecision, significant power losses, and a complicated output filter design [17].

On the other hand, the proportional–integral (PI) controller and the proportional-resonant (PR) controller are both types of linear control techniques that can be used in current-controlled inverters [10]. The PI controller has two drawbacks that are well-known in the industry: The weakness of PI controller performance in the stationary frame, which results in steady state error and a phase shift in the current as compared to the reference [18]. Both drawbacks apply to the controller. This is a result of the integral action not performing effectively with sinusoidal reference [19]. Synchronous frame PI control with voltage feed-forward is a popular option [20]. However, it requires multiple conversions in frames and can be difficult to set up with a low-cost fixed-point digital signal processor [21,22]. The PR controller is a type of current controller that does not have the aforementioned disadvantages and is more suited to working with the sinusoidal references and stationary frame than other controllers do [23]. The PR controller only produces gain at one frequency, called the resonant frequency. At all other frequencies, the controller has almost no gain [21].

This paper focuses on two types of controllers, the PI controller in dq frame and the high-order controller in αβ frame. These two different current controllers have been designed and their performance has been compared under different operational conditions for controlling the two-level inverter as well as the three-level NPC inverters. The comparison between the controllers and topologies is conducted using the simulation platform MATLAB/Simulink.

2. Materials and Methods

2.1. Converter Modeling

A half-bridge is the fundamental topology of any voltage source converter because it is the topology that contains only one leg of the converter. In this section, an average model of a two-level half-bridge converter and a three-level half-bridge NPC converter is developed. This gives us the ability to explain the dynamics of the converter as a function of the modulating signal [16].

2.1.1. Two-Level Half-Bridge Converter Averaged Model

For the purpose of describing the fundamental half-bridge two-level converter seen in Figure 1, we will refer to the state of the switch as s(t). This value will be either 1 if the switch is conducting or 0 if it is blocked, and these values are complementary to one another.

$$s_1(t) + s_2(t) = 1 \tag{1}$$

when s_1 is on, $V_t(t)$ is equal to $\left(\frac{V_{DC}}{2}\right)$, but when s_4 is on, it is equal to $-\left(\frac{V_{DC}}{2}\right)$ when s_2 is on, so $V_t(t)$ can be expressed as a function of both $s_1(t)$ and $s_2(t)$ as follows:

$$V_t(t) = \left(\frac{V_{DC}}{2}\right)s_1(t) - \left(\frac{V_{DC}}{2}\right)s_2 \tag{2}$$

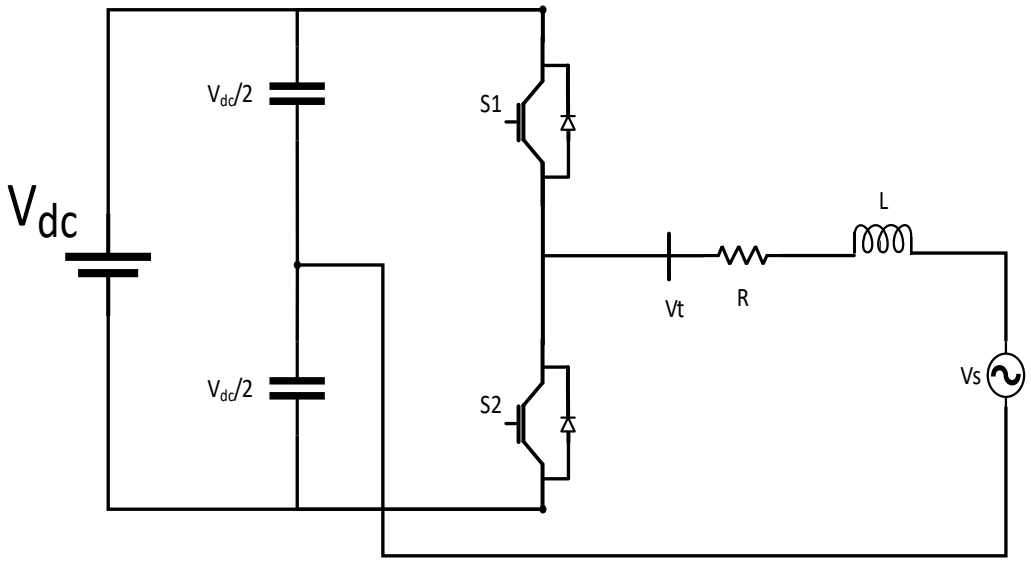

Figure 1. Two-level half-bridge converter.

Using the averaging operator [24] to calculate the average of a variable as a function of time:

$$\overline{x}(t) = \frac{1}{T}\int_{t-T}^{t} x(\tau)\, d\tau \tag{3}$$

Additionally, applying the operator to $s_1(t)$ and $s_2(t)$, it can be concluded that

$$\overline{s}_1(t) = d \tag{4}$$

$$\bar{s}_2(t) = 1 - d \tag{5}$$

where d is the duty ratio. Substituting (4) and (5) in (2)

$$\overline{V_t}(t) = \left(\frac{V_{DC}}{2}\right)(2d - 1) \tag{6}$$

In the SPWM strategy, the relationship between the reference signal (m) and the duty ratio is [25]:

$$m = (2d - 1) \tag{7}$$

From (6) and (7), it is safe to say that

$$(t) = \left(\frac{V_{DC}}{2}\right)(m) \tag{8}$$

2.1.2. Three-Level Half-Bridge Converter Averaged Model

In the three-level half-bridge shown in Figure 2, the AC-side voltage may be represented for a positive modulating signal m as follows:

$$V_t(t) = \left(\frac{V_{DC}}{2}\right)s_1(t) + (0)\ s_3(t) \tag{9}$$

where $s_1(t) + s_3(t) = 1$. In the same way, the AC-side voltage for negative modulating functions is

$$V_t(t) = -\left(\frac{V_{DC}}{2}\right)s_4(t) + (0)\ s_2(t) \tag{10}$$

where $s_4(t) + s_2(t) = 1$. Equations (9) and (10) can be unified through

$$V_t(t) = \left(\frac{V_{DC}}{2}\right)s_1(t)\ sgn(m) - \left(\frac{V_{DC}}{2}\right)s_4(t)\ sgn(-m) \tag{11}$$

where the function $sgn(x)$ is defined by

$$sgn(x) = \begin{cases} 1, & x \geq 0 \\ 0, & x < 0 \end{cases} \tag{12}$$

Applying the averaging operator to both sides of (9) and (10), over one switching cycle, we reach the conclusion

$$\overline{V_t}(t) = \left(\frac{V_{DC}}{2}\right)m(t)\ ,\ m\ \leq 0 \tag{13}$$

$$\overline{V_t}(t) = \left(\frac{V_{DC}}{2}\right)m(t)\ ,\ m\ \leq 0 \tag{14}$$

Equations (13) and (14) can be unified as

$$V_t(t) = \left[\left(\frac{V_{DC}}{2}\right)\ sgn(m) + \left(\frac{V_{DC}}{2}\right)\ sgn(-m)\right]\ m(t) \tag{15}$$

Since $sgn(m) + sgn(-m) = 1$, Equation (15) can be written as

$$\overline{V_t}(t) = \left(\frac{V_{DC}}{2}\right)m(t) \tag{16}$$

Therefore, it is obvious that (16) is identical to (8), which indicates that the average model can be applied for both converters [25].

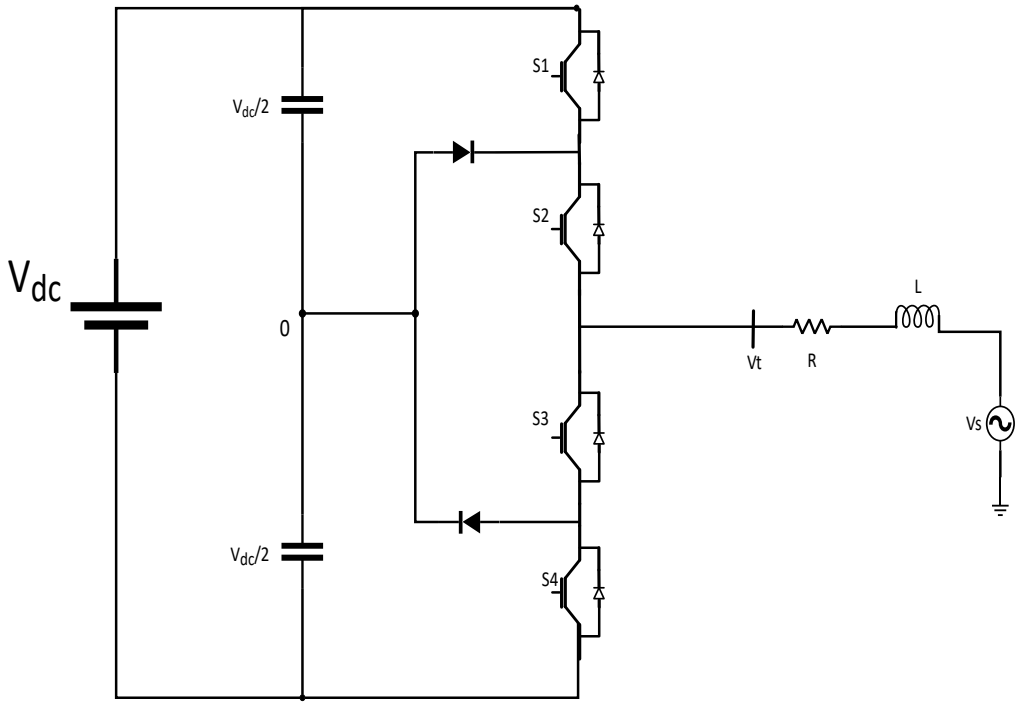

Figure 2. Three-level half-bridge converter.

2.2. AC Side Control Model of Both Converters

Considering Figures 1 and 2, the dynamics of the AC current are described by

$$L\frac{d}{dt}i(t) + Ri(t) = V_t(t) - V_s \tag{17}$$

However, based on Equations (8) and (16), V_t can be controlled by the modulating signal m. Figure 3 shows a control block diagram of the system described by (17).

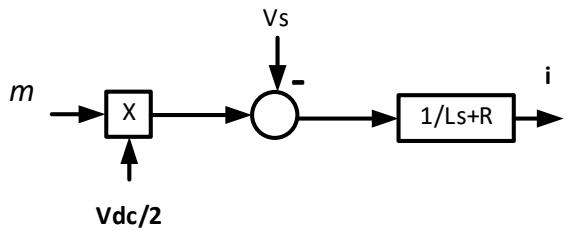

Figure 3. Control model of both converters.

Equation (17) can be expanded for the three-phase system as follows:

$$L\frac{di_a}{dt} = -Ri_a + V_{ta} - V_{sa} \tag{18}$$

$$L\frac{di_b}{dt} = -Ri_b + V_{tb} - V_{sb} \tag{19}$$

$$L\frac{di_c}{dt} = -Ri_c + V_{tc} - V_{sc} \tag{20}$$

2.3. Controller Modelling and Design [25]

2.3.1. High-Order Stationary Frame αβ Controller [25]

Equations (18)–(20) can be expressed in αβ frame using the Clarke transformation as follows:

$$L\frac{di_\alpha}{dt} = -Ri_\alpha + V_{t\alpha} - V_{s\alpha} \tag{21}$$

$$L\frac{di_\beta}{dt} = -Ri_\beta + V_{t\beta} - V_{s\beta} \tag{22}$$

Expressing $V_{t\alpha}$ and $V_{t\beta}$ in terms of m_α and m_β

$$L\frac{di_\alpha}{dt} = -Ri_\alpha + \frac{V_{DC}}{2}m_\alpha - V_{s\alpha} \tag{23}$$

$$L\frac{di_\beta}{dt} = -Ri_\beta + \frac{V_{DC}}{2}m_\beta - V_{s\beta} \tag{24}$$

Based on Equations (23) and (24), the control loop shown in Figure 4 is developed.

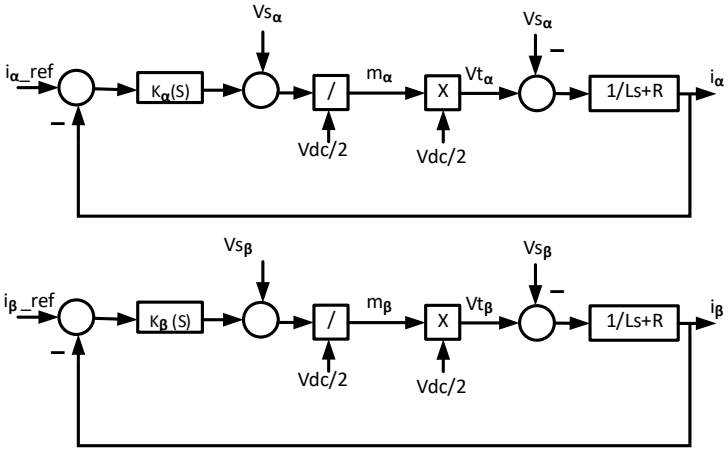

Figure 4. Current control loop in αβ frame.

For real/reactive power controller, the currents $i_{\alpha-ref}$ and $i_{\beta-ref}$ are generated using the following equations:

$$i_{\alpha-ref}(t) = \frac{2}{3}\left[\frac{V_{s\alpha}}{{V_{s\alpha}}^2 + {V_{s\beta}}^2}\,P_{s-ref(t)} + \frac{V_{s\beta}}{{V_{s\alpha}}^2 + {V_{s\beta}}^2}\,Q_{s-ref(t)}\right] \tag{25}$$

$$i_{\beta-ref}(t) = \frac{2}{3}\left[\frac{V_{s\alpha}}{{V_{s\alpha}}^2 + {V_{s\beta}}^2}\,P_{s-ref(t)} + \frac{V_{s\beta}}{{V_{s\alpha}}^2 + {V_{s\beta}}^2}\,Q_{s-ref(t)}\right] \tag{26}$$

2.3.2. High-Order Stationary Frame αβ Compensator Design

First of all, the gain crossover frequency ω_C of the designed compensator should be determined and it must satisfy the inequality $\omega_C < \omega_b < 2\omega_C$, where ω_b is the bandwidth of the closed loop which should be very larger than the command signal frequency ω_o in such a way that $\omega_b \approx 9\omega_o$. However, the loop gain of Figure 4 is dictated by:

$$l(s) = k(s)\,\frac{1}{Ls + R} \tag{27}$$

Since the command is a sinusoidal signal, the compensator should include complex-conjugate poles at the rated frequency ($s^2 + {\omega_o}^2$) to ensure zero steady-state error. Figure 5 shows the frequency response of $l(j\omega)$ in dashed lines after adding the complex-conjugate

poles, which contain a phase shift of -90° at low frequencies owing to the pole $s = -\frac{R}{L}$, which must be canceled out by the compensator $k(s)$ by including a zero at the same value. Figure 5 shows the frequency response after the pole cancelation in solid lines.

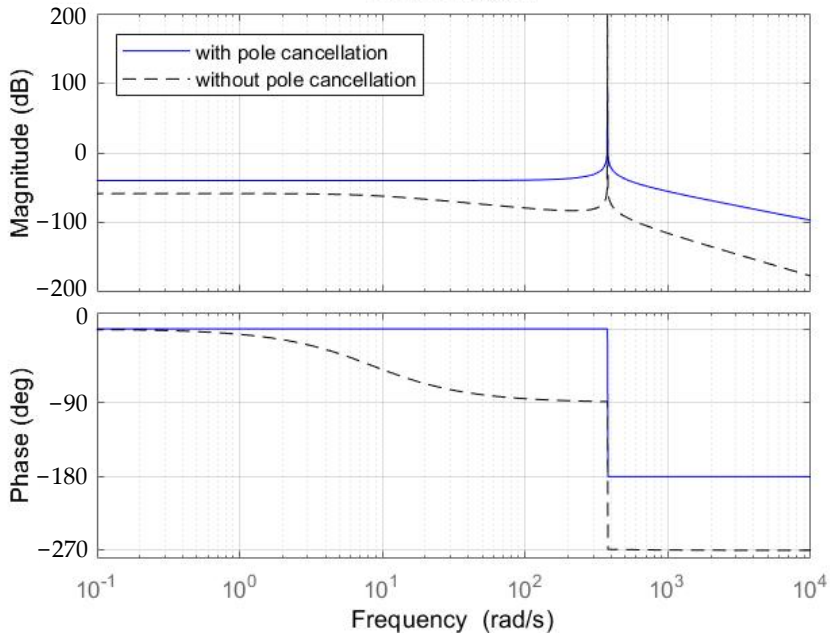

Figure 5. Bode plot of the compensator with and without pole cancelation.

However, even after the pole cancelation, the phase margin at ω_C is zero and a lead compensator is needed to add a phase margin of 45° at ω_C to improve the stability. The dashed line in Figure 6 shows the frequency response after adding the lead compensator and it is noted that the system is stable, but the gain is almost constant at low frequencies. In order to exhibit a large gain at low frequencies, a lag compensator needs to be added to the compensator, and the solid lines in Figure 6 show the final compensator frequency response.

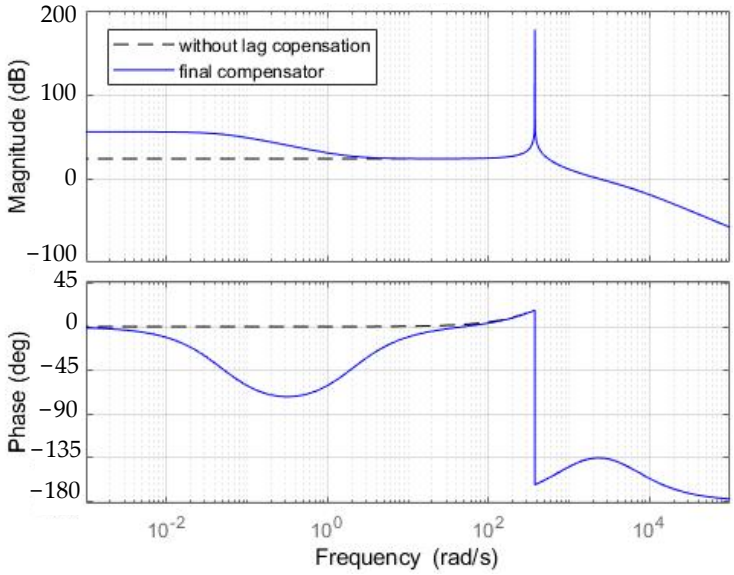

Figure 6. Bode plot of the compensator with and without lag compensation.

The final compensator is:

$$k(s) = h\left(\frac{s + {}^{R}/_{L}}{s^2 + {\omega_o}^2}\right) k_{lead}(s)\, k_{lag}(s) \tag{28}$$

2.3.3. Synchronous Frame dq Controller [25]

Equations (18)–(20) can be expressed in dq frame using the Park transformation as follows:

$$L\frac{di_d}{dt} = L\omega_o\, i_d - Ri_d + V_{td} - V_{sd} \tag{29}$$

$$L\frac{di_q}{dt} = -L\omega_o\, i_q - Ri_q + V_{tq} - V_{sq} \tag{30}$$

Expressing V_{td} and V_{tq} in terms of m_d and m_q

$$L\frac{di_d}{dt} = L\omega_o\, i_d - Ri_d + \frac{V_{DC}}{2}m_d - V_{sd} \tag{31}$$

$$L\frac{di_q}{dt} = -L\omega_o\, i_q - Ri_q + \frac{V_{DC}}{2}m_q - V_{sq} \tag{32}$$

Based on (31) and (32), the control loop shown in Figure 7 is developed.

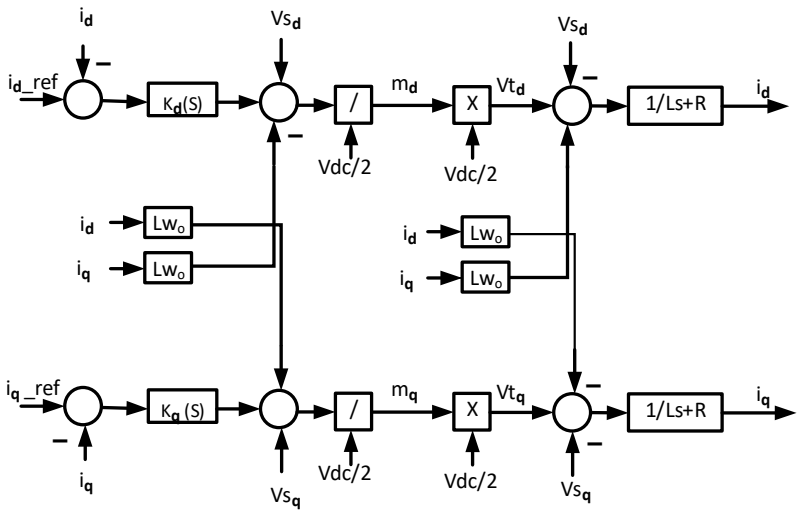

Figure 7. Current control loop in dq frame.

For the real-/reactive-power controller, the currents i_{d-ref} and i_{q-ref} are generated using the following equations:

$$i_{d-ref}(t) = \frac{2}{3\,V_{sd}} P_{s-ref(t)} \tag{33}$$

$$i_{q-ref}(t) = \frac{2}{3\,V_{sd}} Q_{s-ref(t)} \tag{34}$$

2.3.4. Synchronous Frame dq Compensator Design

For simplicity, the control loop can be simplified as shown in Figure 8. However, an integral-proportional (PI) compensator can follow a DC reference in synchronous frame control, in contrast to stationary frame control where compensators are difficult to adjust and have large dynamic orders. The transfer function of the PI controller is given as follows:

$$k(s) = \frac{k_p s + k_i}{s} \tag{35}$$

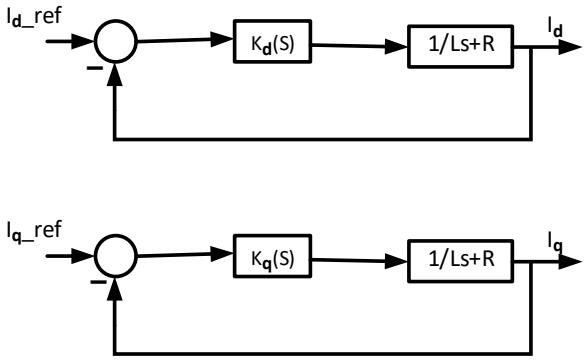

Figure 8. Simplified current control loop in dq frame.

As a result, the loop gain of the simplified loop will be given as follows:

$$k(s) = \left(\frac{k_p}{Ls}\right)\frac{s + {}^{k_i}/_{k_p}}{s + {}^{R}/_{L}} \tag{36}$$

From (35), it is noted that ${}^{k_i}/_{k_p}$ must be equal to ${}^{R}/_{L}$ in order to cancel the pole effect, which can be achieved by making the constants k_p and k_i as follows:

$$k_p = {}^{L}/_{\tau} \tag{37}$$

$$k_i = {}^{R}/_{\tau} \tag{38}$$

where τ is the time constant of the closed loop and should be in the range of (0.5–5) ms.

2.3.5. Phase-Locked Loop (PLL)

Unlike the stationary frame, the synchronous frame needs to be synchronized with the grid. Phase Locked-Loop is a technique for calculating the grid angle. The grid voltage is fed into the system, and the grid angle θ and the frequency ω are outputs. For the PLL diagram shown in Figure 9, the input to the Park transformation is the voltage of each of the three phases of the grid (abc), and the outputs are the voltages in the Synchronous Rotating Frame (dq). Since the q voltage should be kept constant at zero, it is measured and compared with the reference value of zero. In order to cancel the component q, a PI controller is used to accelerate the dq frame within this feedback loop [26].

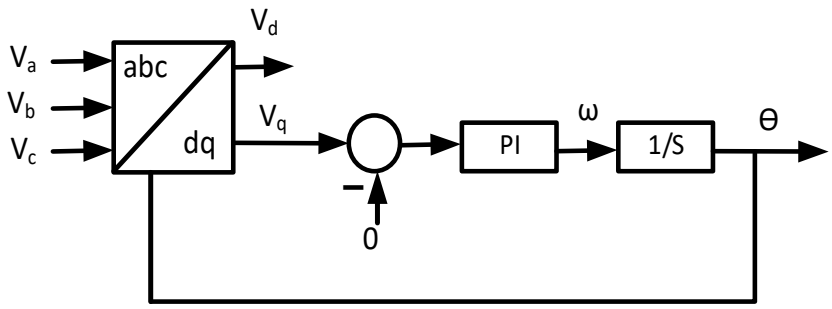

Figure 9. The PLL control loop.

2.3.6. NPC DC Voltage Equalizer

Unlike the two-level inverter, technically the NPC's key issue is to keep the voltages of the two DC-side capacitors equal and at a predetermined level. Due to system flaws, the voltages of DC capacitors may either significantly diverge during transients or steadily drift during steady-state operation. Voltage drift can be avoided through the use of an external converter to correct the DC component [27,28]. Here, the external converter is instructed on how much current to inject into the midpoint based on the (DC) voltage difference between

the two capacitors. The biggest issue with this strategy is that it necessitates extra hardware to generate current, which raises both the cost and complexity of the overall system. However, an alternative approach is the control strategy proposed in [29], which recommends altering the converter switching pattern in order to keep the DC-side voltage at the appropriate value. The control strategy is based on the idea that if the neutral point voltage changes, the control scheme responds by adding a DC offset to the modulating signal, The capacitor balance is restored as a result of the offset creating a current in the neutral point. The controller in Figure 10 is responsible for generating the DC offset. This method is a good way to solve the NPC's biggest technical problem from an economic point of view.

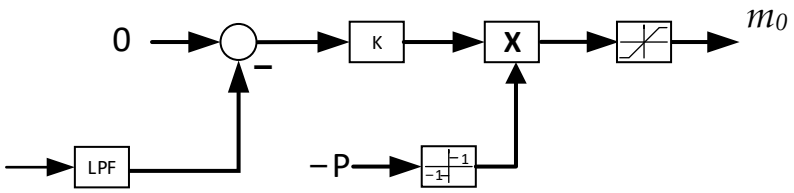

Figure 10. DC voltage equalizer controller.

3. Results and Discussion

The system shown in Figures 11 and 12 with parameters in Table 1 has been studied using the two controllers having the parameters given in Table 2. The performance of the two converters controlled by both controllers is compared in terms of power quality under five cases:

Case 1: Balanced voltage grid (normal conditions).
Case 2: Balanced voltage dip and swell.
Case 3: Unbalanced voltage dip and swell.
Case 4: Symmetrical and unsymmetrical faults at PCC point.
Case 5: Transient analysis.

Table 1. System parameters [25].

Parameter	Value
V_{dc}	1250 V
Grid $V_{L\text{-}L}$ RMS	480 V
Filter inductor L_f	100 µH
Filter Resistor	1.19 mΩ
Switch frequency f_{sw}	3420 Hz
P_{ref}	1 MW
Q_{ref}	0 VAR

Table 2. Controller parameters.

dq Controller	
Parameter	**Value**
Time constant τ	2 ms
Porpotional gain k_p	0.05
Integral gain k_i	0.595
αβ controller	
Parameter	**Value**
Gain h	1258
Transfer function	$\frac{S+11.9}{S^2+377^2}$
Lead compensator	$\frac{S+966}{S+5633}$
Lag compensator	$\frac{S+2}{S+0.05}$
NPC DC voltage equalizer	
Parameter	**Value**
gain k	0.0014

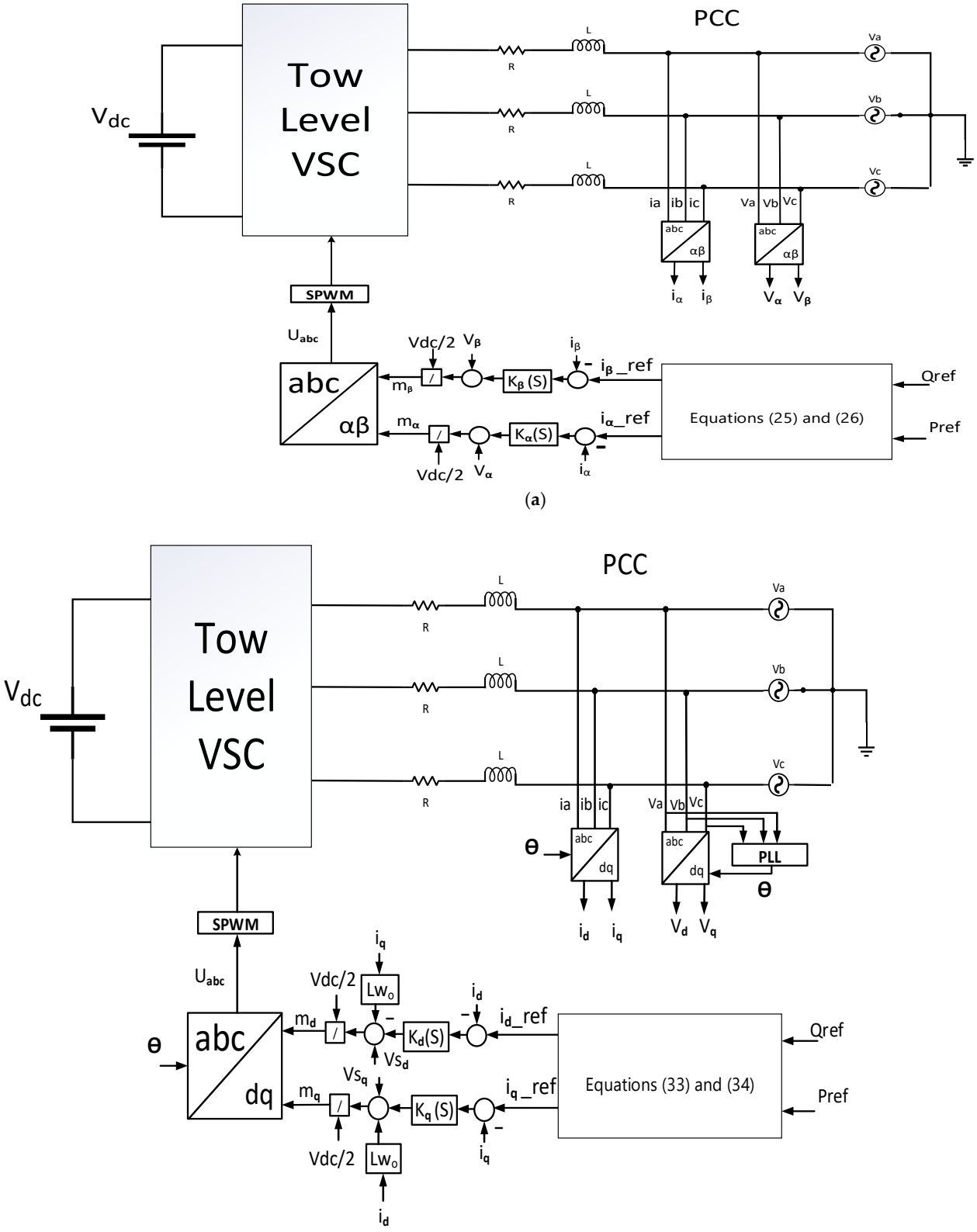

Figure 11. Studied system configurations with two-level inverter using (**a**) the αβ controller and (**b**) the dq controller.

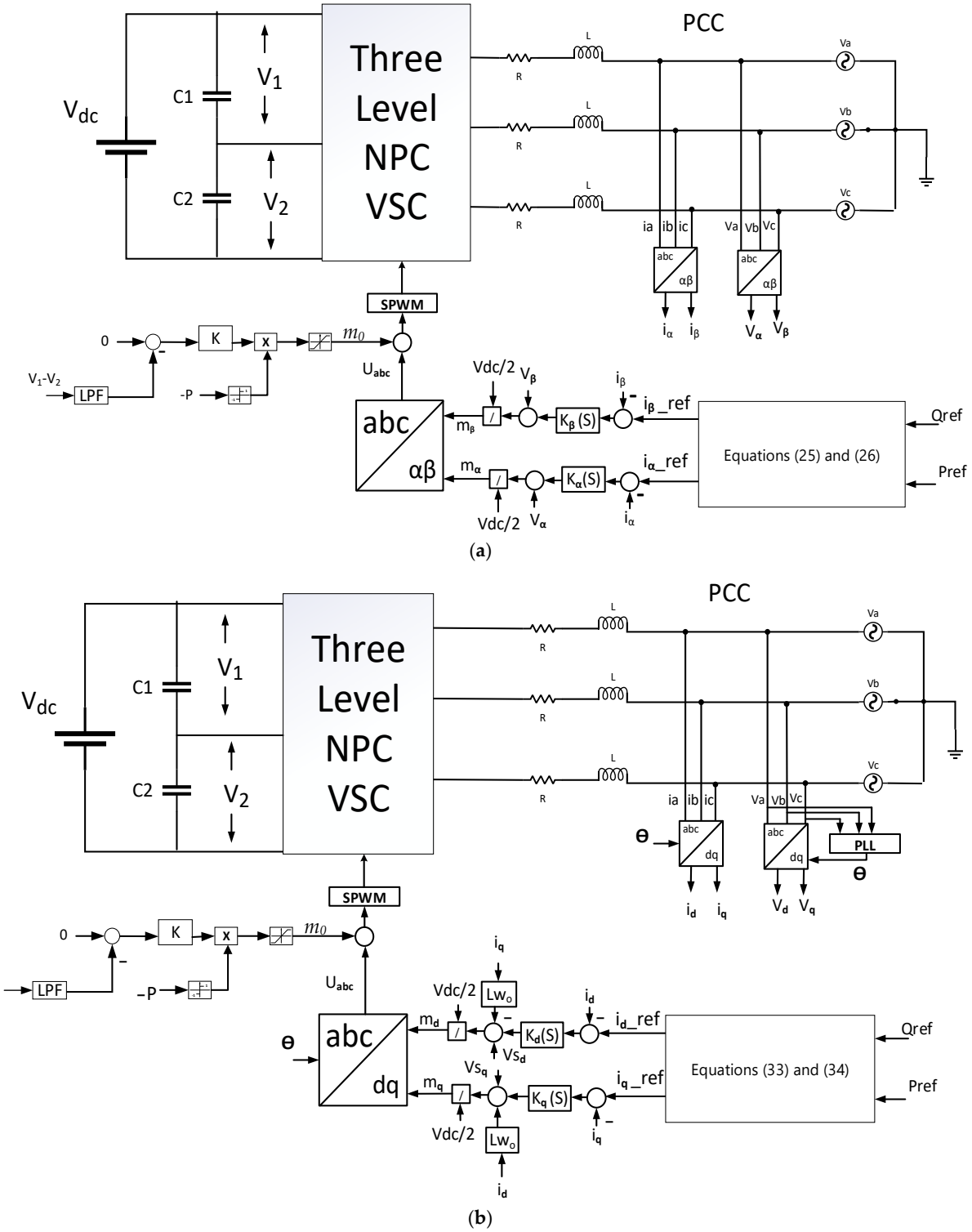

Figure 12. Studied system configurations with three-level NPC inverter using (**a**) the αβ controller and (**b**) the dq controller.

3.1. Case 1

Table 3 shows the results of all topologies and controllers under normal conditions.

Table 3. Case 1 results.

Converter	I_{THD}	V_{THD}
2L-αβ	1.33%	Less than 1%
2L-dq	2.48%	Less than 1%
3 L-αβ	1.29%	Less than 1%
3L-dq	2.19%	Less than 1%

The output three-phase voltages are balanced and constant as shown in Figure 13, and the injected current is shown in Figure 14, indicating that all possible topologies and controllers are performing well and delivering power as the reference values as shown in Figure 15. However, the injected current in the three-level topology has lower Total Harmonic Distortion (THD) than the two-level topology. On the other hand, the high-order αβ controller outperforms the dq controller. The three-level high order αβ controller converter is superior; however, the other converter did not exceed the standard limits [30].

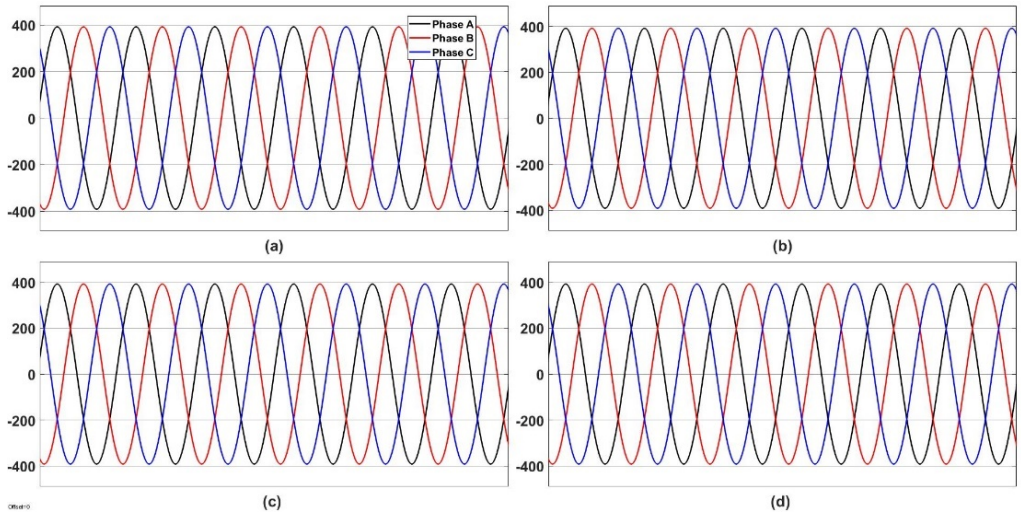

Figure 13. Three-phase pcc voltages in the case of (**a**) 2L-αβ, (**b**) 3L-αβ, (**c**) 2L-dq and (**d**) 3L-dq.

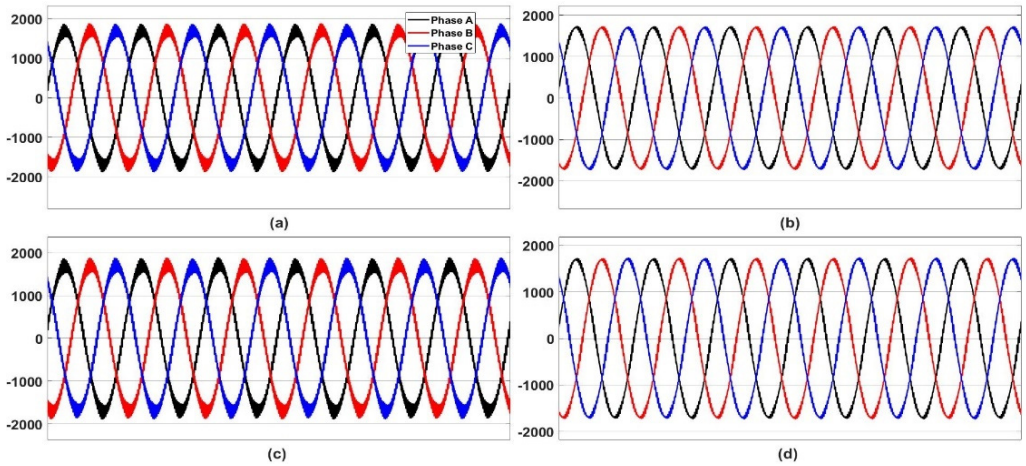

Figure 14. Three-phase pcc currents in the case of (**a**) 2L-αβ, (**b**) 3L-αβ, (**c**) 2L-dq and (**d**) 3L-dq.

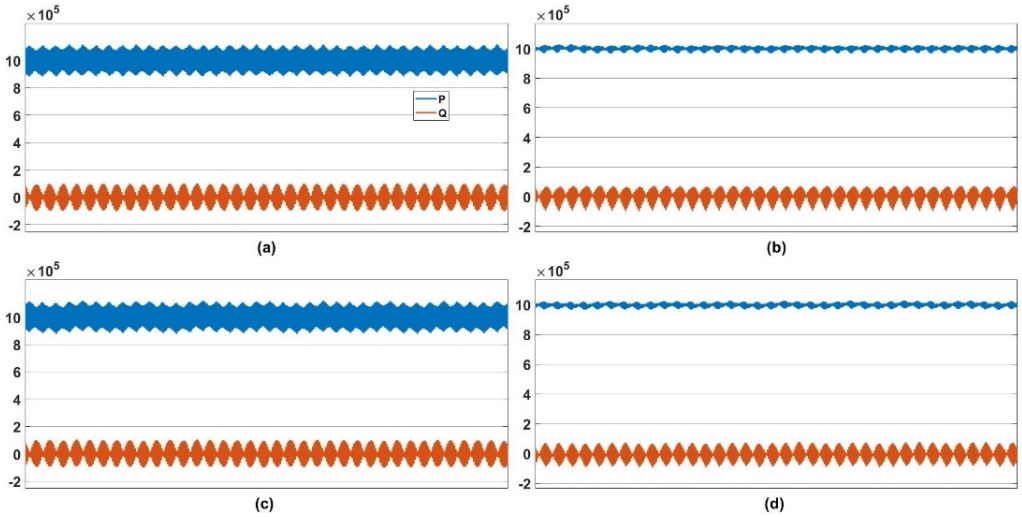

Figure 15. Power flow in the case of (**a**) 2L-αβ, (**b**) 3L-αβ, (**c**) 2L-dq and (**d**) 3L-dq.

3.2. Case 2

Table 4 shows the results for all topologies and controllers at 30% balanced voltage dip and 30% balanced voltage swell occurring at 0.1 s.

Table 4. Case 2 results.

Converter	Swell		Dip	
	I_{THD}	V_{THD}	I_{THD}	V_{THD}
2L-αβ	9.05%	7.88%	10.46%	11.81%
2L-dq	9.55%	7.88%	10.64%	11.81%
3 L-αβ	8.97%	7.88%	10.49%	11.81%
3L-dq	9.15%	7.88%	10.84%	11.81%

All topologies and controllers exceeded the THD standard constraints; the pcc voltages and currents in the case of the balanced voltage dip are shown in Figures 16 and 17, respectively. The conventional two-level topology performs better than the three-level topology, and the high-order αβ controller has a lower THD in the injected current than the dq controller. As demonstrated in Figure 18, all controllers successfully followed the power reference even under the voltage dip, despite the fact that the injected power experienced a minor transient dip at the time the voltage dip occurred.

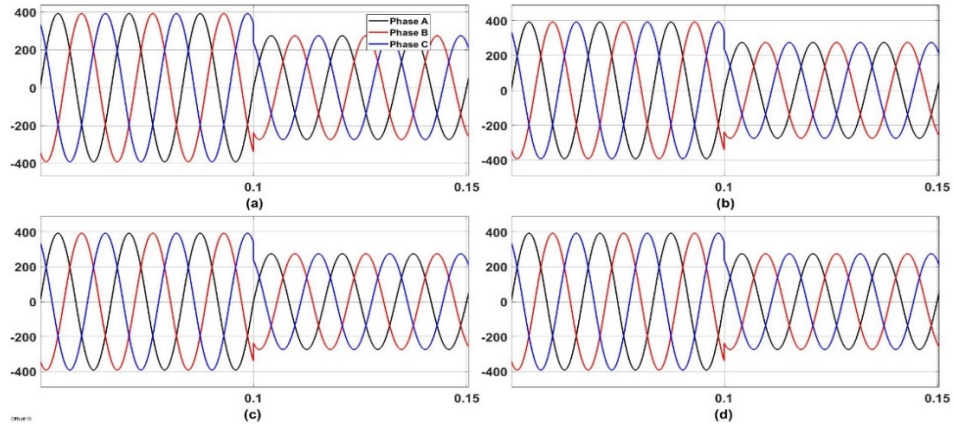

Figure 16. Three-phase pcc voltages in a balance dip in the case of (**a**) 2L-αβ, (**b**) 3L-αβ, (**c**) 2L-dq and (**d**) 3L-dq.

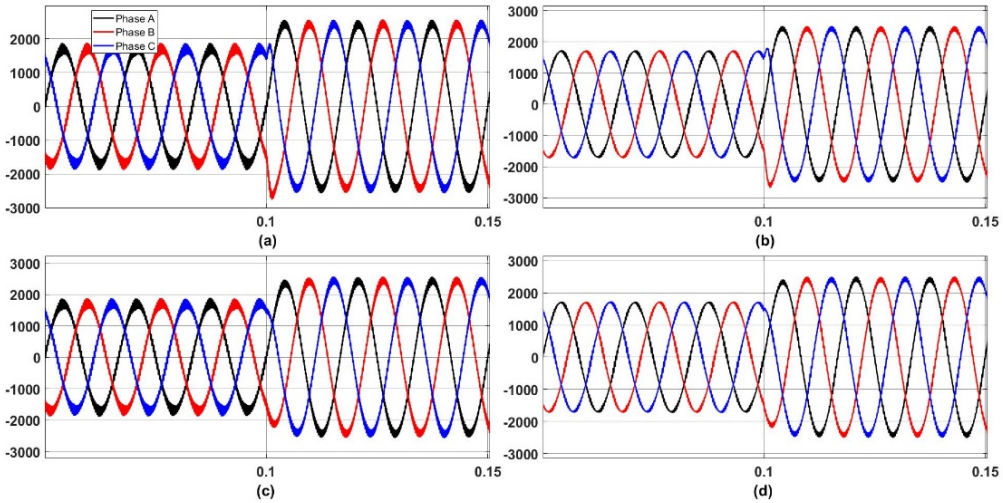

Figure 17. Three-phase pcc currents in a balance voltage dip in the case of (**a**) 2L-αβ, (**b**) 3L-αβ, (**c**) 2L-dq and (**d**) 3L-dq.

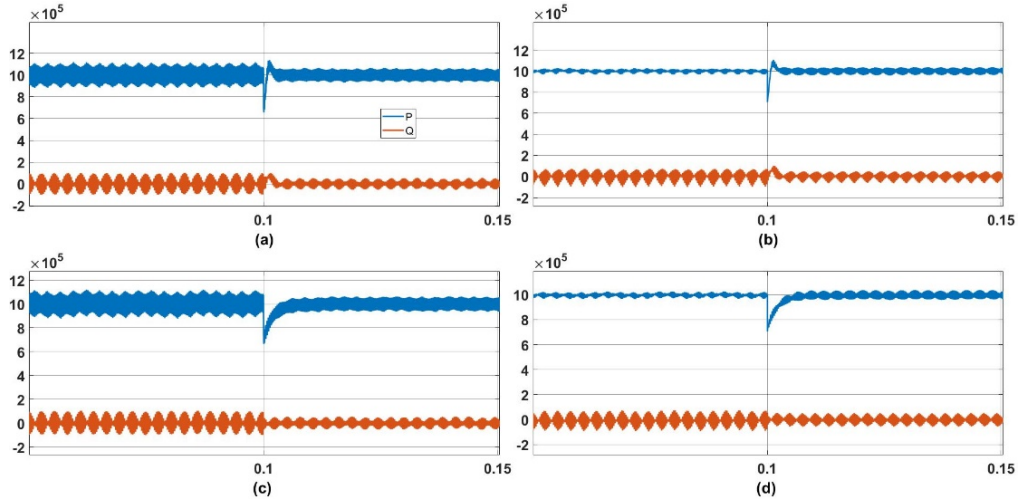

Figure 18. Power flow in a balanced voltage dip in the case of (**a**) 2L-αβ, (**b**) 3L-αβ, (**c**) 2L-dq and (**d**) 3L-dq.

The pcc voltages and currents for balanced voltage swell are depicted in Figures 19 and 20, respectively. Although the three-level topology performs better than the two-level topology, the high-order αβ controller still has a lower THD in the injected current than the dq controller. Additionally, as shown in Figure 21, all controllers maintained the injected power as the reference value after the voltage swell occurred with a short transient swell at the time the voltage swell occurred.

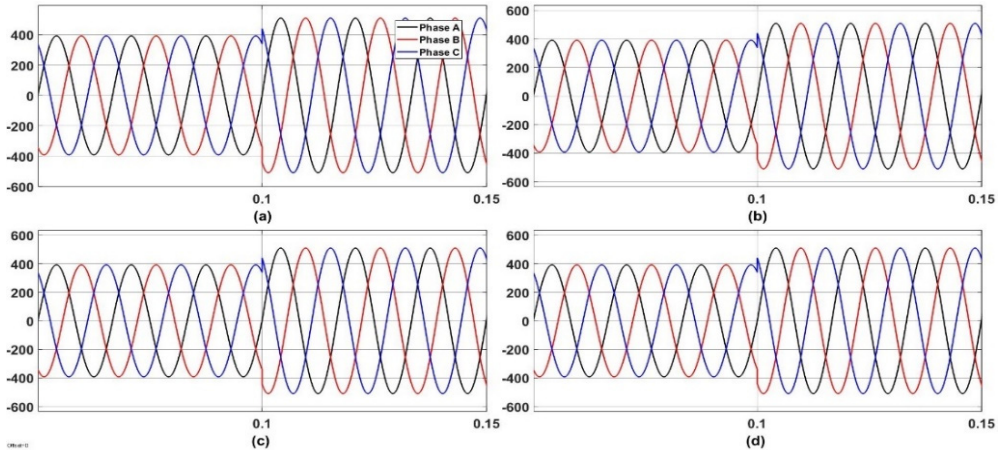

Figure 19. Three-phase voltages in a balanced swell in the case of (**a**) 2L-αβ, (**b**) 3L-αβ, (**c**) 2L-dq and (**d**) 3L-dq.

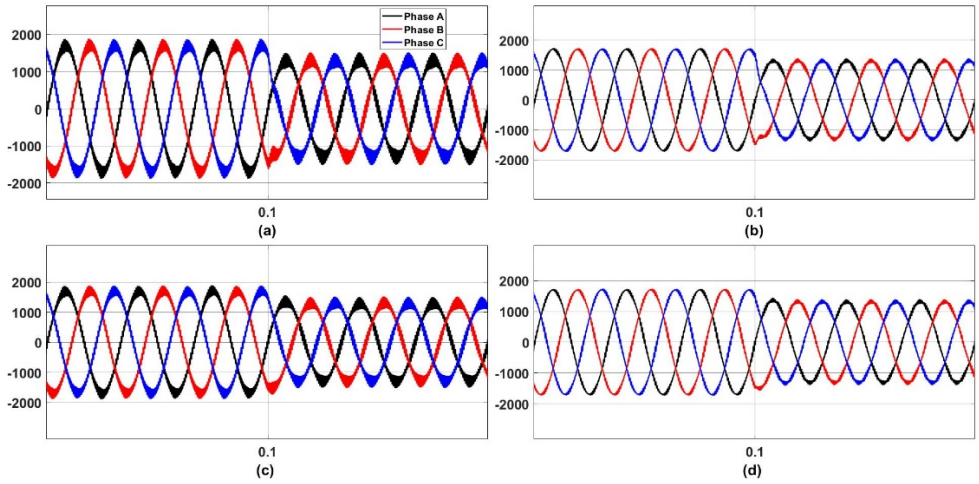

Figure 20. Three-phase pcc currents in a balanced voltage swell in the case of (**a**) 2L-αβ, (**b**) 3L-αβ, (**c**) 2L-dq and (**d**) 3L-dq.

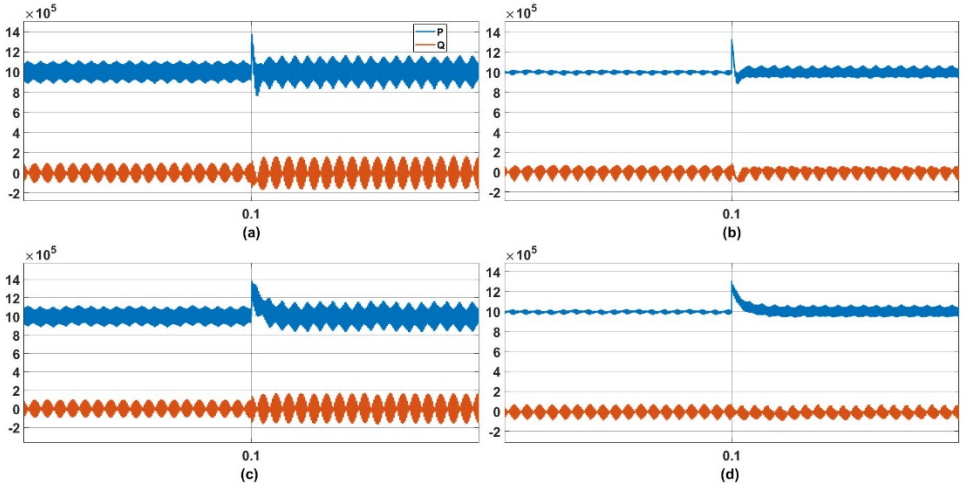

Figure 21. Power flow in a balanced voltage swell in the case of (**a**) 2L-αβ, (**b**) 3L-αβ, (**c**) 2L-dq and (**d**) 3L-dq.

3.3. Case 3

Table 5 shows the result for all topologies and controllers at 30% unbalanced voltage dip and 30% unbalanced voltage swell occurring at 0.1 s.

Table 5. Case 3 results.

Converter	Swell		Dip	
	I_{THD}	V_{THD}	I_{THD}	V_{THD}
2L-αβ	10.70%	7.88%	16.22%	11.81%
2L-dq	7.76%	7.88%	8.78%	11.81%
3 L-αβ	10.61%	7.88%	16.24%	11.81%
3L-dq	7.22%	7.88%	8.93%	11.81%

Identical to the previous case, each topology and each controller failed to meet the THD requirements. The currents and voltages at pcc are shown in Figures 22 and 23 during the unbalanced voltage drop. The conventional two-level topology is superior to the three-level structure, and the THD of the injected current is lower for a high-level αβ controller than for a dq controller. As can be seen in Figure 24, after an unbalanced voltage drop occurred, no control device was able to prevent the injected power from fluctuating around the reference value.

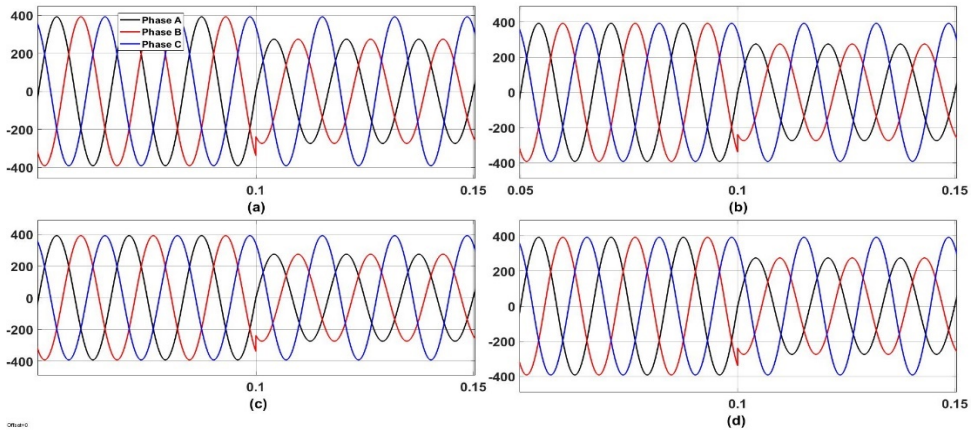

Figure 22. Three-phase pcc voltages in an unbalance dip in the case of (**a**) 2L-αβ, (**b**) 3L-αβ, (**c**) 2L-dq and (**d**) 3L-dq.

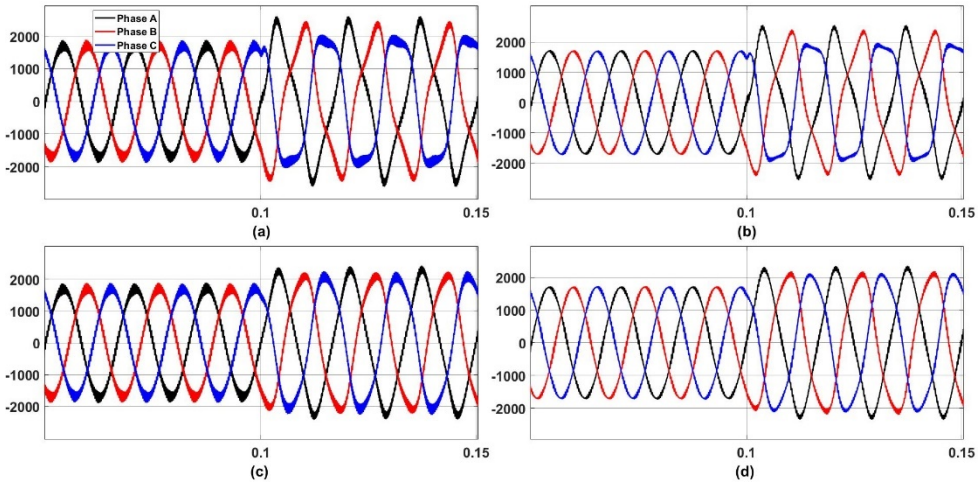

Figure 23. Three-phase pcc currents in an unbalance dip in the case of (**a**) 2L-αβ, (**b**) 3L-αβ, (**c**) 2L-dq and (**d**) 3L-dq.

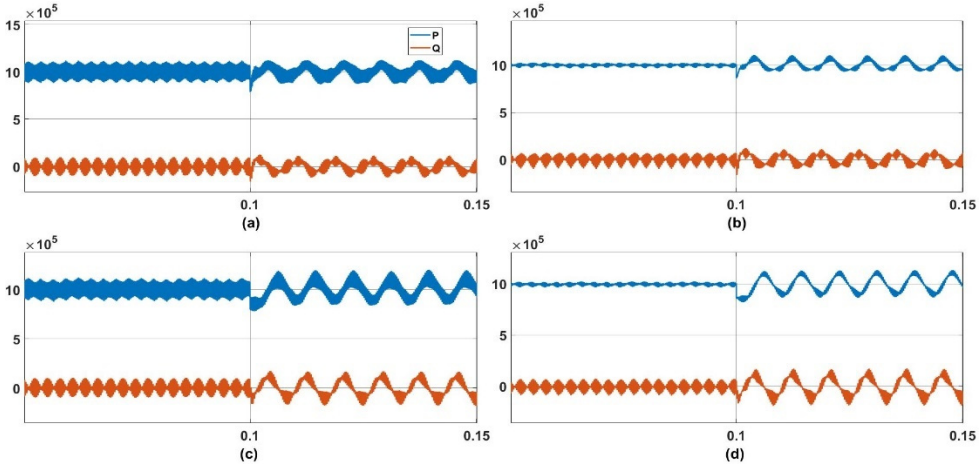

Figure 24. Power flow in an unbalance voltage dip in the case of (**a**) 2L-αβ, (**b**) 3L-αβ, (**c**) 2L-dq and (**d**) 3L-dq.

Figures 25 and 26 show the pcc voltages and currents during an unbalanced voltage swell. While the dq controller still has a lower THD in the injected current than the high-level αβ controller, the performance of the three-level structure is superior to that of the two-level structure. Moreover, as can be seen in Figure 27, after an unbalanced voltage swell occurs, the injected power oscillates around the reference value, indicating that no controller is able to keep it stable.

3.4. Case 4

In this case, all converters were subjected to a comprehensive short circuit test. Figures 28 and 29 show the power flow in the symmetrical and unsymmetrical fault cases occurring at 0.1s, respectively. It can be seen that the dq controller has a significantly superior fault performance than the higher-level αβ controller, especially in terms of symmetrical fault power fluctuation. However, under the unsymmetrical fault, both controllers failed to maintain a constant flow of power.

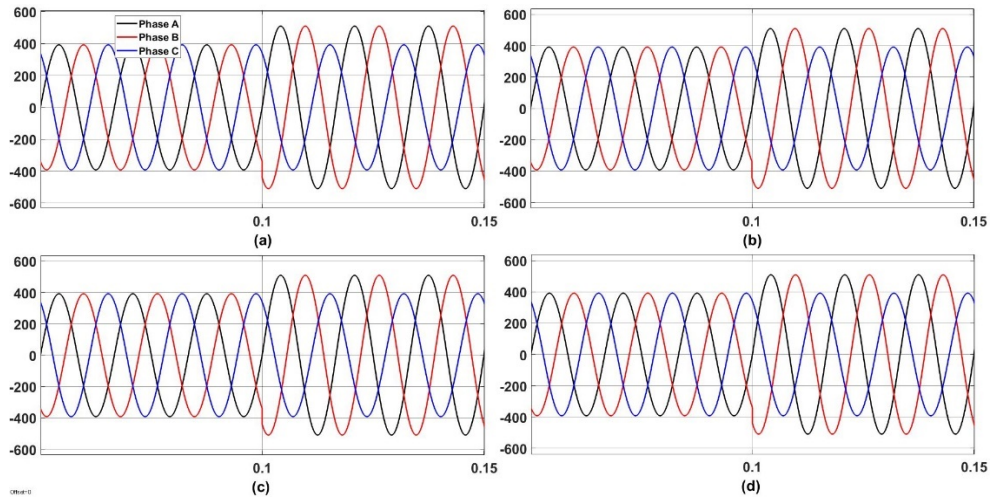

Figure 25. Three-phase pcc voltages in an unbalanced swell in the case of (**a**) 2L-αβ, (**b**) 3L-αβ, (**c**) 2L-dq and (**d**) 3L-dq.

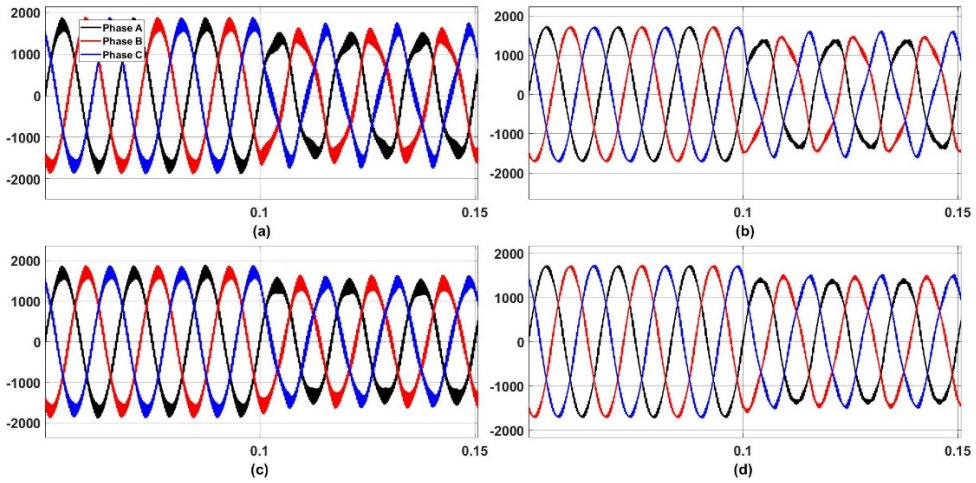

Figure 26. Three-phase pcc currents in an unbalanced swell in the case of (**a**) 2L-αβ, (**b**) 3L-αβ, (**c**) 2L-dq and (**d**) 3L-dq.

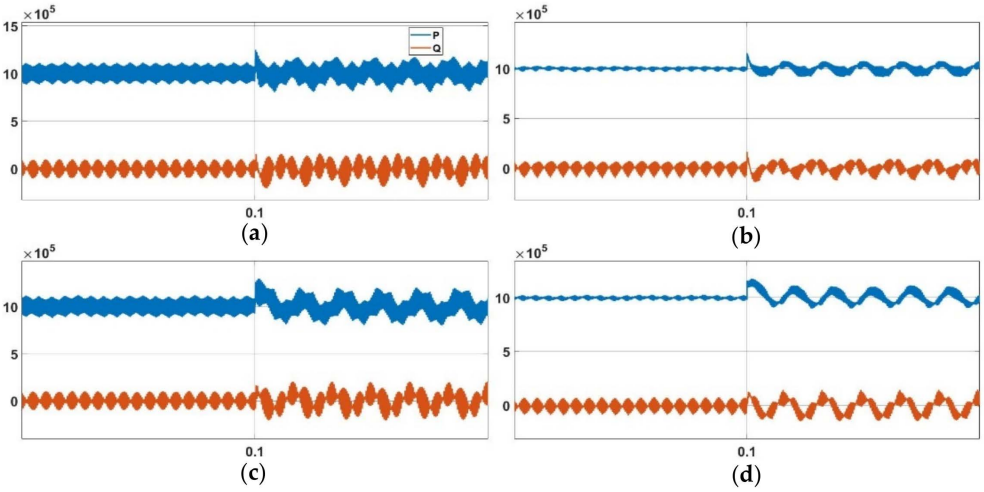

Figure 27. Power flow in an unbalanced voltage swell in the case of (**a**) 2L-αβ, (**b**) 3L-αβ, (**c**) 2L-dq and (**d**) 3L-dq.

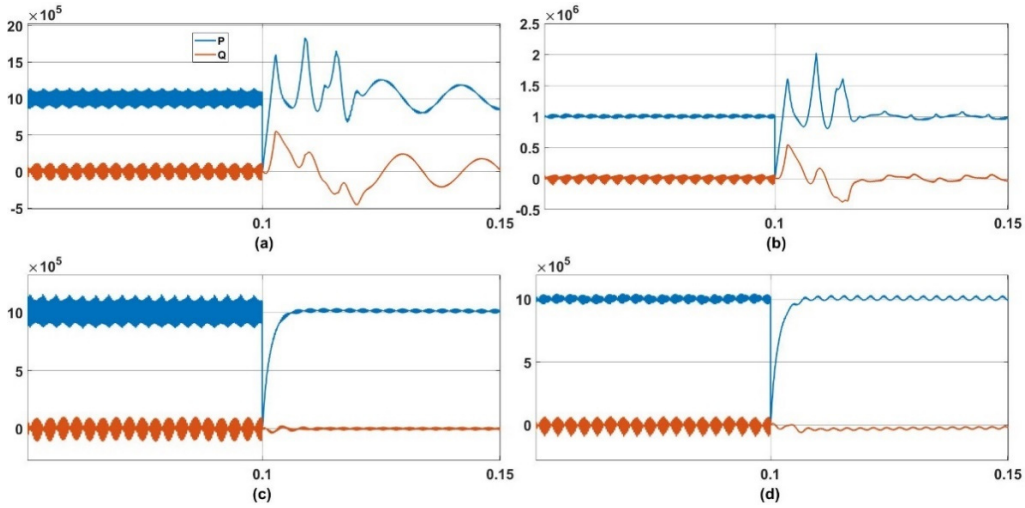

Figure 28. Power flow in symmetrical fault in the case of (**a**) 2L-αβ, (**b**)3L-αβ, (**c**) 2L-dq and (**d**) 3L-dq.

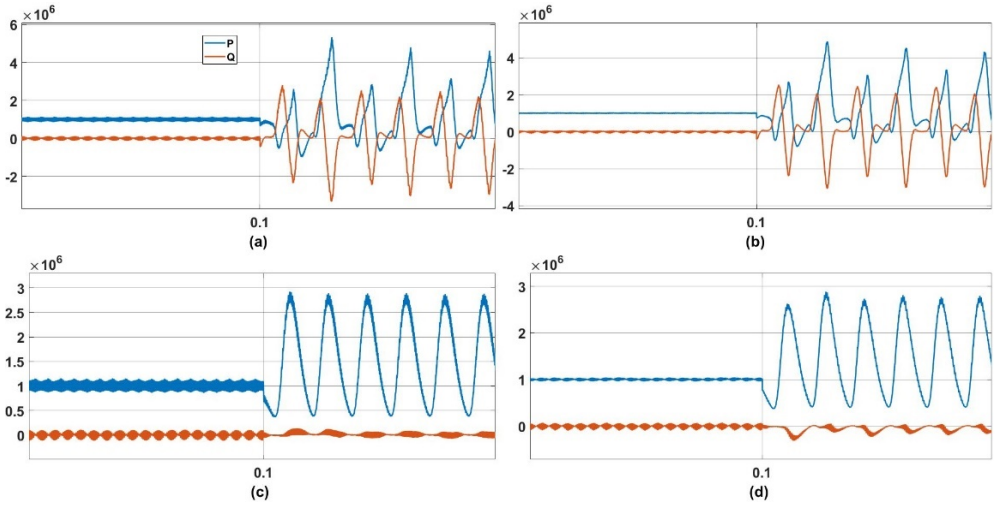

Figure 29. Power flow in unsymmetrical fault in the case of (**a**) 2L-αβ, (**b**) 3L-αβ, (**c**) 2L-dq and (**d**) 3L-dq.

3.5. Case 5

In this case, the coupling between active and reactive power has been investigated for both controllers under a transient analysis. At t = 0.1 s, P_{ref} experiences a step change from 0 to 1 MW, followed by another step change from 1 MW to -1 MW at t = 0.2 s. At t = 0.15s, Q_{ref} is exposed to a step change that goes from 0 to 600 MVAR. Figure 30a,b demonstrates that active and reactive powers are not totally decoupled from one other in αβ frame, as indicated by Equations (25) and (26). In contrast, as shown in Figure 30c,d, the active and reactive powers in the dq frame are decoupled from one another when any of them are changed, as indicated by Equations (33) and (34). This is the case even though the performance of both controllers following the reference power is satisfactory.

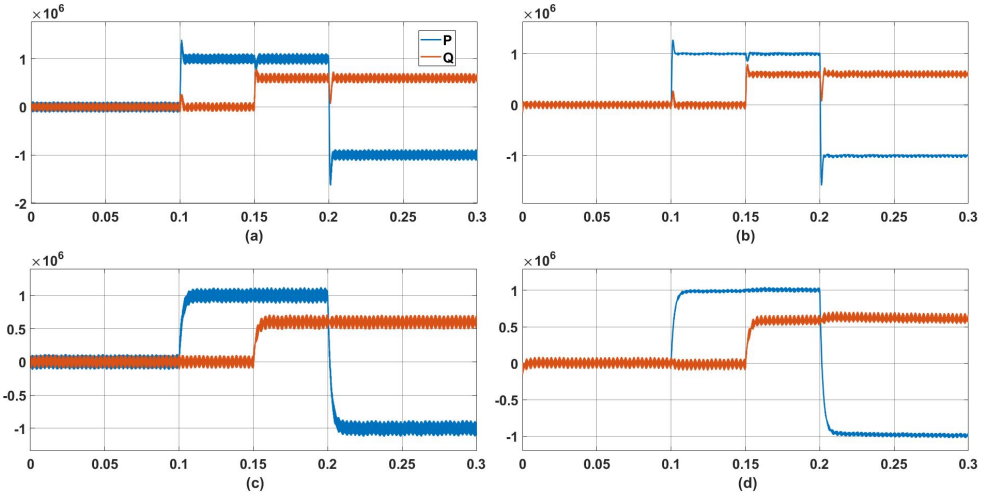

Figure 30. Power under step changes in the case of (**a**) 2L-αβ, (**b**) 3L-αβ, (**c**) 2L-dq and (**d**) 3L-dq.

4. Conclusions

In this paper, the design of both dq and higher-order αβ controllers for a three-level NPC inverter and a two-level conventional grid-connected inverter is presented, and the performances are compared through simulations under different operational conditions. From the simulation results summarized in Table 6, it can be seen that under normal conditions, balanced voltage swell and balanced voltage dip, the higher-order αβ controller obtains a lower THD than the dq controller. The dq controller has a lower THD during unbalanced and short circuit conditions.

Table 6. Results summary.

Case	Lower THD Topology	Lower THD Controller
Balanced voltage	Three-level	αβ controller
Balanced voltage dip	Two-level	αβ controller
Balanced voltage swell	Three-level	αβ controller
Unbalanced voltage dip	Two-level	dq controller
Unbalanced voltage swell	Three-level	dq controller
Symmetrical fault	Two-level	dq controller
Unsymmetrical fault	Two-level	dq controller

From a topological perspective, a three-level NPC inverter injected a current with lower total harmonic distortion (THD) under normal, balanced, and unbalanced voltage swell. THD is lower for both levels in other cases.

In the weak grid, the high-order αβ controller can be investigated for future research. In addition, their performance under unbalanced conditions must be investigated with properly designed additional harmonic compensation.

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